General Description

The DM9331 is a physical-layer, single-chip, low power transceiver for media converter application. On the media side, it provides a direct interface either to Unshielded Twisted Pair Category 5 Cable (UTP5) for 100BASE-TX Fast Ethernet, and it also provides PECL interface to connect the external fiber optical transceiver. Through the Media Converter Interface (MCI), the DM9331 connects to another DM9331 for the twisted pair to the fiber media converter, or fiber to fiber repeater.

The DM9331 uses a low-power and high-performance CMOS process. It contains the entire physical layer functions of 100BASE-TX as defined by IEEE802.3u, including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Twisted Pair Physical Medium Dependent Sublayer (TP-PMD) and a PECL compliant interface for a fiber optical module, compliant with ANSI X3.166. The DM9331 provides a strong support for the auto-negotiation function utilizing automatic selection of full- or half-duplex mode. Furthermore, due to the built-in wave-shaping filter, the DM9331 needs no external filter to transport signals to the media on the 100base-TX Ethernet operation.

Block Diagram

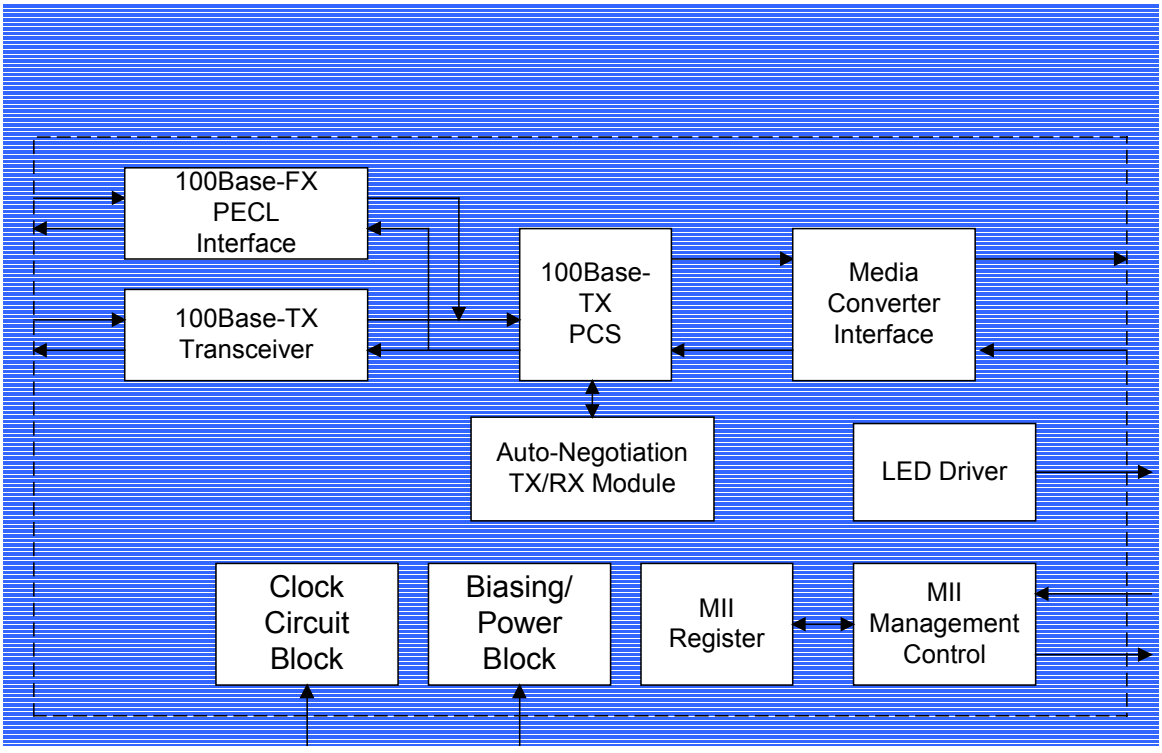
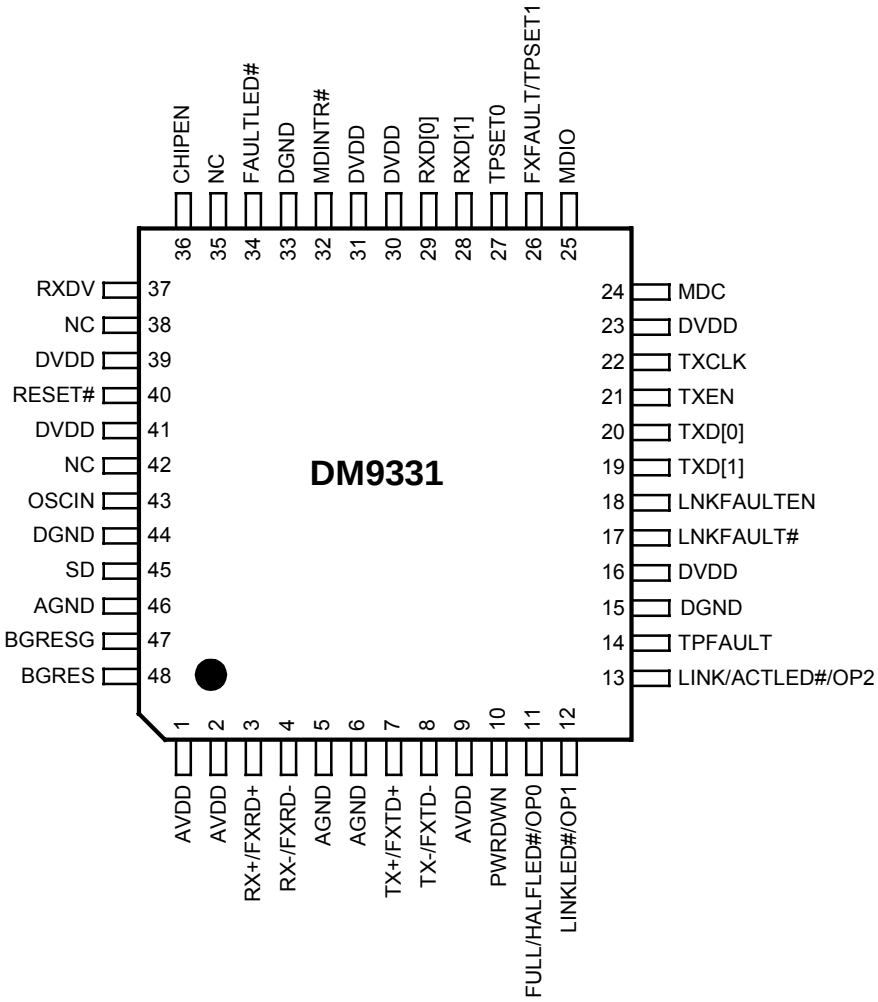


Table of Contents

Features

- 100Base-TX to 100Base-FX media converter application chip set.
- 100Base-FX to 100Base-FX repeater application chip set under full duplex mode.
- 100Base-TX to 100Base-TX repeater application chip set under full duplex mode.
- Optional Fault propagation on no link condition.
- Fully compliant with IEEE 802.3u 100Base-TX/FX
- Compliant with ANSI X3T12 TP-PMD 1995 standard
- Supports Auto-Negotiation function to 100 Mbps full/half duplex, compliant with IEEE 802.3u.
- Remote fault detection capability
- Far end fault signaling option in FX mode
- Selectable twisted-pair or fiber mode output
- Selectable full-duplex or half-duplex operation
- Provides Loopback mode for easy system diagnostics
- LED status outputs indicate Link/Activity, Full/Half-duplex and Fault LED.
- Single Low-Power Supply of 3.3V with 0.35µm CMOS technology
- Very Low Power consumption modes:
  - Power Reduced mode (cable detection)
  - Power Down mode
  - Selectable TX drivers for 1:1 or 1.25:1 transformers for additional power reduction.
- Compatible with 3.3V and 5.0V tolerant I/Os
- 48-pin LQFP small package (1x1 cm)

Pin Configuration



Pin Description

I : Input, O : Output, LI : Latch input when power-up/reset, Z : Tri-State output, U : Pull-up
D : Pull-down

Media converter interface, 18 pins

Pin No.	Pin Name	I/O	Description
14	TPFAULT	O	Twisted Pair Fault 0 = Twisted pair link fault. 1 = Twisted pair normal work.
17	LNKFAULT#	I	Link Fault Propagation 0 = Link fault propagation is active. 1 = normal operation.
18	LNKFAULTEN	I	Link Fault Propagation Enable 0 = Link fault propagation disable. 1 = Link fault propagation enable
20,19	TXD[0:1]	I	Transmit Data 2-bit data inputs (synchronous to the 50MHz OSCIN).
21	TXEN	I	Transmit Enable Active high indicates the presence of valid data on the TXD[0:1] for 100Mbps mode
22	TXCLK	O	Transmit Clock 25MHz transmit clock.
24	MDC	I	Management Data Clock Synchronous clock for the MDIO management data. This clock is provided by management entity, and it is up to 2.5MHz
25	MDIO	I/O	Management Data I/O Bi-directional management data that may be provided by the station management entity or the PHY.
26	FXFAULT/ TPSET1	O,Z,LI (D)	Fiber Fault 0 = Fiber link fault; Fiber receive far end fault package or fiber disconnect. 1 = Fiber normal work. TPSET1 (reset latch input) 0 = Fiber mode; default pull low. 1 = Twisted pair mode; need 4.7kΩ resistor to pull high.
27	TPSET0	Z,LI (D)	Twisted Pair set (reset latch input) 0 = Fiber mode; default pull low. 1 = Twisted pair mode; need 4.7kΩ resistor to pull high.
29,28	RXD[0:1]	O,Z,LI (D)	Receive Data Output 2-bit data outputs (synchronous to the 50MHz OSCIN)
32	MDINTR#	O, Z	Status Interrupt Output: Asserted low whenever there is a status change (link, speed, duplex). The MDINTR# pin has a high impedance output, a 2.2KΩ pull-high resistor is needed.

34	FAULTLED#	O,Z	Link Fault LED Active Low. In TP mode, Indicates TP Fault LED. In FX mode, Indicates FX Fault LED.
36	CHIPEN	Z,LI (D)	Chip Set Enable Need a 4.7kΩ resistor pull high for enabling a chip set.
37	RXDV	O,Z	Receive Data Valid Asserted high to indicate that the valid data is present on the RXD[0:1].
40	RESET#	I	Reset Active low input initializes the DM9331.

Media interface, 5 pins

Pin No.	Pin Name	I/O	Description
3,4	RX+/FXRD+ RX-/FXRD-	I	Differential receive pair/PECL receive pair Differential data is received from the media. Differential Pseudo ECL signal is received from the media in fiber mode.
7,8	TX+/FXTD+ TX-/FXTD-	O	Differential transmit pair/PECL transmit pair Differential data is transmitted to the media in TP mode. Differential Pseudo ECL signal transmits to the media in fiber mode.
45	SD	I	Fiber-optic signal detect PECL signal which indicates whether or not the fiber-optic receive pair is receiving valid signal levels.

LED interface, 3 pins

Pin No.	Pin Name	I/O	Description
11	FULL /HALF LED# /OP0	O ,LI (U)	Full-Duplex/ Half-Duplex LED Active states indicate Full-duplex mode. Active states see LED configuration. OP0 : (power up reset latch input) This pin is used to control the forced or advertised operating mode of the DM9331 according to the Table A. The value is latched into the DM9331 registers at power-up/reset.
12	LINK LED# /OP1	O ,LI (U)	Link LED Active states indicate good link. Active states see LED configuration. OP1 : (power up reset latch input) This pin is used to control the forced or advertised operating mode of the DM9331 according to the Table A. The value is latched into the DM9331 registers at power-up/reset.
13	LINK/ACT LED# /OP2	O ,LI (U)	Link LED & Activity LED : Active states indicate good link. It is also an activity LED function when transmitting or receiving data. Active states see LED configuration. OP2 : (power up reset latch input) This pin is used to control the forced or advertised operating mode of the DM9331 according to the Table A. The value is latched into the DM9331 registers at power-up/reset.

Mode, 1 pin

Pin No.	Pin Name	I/O	Description
10	PWRDWN	I	Power down control Asserted high to force DM9331 into power down mode. When in power down mode, most of the DM9331 circuit block's power is turned off, only the MII management interface (MDC, MDIO) logic is available. To leave power down mode, DM9331 need the hardware or software reset with the PWRDWN pin low.

Bias and clock, 3 pins

Pin No.	Pin Name	I/O	Description
47	BGRESG	P	Bandgap Ground
48	BGRES	I/O	Bandgap Voltage Reference Resistor 6.8K ohm
43	OSCIN	I	3.3V 50MHz clock input.must be using 3.3v output oscillators.

Power, 15 pins

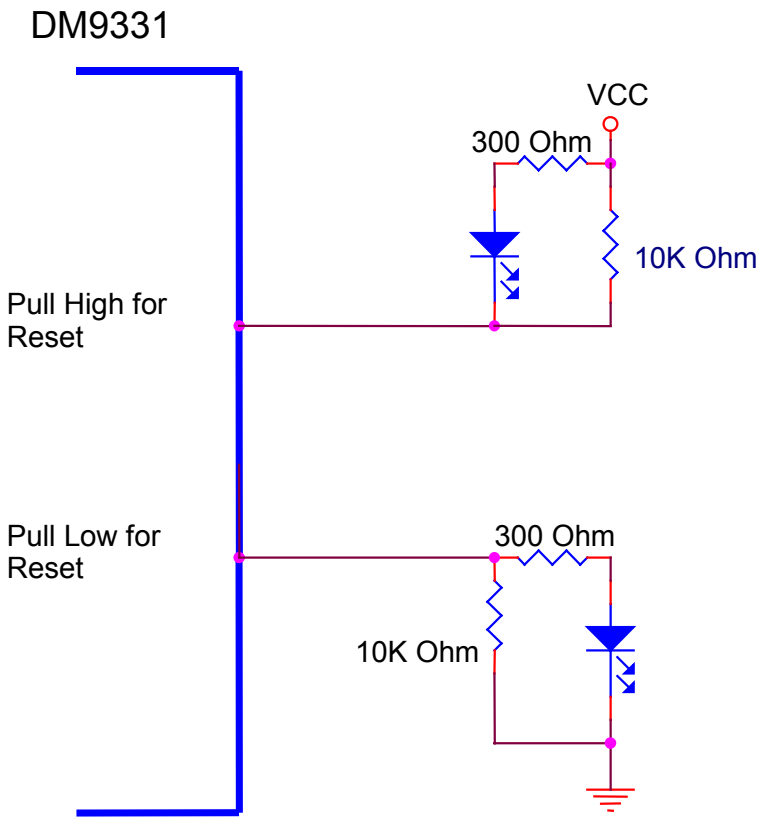
Pin No.	Pin Name	I/O	Description
1,2,9	AVDD	P	Analog Power
5,6,46	AGND	P	Analog Ground
16,23,30,31, 39,41	DVDD	P	Digital Power
15,33,44	DGND	P	Digital Ground

Table A

OP2	OP1	OP0	Function
0	0	0	Auto negotiation enables 100TX Full/Half capabilities
0	0	1	Manually select 100FX HDX
0	1	0	Manually select 100FX FDX
1	0	1	Manually select 100TX HDX

LED Configuration

LEDs flash once for about 200ms after power-on reset or software reset by writing PHY register. All LED pins are dual function pins, which can be configured as either active high or low by pulling them low or high accordingly. If the pin is pulled high, the LED is active low after reset. Likewise, if the pin is pulled low, the LED is active high.



Functional Description

The DM9331 Fast Ethernet single-chip transceiver, providing the functionality as specified in IEEE 802.3u, integrates a complete 100Base-TX module and a complete 100Base-FX module. The DM9331 provides a Media Converter Interface (MCI) as connection interface.
The DM9331 performs all PCS (Physical Coding Sublayer), PMA (Physical Media Access), TP-PMD (Twisted Pair Physical Medium Dependent) sublayer and a PECL compliant interface for a fiber optic module. Figure 1 shows the major functional blocks implemented in the DM9331.

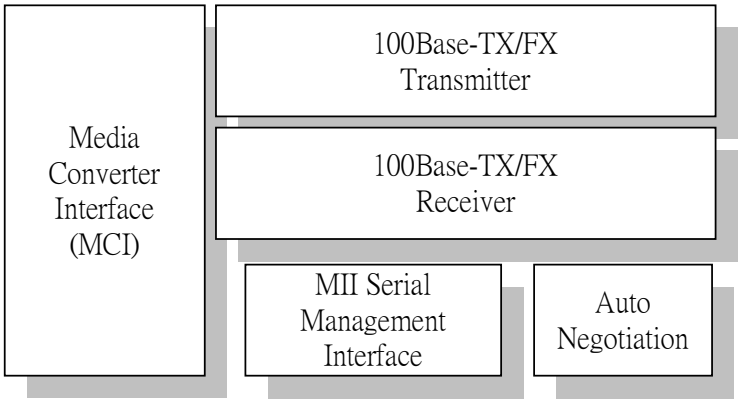


Figure 1

MCI Interface

The DM 9331 provides a Media Converter Interface (MCI) .
The purpose of the MCI interface is to provide a simple, easy to implement connection to another DM9331.
The MCI consists of a 2 bits receive data bus, a two bits transmit data bus, and control signals to facilitate data transfers between the two DM9331 chips.

- TXD (transmit data) is a two bits of data that are driven by the reconciliation sublayer synchronously with respect to OSCIN clock For each OSCIN clock period which TXEN is asserted, TXD (1:0) are accepted for transmission by the PHY.
- TXEN (transmit enable) input from another DM9331 RXDV signal reconciliation sublayer indicates that data are being presented on the MCI for transmission on the physical medium.
- RXD (receive data) is a two bits of data that are sampled by the reconciliation sublayer synchronously with respect to OSCIN clock. For each OSCIN clock period which RXDV is asserted, RXD (1:0) are transferred from the PHY to another DM9331.
- RXDV (receive data valid) output to another DM9331 TXEN signal indicates that the DM9331 is data ready.

100Base-TX Operation

The 100Base-TX transmitter receives 2-bits data clocked in at 50MHz from the MCI, and outputs a scrambled 5-bit encoded MLT-3 signal to the media at 100Mbps. The on-chip clock circuit converts the 25MHz clock into a 125MHz clock for internal use.

These two busses include various controls and signal indications that facilitate data transfers between the DM9331 chip set.

100Base-TX Transmit

The 100Base-TX transmitter consists of the functional blocks shown in figure 2. The 100Base-TX transmit section converts 2-bits synchronous data provided by the MCI to a scrambled MLT-3 125 million symbols per second serial data stream.

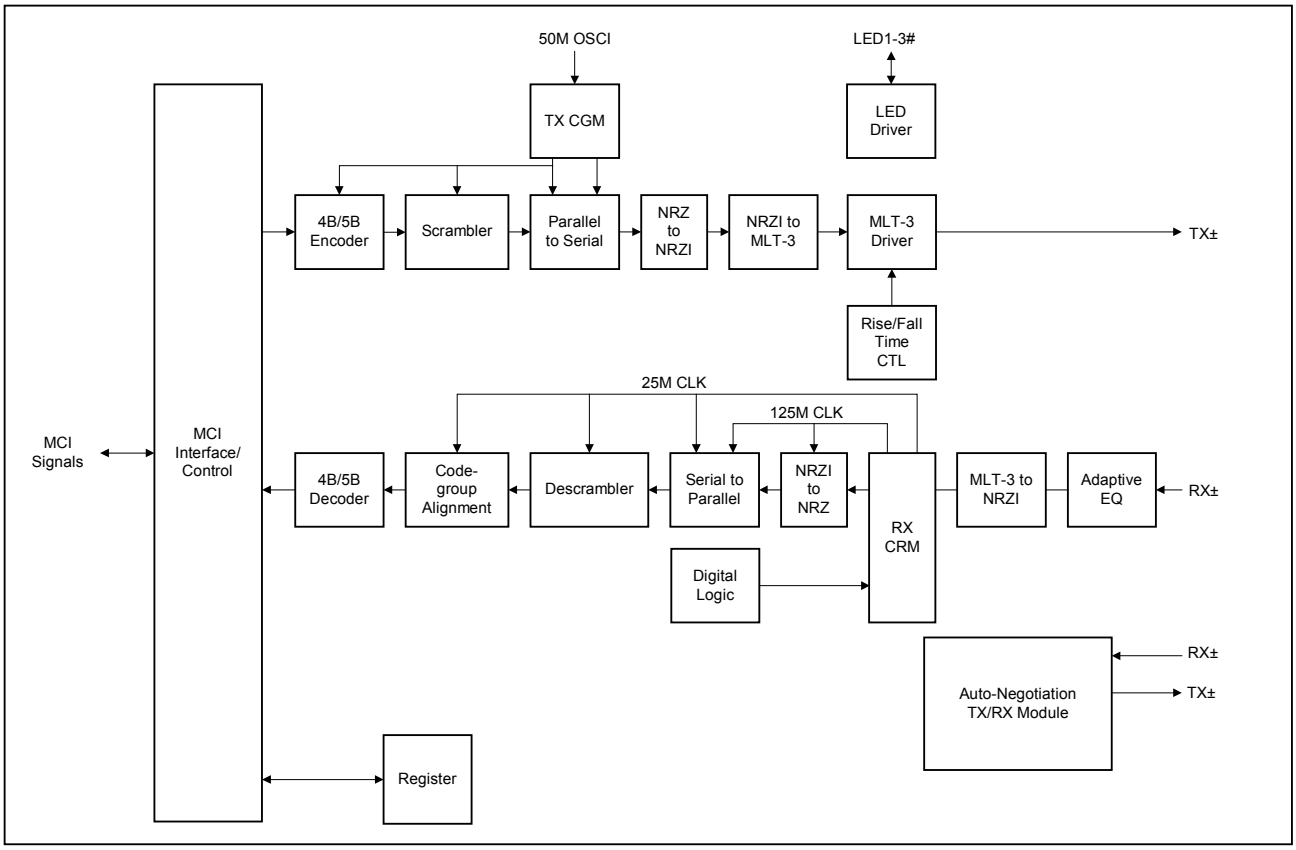


Figure 2

100Base-TX Operation

The block diagram in figure 2 provides an overview of the functional blocks contained in the transmit section.
The transmitter section contains the following functional blocks:

- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Encoder
- NRZI to MLT-3
- MLT-3 Driver

4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

The DM9331 includes a Bypass 4B5B conversion option within the 100Base-TX Transmitter for support of applications like 100 Mbps repeaters which do not require 4B5B conversion.

Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to repeated 5B sequences like continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

Parallel to Serial Converter

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI Encoder block

NRZ to NRZI Encoder

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable.

NRZI to MLT-3

The MLT-3 conversion is accomplished by converting the data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events.

MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver which converts these streams to current sources and alternately drives either side of the transmit transformer primary winding resulting in a minimal current MLT-3 signal.

4B5B Code Group

Symbol	Meaning	4B code 3210	5B code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	undefined	01101
R	ESD (2)	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V	Invalid	undefined	11001

Table 1

100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 2-bit nibble data that is then provided to the MCI.

The receive section contains the following functional blocks:

- Signal Detect
- Digital Adaptive Equalizer
- MLT-3 to NRZI Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

Signal Detect

The signal detect function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX Standards for both voltage thresholds and timing parameters.

Adaptive Equalizer

When transmitting data at high speeds over copper twisted pair cable, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation caused by frequency variations must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation, requires significant compensation which will be over-kill in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

MLT-3 to NRZI Decoder

The DM9331 decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data.

Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125MHz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ Decoder.

NRZI to NRZ

The transmit data stream is required to be NRZI encoded in for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder, receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

Serial to Parallel

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter, and converts the data stream to parallel data to be presented to the descrambler.

Descrambler

Because of the scrambling process required to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, descrambles the data streams, and presents the data streams to the Code Group alignment block.

Code Group Alignment

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected, and subsequent data is aligned on a fixed boundary.

4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups received are the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R symbols).

The T/R symbol pair is also stripped from the nibble presented to the Reconciliation layer.

Auto-Negotiation

The objective of Auto-negotiation is to provide a means to exchange information between segment linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-negotiation does not test the link segment characteristics. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

Auto-negotiation also provides a parallel detection function for devices that do not support the Auto-negotiation feature. During Parallel detection there is no exchange of configuration information, instead, the receive signal is examined. If it is discovered that the signal matches a technology that the receiving device supports, a connection will be automatically established using that technology. This allows devices that do not support Auto-negotiation but support a common mode of operation to establish a link.

MII Serial Management

The MII serial management interface consists of a data interface, basic register set, and a serial management interface to the register set. Through this interface it is possible to control and configure multiple PHY devices, get status and error information, and determine the type and capabilities of the attached PHY device(s).

The DM9331 management functions correspond to MII specification for IEEE 802.3u-1995 (Clause 22) for registers 0 through 6 with vendor-specific registers 16,17, and 18.

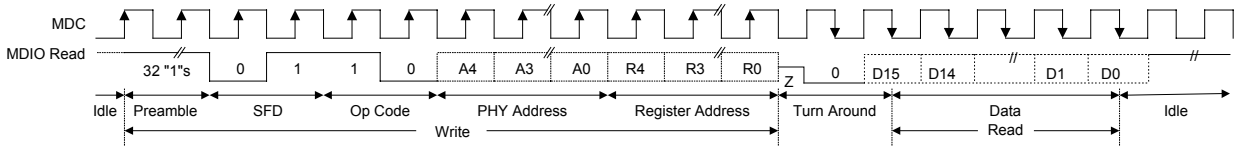
In read/write operation, the management data frame is 64-bits long and starts with 32 contiguous logic one bits (preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP):<10> indicates Read operation and <01> indicates Write operation. For read operation, a 2-bit turnaround (TA) filing between Register Address field and Data field is provided for MDIO to avoid contention. Following the turnaround time, 16-bit data is read from or written onto management registers.

Serial Management Interface

The serial control interface uses a simple two-wired serial interface to obtain and control the status of the physical layer through the MII interface. The serial control interface consists of MDC (Management Data Clock), and MDI/O (Management Data Input/Output) signals.

The MDIO pin is bi-directional and may be shared by up to 32 devices.

Management Interface - Read Frame Structure



Management Interface - Write Frame Structure

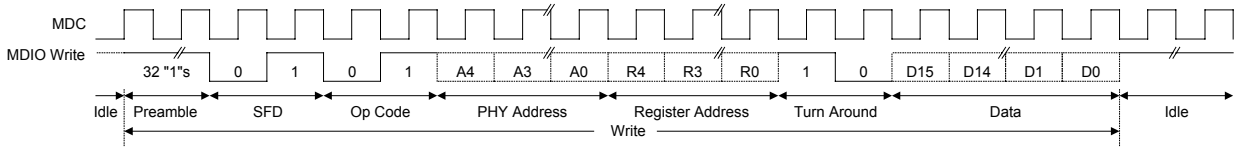


Figure 5

Power Reduced Mode

The Signal detect circuit is always turned on to monitor whether there is any signal on the media. In case of cable disconnection, DM9331 will automatically turn off the power and enter the Power Reduced mode, regardless of its operation mode being N-way auto-negotiation or forced mode. While in the Power Reduced mode, the transmit circuit will continue sending out fast link pules with minimum power consumption. If a valid signal is detected from the media, which might be N-way fast link pules, 10Base-T normal link pules, or 100Base-TX MLT3 signals, the device wakes up and resumes normal operation mode.

Automatic reduced power down mode can be disabled by writing Zero to Reg.16.4.

Power Down Mode

Power Down mode is entered by setting Reg.0.11 to ONE or pulling PWRDWN pin high, which disables all transmit, receive functions and MCI interface functions except the MDC/MDIO management interface.

Reduced Transmit Power Mode

Additional Transmit power reduction can be gained by designing with 1.25:1 turns ration magnetics on its TX side and using a 8.5KΩ resistor on BGRES and BGRESG pins, and the TX+/TX- pull-high resistors being changed from 50 Ω to 78Ω. This configuration could reduce about 20% of transmit power.

Link Fault Propagation

The DM9331 will propagate link fault signals from media to another DM9331. If link fault happens, the DM9331 will send out fault signals to another DM9331.

In FX mode, their are two types of link failure, receive link failure or remote fault (receive far end fault).In the event of a fiber receive link failure, the DM9331 will send out an FX fault signal. The DM9331 will send out a far end fault signal to the fiber optic media, if the DM9331 receive the fault signal from the other device.

In TP mode, In the event of a TP receive link failure, the DM9331 will send out a TP fault signal. The DM9331 will stop to transmit idle signal to the CAT5 media, if the DM9331 receive the fault signal from the other device.

MII Register Description

ADD	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	CONTROL	Reset	Loop back	Speed select	Auto-N Enable	Power Down	Isolate	Restart Auto-N	Full Duplex	Coll. Test	Reserved						
01	STATUS	T4 Cap.	TX FDX Cap.	TX HDX Cap.	Reserved						Pream. Supr.	Auto-N Compl.	Remote Fault	Auto-N Cap.	Link Status	Rsvd	Extd Cap.
04	Auto-Neg. Advertise	Next Page	FLP Rcv Ack	Remote Fault	Reserved		FC Adv	T4 Adv	TX FDX Adv	TX HDX Adv	Rsvd	Rsvd	Advertised Protocol Selector Field				
05	Link Part. Ability	LP Next Page	LP Ack	LP RF	Reserved		LP FC	LP T4	LP TX FDX	LP TX HDX	LP 10 FDX	LP 10 HDX	Link Partner Protocol Selector Field				
06	Auto-Neg. Expansion	Reserved											Pardet Fault	LP Next Pg Able	Next Pg Able	New Pg Rcv	LP AutoN Cap.
16	Aux. Config.	BP 4B5B	BP SCR	BP ALIGN	BP_A DPOK	Rsvd	TX/FX Select	FEF Enable	RMCI Enable	Force 100LNK	SPDLE D_CTL	Rsvd	RPDCT R-EN	Reset St. Mch	Pream. Supr.	Sleep mode	Remote LoopOut
17	Aux. Conf/Stat	100 FDX	100 HDX	Reserved		Reserved								Auto-N. Monitor Bit [3:0]			
21	MDINTR	INTR PEND	Reserved			FDX Mask	Rsvd	Link Mask	INTR Mask	Reserved			FDX Change	Rsvd	Link Change	Rsvd	INTR Status

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type> / <Attribute(s)>

Where：

<Reset Value>:

1	Bit set to logic one
0	Bit set to logic zero
X	No default value
(PIN#)	Value latched in from pin # at reset

<Access Type>:

RO = Read only
RW = Read/Write

<Attribute (s)>:

SC = Self clearing
P = Value permanently set
LL = Latching low
LH = Latching high

Basic Mode Control Register (BMCR) - 00

Bit	Bit Name	Default	Description
0.15	Reset	0, RW/SC	**Reset:** 1=Software reset 0=Normal operation This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed
0.14	Loopback	0, RW	**Loopback:** Loop-back control register 1 = Loop-back enabled 0 = Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appears at the MCI receive outputs
0.13	Speed selection	1, RW	**Speed select:** 1 = 100Mbps 0 = invalid
0.12	Auto-negotiation enable	1, RW	**Auto-negotiation enable:** 1 = Auto-negotiation is enabled, bit 8 and 13 will be in auto-negotiation status.
0.11	Power down	0, RW	**Power Down:** While in the power-down state, the PHY should respond to management transactions. During the transition to power-down state and while in the power-down state, the PHY should not generate spurious signals on the MCI. 1=Power down 0=Normal operation
0.10	Isolate	0,RW	**Isolate:** 1 = Isolates the DM9331 from the MCI with the exception of the serial management. (When this bit is asserted, the DM9331 does not respond to the TXD[0:1] and TXEN inputs, and it shall present a high impedance on its TXCLK, RXDV, and RXD[0:1] outputs. When the PHY is isolated from the MCI, it shall respond to the management transactions) 0 = Normal operation
0.9	Restart auto-negotiation	0,RW/SC	**Restart auto-negotiation:** 1 = Restart auto-negotiation. Re-initiates the auto-negotiation process. When auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning a value of 1 until auto-negotiation is initiated by the DM9331. The operation of the auto-negotiation process will not be affected by the management entity that clears this bit 0 = Normal operation
0.8	Duplex mode	1,RW	**Duplex mode:** 1 = Full duplex operation. Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With auto-negotiation enabled, this bit reflects the duplex capability selected by auto-negotiation 0 = Normal operation

0.7	Collision test	0,RW	**Collision test:** 1 = Collision test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TXEN 0 = Normal operation
0.6-0.0	Reserved	0,RO	**Reserved:** Write as 0, ignore on read

Basic Mode Status Register (BMSR) - 01

Bit	Bit Name	Default	Description
1.15	100BASE-T4	0,RO/P	**100BASE-T4 capable:** 1 = DM9331 is able to perform in 100BASE-T4 mode 0 = DM9331 is not able to perform in 100BASE-T4 mode
1.14	100BASE-TX full duplex	1,RO/P	**100BASE-TX full duplex capable:** 1 = DM9331 is able to perform 100BASE-TX in full duplex mode 0 = DM9331 is not able to perform 100BASE-TX in full duplex mode
1.13	100BASE-TX half duplex	1,RO/P	**100BASE-TX half duplex capable:** 1 = DM9331 is able to perform 100BASE-TX in half duplex mode 0 = DM9331 is not able to perform 100BASE-TX in half duplex mode
1.12	Reserved	0,RO/P	**Reserved**
1.11	Reserved	0,RO/P	**Reserved**
1.10-1.7	Reserved	0,RO	**Reserved:** Write as 0, ignore on read
1.6	MF preamble suppression	0,RO	**MII frame preamble suppression:** 1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed
1.5	Auto-negotiation Complete	0,RO	**Auto-negotiation complete:** 1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed
1.4	Remote fault	0, RO/LH	**Remote fault:** 1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM9331 implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0 = No remote fault condition detected
1.3	Auto-negotiation ability	1,RO/P	**Auto configuration ability:** 1 = DM9331 is able to perform auto-negotiation 0 = DM9331 is not able to perform auto-negotiation
1.2	Link status	0,RO/LL	**Link status:** 1 = Valid link is established (for 100Mbps operation) 0 = Link is not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface
1.1	Reserved	0,RO/LH	**Reserved**
1.0	Extended capability	1,RO/P	**Extended capability:** 1 = Extended register capable. 0 = Basic register capable only

Auto-negotiation Advertisement Register (ANAR) - 04
This register contains the advertised abilities of this DM9331 device as they will be transmitted to its link partner during Auto-negotiation.

Bit	Bit Name	Default	Description
4.15	NP	0,RO/P	**Next page indication:** 0 = No next page available 1 = Next page available The DM9331 has no next page, so this bit is permanently set to 0
4.14	ACK	0,RO	**Acknowledge:** 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM9331's auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the auto-negotiation process. Software should not attempt to write to this bit.
4.13	RF	0, RW	**Remote fault:** 1 = Local device senses a fault condition 0 = No fault detected
4.12-4.11	Reserved	0, RW	**Reserved:** Write as 0, ignore on read
4.10	FCS	0, RW	**Flow control support:** 1 = Controller chip supports flow control ability 0 = Controller chip doesn't support flow control ability
4.9	T4	0, RO/P	**100BASE-T4 support:** 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 is not supported The DM9331 does not support 100BASE-T4 so this bit is permanently set to 0
4.8	TX_FDX	1, RW	**100BASE-TX full duplex support:** 1 = 100BASE-TX full duplex is supported by the local device 0 = 100BASE-TX full duplex is not supported
4.7	TX_HDX	1, RW	**100BASE-TX support:** 1 = 100BASE-TX is supported by the local device 0 = 100BASE-TX is not supported
4.6	Reserved	0, RW	**Reserved**
4.5	Reserved	0, RW	**Reserved**
4.4-4.0	Selector	<00001>, RW	**Protocol selection bits:** These bits contain the binary encoded protocol selector supported by this node. <00001> indicates that this device supports IEEE 802.3 CSMA/CD.

Auto-negotiation Link Partner Ability Register (ANLPAR) – 05
This register contains the advertised abilities of the link partner when received during Auto-negotiation.

Bit	Bit Name	Default	Description
5.15	NP	0, RO	**Next page indication:** 0 = Link partner, no next page available 1 = Link partner, next page available
5.14	ACK	0, RO	**Acknowledge:** 1 = Link partner ability data reception acknowledged

			0 = Not acknowledged The DM9331's auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit.
5.13	RF	0, RO	**Remote Fault:** 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner
5.12-5.11	Reserved	X, RO	**Reserved:** Write as 0, ignore on read
5.10	FCS	0, RW	**Flow control support:** 1 = Controller chip supports flow control ability by link partner 0 = Controller chip doesn't support flow control ability by link partner
5.9	T4	0, RO	**100BASE-T4 support:** 1 = 100BASE-T4 is supported by the link partner 0 = 100BASE-T4 is not supported by the link partner
5.8	TX_FDX	0, RO	**100BASE-TX full duplex support:** 1 = 100BASE-TX full duplex is supported by the link partner 0 = 100BASE-TX full duplex is not supported by the link partner
5.7	TX_HDX	0, RO	**100BASE-TX support:** 1 = 100BASE-TX half duplex is supported by the link partner 0 = 100BASE-TX half duplex is not supported by the link partner
5.6	10_FDX	0, RO	**10BASE-T full duplex support:** 1 = 10BASE-T full duplex is supported by the link partner 0 = 10BASE-T full duplex is not supported by the link partner
5.5	10_HDX	0, RO	**10BASE-T support:** 1 = 10BASE-T half duplex is supported by the link partner 0 = 10BASE-T half duplex is not supported by the link partner
5.4-5.0	Selector	<00000>, RO	**Protocol selection bits:** Link partner's binary encoded protocol selector

Auto-negotiation Expansion Register (ANER)- 06

6.15-6.5	Reserved	X, RO	**Reserved:** Write as 0, ignore on read
6.4	PDF	0, RO/LH	**Local device parallel detection fault:** PDF = 1 : A fault detected via parallel detection function. PDF = 0 : No fault detected via parallel detection function
6.3	LP_NP_ABLE	0, RO	**Link partner next page able:** LP_NP_ABLE = 1 : Link partner, next page available LP_NP_ABLE = 0 : Link partner, no next page
6.2	NP_ABLE	0,RO/P	**Local device next page able:** NP_ABLE = 1 : DM9331, next page available NP_ABLE = 0 : DM9331, no next page DM9331 does not support this function, so this bit is always 0.
6.1	PAGE_RX	0, RO/LH	**New page received:** A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management.
6.0	LP_AN_ABLE	0, RO	**Link partner auto-negotiation able:** A "1" in this bit indicates that the link partner supports Auto-negotiation.

DAVICOM Specified Configuration Register (DSCR) - 16

Bit	Bit Name	Default	Description
16.15	BP_4B5B	0, RW	**Bypass 4B5B encoding and 5B4B decoding :** 1 = 4B5B encoder and 5B4B decoder function bypassed 0 = Normal 4B5B and 5B4B operation
16.14	BP_SCR	0, RW	**Bypass scrambler/descrambler function :** 1 = Scrambler and descrambler function bypassed 0 = Normal scrambler and descrambler operation
16.13	BP_ALIGN	0, RW	**Bypass symbol alignment function:** 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0 = Normal operation
16.12	BP_ADPOK	0, RW	**BYPASS ADPOK :** Force signal detector (SD) active. This register is for debug only, not release to customer. 1=Force SD is OK, 0=Normal operation
16.11	Reserved	0,RW	**Reserved**
16.10	TX	1, RW	**100BASE-TX or FX mode control:** 1 = 100BASE-TX operation 0 = 100BASE-FX operation
16.9	FEF	0, RW	**Far End Fault enable :** Control the Far End Fault mechanism associated with 100Base-FX operation. 1 = Enable 0 = Disable
16.8	Reserved	1, RW	**Reserved:** Write as 1.
16.7	F_LINK_100	0, RW	**Force good link in 100Mbps:** 0 = Normal 100Mbps operation 1 = Force 100Mbps good link status This bit is useful for diagnostic purposes.
16.6	Reserved	0, RW	**Reserved:** **Write as 0.**
16.5	Reserved	0, RO	**Reserved:** Write as 0, ignore on read.
16.4	RPDCTR-EN	1, RW	**Reduced power down control enable:** This bit is used to enable automatic reduced power down. 0: Disable automatic reduced power down. 1: Enable automatic reduced power down.
16.3	SMRST	0, RW	**Reset state machine:** When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed.
16.2	MFPSC	0, RW	**MF preamble suppression control:** MCI frame preamble suppression control bit 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off
16.1	SLEEP	0, RW	**Sleep mode:**

			Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset
16.0	RLOUT	0, RW	**Remote loopout control:** When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for bit error rate testing

DAVICOM Specified Configuration and Status Register (DSCSR) - 17

Bit	Bit Name	Default	Description
17.15	100FDX	1, RO	**100M full duplex operation mode:** After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M full duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode.
17.14	100HDX	1, RO	**100M half duplex operation mode:** After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M half-duplex mode. The software can read bit[15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode.
17.13	Reserved	0, RO	**Reserved**
17.12	Reserved	0, RO	**Reserved**
17.11-17.9	Reserved	0, RO	**Reserved:** Read as 0, ignore on write
17.8-17.4	Reserved	0, RW	**Reserved**.
17.3-17.0	ANMB[3:0]	0, RO	**Auto-negotiation monitor bits:** These bits are for debug only. The auto-negotiation status will be written to these bits.

B3	b2	b1	b0	
0	0	0	0	In IDLE state
0	0	0	1	Ability match
0	0	1	0	Acknowledge match
0	0	1	1	Acknowledge match fail
0	1	0	0	Consistency match
0	1	0	1	Consistency match fail
0	1	1	0	Parallel detects signal_link_ready
0	1	1	1	Parallel detects signal_link_ready fail
1	0	0	0	Auto-negotiation completed successfully

DAVICOM Specified Interrupt Register – 21

Bit	Bit Name	Default	Description
21.15	INTR PEND	0, RO	**Interrupt pending :** Indicates that the interrupt is pending and is cleared by the current read. This bit shows the same result as bit 0. (INTR Status)
21.14-21.12	Reserved	0, RO	**Reserved**
21.11	FDX mask	1, RW	**Full-duplex interrupt mask :** When this bit is set, the Duplex status change will not generate the interrupt
21.10	Reserved	1, RW	**Reserved**
21.9	LINK mask	1, RW	**Link interrupt mask :** When this bit is set, the link status change will not generate the interrupt
21.8	INTR mask	1, RW	**Master interrupt mask :** When this bit is set, no interrupts will be generated under any condition.
21.7-21.5	Reserved	0, RO	**Reserved**
21.4	FDX change	0,RO/LH	**Duplex status change interrupt :** “1” indicates a change of duplex since last register read. A read of this register will clear this bit.
21.3	Reserved	0, RO/LH	**Reserved**
21.2	LINK change	0, RO/LH	**Link status change interrupt :** “1” indicates a change of link since last register read. A read of this register will clear this bit.
21.1	Reserved	0, RO	**Reserved**
21.0	INTR status	0, RO/LH	**Interrupt status :** The status of MDINTR#. “1” indicates that the interrupt mask is off that one or more of the change bits are set. A read of this register will clear this bit.

Absolute Maximum Ratings

Absolute Maximum Ratings (25°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVCC, AVCC	Supply Voltage	-0.3	3.6	V	
VIN	DC Input Voltage (VIN)	-0.5	5.5	V	
VOUT	DC Output Voltage(VOUT)	-0.3	3.6	V	
Tstg	Storage Temperature Rang (Tstg)	-65	+125	°C	EIAJ-4701B
Tc	Case Temperature	0	85	°C	
LT	Lead Temp. (TL, Soldering, 10 sec.)	---	235	°C	JEDEC J-STD-020A

Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVCC,AVCC	Supply Voltage	3.135	3.465	V	
TA	Operating Ambient Temperature	0	70	°C	
Tc	Case Temperature	0	85	°C	As TA = 70°C
PD (Power Dissipation)	100BASE-TX	---	88	mA	3.3V
	100BASE-FX	---	25	mA	3.3V
	Auto-negotiation	---	45	mA	3.3V
	Power Reduced Mode (without cable)	---	18	mA	3.3V
	Power Down Mode	---	3	mA	3.3V

Comments

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 3.3V, TA = 0 ~ 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
TTL Inputs (TXD0, TXD1, TXEN, LNKFAULTPROG, LNKFAULTEN, MDC, MDIO,CHIPEN, OPMODE0-2, TPSET0, TPSET1, DISFEF,SCRAMEN, RESET#)						
VIL	Input Low Voltage	---	---	0.8	V	
VIH	Input High Voltage	2.0	---	---	V	
IIL	Input Low Leakage Current	---	---	10	uA	VIN = 0.4V
IIH	Input High Leakage Current	---	---	-10	uA	VIN = 2.7V
MCI TTL Outputs (RXD0, RXD1, RXDV, RXER,TPFAULT, FXFAULT MDIO)						
VOL	Output Low Voltage	---	---	0.4	V	IOL = 4mA
VOH	Output High Voltage	2.4	---	---	V	IOH = -4mA
Non-MCI TTL Outputs (LINKLED#, ACTIVELED#, FULL/HALFLED#, FAULTLED#, MDINTR#)						
VOL	Output Low Voltage	---	---	0.4	V	IOL = 2mA
VOH	Output High Voltage	2.4	---	---	V	IOH = -2mA
Receiver						
VICM	RX+/RX- Common mode Input Voltage	---	1.2	---	V	100 Ω Termination Across
Transmitter						
VTD100	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
ITD100	100TX+/- Differential Output Current	|19|	|20|	|21|	mA	
VOH	PECL Output Voltage – High	VCC-1.05		VCC-0.88	V	
VOL	PECL Output Voltage – Low	VCC-1.81		VCC-1.62	V	
VIH	PECL Input Voltage – High	VCC-1.16		VCC-0.88	V	
VIL	PECL Input Voltage – Low	VCC-1.81		VCC-1.48	V	
IFD100	100FX+/- Differential Output Current	|17|	|18|	|19|	mA	

AC Electrical Characteristics & Timing Waveforms

TP Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_{TR/F}$	100TX+/- Differential Rise/Fall Time	3.0	---	5.0	ns	
t_{TM}	100TX+/- Differential Rise/Fall Time Mismatch	0	---	0.5	ns	
t_{TDC}	100TX+/- Differential Output Duty Cycle Distortion	0	---	0.5	ns	
$t_{T/T}$	100TX+/- Differential Output Peak-to-Peak Jitter	0	---	1.4	ns	
X_{OST}	100TX+/- Differential Voltage Overshoot	0	---	5	%	

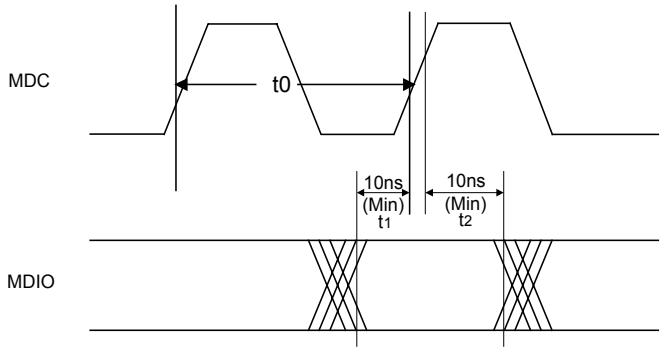
Oscillator Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CKC}	OSC Cycle Time	19.998	20	20.002	ns	50ppm
t_{PWH}	OSC Pulse Width High	8	10	12	ns	
t_{PWL}	OSC Pulse Width Low	8	10	12	ns	

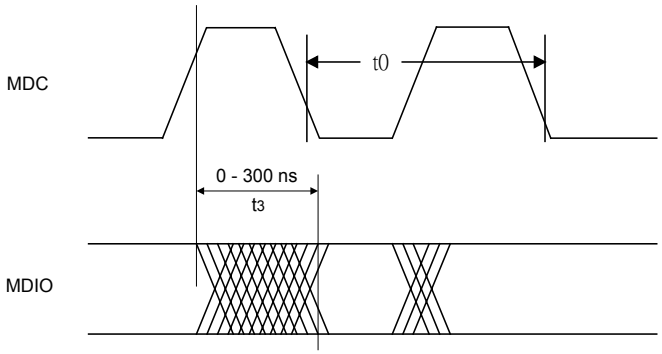
MDC/MDIO Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_0	MDC Cycle Time	80	---	---	ns	
t_1	MDIO Setup Before MDC	10	---	---	ns	When OUTPUT By STA
t_2	MDIO Hold After MDC	10	---	---	ns	When OUTPUT By STA
t_3	MDC To MDIO Output Delay	0	---	300	ns	When OUTPUT By DM9331

MDIO timing when OUTPUT by STA



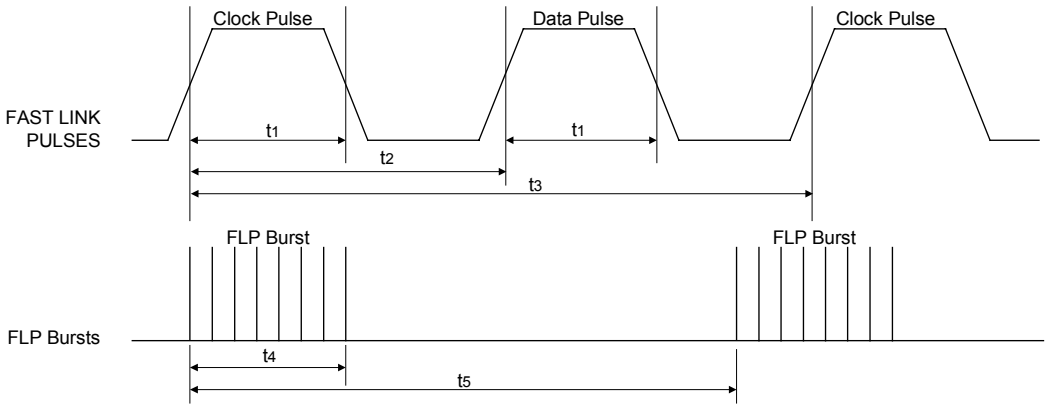
MDIO timing when OUTPUT by DM9331



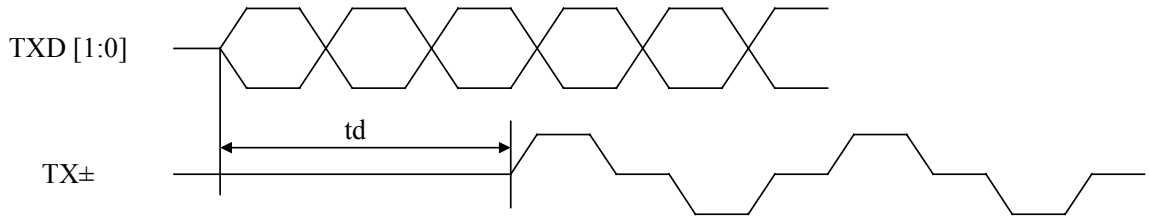
Auto-negotiation and Fast Link Pulse Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t1	Clock/Data Pulse Width	---	100	---	ns	
t2	Clock Pulse To Data Pulse Period	55.5	62.5	69.5	us	DATA = 1
t3	Clock Pulse To Clock Pulse Period	111	125	139	us	
t4	FLP Burst Width	-	2	-	ms	
t5	FLP Burst To FLP Burst Period	8		24	ms	
-	Clock/Data Pulses in a Burst	17		33	pulse	

Auto-negotiation and Fast Link Pulse Timing Diagram



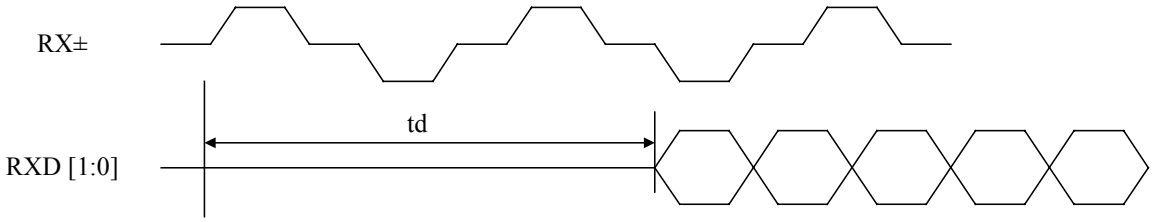
TXD to TP or FX Transmit Latency Timing Diagram



TXD to TP or FX Transmit Latency Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
td	TXD[1:0] to TX± or FXTD± (TX Latency)	-	-	165	ns	

TP or FX to RXD Receive Latency Timing Diagram



TP or FX to RXD Receive Latency Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
td	RX± or FXRD± to RXD[1:0] (RX Latency)	-	-	205	ns	

Application Notes

Network Interface Signal Routing

Place the transformer as close as possible to the RJ-45 connector. Place all the 50Ω resistors as close as possible to the DM9331 RX± and TX± pins. Traces routed from RX± and TX± to the transformer should run in close pairs directly to the transformer. The designer should be careful not to place the transmit pair across the receive pair. As always, vias should be avoided as much as possible. The network interface should be void of any signals other than the TX± and RX± pairs between the RJ-45 to the transformer and the transformer to the DM9331. There should be no power or ground planes in the area under the network side of the transformer to include the area under the RJ-45 connector. (Refer to Figure 5 and 6.) Keep chassis ground away from all active signals. The RJ-45 connector and any unused pin should be tied to chassis ground through a resistor divider network and a 2KV bypass capacitor.

The Band Gap resistor should be placed as physically close to pins 47 and 48 as possible. (Refer to Figure 1, 2, 3-1, and 3-2). The designer should not run any high-speed signal near the Band Gap resistor placement.

1. 100Base-TX Side Application

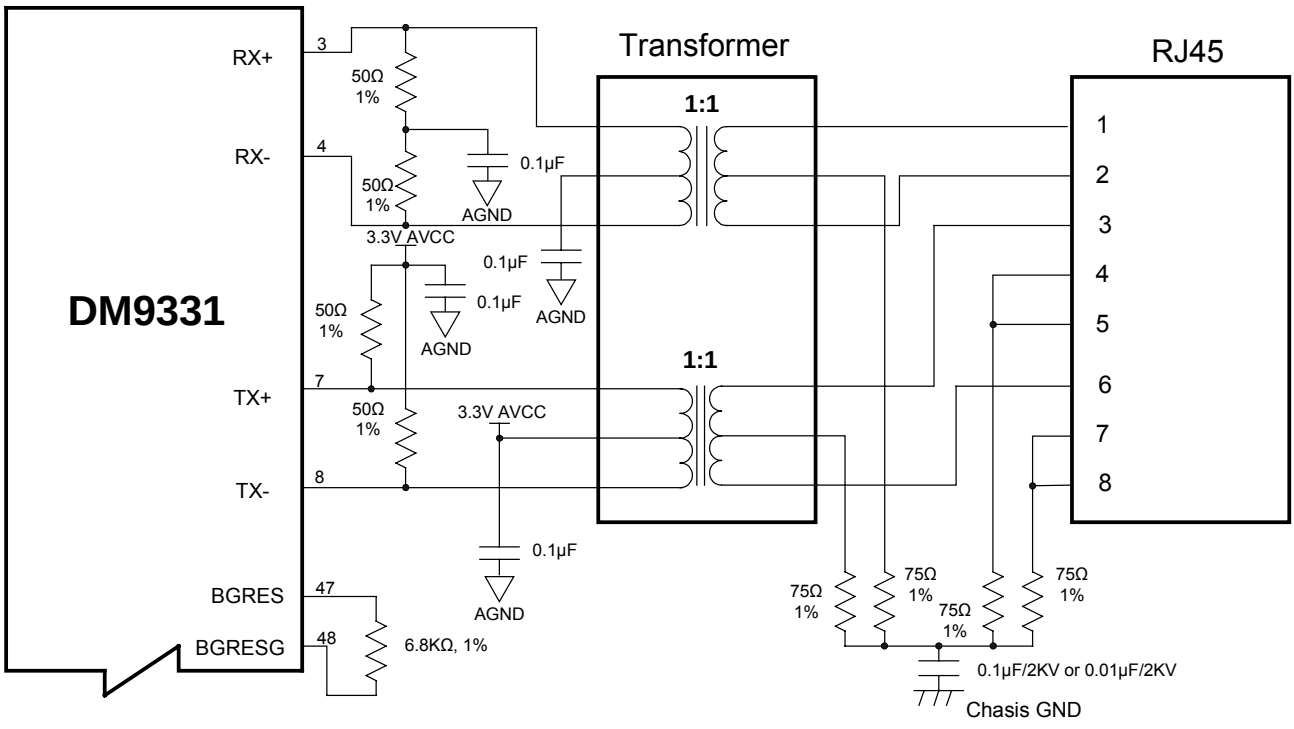


Figure 1

2. 100Base-TX Side (Power Reduction Application)

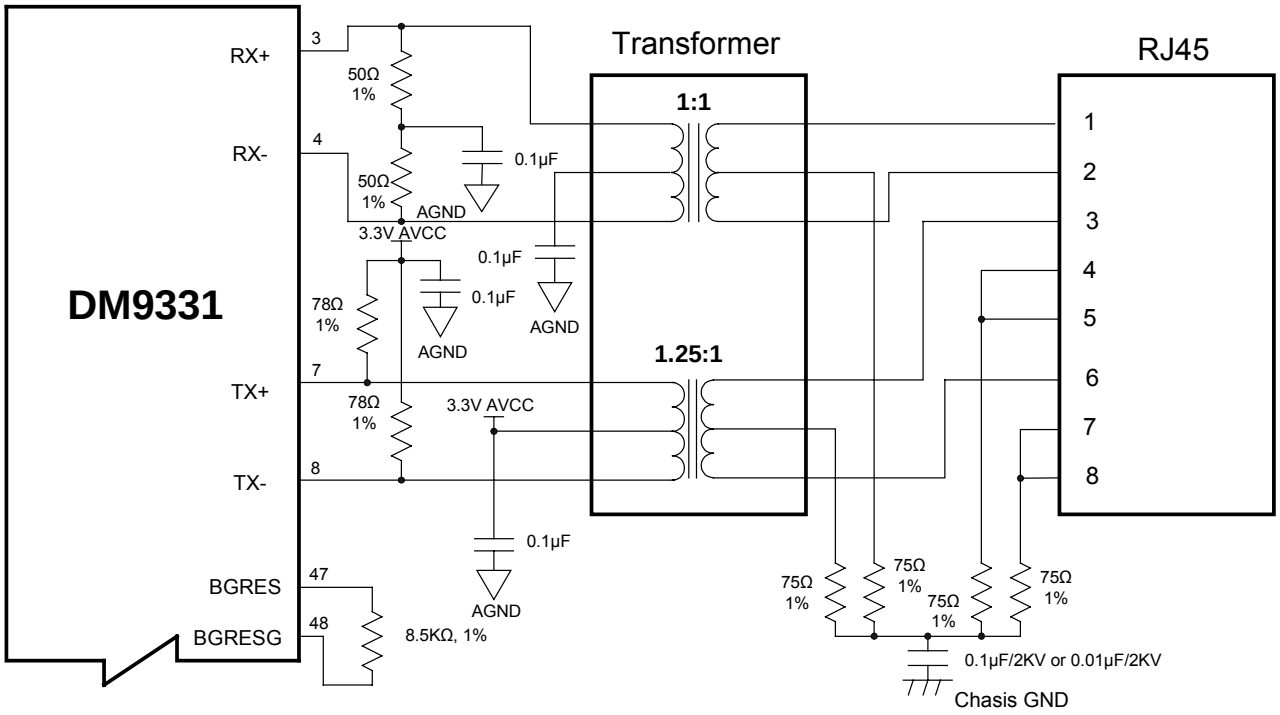


Figure 2

3. 100Base-FX Side Application

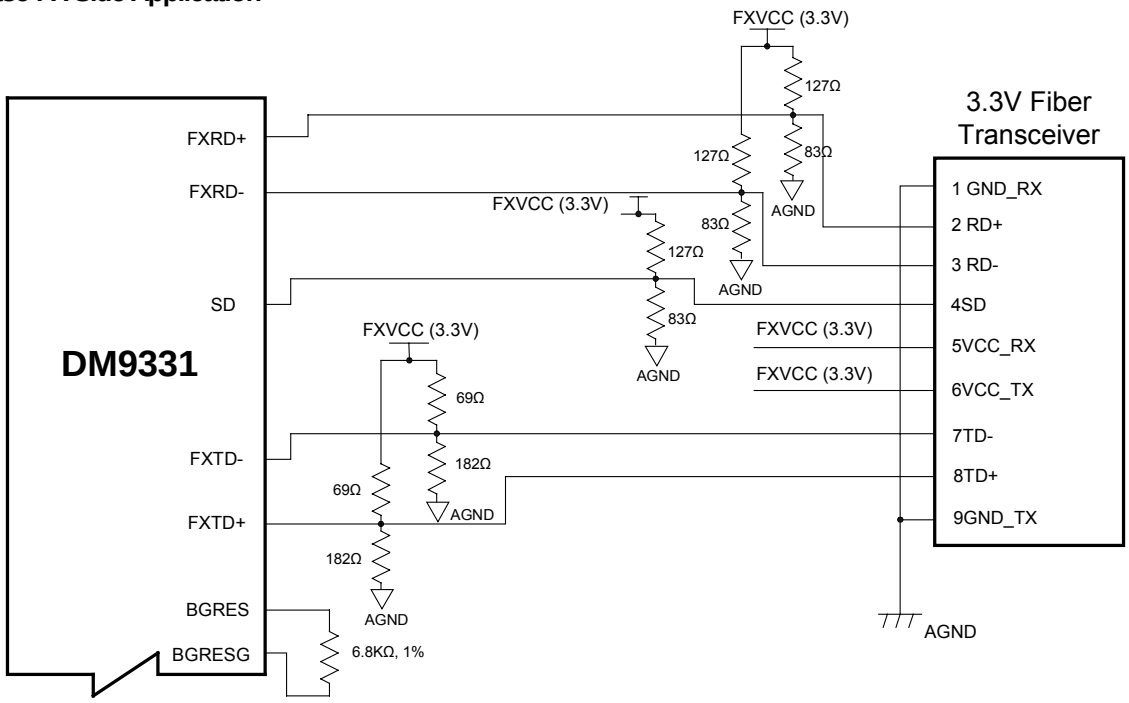


Figure 3-1

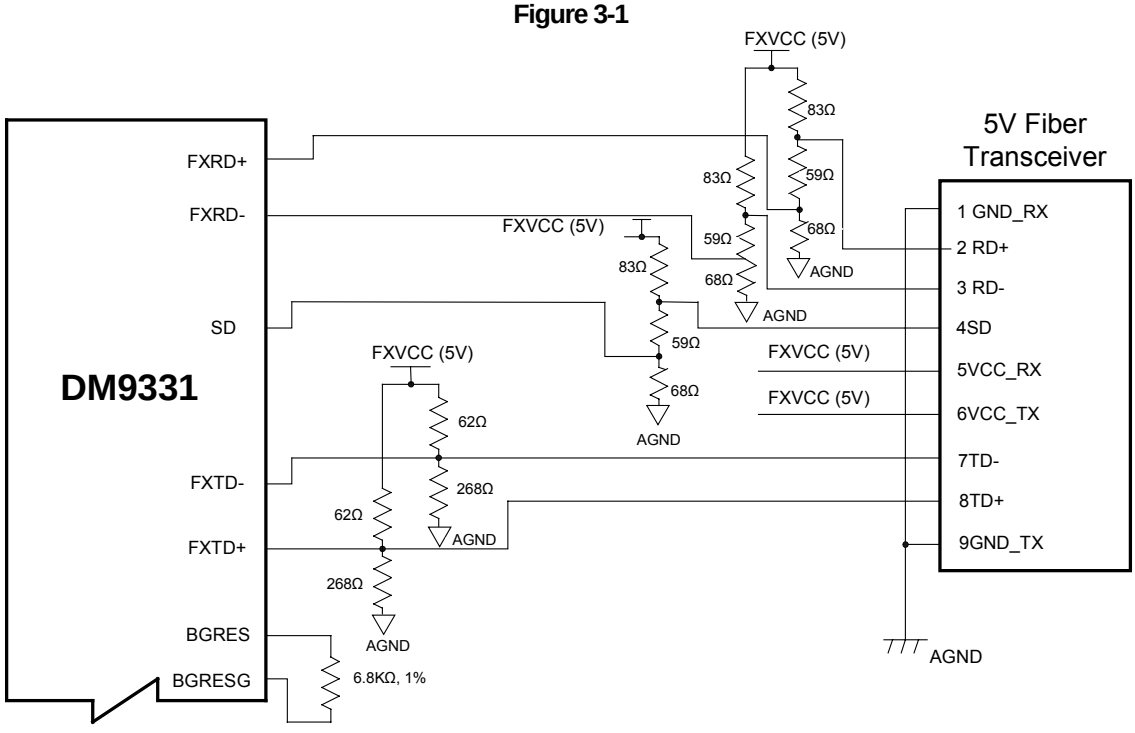


Figure 3-2

4. Power Decoupling Capacitors

Davicom Semiconductor recommends all the decoupling capacitors for all power supply pins are placed as close as possible to the power pads of the DM9331 (The best placed distance is < 3mm from the above mentioned pins). The recommended decoupling capacitance is 0.1μF or 0.01μF, as required by the design layout.

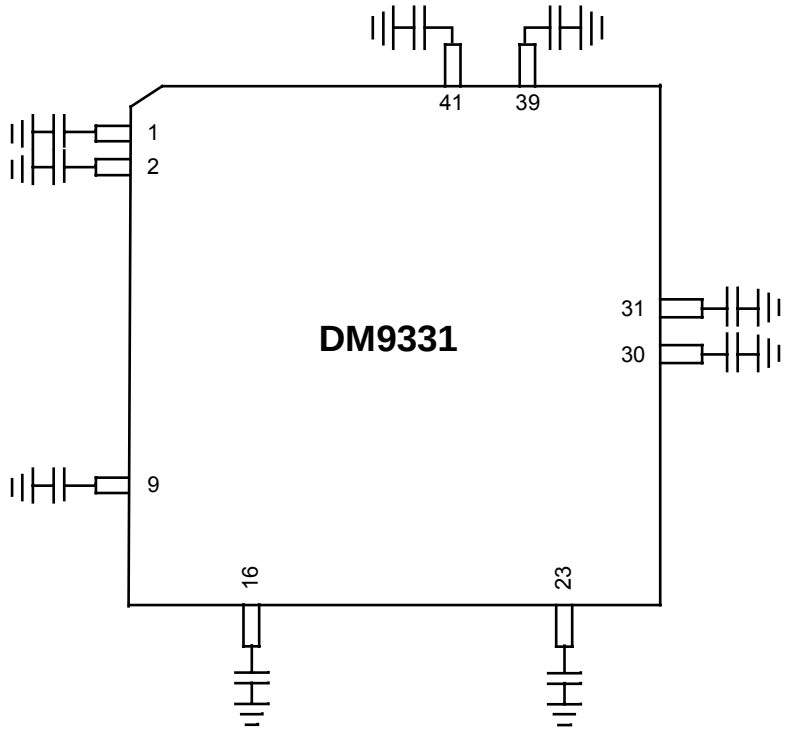


Figure 4

5. Ground Plane Layout

A single ground plane approach is recommended to minimize EMI. Bad ground plane partitioning can cause more EMI emissions that could make the network interface card not compliant with specific FCC regulations (part 15). Figure 5 shows a recommended ground layout scheme.

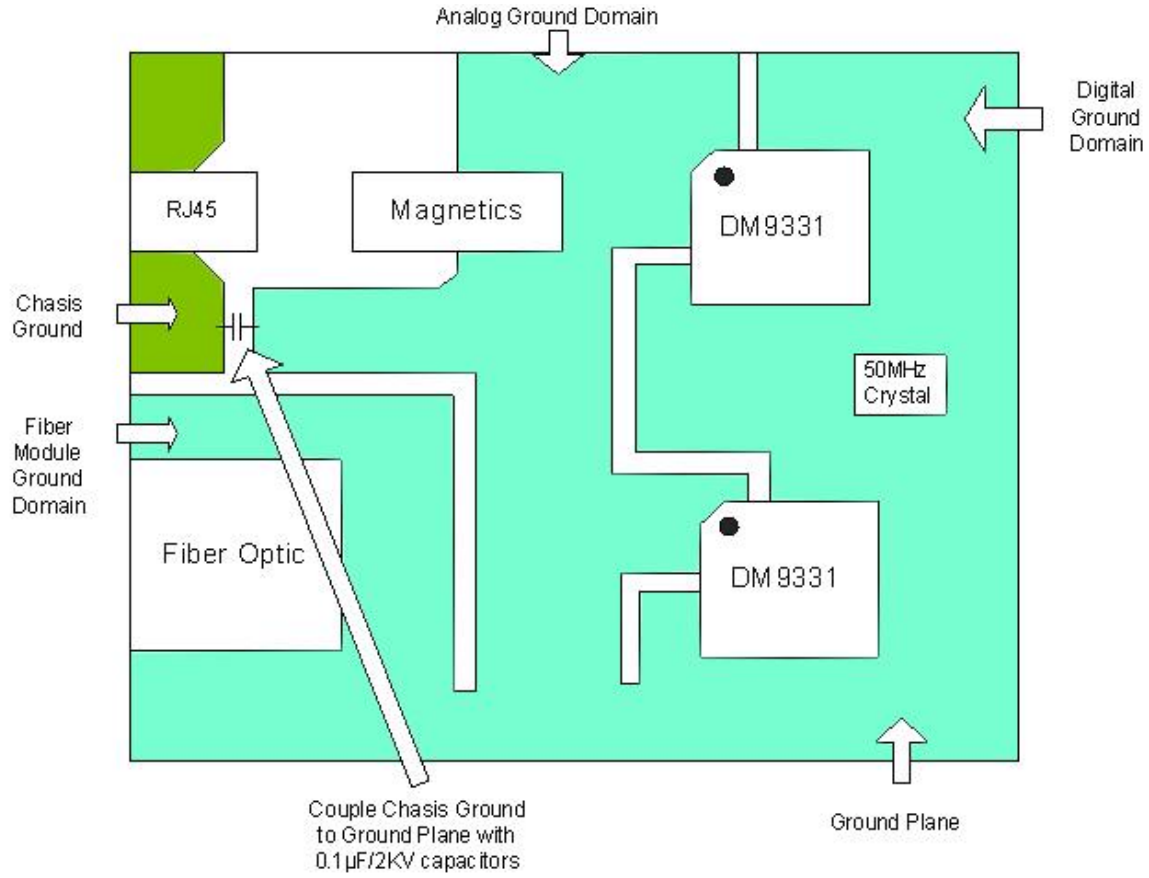


Figure 5

6. Power Plane Partitioning

The power planes are approximately illustrated in Figure 6. The ferrite bead used should have an impedance at least 75 Ω at 100MHz. A suitable bead is the Panasonic surface mound bead, part number EXCCL4532U or an equivalent. A 10μF electrolytic bypass capacitors should be connected between VCC and Ground at each side of the ferrite bead.

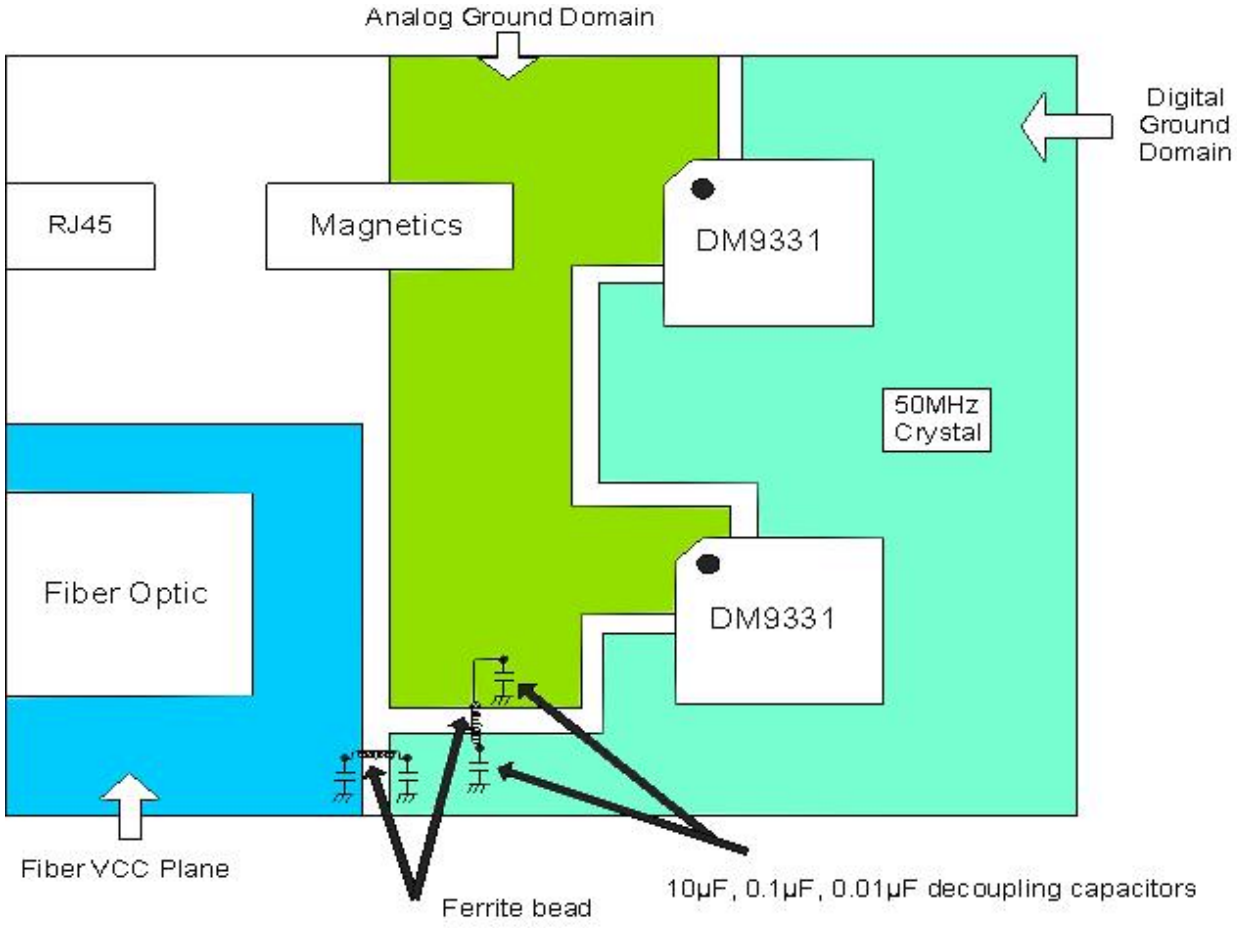


Figure 6

7. Media Converter Interface

Through the Media Converter Interface (MCI), the DM9331 connects to another DM9331 for the FX to TP media converter or FX to FX, TP to TP repeater application.

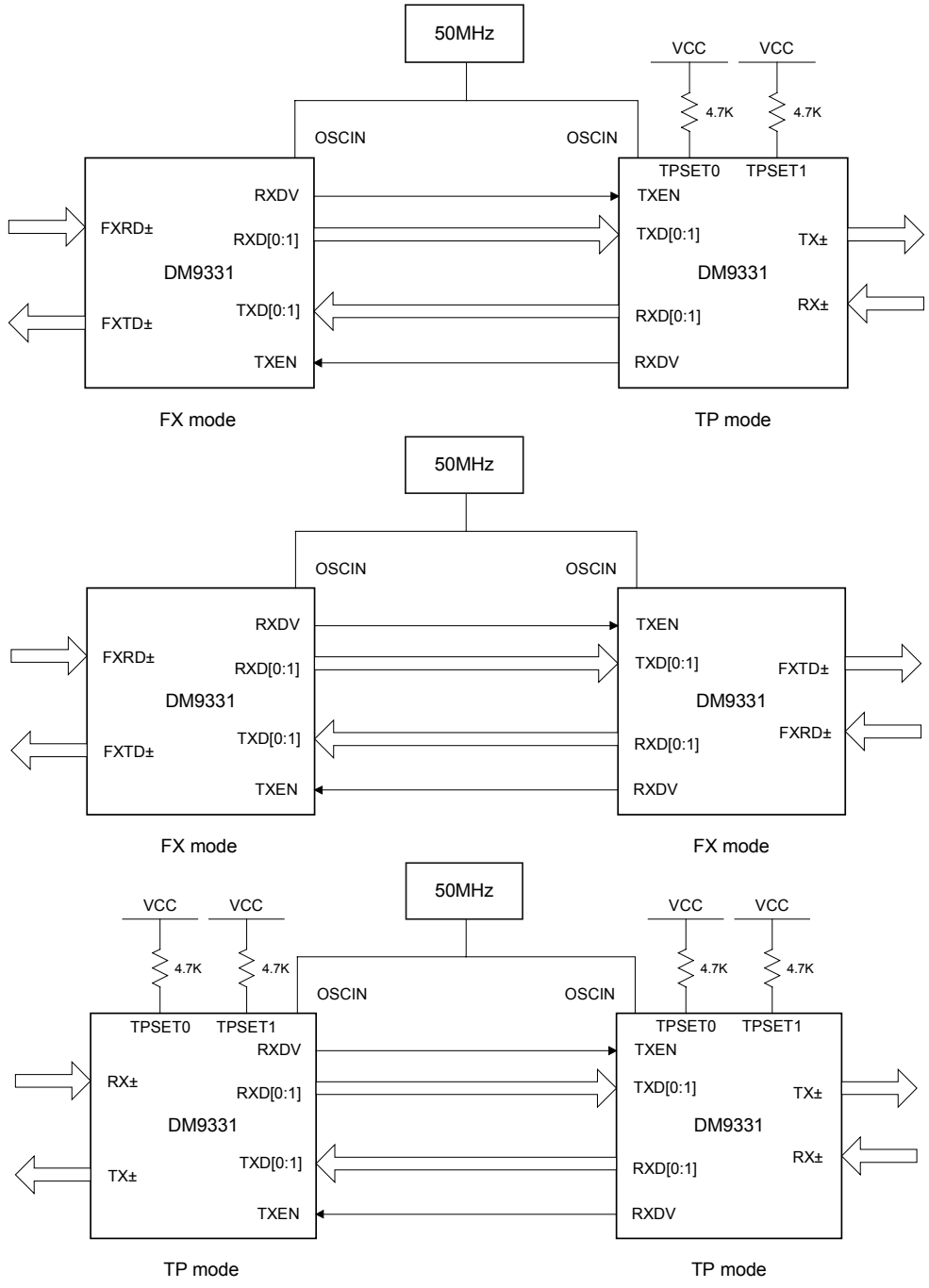


Figure 7

8. Link Fault propagation Application

The DM9331 will propagate link fault signals from media to another DM9331. If link fault happens, the DM9331 will send out fault signal to another DM9331.

In FX mode, there are two types of link failures, receive link failure or remote fault (receive far end fault). In the event of a fiber receive link failure, the DM9331 will send out an FX fault signal. The DM9331 will send out a far end fault signal to the fiber optic media, if the DM9331 receive the fault signal from the other device.

In TP mode, in the event of a TP receive link failure, the DM9331 will send out a TP fault signal. The DM9331 will stop to transmit idle signal to the CAT5 media, if the DM9331 receive the fault signal from the other device.

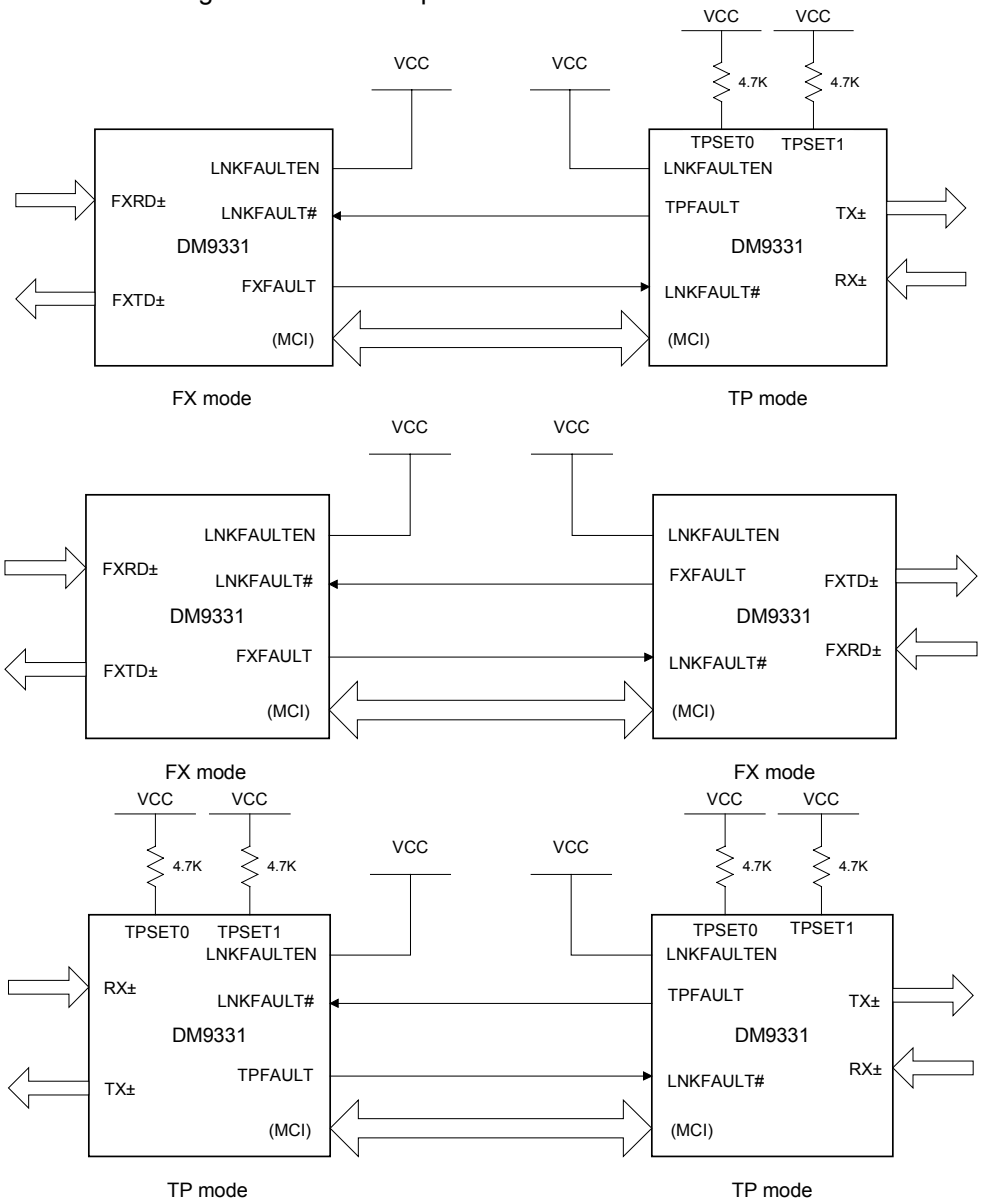


Figure 8

9. Media Converter or Repeater Application

The DM9331 chip set can easily use media converters or repeaters for long distance device connection. You can use two media converters to connect two devices whose distance is 2.2km. See Figure 9-1. If the distance is more than 2.2km, you can add an FX repeater to extend distance. See Figure 9-2. In the last miles, if the distance of the user device is more than 100m, you can add TP repeaters to extend the distance to 400m. See figure 9-3.

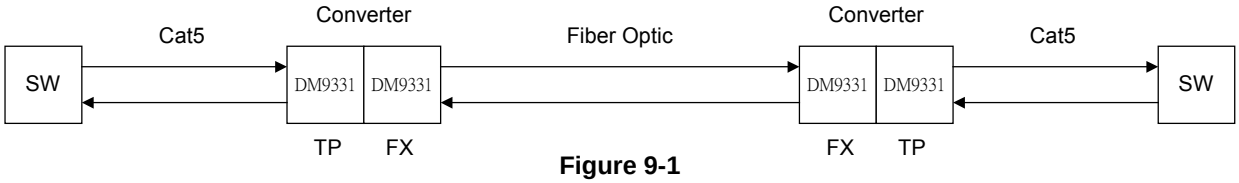


Figure 9-1

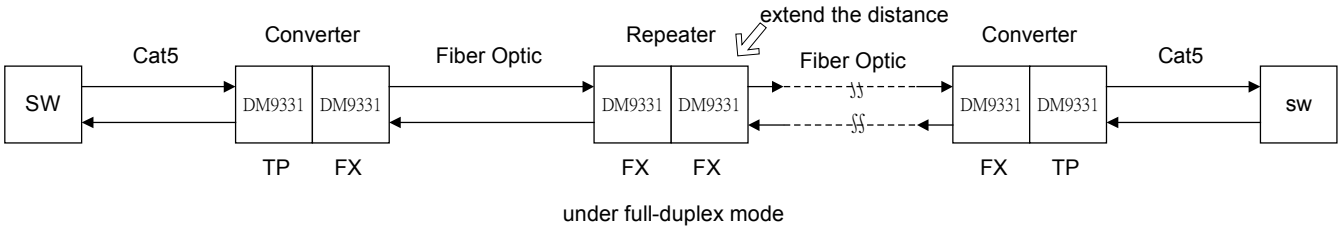


Figure 9-2

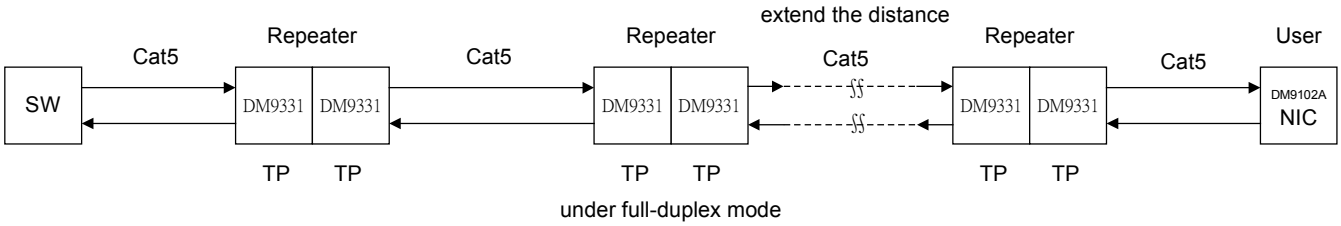


Figure 9-3

10. Link Fault Propagation LED Display

Since the media converter is a "dummy" device, the link fault propagation becomes very important. The devices at the both ends need to know whether the link is OK or Non-OK on the whole path.

Figure 10 shows the DM9331 to the DM9331 connection. The whole path is separated into local device (LD), local converter (LC), remote converter (RC) and remote device (RD), and three segments of transmit and receive connection. Table 10 lists the LED status of all devices. It shows the current link status of all the devices when they are at auto-negotiation modes.

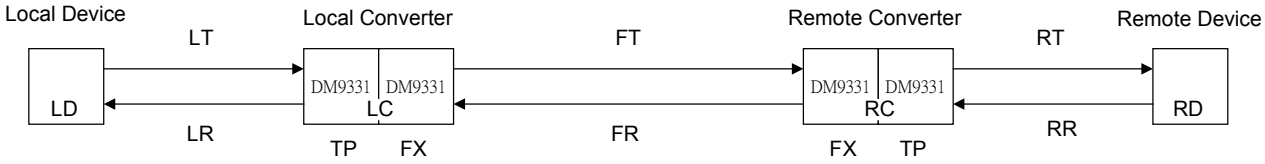


Figure 10

Condition (auto-negotiation)	Local device	Local Converter				Remote Converter				Remote device
	Link LED	TP side		FX side		FX side		TP side		Link LED
		Link LED	Fault LED	Link LED	Fault LED	Link LED	Fault LED	Link LED	Fault LED	
LT disconnect	off	off	on	on	off	on	on	off	off	off
LR disconnect	off	off	off	on	off	on	off	on	off	on
LT & LR disconnect	off	off	on	on	off	on	on	off	off	off
FT disconnect	off	off	off	on	on	off	on	off	off	off
FR disconnect	off	off	off	off	on	on	on	off	off	off
FT & FR disconnect	off	off	off	off	on	off	on	off	off	off
RT disconnect	on	on	off	on	off	on	off	off	off	off
RR disconnect	off	off	off	on	on	on	off	off	on	off
RT & RR disconnect	off	off	off	on	on	on	off	off	on	off

Table 10

Magnetics Selection Guide

Refer to Table 2 for transformer requirements. Transformers meeting these requirements are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetics before using them in an application. The transformers listed in Table 2 are electrical equivalents, but may not be pin-to-pin equivalents.

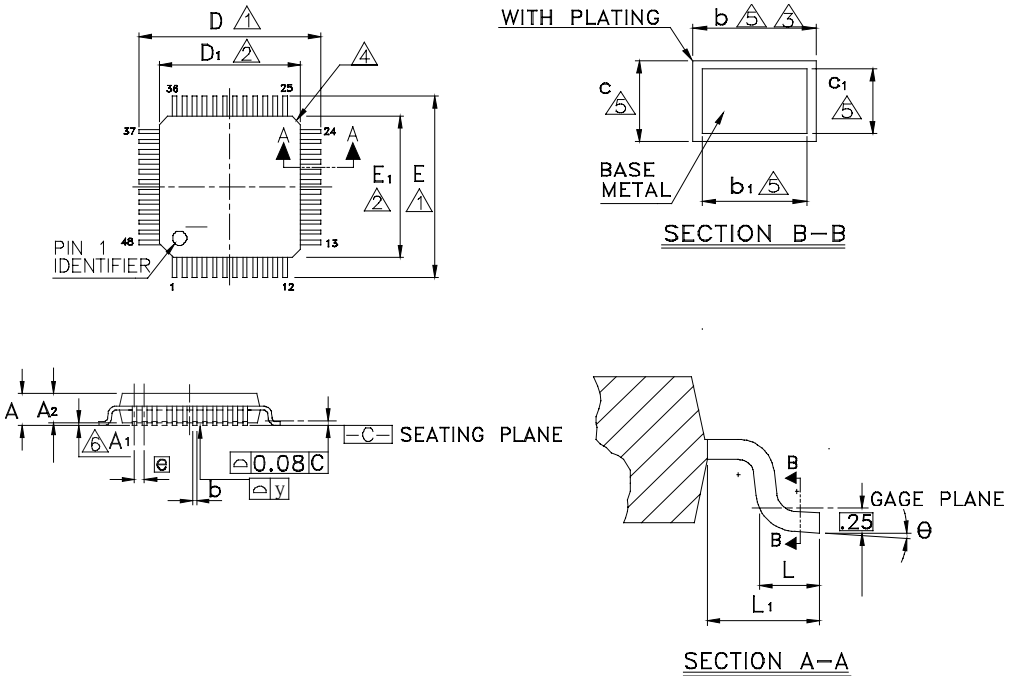
Manufacturer	Part Number
Pulse Engineering	PE-68515, H1078, H1012 H1102
Delta	LF8200, LF8221x
YCL	20PMT04, 20PMT05
Halo	TG22-3506ND, TD22-3506G1, TG22-S010ND TG22-S012ND
Nano Pulse Inc.	NPI 6181-37, NPI 6120-30, NPI 6120-37 NPI 6170-30
Fil-Mag	PT41715
Bel Fuse	S558-5999-01
Valor	ST6114, ST6118
Macronics	HS2123, HS2213

Table 2

Package Information

LQFP 48L (F.P. 2mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.6
A1	0.002	-	0.006	0.05	-	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
b1	0.007	0.008	0.009	0.17	0.20	0.23
C	0.004	-	0.008	0.09	-	0.20
C1	0.004	-	0.006	0.09	-	0.16
D	0.354BSC			9.00BSC		
D1	0.276BSC			7.00BSC		
E	0.354BSC			9.00BSC		
E1	0.276BSC			7.00BSC		
e	0.020BSC			0.50BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	0.039REF			1.00REF		
y	0.004MAX			0.1MAX		
θ	0°	-	12°	0°	-	12°

Notes:

1. To be determined at seating plane.
2. Dimensions D1 and E 1do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimensions b do not include dambar protrusion. Total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7. Controlling dimension: millimeter.
8. Reference documents: JEDEC MS-026 , BBC.

Ordering Information

Part Number	Pin Count	Package
DM9331E	48	LQFP

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WARNING
Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.