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9309.pdf	25-Aug-97 15:14	115K	
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93L38.pdf	01-Apr-98 00:00	136K

National Semiconductor

June 1989

9300/DM9300 4-Bit Parallel-Access Shift Register

General Description

The 9300 4-bit registers feature parallel inputs, parallel outputs, $J\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load and shift (in direction Q_A toward Q_D).

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops, and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the $J\overline{K}$ inputs. These inputs permit the first stage to perform as a $J\overline{K}$, D or T-type flip-flop as shown in the function table.

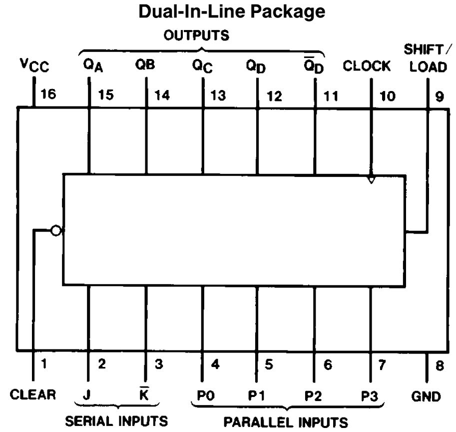
These shift registers are fully compatible with most other TTL and DTL families. All inputs, including the clock, are buffered to lower the drive requirements to one normalized Series 54/74 load.

Features

- Fully buffered inputs
- Direct overriding clear
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Positive edge-triggered clocking
- J and $\overline{K}$ inputs to first stage
- Typical shift frequency—39 MHz

Connection Diagram

Dual-In-Line Package



TL/F/6600–1

Order Number 9300DMQB, 9300FMQB or DM9300N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	P0	P1	P2	P3					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Bn}	$\overline{Q}_{Cn}$

H = High Level (Steady State)

L = Low Level (Steady State)

X = Don't Care

↑ = Transition from low-to-high level

a, b, c, d, = The level of steady state input at P0, P1, P2, or P3 respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent ↑ transition of the clock.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Military Min	Military Nom	Military Max	Commercial Min	Commercial Nom	Commercial Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.48			−0.8	mA
I_{OL}	Low Level Output Current				9.6			16	mA
f_{CLK}	Clock Frequency (Note 5)		0		30	0		30	MHz
t_W	Pulse Width (Note 5)	Clock	17			16	11		ns
		Clear	25			30	15		
t_{SU}	Setup Time (Note 5)	S/L	36			30	13		ns
		Data	18			20	13		
		Clear	36			30	13		
t_H	Data Hold Time (Note 5)		0			0	−11		ns
t_{REL}	S/L Release Time (Notes 1 and 5)		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Input			40	μA
			CP Input			80	
			$\overline{PE}$ Input			92	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Input			−1.6	mA
			CP Input			−3.2	
			$\overline{PE}$ Input			−3.7	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	MIL	−20		−80	mA
			COM	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)	MIL			86	mA
			COM			92	

Note 1: RELEASE TIME: $t_{RELEASE}$ is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) *not* to respond.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

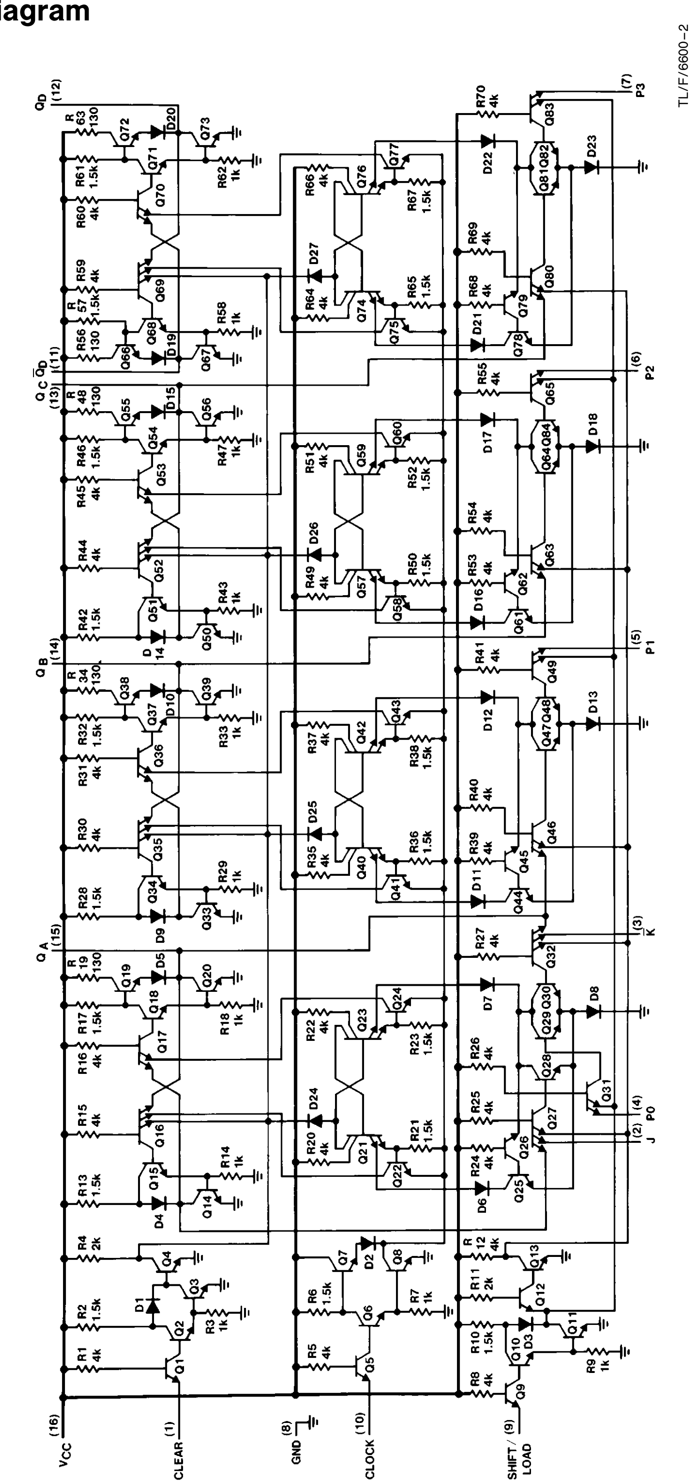
Note 4: With all outputs open, SHIFT/LOAD grounded, and 4.5V applied to J, K, and data inputs, I_{CC} is measured by applying momentary ground, then 4.5V to CLEAR, and then to CLOCK.

Note 5: T_A = 25°C and V_{CC} = 5V.

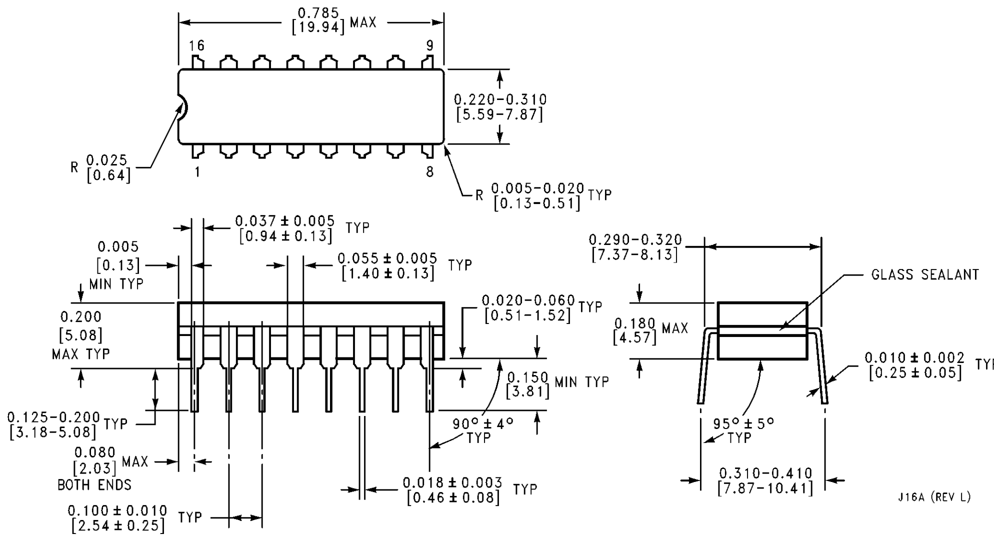
Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Military $R_L = 400\Omega$, $C_L = 15$ pF		Commercial $R_L = 400\Omega$, $C_L = 15$ pF		Units
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		20		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		24		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		37		30	ns

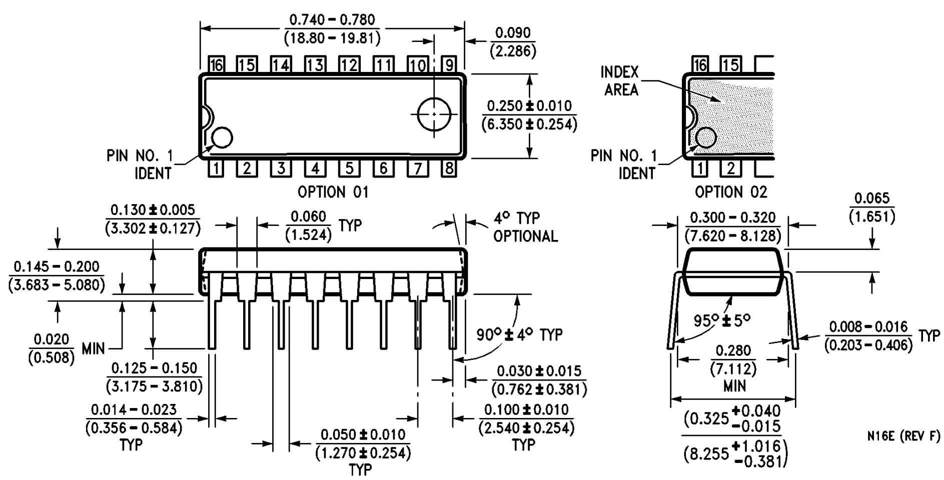
Schematic Diagram



Physical Dimensions inches (millimeters)

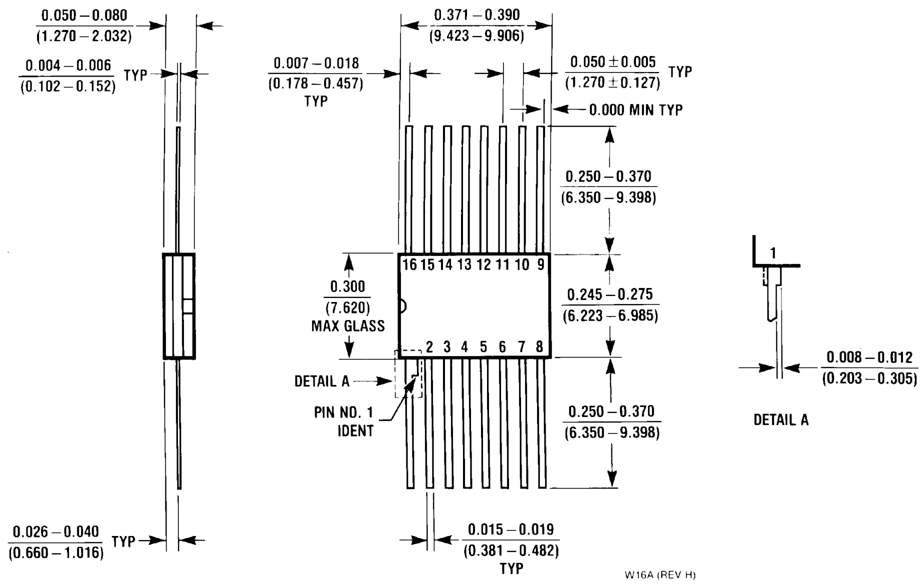


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9300DMQB
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9300N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9300FMQB
NS Package Number W16A

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National Semiconductor

June 1989

9301/DM9301
1-of-10 Decoders

General Description

These BCD-to-decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain "OFF" for all invalid input conditions.

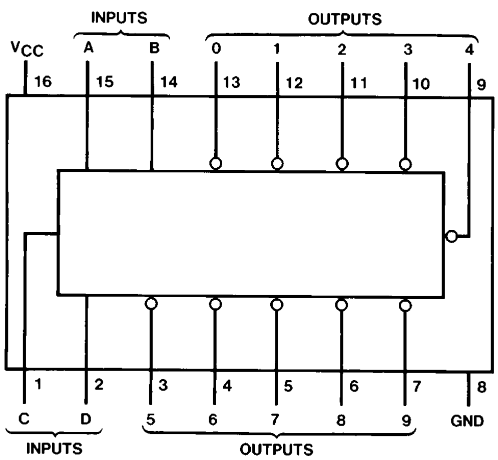
These circuits provide familiar TTL inputs and outputs which are compatible for use with other TTL and DTL circuits. DC noise margins are typically 1V and power dissipation is typically 125 mW. The diode-clamped, buffered inputs represent only one normalized Series 54/74 load.

Features

- Direct replacement for Signetics 8252
- Diode-clamped inputs
- All outputs are high for invalid BCD input conditions
- Typical power dissipation 125 mW
- Typical propagation delay 20 ns

Connection Diagram

Dual-In-Line Package



TL/F/6601–1

Order Number 9301DMQB, 9301FMQB or DM9301N
See NS Package Number J16A, N16E or W16A

Function Table

No.	BCD Inputs				Decimal Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to 70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−70	mA
			COM	−20		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	MIL			44	mA
			COM		25	41	

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

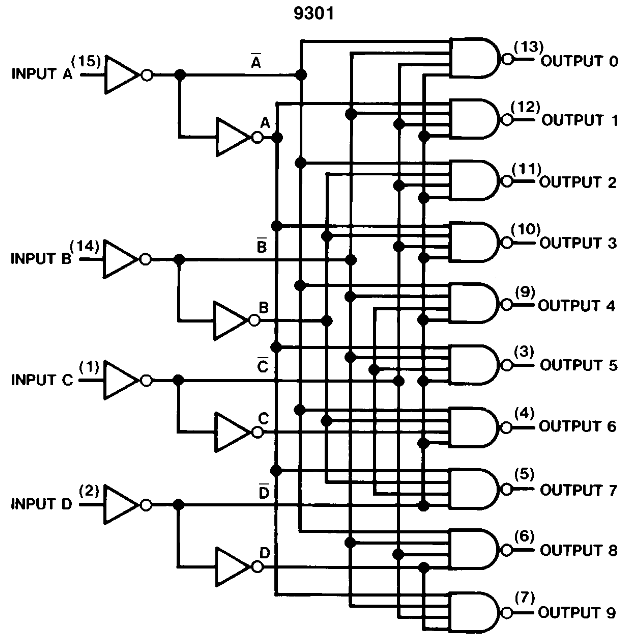
Symbol	Parameter	Conditions	Military		Commercial		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		35		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			30		30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

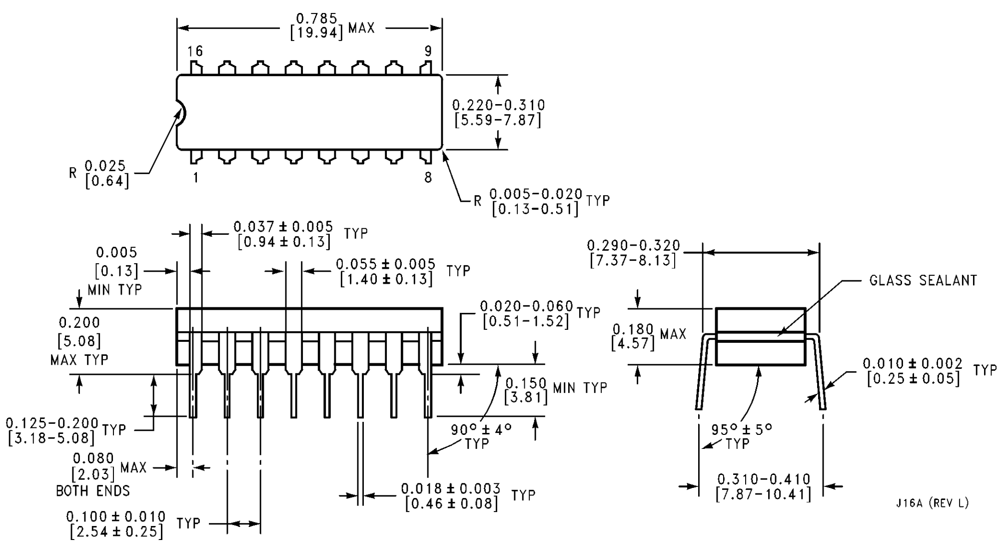
Note 3: I_{CC} is measured with the outputs open and all inputs grounded.

Logic Diagram



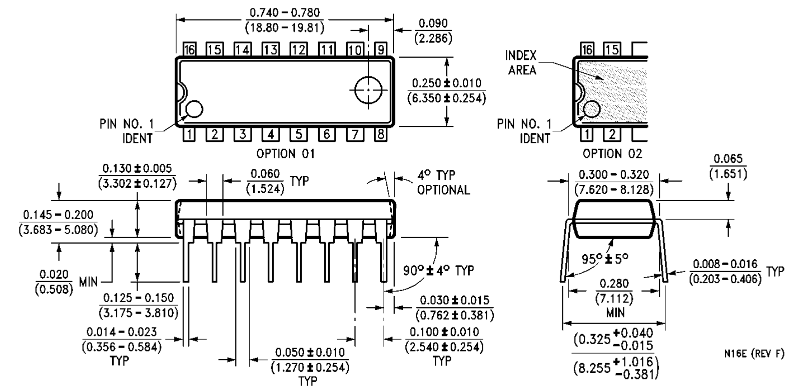
TL/F/6601–2

Physical Dimensions inches (millimeters)

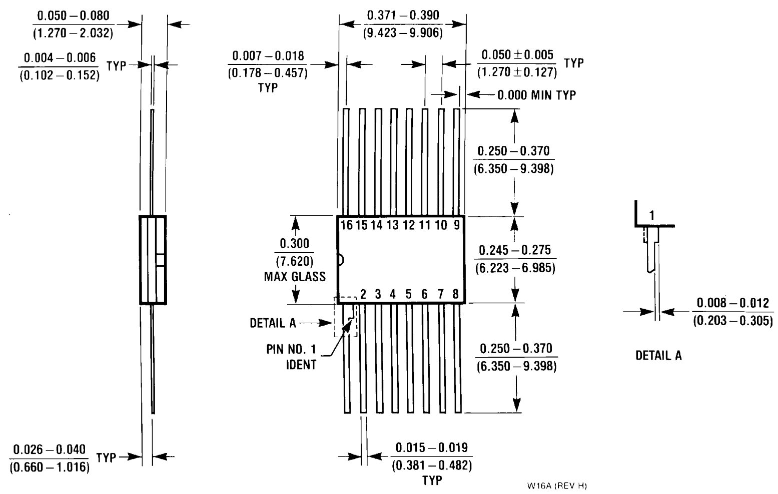


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9301DMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9301N
NS Package Number N16E



16-Lead Ceramic Flat Package (W)
Order Number 9301FMQB
NS Package Number W16A

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National Semiconductor

June 1989

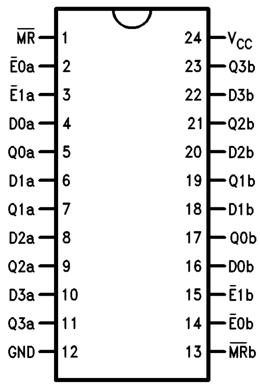
9308/DM9308 Dual 4-Bit Latch

General Description

The 9308 is a dual 4-bit D-type latch designed for general purpose storage applications in digital systems. Each latch contains both an active LOW Master Reset input an active LOW Enable inputs. The 74116 is a pin for pin equivalent of the 9308.

Connection Diagram

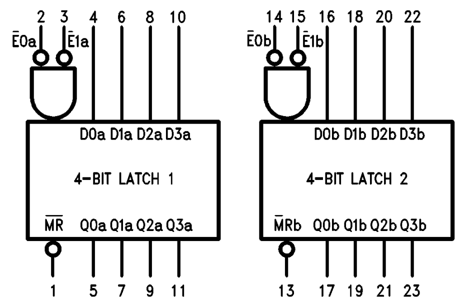
Dual-In-Line Package



TL/F/10208–1

Order Number 9308DMQB, 9308FMQB or DM9308N
See NS Package Number J24A, N24A or W24C

Logic Symbol



TL/F/10208–2

V_{CC} = Pin 24
GND = Pin 12

Pin Names	Description
D_{0a}–D_{3a} D_{0b}–D_{3b}	Parallel Latch Inputs
$\overline{E}_{0a}$, $\overline{E}_{1a}$, $\overline{E}_{0b}$, $\overline{E}_{1b}$	AND Enable Inputs (Active LOW)
$\overline{MR}_a$, $\overline{MR}_b$	Master Reset Inputs (Active LOW)
$\overline{Q}_{0a}$–$\overline{Q}_{3a}$ $\overline{Q}_{0b}$–$\overline{Q}_{3b}$	Parallel Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
COM	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H)	Setup Time HIGH, D_n to $\overline{E}_n$	6			10			ns
t_h (H)	Hold Time HIGH, D_n to $\overline{E}_n$	4			−2.0			ns
t_s (L)	Setup Time LOW, D_n to $\overline{E}_n$	10			12			ns
t_h (L)	Hold Time LOW, D_n to $\overline{E}_n$	4			8			ns
t_w (L)	$\overline{E}_n$ Pulse Width LOW	18			18			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	18			18			ns
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}_n$	10			8			ns

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−70	mA
			COM	−20		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				100	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Functional Description

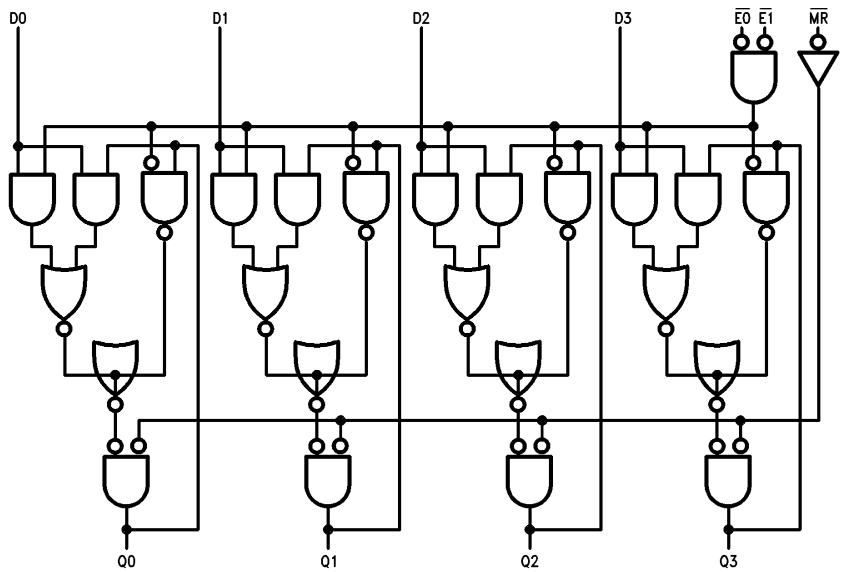
Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input. The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the Master Reset input.

Truth Table

$\overline{MR}$	$\overline{E}0$	$\overline{E}1$	D	Qn	Operation
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Qn−1	Hold
H	H	L	X	Qn−1	Hold
H	H	H	X	Qn−1	Hold
L	X	X	X	L	Reset

Q_{n-1} = Previous Output State
Q_n = Present Output State
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram

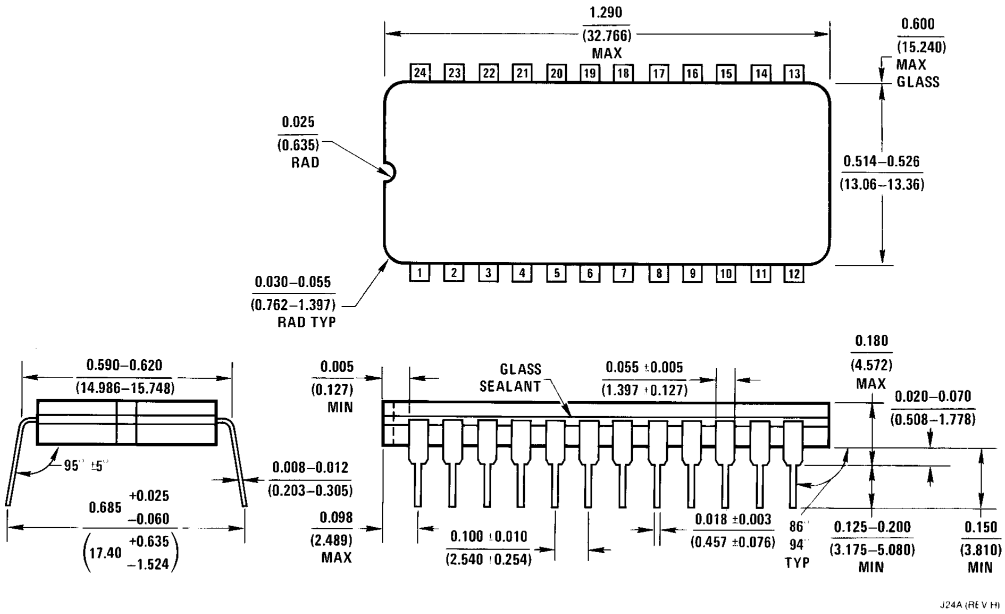


TL/F/10208–3

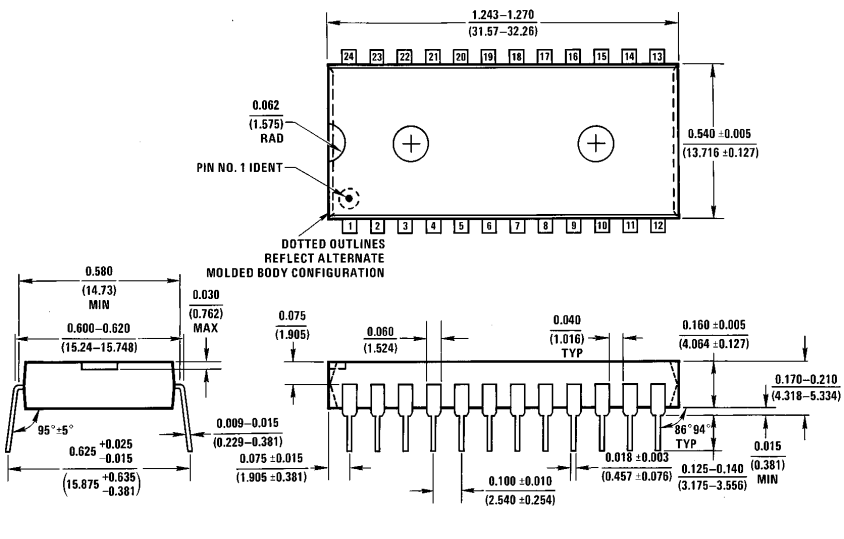
Switching Characteristics V_{CC} = +5.0V, T_A = +25°C (See Section 5 for test waveforms and output load.)

Symbol	Parameter	9308		Units
		C_L = 15 pF, R_L = 400Ω		
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$n to Qn		30 22	ns
t_{PLH} t_{PHL}	Propagation Delay Dn to Qn		15 18	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Qn		22	ns

Physical Dimensions inches (millimeters)

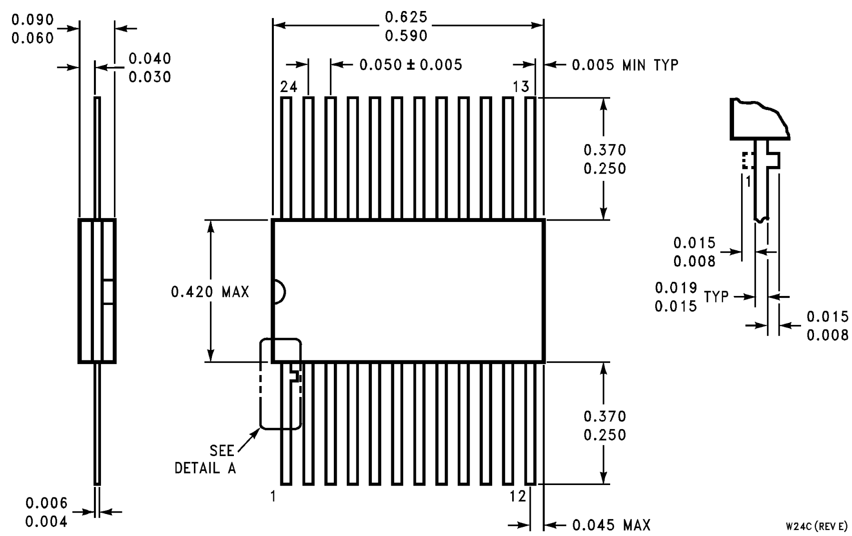


24-Lead Ceramic Dual-In-Line Package (J)
Order Number 9308DMQB
NS Package Number J24A



24-Lead Molded Dual-In-Line Package (N)
Order Number DM9308N
NS Package Number N24A

Physical Dimensions inches (millimeters) (Continued)



24-Lead Ceramic Flat Package (W)
Order Number 9308FMQB
NS Package Number W24C

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National Semiconductor

June 1989

9309/DM9309 Dual 4-Bit Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverter/drivers to supply full complementary, on-chip, binary decoded data selection.

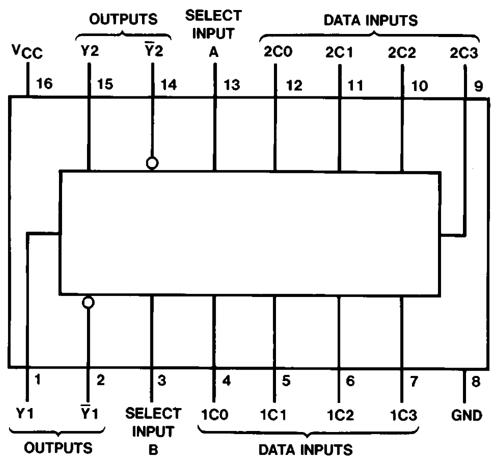
The 9309/DM9309 contains two separate 4-bit multiplexers with complementary Y and $\overline{Y}$ outputs; however, the two sections have common address select inputs.

Features

- Complementary outputs
- Dual one-of-four data selectors

Connection Diagram

Dual-In-Line Package



TL/F/6602–1

Order Number 9309DMQB, 9309FMQB or DM9309N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs						Outputs	
Select		Data				Y	$\overline{Y}$
B	A	C0	C1	C2	C3		
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	H	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−70	mA
			COM	−30		−85	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			27	44	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

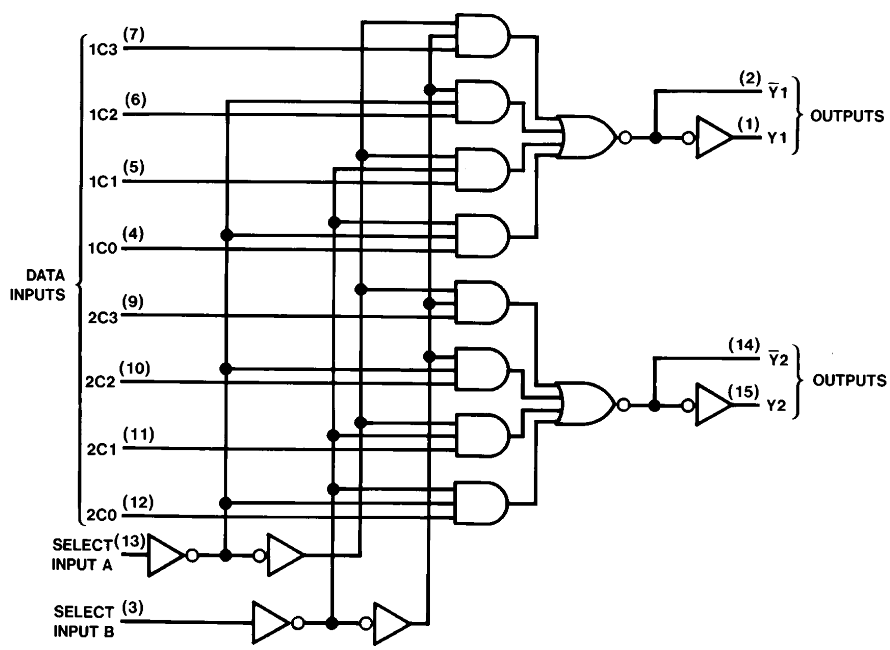
Note 3: I_{CC} is measured with the outputs open and all inputs at 4.5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Military		Commercial		Units
			$R_L = 400\Omega, C_L = 15$ pF				
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		29		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		27		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to $\overline{Y}$		21		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to $\overline{Y}$		21		29	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		20		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		21		34	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to $\overline{Y}$		12		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to $\overline{Y}$		13		13	ns

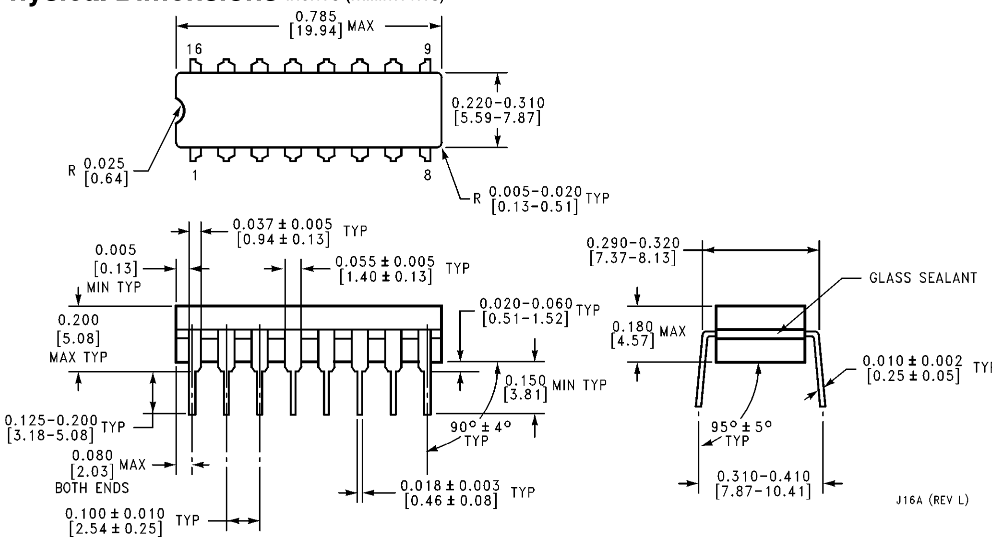
Logic Diagram

9309

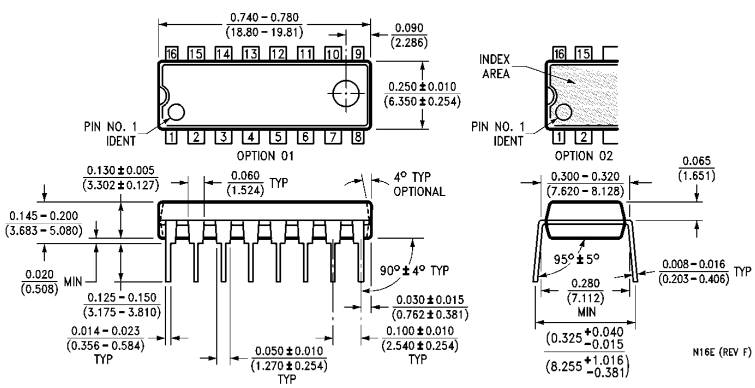


TL/F/6602–2

Physical Dimensions inches (millimeters)

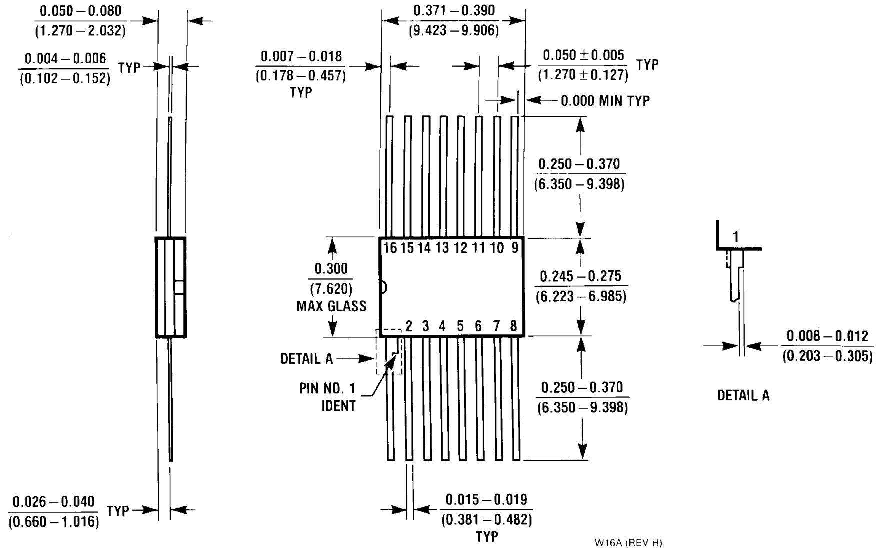


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9309DMQB
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9309N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9309FMQB
NS Package Number W16A

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National Semiconductor

June 1989

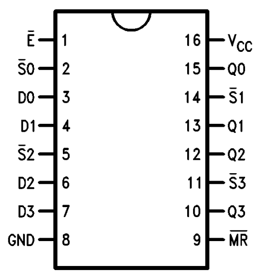
9314/DM9314 Quad Latch

General Description

The '9314 is a multifunctional 4-bit latch designed for general purpose storage applications in high speed digital systems. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good noise immunity.

Connection Diagram

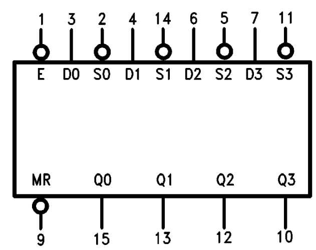
Dual-In-Line Package



TL/F/9788–1

Order Number 9314DMQB, 9314FMQB or DM9314N
See NS Package Number J16A, N16E or W16A

Logic Symbol



TL/F/9788–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
D0–D3	Data Inputs
$\overline{S}0$–$\overline{S}3$	Set Inputs (Active LOW)
$\overline{MR}$	Master Reset Input (Active LOW)
Q0–Q3	Latch Outputs

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to $\overline{E}$	5.0 18			5.0 18			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to $\overline{E}$	0 5.0			0 5.0			ns
t_s (H)	Setup Time HIGH, D_n to $\overline{S}_n$	8.0			8.0			ns
t_h (L)	Hold Time LOW, D_n to $\overline{S}_n$	8.0			8.0			ns
t_w (L)	$\overline{E}$ Pulse Width LOW	18			18			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	18			18			ns
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}$	0			0			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Min, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
		Data Inputs				60	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
		Data Inputs				−2.7	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−70	mA
			COM	−20		−70	
I_{CC}	Supply Current	V_{CC} = Max				55	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		24 24	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		12 24	ns
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n		18	ns
t_{PHL}	Propagation Delay $\overline{S}_n$ to Q_n		24	ns

Functional Description

The '9314 consists of four latches with a common active LOW Enable input and active LOW Master Reset input. When the Enable goes HIGH, data present in the latches is stored and the state of the latch is no longer affected by the $\overline{S}_n$ and D_n inputs. The Master Reset when activated overrides all other input conditions forcing all latch outputs LOW. Each of the four latches can be operated in one of two modes:

D-TYPE LATCH—For D-type operation the $\overline{S}$ input of a latch is held LOW. While the common Enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the Enable goes HIGH.

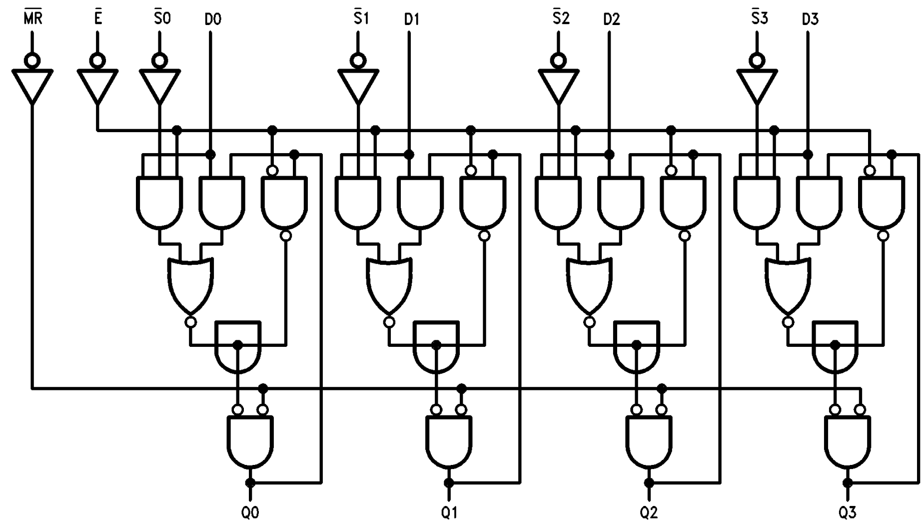
SET/RESET LATCH—During set/reset operation when the common Enable is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the $\overline{S}$ input if the D input is HIGH. If both $\overline{S}$ and D inputs are LOW, the D input will dominate and the latch will be reset. When the Enable goes HIGH, the latch remains in the last state prior to disablement. The two modes of latch operation are shown in the Truth Table.

Truth Table

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_n	Operation
H	L	L	L	L	D Mode
H	L	H	L	H	
H	H	X	X	Q_{n-1}	
H	L	L	L	L	R/S Mode
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{n-1}	
H	H	X	X	Q_{n-1}	
L	X	X	X	L	Reset

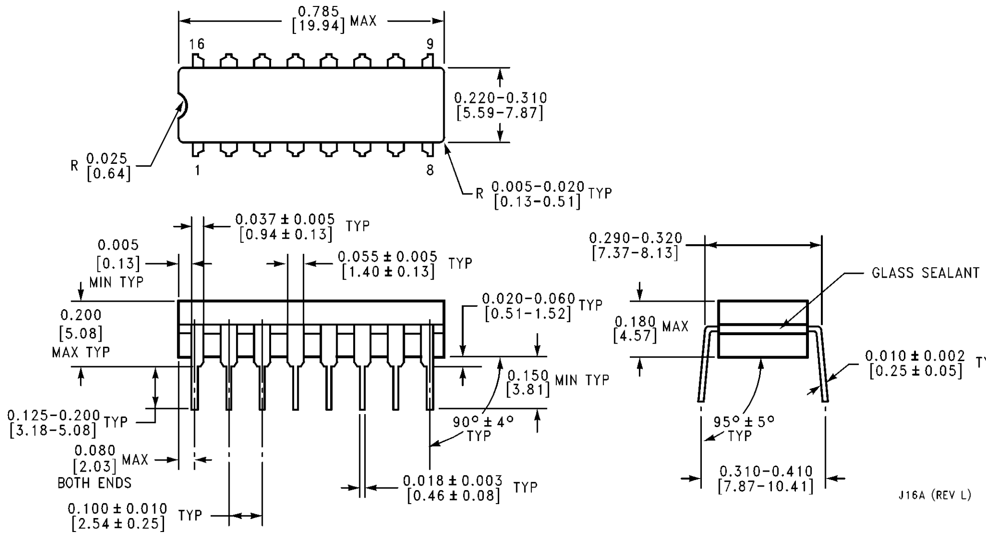
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Q_{n-1} = Previous Output State
Q_n = Present Output State

Logic Diagram

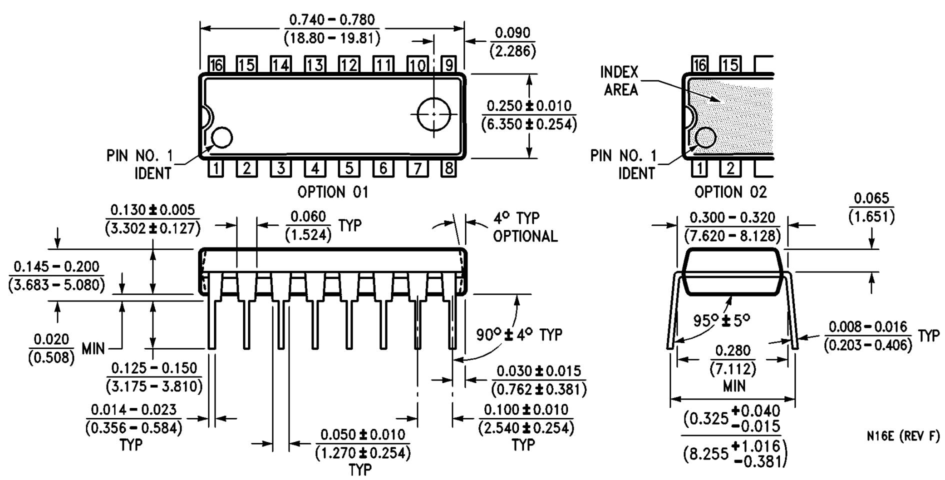


TL/F/9788–3

Physical Dimensions inches (millimeters)

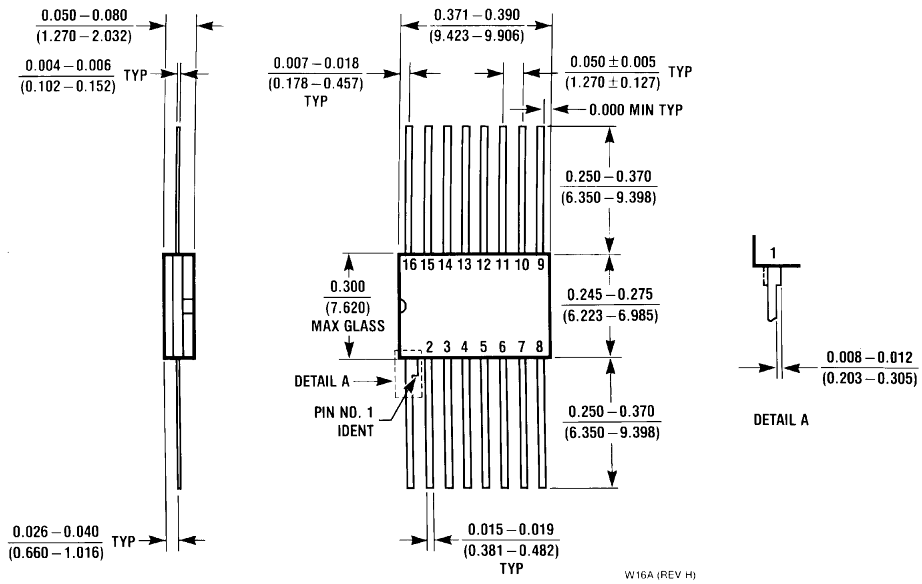


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9314DMQB
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9314N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9314FMQB
NS Package Number W16A

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National Semiconductor

June 1989

9316/DM9316 Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 9316 is a 4-bit binary counter. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enables inputs and internal gating. This mode of operating eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs. The clear function is asynchronous and a low level at the clear input sets of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs.

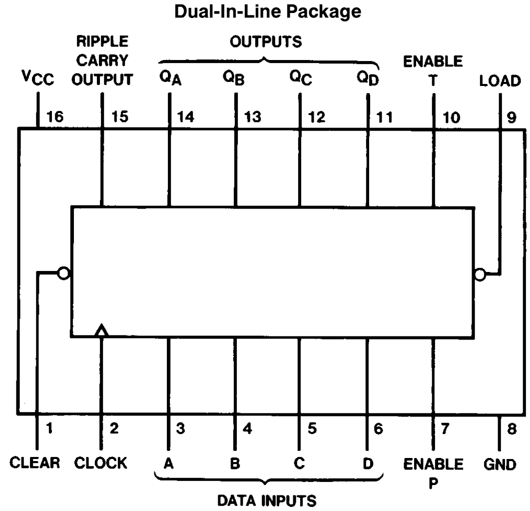
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed-forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur regardless of the logic level in the clock.

Features

- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical clock frequency 35 MHz
- Pin-for-pin replacements popular 54/74 counters 5416A/7416A (binary)
- Alternate Military/Aerospace device (9316) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6606–1

Order Number 9316DMQB, 9316FMQB, DM9316J DM9316W or DM9316N
See NS Package Number J16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 6)		0		25	0		25	MHz
t_W	Pulse Width (Note 6)	Clock	25			25			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 6)	Data	20			20			ns
		Enable P	20			20			
		Load	25			25			
		Clear	20			20			
t_H	Any Hold Time (Notes 1 & 6)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4 V	Clock			80	μA
			Enable T			80	
			Other			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Clock			−3.2	μA
			Enable T			−3.2	
			Other			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	MIL	−20		−57	mA
			COM	−18		−57	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 4)	MIL		59	85	mA
			COM		59	94	
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 5)	MIL		63	91	mA
			COM		63	101	

Note 1: The minimum HOLD time is as specified or as long as the CLOCK input takes to rise from 0.8V to 2V, whichever is longer.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: I_{CCH} is measured with the LOAD input high, then again with the LOAD input low, with all other inputs high and all outputs open.

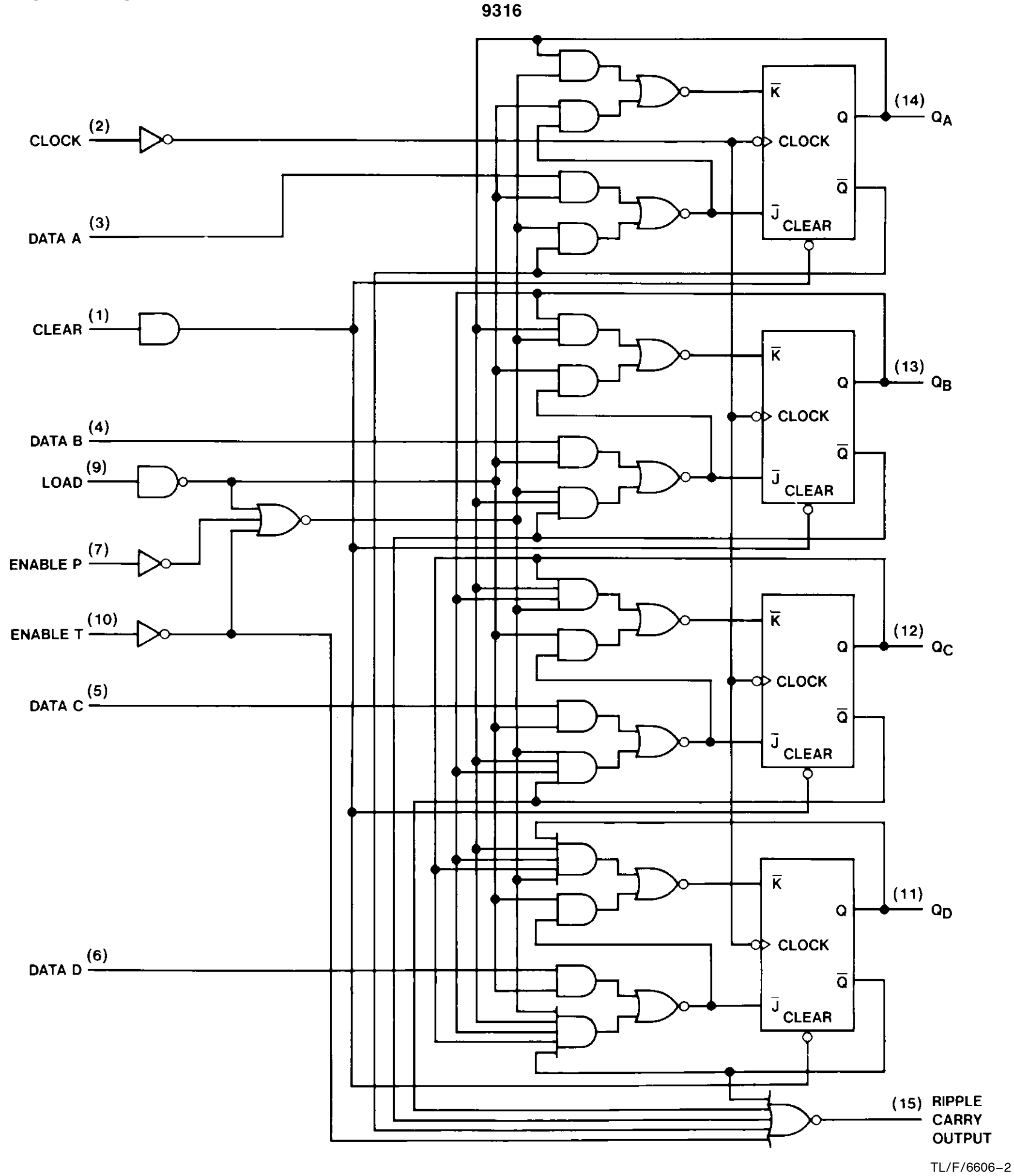
Note 5: I_{CCL} is measured with the CLOCK input high, then again with the CLOCK input low, with all other inputs low and all outputs open.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

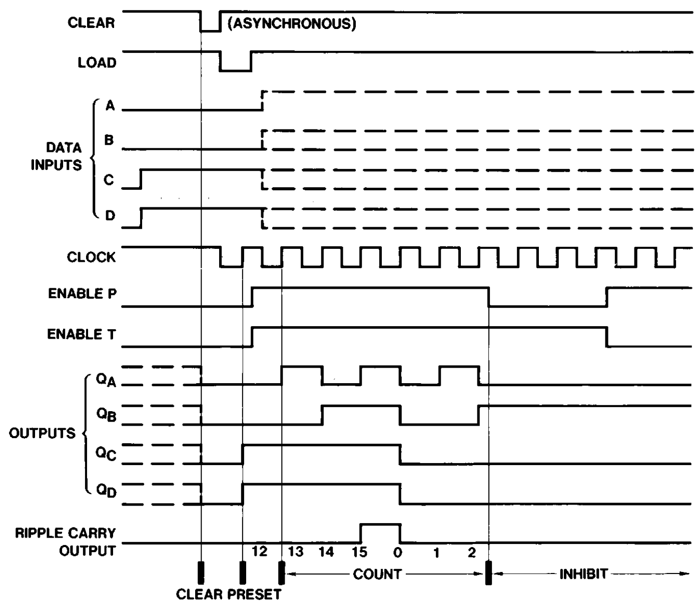
Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to RC		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to RC		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	ENT to RC		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	ENT to RC		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		36	ns

Logic Diagram



Timing Diagram

9316 Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences



TL/F/6606–3

Sequence:

(1) Clear outputs to zero.

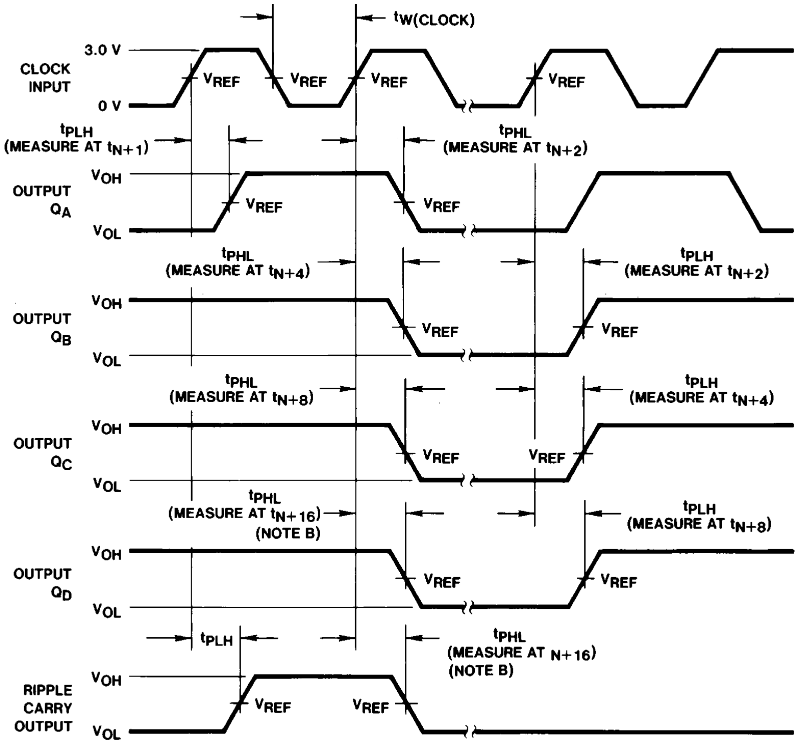
(2) Preset to binary twelve.

(3) Count to thirteen, fourteen, fifteen, zero, one, and two.

(4) Inhibit

Parameter Measurement Information

Switching Time Waveforms



TL/F/6606–4

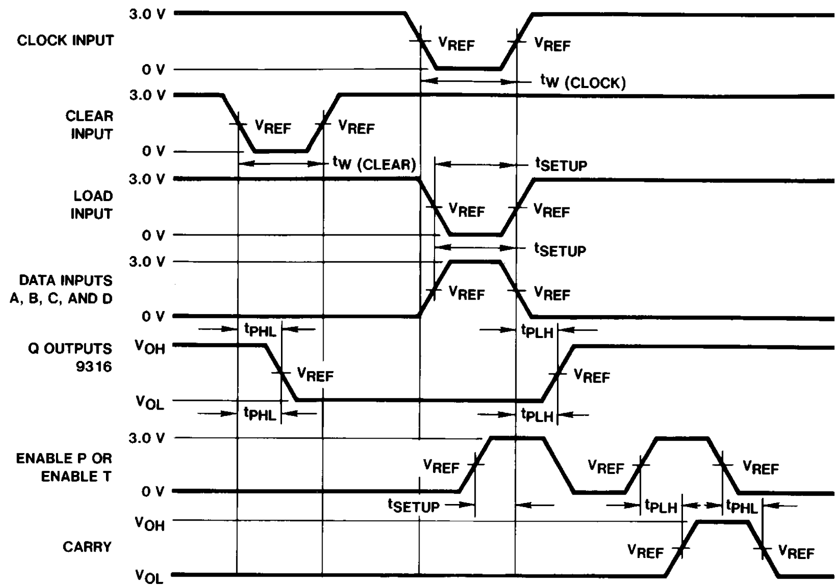
Note A: The input pulses are supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+16} for 9316/8316, where t_n is the bit time when all outputs are low.

Note C: V_{REF} = 1.5V.

Parameter Measurement Information (Continued)

Switching Time Waveforms



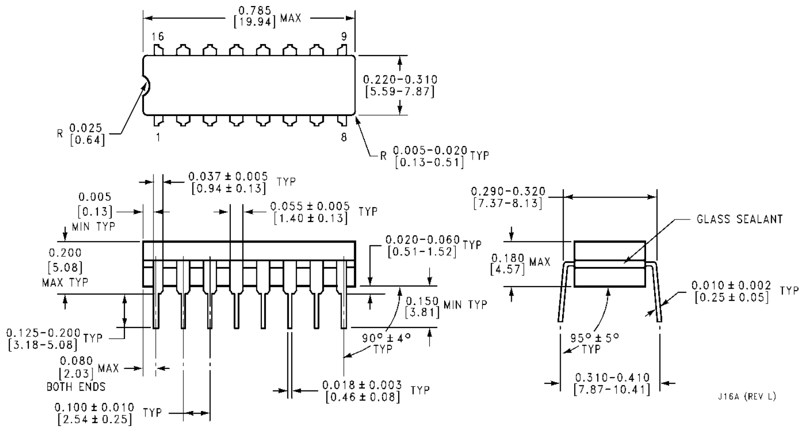
TL/F/6606–5

Note A: The input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

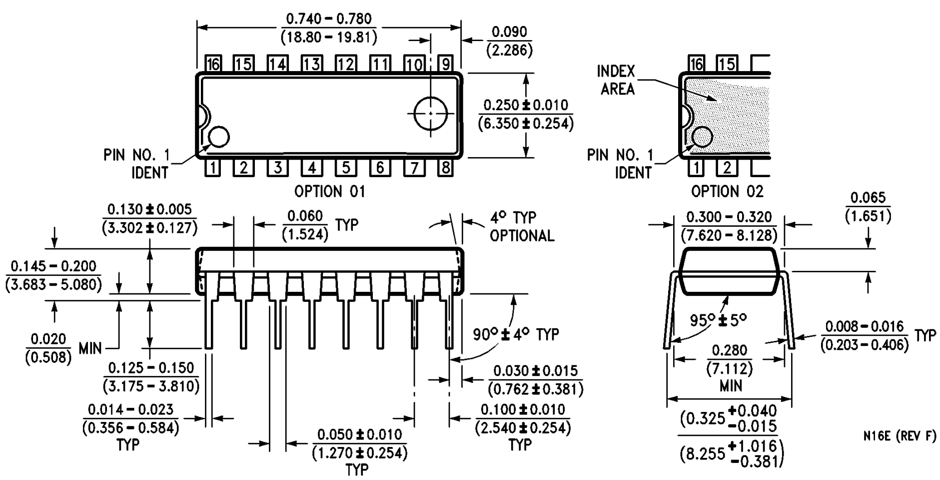
Note B: Enable P and Enable T setup times are measured at t_{n+16} for 8316/9316.

Note C: V_{REF} = 1.5V.

Physical Dimensions inches (millimeters)

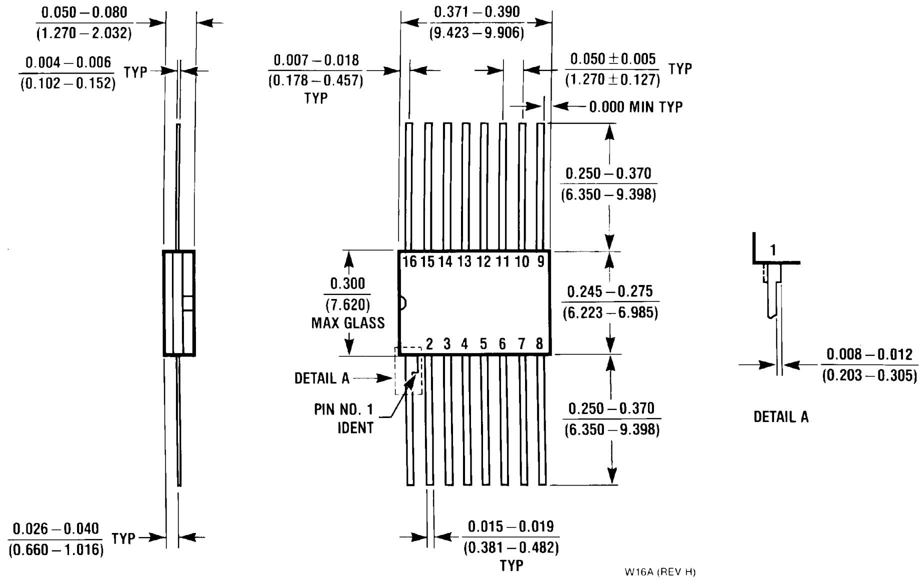


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9316DMQB or DM9316J
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9316N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9316FMQB or DM9316W
NS Package Number W16A

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National Semiconductor

June 1989

9321/DM9321 Dual 1-of-4 Decoder

General Description

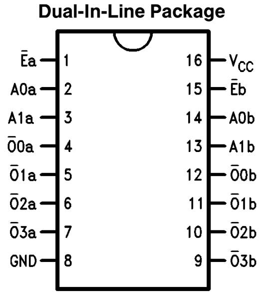
The 9321 consists of two independent multipurpose decoders, each designed to accept two inputs and provide four mutually exclusive outputs. In addition an active LOW enable input, which gives demultiplexing capability, is provided for each decoder.

Features

- Multifunction capability
- Mutually exclusive outputs
- Demultiplexing capability
- Active low enable for each decoder

Connection Diagram

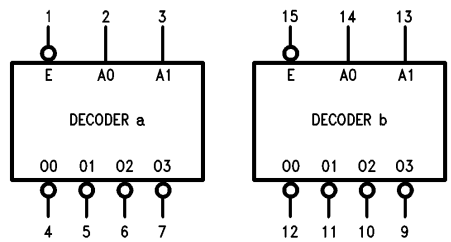
Dual-In-Line Package



TL/F/10209–1

Order Number 9321DMQB, 9321FMQB or DM9321N
See NS Package Number J16A, N16E or W16A

Logic Symbol



TL/F/10209–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{E}$a, $\overline{E}$b	Enable Inputs (Active LOW)
A0a, A1a, A0b, A1b	Address Inputs
$\overline{O}$0a–$\overline{O}$3a, $\overline{O}$0b–$\overline{O}$3b	Decoder Outputs (Active LOW)

 TL/F/10209 RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
COMM	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−70	mA
			COM	−1.3		−3.7	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				50	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay, An to $\overline{O}$n		20 21	ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}$ to $\overline{O}$n		14 18	ns

Functional Description

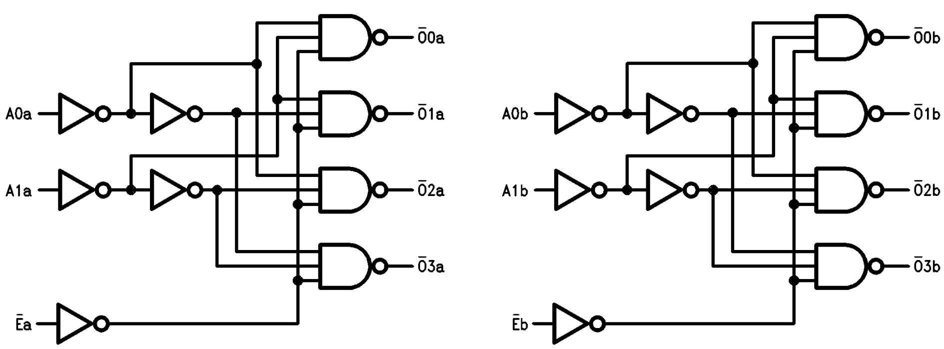
The 9321 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs as shown in the logic symbol. Each decoder can be used as a 4-output demultiplexer by using the enable as a data input.

Truth Table (Each Decoder)

Inputs			Outputs			
$\overline{E}$	A0	A1	$\overline{O}0$	$\overline{O}1$	$\overline{O}2$	$\overline{O}3$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

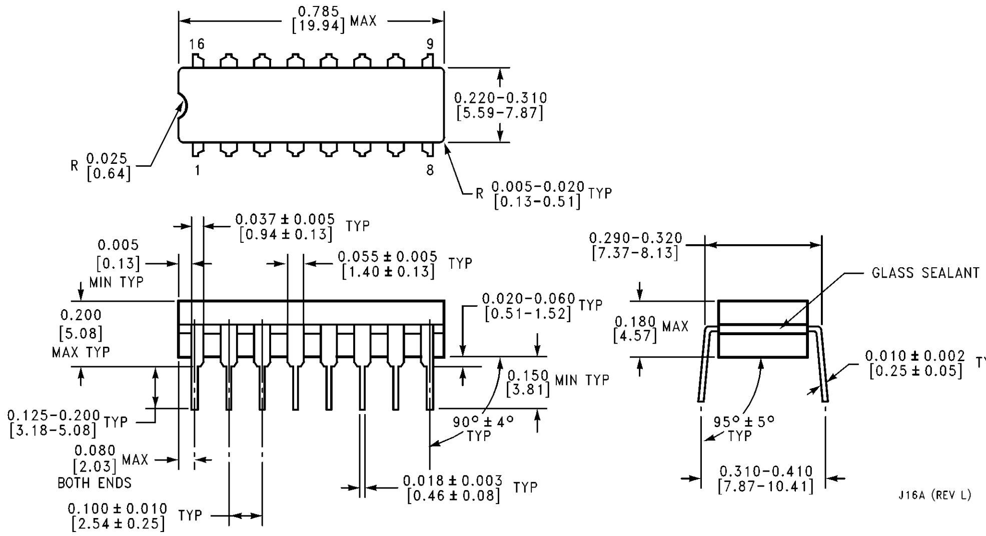
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram

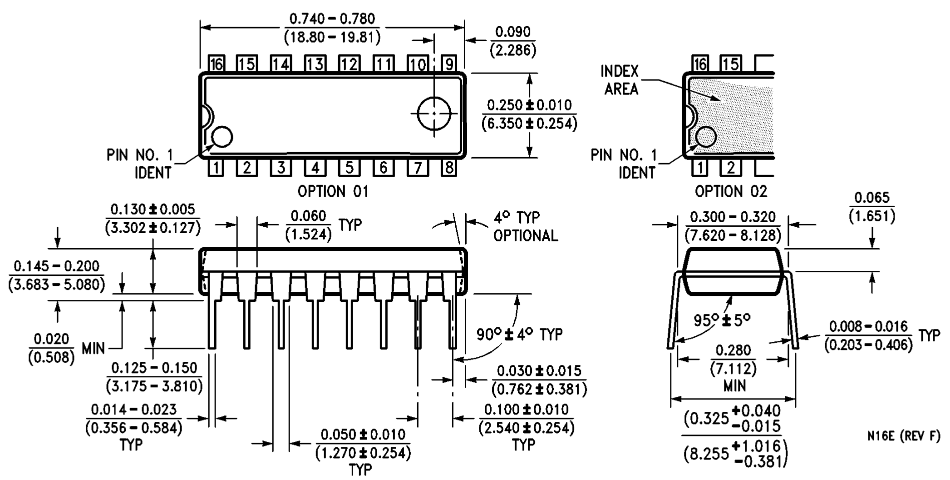


TL/F/10209–3

Physical Dimensions inches (millimeters)

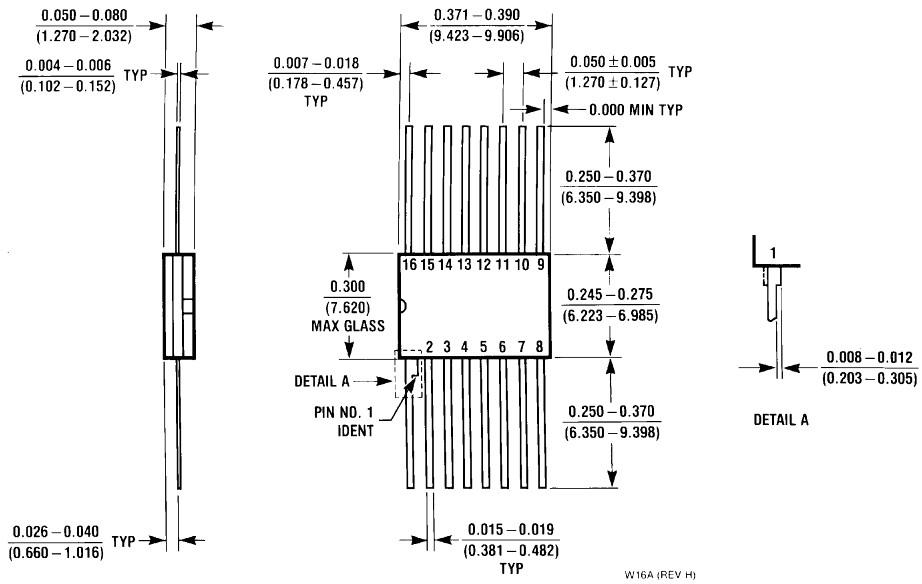


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9321DMQB
NS Package Number J16A



16 Lead Molded Dual-In-Line Package (N)
Order Number DM9321N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9321FMQB
NS Package Number W16A

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National Semiconductor

June 1989

9322/DM9322 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. True data is presented at the outputs.

Features

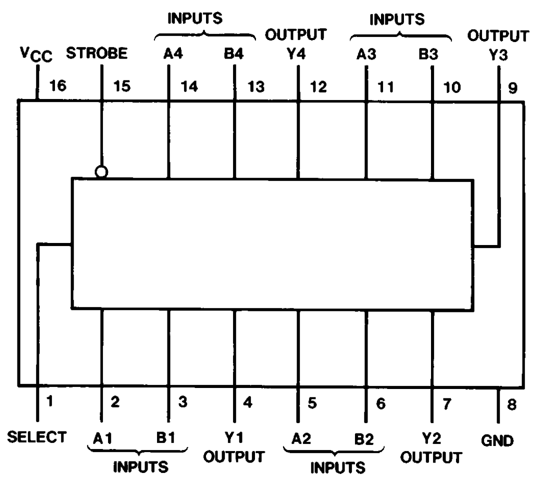
- Pin-for-pin with popular DM54157/74157
- Buffered inputs and outputs

Applications

- Expand any data input point
- Multiplex dual-data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters
- Alternate Military/Aerospace device (9322) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6608–1

Order Number 9322DMQB, 9322FMQB, DM9322J, DM9322W or DM8322N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs				Output
Strobe	Select	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level, L = Low Level, X = Don't Care.

 RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−20		−55	mA
			COM	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	48	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

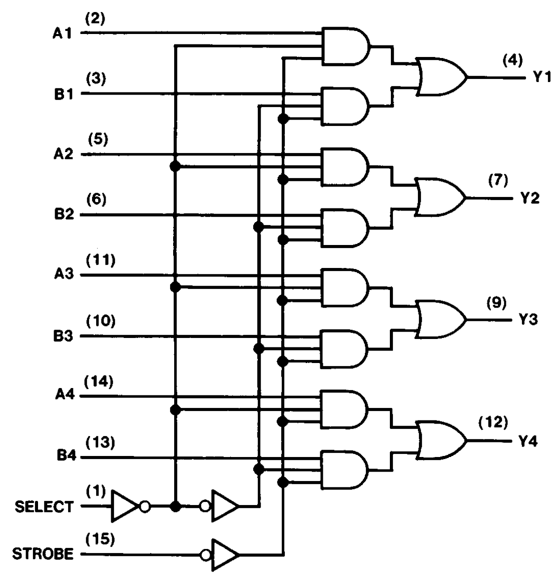
Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		27	ns

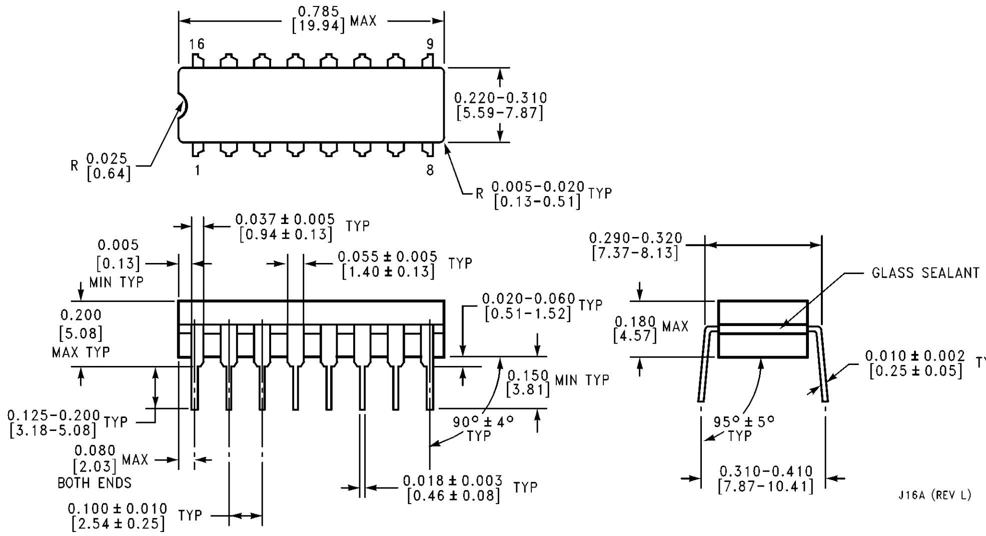
Logic Diagram

9322

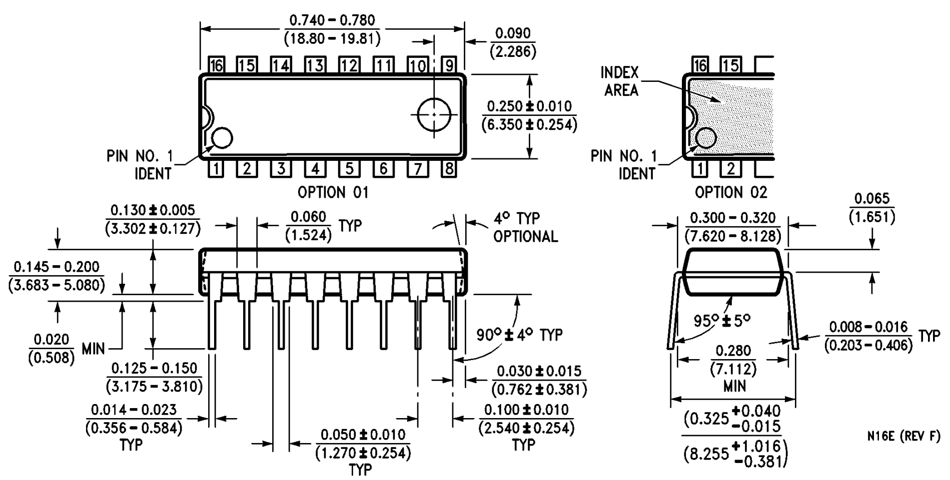


TL/F/6608–2

Physical Dimensions inches (millimeters)

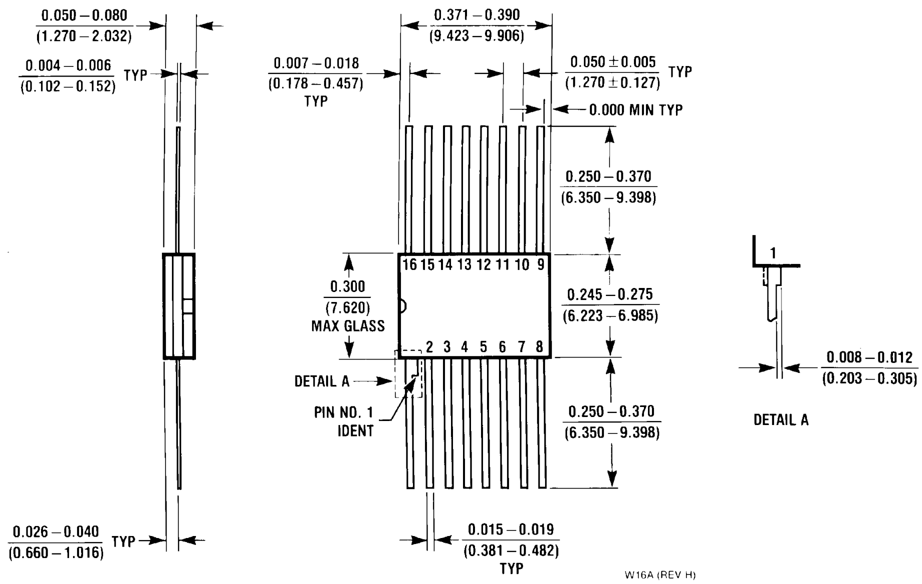


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9322DMQB or DM9322J
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9322N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9322FMQB or DM9322W
NS Package Number W16A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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March 1998

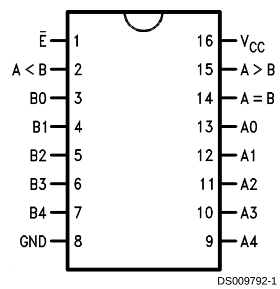
9324/DM9324
5-Bit Comparator

General Description

The 9324 expandable comparators provide comparison between two 5-bit words and give three outputs—“less than”, “greater than” and “equal to”. A HIGH on the active LOW Enable Input forces all three outputs LOW.

Connection Diagram

Dual-In-Line Package



Order Number 9324DMQB, 9324FMQB, or DM9324N
See Package Number J16A, N16E or W16A

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
A0–A4	Word A Parallel Inputs
B0–B4	Word B Parallel Inputs
A < B	A Less than B Output (Active HIGH)
A > B	A Greater than B Output (Active HIGH)
A = B	A Equal to B Output (Active HIGH)

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55˚C to +125˚C
Commercial	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	MIL	−20		−70	mA
			COM	−20		−70	
I_{CC}	Supply Current	V_{CC} = Max				81	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25˚C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to A = B		14 14	ns
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to A > B		25 22	ns
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to A < B		26 21	ns
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to A = B		30 32	ns

Functional Description

The ’24 5-bit comparators use combinational circuitry to directly generate “A greater than B” and “A less than B” outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The “A equals B” output is generated in one additional gate delay by decoding the “A neither less than nor greater than B” condition with a NOR gate. All three outputs are activated by the active LOW Enable Input ($\overline{E}$).

Tying the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion.

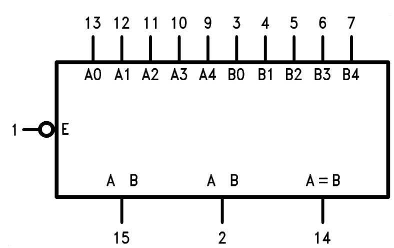
The A4 and B4 inputs are the most significant inputs and A0, B0 the least significant. Thus if A4 is HIGH and B4 is LOW, the A > B output will be HIGH regardless of all other inputs except $\overline{E}$.

Truth Table

Inputs			Outputs		
$\overline{E}$	A_n	B_n	A < B	A > B	A = B
H	X	X	L	L	L
L	Word A = Word B		L	L	H
L	Word A > Word B		L	H	L
L	Word B > Word A		H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

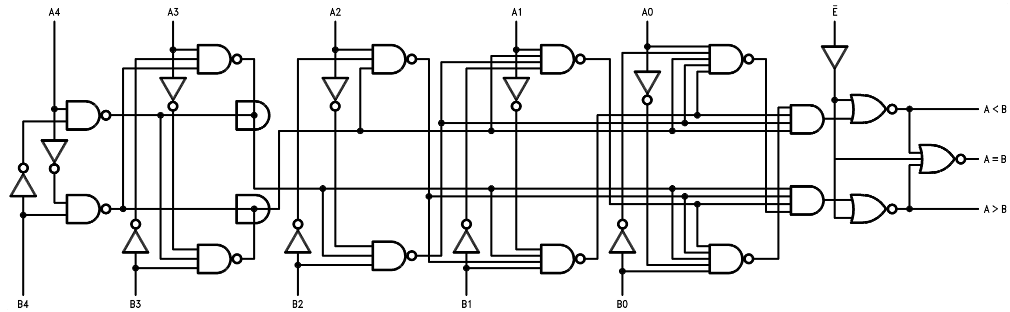
Logic Symbol



DS009792-2

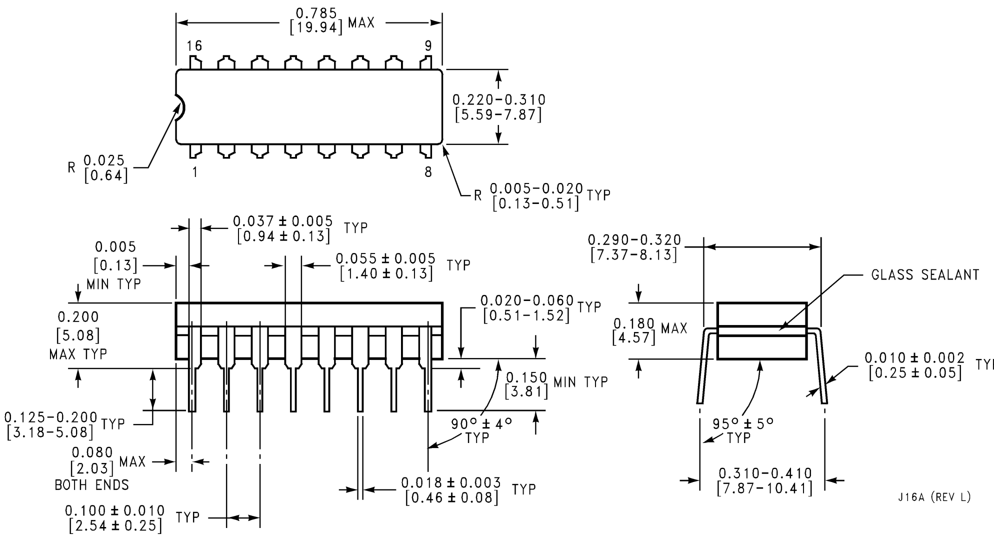
V_{CC} = Pin 16
GND = Pin 6

Logic Diagram

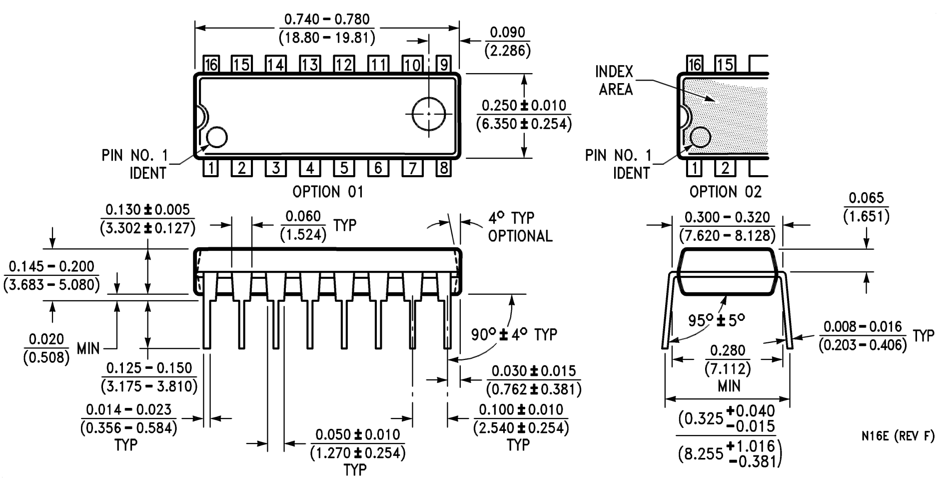


DS009792-3

Physical Dimensions inches (millimeters) unless otherwise noted

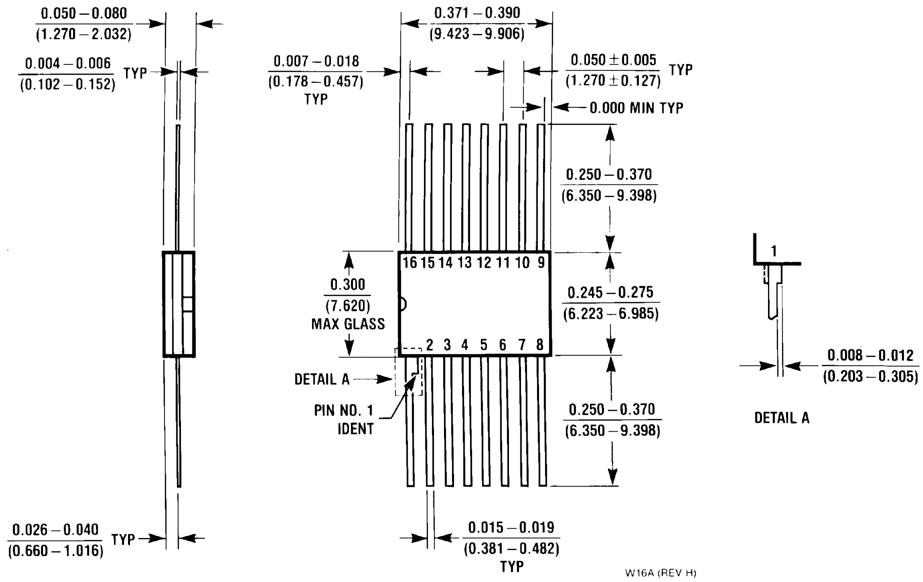


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9324DMQB
Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9324N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9324FMQB
Package Number W16A

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March 1998

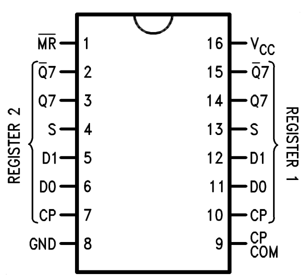
9328/DM9328
Dual 8-Bit Shift Register

General Description

The ’9328 is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers. The multifunctional capability of this device is provided by several features: 1) additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources; 2) the clock of each register may be provided separately or together; 3) both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

Connection Diagram

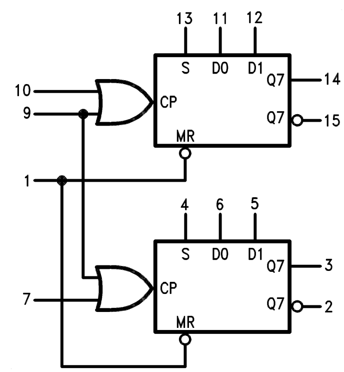
Dual-In-Line Package



DS009793-1

Order Number 9328DMQB, 9328FMQB or DM9328N
See Package Number J16A, N16E or W16A

Logic Symbol



DS009793-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
S	Data Select Input
D0, D1	Data Inputs
CP	Clock Pulse Input (Active HIGH)
	Common (Pin 9)
	Separate (Pins 7 and 10)
$\overline{MR}$	Master Reset Input (Active LOW)
Q7	Last Stage Output
$\overline{Q7}$	Complementary Output

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55˚C to +125˚C
Commercial	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20			20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	0 0			0 0			ns
t_w (H) t_w (L)	Clock Pulse Width HIGH or LOW	25 25			25 25			ns
t_w (L)	$\overline{MR}$ Pulse Width with CP HIGH	30			30			ns
t_w (L)	$\overline{MR}$ Pulse Width with CP LOW	40			40			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	33			33			ns

Note 1: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V $\overline{MR}$, D_n Inputs			40	µA
		CP Inputs			60	
		S Inputs			80	
		CP (COM) Inputs			120	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V $\overline{MR}$, D_n Inputs			−1.6	mA
		CP Inputs			−2.4	
		S Inputs			−3.2	
		CP (COM) Input			−4.8	

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	MIL	−20		−70	mA
			COMM	−20		−70	
I_{CC}	Supply Current	V_{CC} = Max				77	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25˚C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF, R_L = 400Ω		Units
		Min	Max	
f_{max}	Maximum Shift Right Frequency	20		MHz
t_{PLH}	Propagation Delay		20	ns
t_{PHL}	CP to Q7 or $\overline{Q}$7		35	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q7		50	ns

Functional Description

The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW-to-HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH-to-LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal. Each 8-bit shift register has a 2-input multiplexer in front of the serial data input. The two data inputs D0 and D1 are controlled by the data select input (S) following the Boolean expression:

Serial data in: $S_D = S\overline{D0} + SD1$

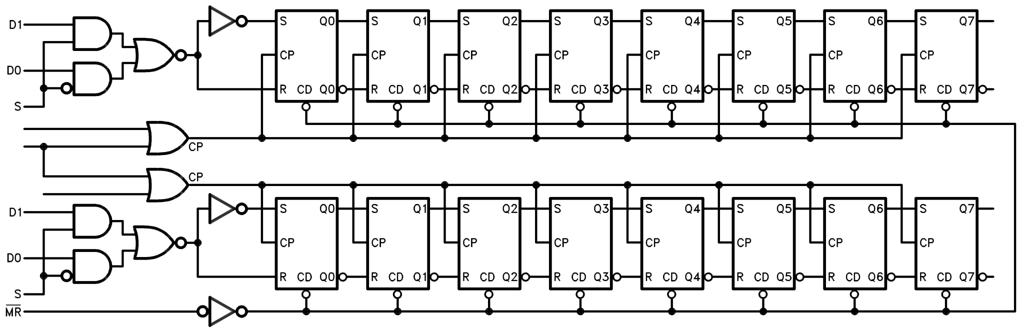
An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all 16 stages independently of any other input signal.

Shift Select Table

INPUTS			OUTPUT
S	D0	D1	Q7 (t_{n+8})
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

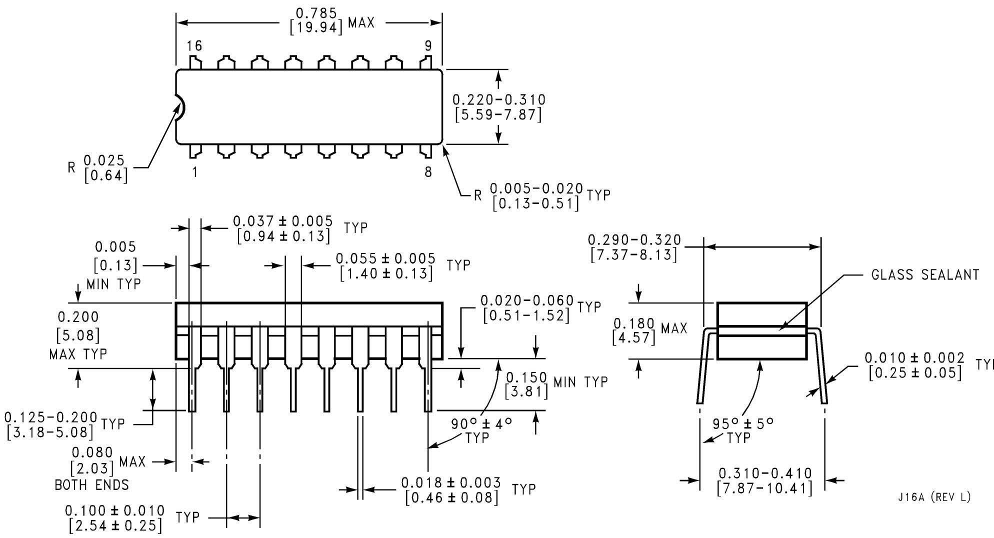
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
n + 8 = indicates state after eight clock pulse

Logic Diagram

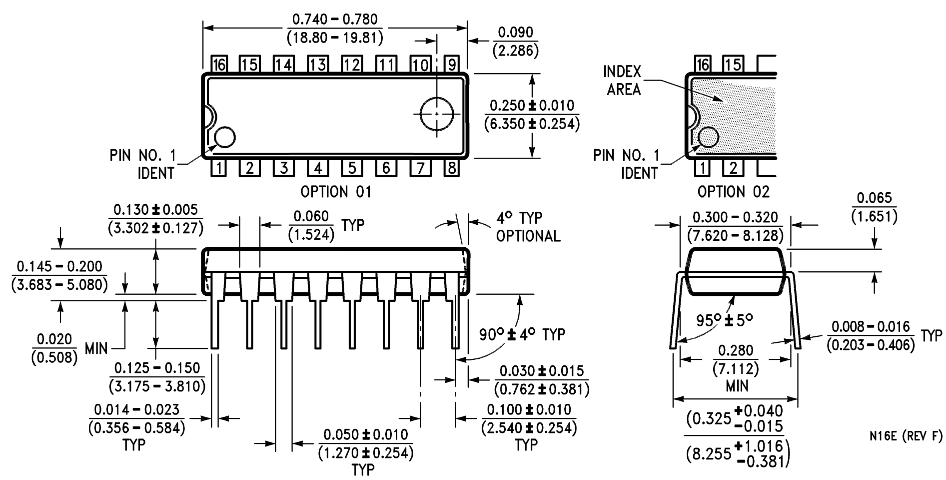


DS009793-3

Physical Dimensions inches (millimeters) unless otherwise noted

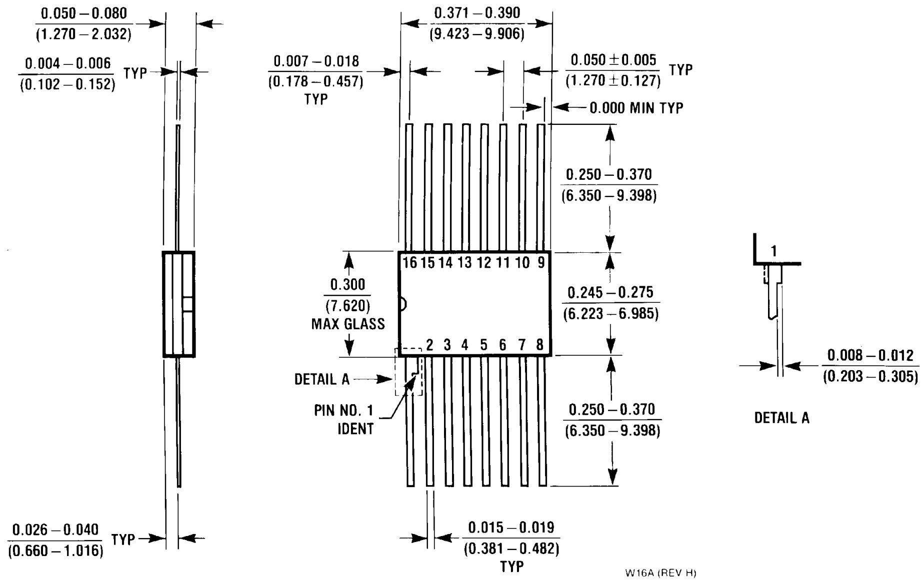


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9328DMQB
Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9328N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9328FMQB
Package Number W16A

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March 1998

9334/DM9334
8-Bit Addressable Latch

General Description

The DM9334 is a high speed 8-bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level high outputs. The device also incorporates an active level low common clear for resetting all latches, as well as an active level low enable.

The DM9334 has four modes of operation which are shown in the mode selection table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the low state. In the clear mode all outputs are low and unaffected by the address and data inputs.

When operating the device as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

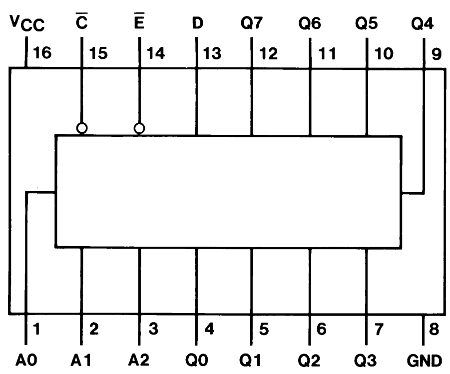
The function tables summarize the operation of the product.

Features

- Common clear
- Easily expandable
- Random (addressable) data entry
- Serial to parallel capability
- 8 bits of storage/output of each bit available
- Active high demultiplexing/decoding capability
- Alternate Military/Aerospace device (9334) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 9334DMQB, 9334FMQB, DM9334J or DM9334N
See Package Number J16A, N16E or W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55˚C to +125˚C
Commercial	0˚ to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
t_W	ENABLE Pulse Width (*Figure 1*) (Note 5)		19	13		19	13		ns
t_{SU}	Setup Time (Note 5)	Data 1 (*Figure 5*)	20	13		20	13		ns
		Data 0 (*Figure 5*)	20	14		20	14		
		Address (*Figure 6*) (Note 2)	10	5		10	5		
t_H	Hold Time (Note 5)	Data 1 (*Figure 5*)	0	−10		0	−10		ns
		Data 0 (*Figure 5*)	0	−13		0	−13		
T_A	Free Air Operating Temperature		−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	$\overline{E}$ Input			60	µA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	$\overline{E}$ Input			−2.4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	MIL	−30		−100	mA
			COM	−30		−100	
I_{CC}	Supply Current	V_{CC} = Max			56	86	mA

Note 2: The ADDRESS setup time is the time before the negative ENABLE transition that the ADDRESS must be stable so that the correct latch is addressed without affecting the other latches.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: T_A = 25˚C and V_{CC} = 5V.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output, (*Figure 1*)		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output, (*Figure 1*)		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output, (*Figure 4*)		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output, (*Figure 4*)		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Address to Output, (*Figure 2*)		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Address to Output, (*Figure 2*)		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output, (*Figure 3*)		31	ns

Function Tables

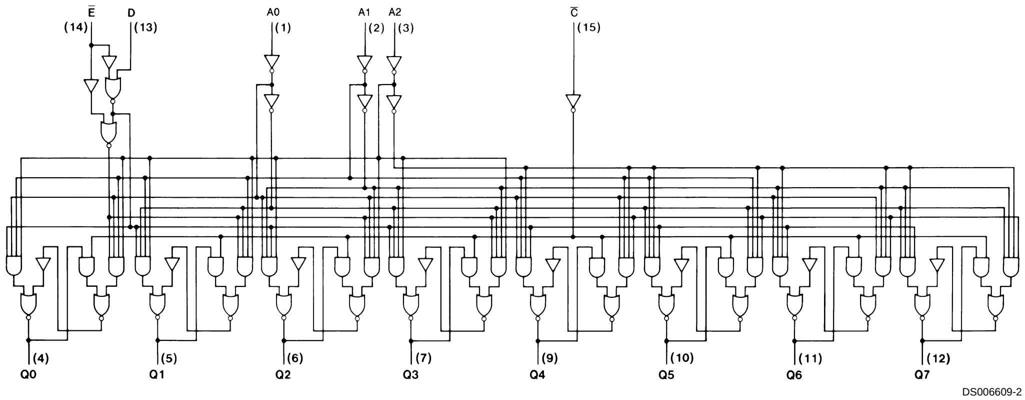
$\overline{E}$	$\overline{C}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active High Eight Channel Demultiplexer
H	L	Clear

Inputs						Present Output States								Mode
$\overline{C}$	$\overline{E}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
•	•	•		•					•					Demultiplex
•	•	•		•					•					
•	•	•		•					•					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1}								Memory
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}					
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1}						
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1}						Addressable Latch
•	•	•		•				•						
•	•	•		•				•						
•	•	•		•				•						
H	L	L	H	H	H	Q_{N-1}						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1}						Q_{N-1}	H	

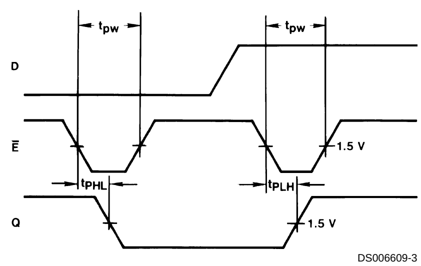
X = Don't Care Condition
L = Low Voltage Level
H = High Voltage Level
Q_{N-1} = Previous Output State

Logic Diagram

9334

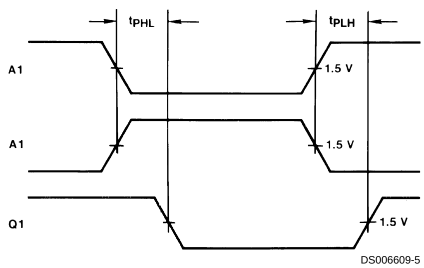


Switching Time Waveforms



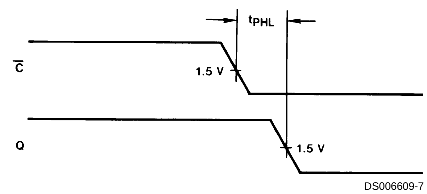
Other Conditions: C = H, A = Stable

FIGURE 1.



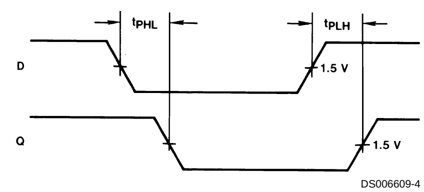
Other Conditions: $\overline{E}$ = L, $\overline{C}$ = L, D = H

FIGURE 2.



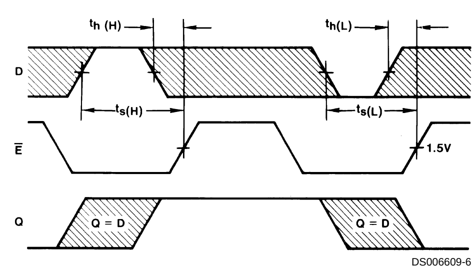
Other Conditons: $\overline{E}$ = H

FIGURE 3.



Other Conditions: $\overline{E}$ = L, $\overline{C}$ = H, A = Stable

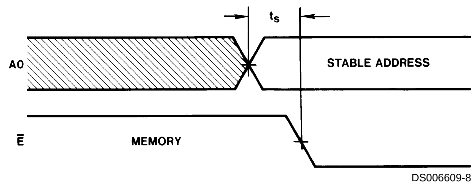
FIGURE 4.



Other Conditions: C = H, A = Stable

FIGURE 5.

Switching Time Waveforms (Continued)



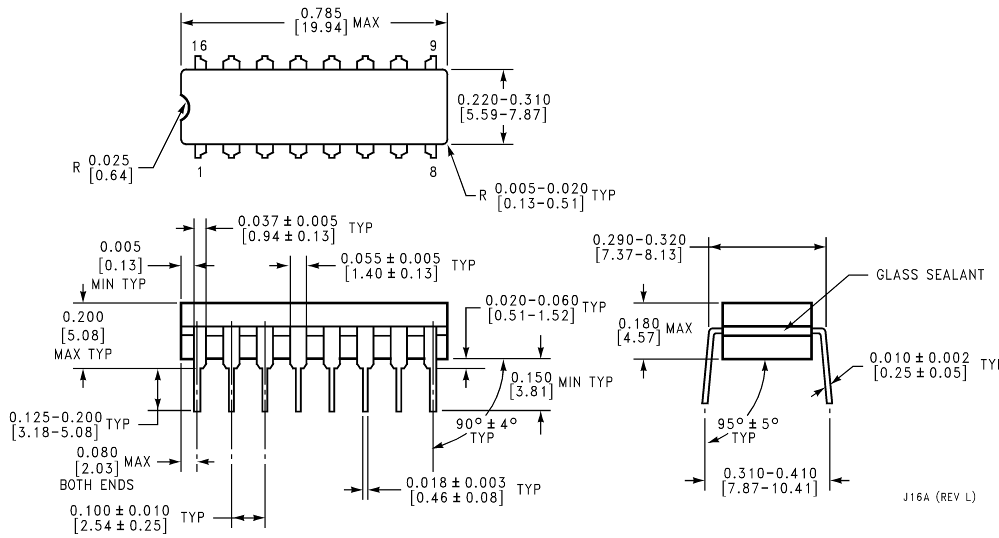
Other Conditions: $\overline{C}$ = H

Note:

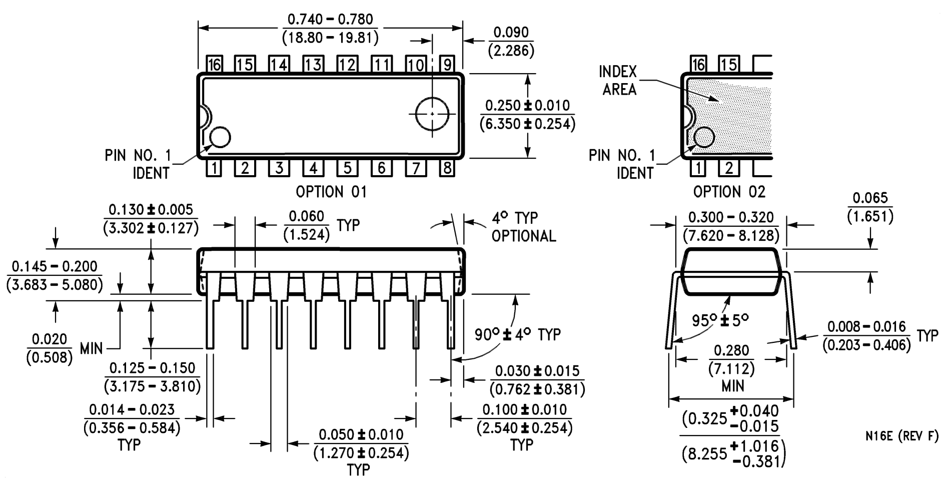
The shaded areas indicate when the inputs are permitted to change for predictable output performance.

FIGURE 6.

Physical Dimensions inches (millimeters) unless otherwise noted

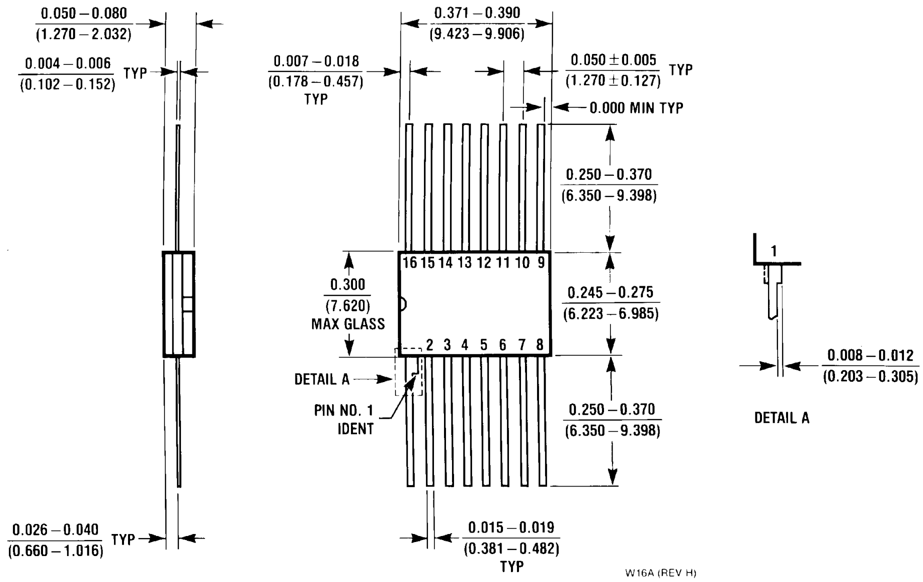


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9334DMQB or DM9334J
Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9334N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9334FMQB
Package Number W16A

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National Semiconductor

June 1989

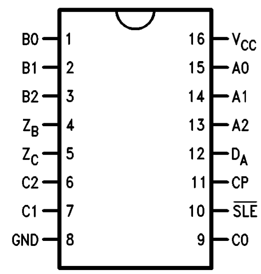
9338/DM9338 8-Bit Multiple Port Register

General Description

The DM9338 is an 8-bit multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously.

Connection Diagrams

Dual-In-Line Package



TL/F/9794–1

Order Number 9338DMQB, 9338FMQB or DM9338N
See NS Package Number J16A, N16E or W16A

Pin Names	Description
A0–A2	Write Address Inputs
D_A	Data Input
B0–B2	B Read Address Inputs
C0–C2	C Read Address Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{SLE}$	Slave Enable Input (Active LOW)
Z_B	B Output
Z_C	C Output

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_A to CP	20 12			20 12			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_A to CP	0 −8.0			0 −8.0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to CP	10 10			10 10			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to CP	0 0			0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	23 13			23 13			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				27	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.1	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−10		−70	mA
			COM	−10		−70	
I_{CC}	Supply Current	V_{CC} = Max				135	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15$ pF				Units
		9338 (MIL)		DM9338 (COM)		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay B_n or C_n to Z_n		40 35	13 18	40 35	ns
t_{PLH} t_{PHL}	Propagation Delay D_A to Z_n		45 50	25 25	45 50	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Z_n		35 30	18 13	35 30	ns

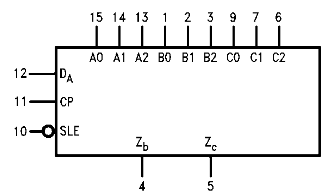
Functional Description

The 9338 8-bit multiple port register can be considered a 1-bit slice of eight high speed working registers. Data can be written into any one and read from any two of the eight locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous read/write activity from the same location. When the clock input (CP) is LOW data applied to the data input line (D_A) enters the selected master. This selection is accomplished by coding the three write input select lines (A0–A2) appropriately. Data is stored synchronously with the rising edge of the clock pulse.

The information for each of the two slaved (output) latches is selected by two sets of read address inputs (B0–B2 and C0–C2). The information enters the slave while the clock is HIGH and is stored while the clock is LOW. If Slave Enable is LOW ($\overline{SLE}$), the slave latches are continuously enabled. The signals are available on the output pins (Z_B and Z_C). The input bit selection and the two output bit selections can be accomplished independently or simultaneously. The data flows into the device, is demultiplexed according to the state of the write address lines and is clocked into the selected latch. The eight latches function as masters and store the input data. The two output latches are slaves and hold the data during the read operation. The state of each slave is determined by the state of the master selected by its associated set of read address inputs.

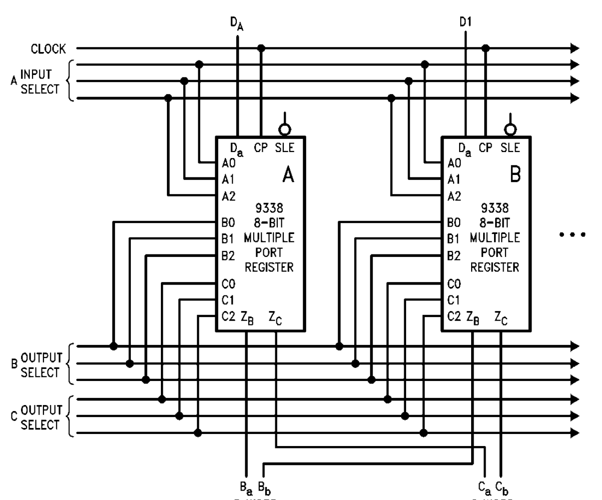
The method of parallel expansion is shown in *Figure a*. One 9338 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of n-bits each at one time, where n devices are connected in parallel.

Logic Symbol



TL/F/9794–2

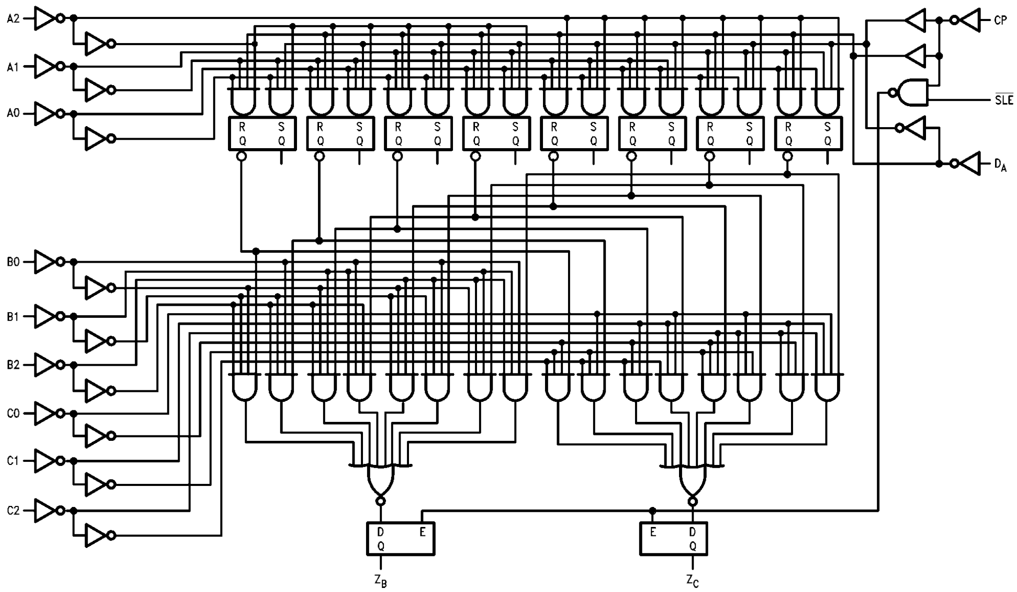
V_{CC} = Pin 16
GND = Pin 8



TL/F/9794–4

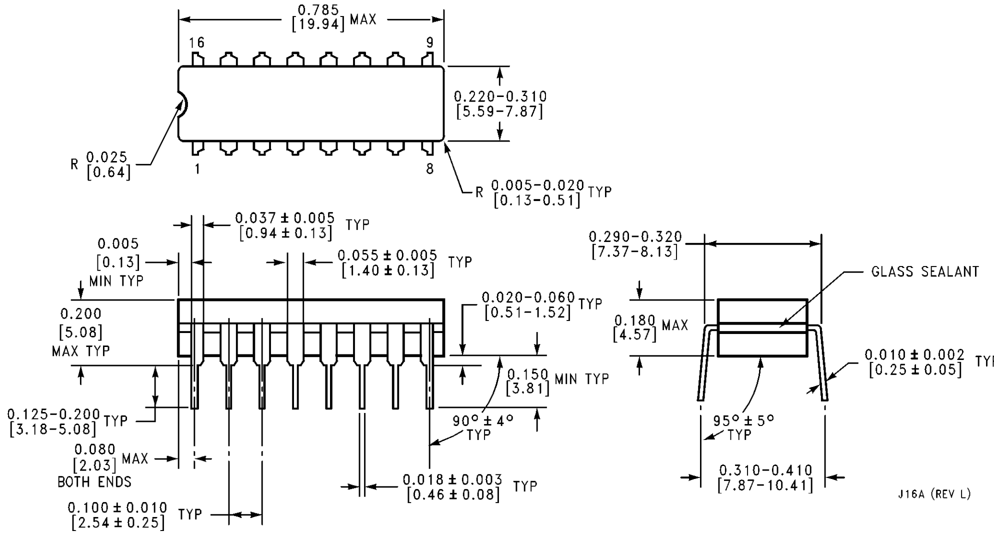
FIGURE a. Parallel Expansion

Logic Diagram

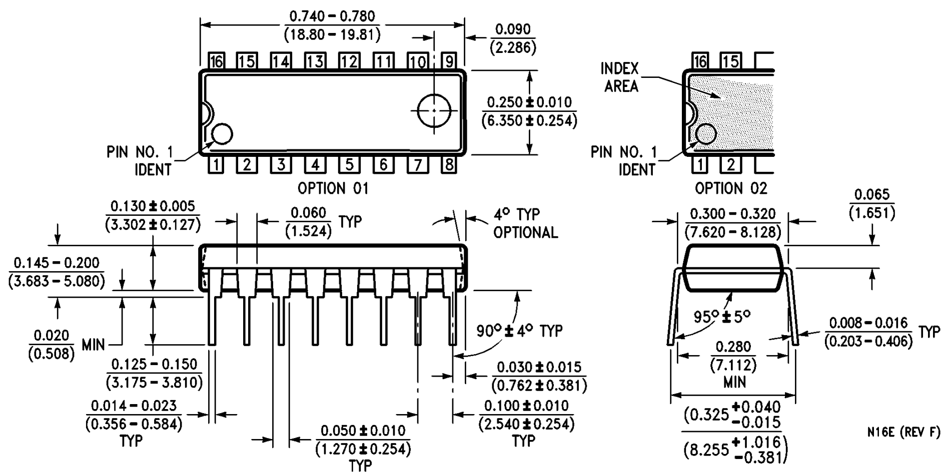


TL/F/9794–3

Physical Dimensions inches (millimeters)

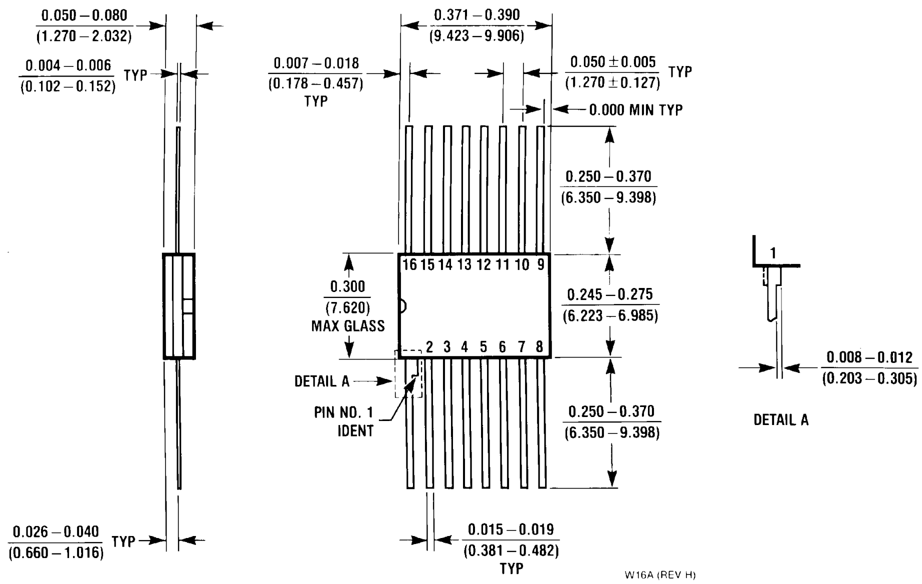


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9338DMQB
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9338N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9338FMQB
NS Package Number W16A

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National Semiconductor

June 1989

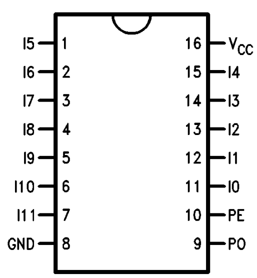
9348
12-Input Parity Checker/Generator

General Description

The 9348 is a 12-input parity checker/generator generating odd and even parity outputs. It can be used in high speed error detection applications.

Connection Diagram

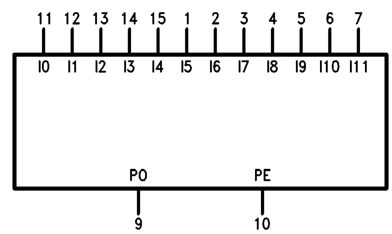
Dual-In-Line Package



TL/F/9795–1

Order Number 9348DMQB or 9348FMQB
See NS Package Number J16A or W16A

Logic Symbol



TL/F/9795–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
I0–I11	Parity Inputs
PO	Odd Parity Output
PE	Even Parity Output

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	$-55^{\circ}C$ to $+125^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	9348			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.8	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			82	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configuration)

Symbol	Parameter	Conditions	C_L = 15 pF, R_L = 400Ω		Units
			Min	Max	
t_{PLH} t_{PHL}	Propagation Delay I4 to PO	I2, I3, I7, I8 = GND; Other Inputs (except I4) HIGH		46 42	ns
t_{PLH} t_{PHL}	Propagation Delay I4 to PE	I2, I3, I7, I8 = GND; Other Inputs (except I4) HIGH		51 48	ns
t_{PLH}	Propagation Delay I3 to PO	I7 = HIGH; Other Inputs (except I3) = GND		27	ns
t_{PHL}	Propagation Delay I4 to PO	All Inputs (except I4) = GND		25	ns

Functional Description

The 9348 is a 12-input parity generator. It provides odd and even parity for up to 12 data bits. The Even Parity output (PE) will be HIGH if an even number of logic ones are present on the inputs. The Odd Parity output (PO) will be HIGH if an odd number of logic ones are present on the inputs. The logic equations for the outputs are shown below.

$$PO = I0 \oplus I1 \oplus I2 \oplus I3 \oplus I4 \oplus I5 \oplus I6 \oplus I7 \oplus I8 \oplus I9 \oplus I10 \oplus I11$$
$$PE = \overline{I0 \oplus I1 \oplus I2 \oplus I3 \oplus I4 \oplus I5 \oplus I6 \oplus I7 \oplus I8 \oplus I9 \oplus I10 \oplus I11}$$

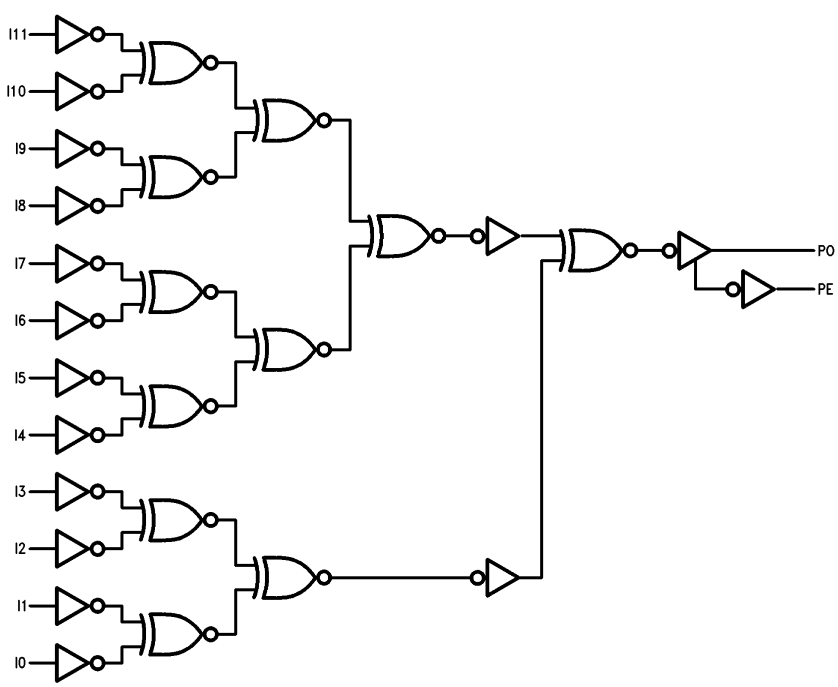
Note: Less through delay is encountered from the I0, I1, I2 and I3 inputs than I4 thru I11 inputs. Therefore, if some signals are slower than others, the slower signals should be applied to these four inputs for maximum speed.

Truth Table

Inputs		Outputs	
I0–I11		PO	PE
All Twelve	Inputs LOW	L	H
Any One	Inputs HIGH	H	L
Any Two	Inputs HIGH	L	H
Any Three	Inputs HIGH	H	L
Any Four	Inputs HIGH	L	H
Any Five	Inputs HIGH	H	L
Any Six	Inputs HIGH	L	H
Any Seven	Inputs HIGH	H	L
Any Eight	Inputs HIGH	L	H
Any Nine	Inputs HIGH	H	L
Any Ten	Inputs HIGH	L	H
Any Eleven	Inputs HIGH	H	L
Any Twelve	Inputs HIGH	L	H

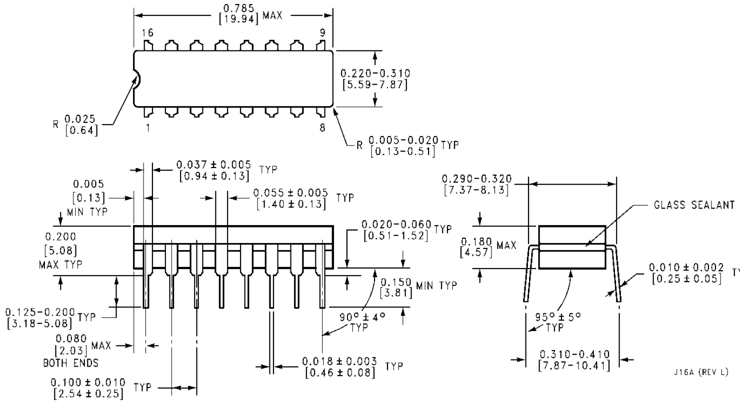
H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram

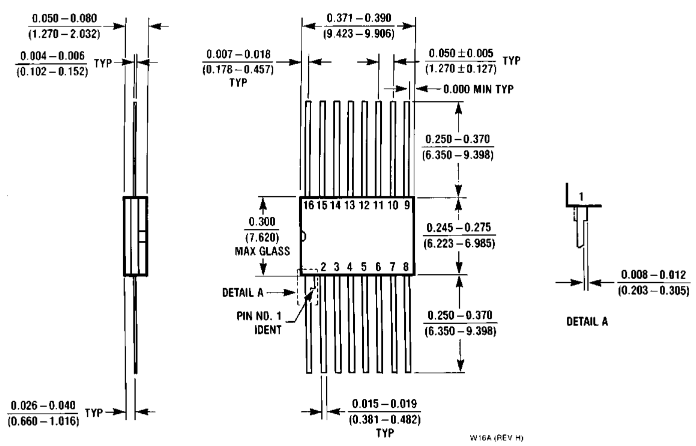


TL/F/9795–3

Physical Dimensions inches (millimeters)



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9348DMQB
NS Package Number J16A



16-Lead Ceramic Flat Package (W)
Order Number 9348FMQB
NS Package Number W16A

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National Semiconductor

June 1989

93L00 4-Bit Universal Shift Register

General Description

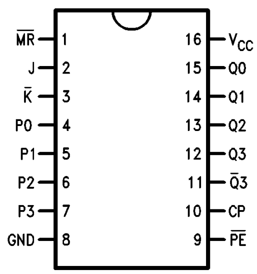
The 93L00 is a 4-bit universal shift register. As a high speed multifunctional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers.

Features

- Asynchronous master reset
- J, $\overline{K}$ inputs to first stage

Connection Diagram

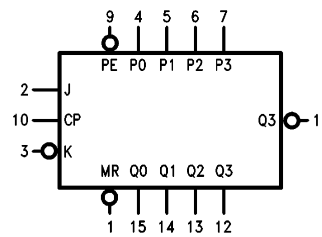
Dual-In-Line Package



TL/F/9576–1

Order Number 93L00DMQB or 93L00FMQB
See NS Package Number J16A or W16A

Logic Symbol



TL/F/9576–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{PE}$	Parallel Enable Input (Active LOW)
P0–P3	Parallel Inputs
J	First Stage J Input (Active HIGH)
$\overline{K}$	First Stage K Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Master Reset Input
Q0–Q3	Parallel Outputs
$\overline{Q3}$	Complementary Last Stage Output

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−65°C to +125°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L00 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Voltage			−0.4	mA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW, J, $\overline{K}$ and P0−P3 to CP	60 60			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW, J, $\overline{K}$ and P0−P3 to CP	0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW, $\overline{PE}$ to CP	68 68			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW, $\overline{PE}$ to CP	0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	38 38			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	53			ns
t_{rec}	Recovery Time, $\overline{MR}$ to CP	70			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -10\text{ mA}$				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$, $V_{IL} = \text{Max}, V_{IH} = \text{Min}$		2.4	3.4		V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$, $V_{IH} = \text{Min}, V_{IL} = \text{Max}$				0.3	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5V$				1	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4V$	Inputs			20	μA
			CP			40	
			$\overline{PE}$			46	
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.3V$	Inputs			−400	μA
			CP			−800	
			$\overline{PE}$			−920	
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$				23	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	93L $C_L = 15$ pF Min	93L $C_L = 15$ pF Max	Units
f_{max}	Maximum Shift Frequency	10		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		35 51	ns
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		60	ns

Functional Description

The Logic Diagrams and Truth Table indicate the functional characteristics of the 93L00 4-bit shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers.

The 93L00 has two primary modes of operation, shift right ($Q0 \rightarrow Q1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ input is HIGH, serial data enters the first flip-flop Q0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction $Q0 \rightarrow Q1 \rightarrow Q2 \rightarrow Q3$ following each LOW-to-HIGH clock transition. The J$\overline{K}$ inputs provide the flexibility of the JK type input for special applications, and the simple D-type input for general applications by tying the two pins together.

When the $\overline{PE}$ input is LOW, the 93L00 appears as four common clocked D flip-flops. The data on the parallel inputs P0–P3 is transferred to the respective Q0–Q3 outputs following the LOW-to-HIGH clock transition. Shift left operation ($Q3 \rightarrow Q2$) can be achieved by tying the Qn outputs to the $Pn-1$ inputs and holding the $\overline{PE}$ input LOW.

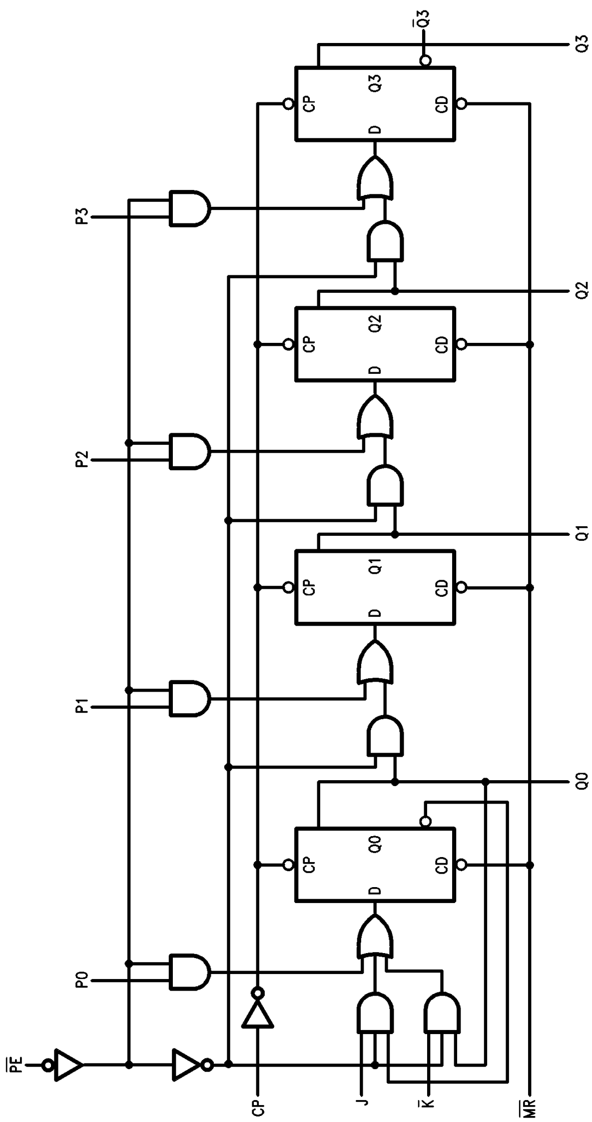
All serial and parallel data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. Since the 93L00 utilizes edge triggering, there is no restriction on the activity of the J, $\overline{K}$, Pn and $\overline{PE}$ inputs for logic operation—except for the setup and release time requirements. A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

Truth Table

Operating Mode	Inputs ($\overline{MR}$ = H)							Outputs @ t_{n+1}				
	$\overline{PE}$	J	$\overline{K}$	P0	P1	P2	P3	Q0	Q1	Q2	Q3	$\overline{Q3}$
Shift Mode	H	L	L	X	X	X	X	L	Q0	Q1	Q2	$\overline{Q2}$
	H	L	H	X	X	X	X	Q0	Q0	Q1	Q2	$\overline{Q2}$
	H	H	L	X	X	X	X	$\overline{Q0}$	Q0	Q1	Q2	$\overline{Q2}$
	H	H	H	X	X	X	X	H	Q0	Q1	Q2	$\overline{Q2}$
Parallel Entry Mode	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

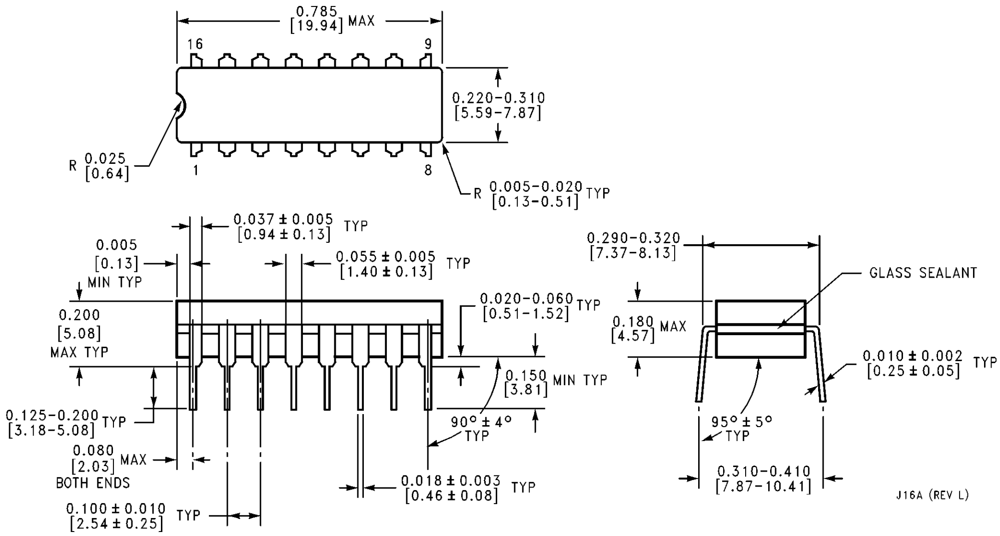
*t_{n+1} = Indicates state after next LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



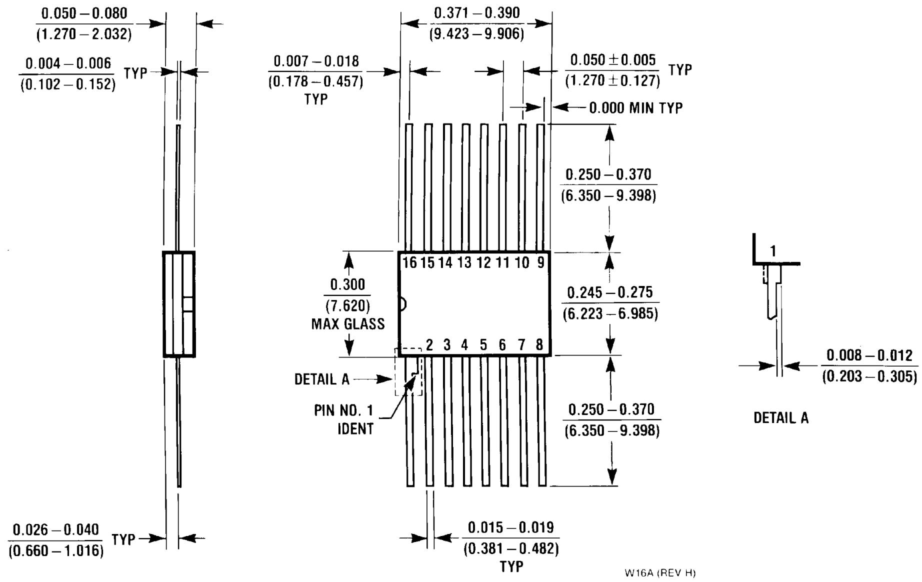
TL/F/9576–3

Physical Dimensions inches (millimeters)



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L00DMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 93L00FMQB
NS Package Number W16A

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

June 1989

93L01
1-of-10 Decoder

General Description

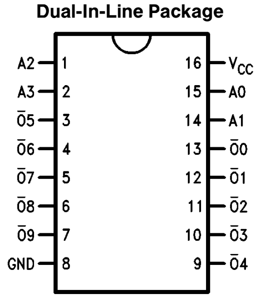
The 93L01 multipurpose decoders are designed to accept four inputs and provide ten mutually exclusive outputs.

Features

- Multifunction capability
- Mutually exclusive outputs
- Demultiplexing capability
- Typical power dissipation of 45 mW

Connection Diagram

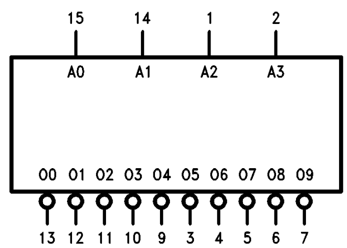
Dual-In-Line Package



TL/F/9583–1

Order Number 93L01DMQB or 93L01FMQB
See Package Number J16A or W16A

Logic Symbol



TL/F/9583–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A3	Address Inputs
$\overline{O}0$–$\overline{O}9$	Decoder Outputs (Active LOW)

 TL/F/9583 RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range MIL	$-55^{\circ}C$ to $+125^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L01 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−400	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 3 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay An to $\overline{O}$n		36 36	ns

Functional Description

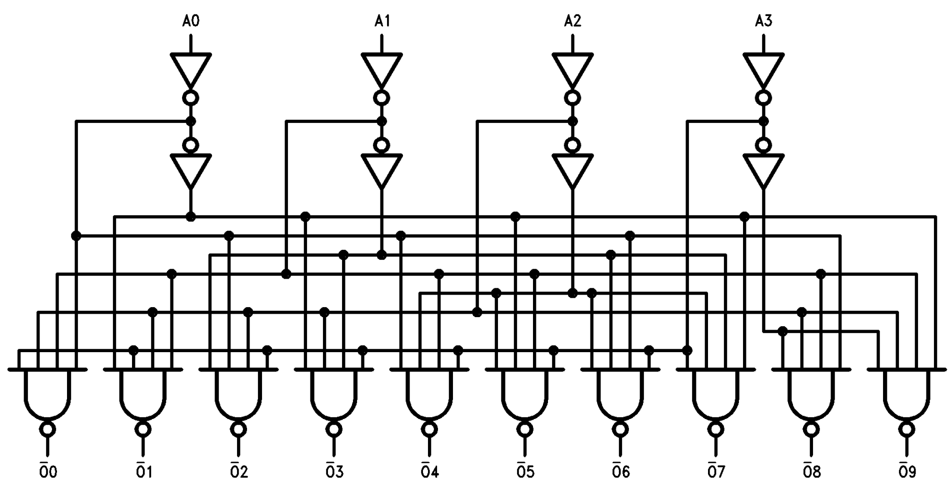
The 93L01 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables. The logic design of the 93L01 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs. The most significant input A3 produces a useful inhibit function when the 93L01 is used as a 1-of-8 decoder.

Truth Table

Inputs				Outputs									
A0	A1	A2	A3	$\overline{O}0$	$\overline{O}1$	$\overline{O}2$	$\overline{O}3$	$\overline{O}4$	$\overline{O}5$	$\overline{O}6$	$\overline{O}7$	$\overline{O}8$	$\overline{O}9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

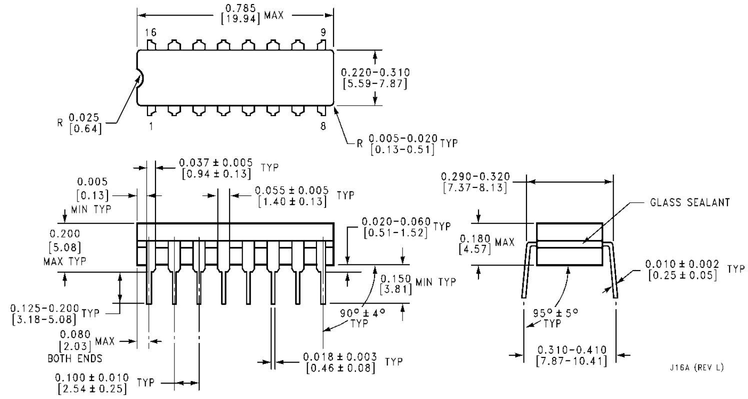
H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram

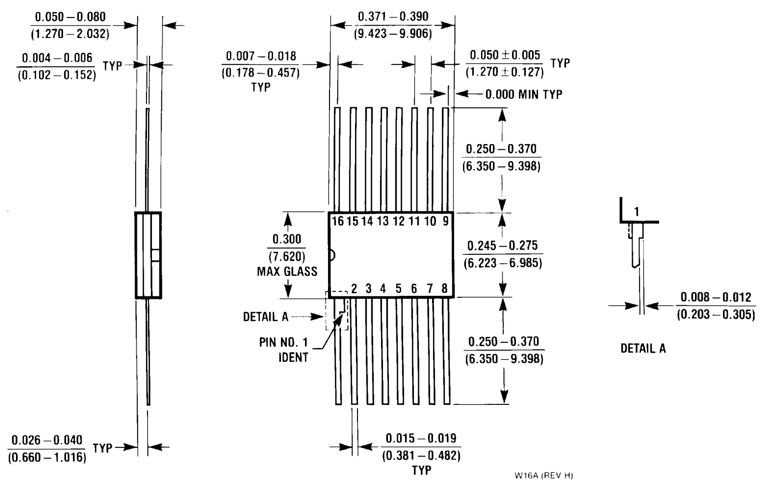


TL/F/9583-3

Physical Dimensions inches (millimeters)



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L01DMQB
NS Package Number J16A



16-Lead Ceramic Flat Package (W)
Order Number 93L01FMQB
NS Package Number W16A

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National Semiconductor

June 1989

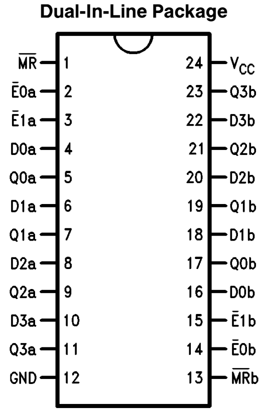
93L08 Dual 4-Bit Latch

General Description

The 93L08 is a dual 4-bit D-type latch designed for general purpose storage applications in digital systems. Each latch contains both an active LOW Master Reset input and active LOW Enable inputs.

Connection Diagram

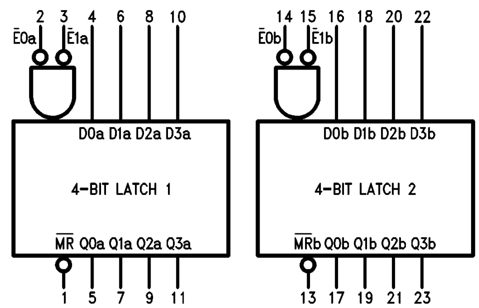
Dual-In-Line Package



TL/F/9594–1

Order Number 93L08DMQB or 93L08FMQB
See NS Package Number J24A or W24C

Logic Symbol



TL/F/9594–2

V_{CC} = Pin 24
GND = Pin 12

Pin Names	Description
D0a–D3a, D0b–D3b	Parallel Latch Inputs
$\overline{\text{E}}$0a, $\overline{\text{E}}$1a, $\overline{\text{E}}$0b, $\overline{\text{E}}$1b,	AND Enable Inputs (Active LOW)
$\overline{\text{MR}}$a, $\overline{\text{MR}}$b	Master Reset Inputs (Active LOW)
Q0a–Q3a, Q0b–Q3b	Parallel Latch Outputs

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H)	Setup Time HIGH, D_n to $\overline{E}_n$	8			ns
t_h (H)	Hold Time HIGH, D_n to $\overline{E}_n$	1			ns
t_s (L)	Setup Time LOW, D_n to $\overline{E}_n$	18			ns
t_h (L)	Hold Time LOW, D_n to $\overline{E}_n$	4			ns
t_w (L)	$\overline{E}_n$ Pulse Width LOW	32			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	30			ns
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}_n$	10			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			D_n			30	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−400	μA
			D_n			−640	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				29	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 3 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$n to Qn		45 38	ns
t_{PLH} t_{PHL}	Propagation Delay Dn to Qn		27 29	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Qn		30	ns

Functional Description

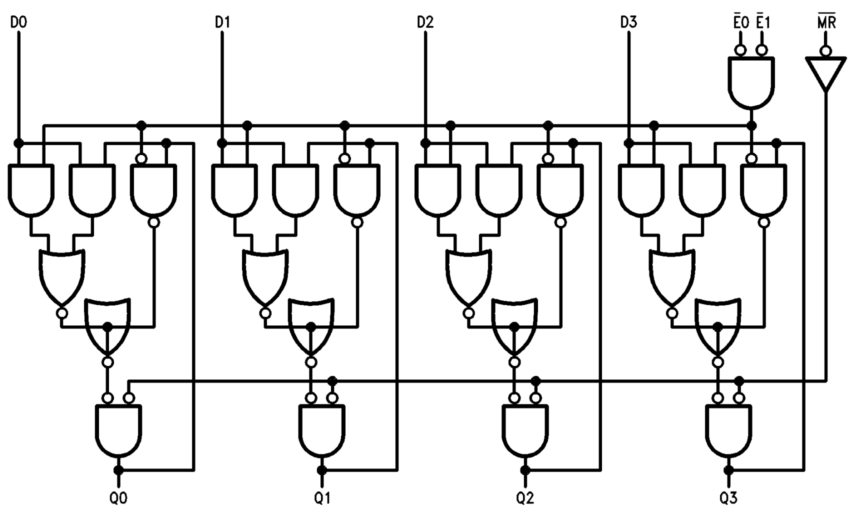
Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input. The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the Master Reset input.

Truth Table

$\overline{MR}$	$\overline{E}0$	$\overline{E}1$	D	Qn	Operation
H	L	L	L	L	Data Entry
H	L	L	H	L	Data Entry
H	L	H	X	Qn−1	Hold
H	H	L	X	Qn−1	Hold
H	H	H	X	Qn−1	Hold
L	X	X	X	L	Reset

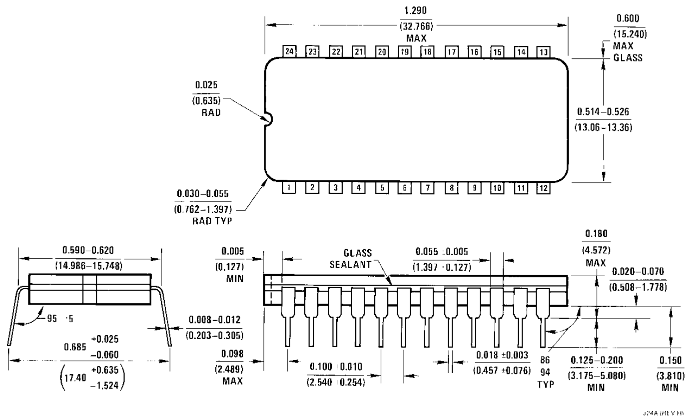
Q_{n-1} = Previous Output State
Q_n = Present Output State
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram

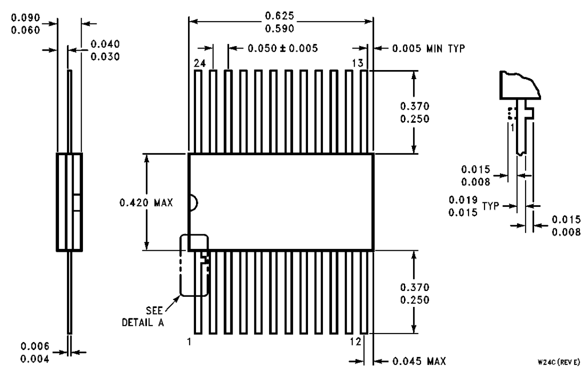


TL/F/9594–3

Physical Dimensions inches (millimeters)



24-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L08DMQB
NS Package Number J24A



24-Lead Ceramic Flat Package (W)
Order Number 93L08FMQB
NS Package Number W24C

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National Semiconductor

June 1989

93L09 Dual 4-Input Multiplexer

General Description

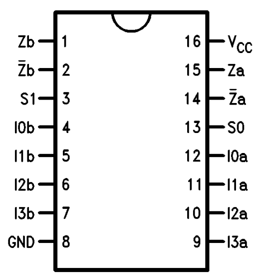
The 93L09 monolithic dual 4-input digital multiplexers consist of two multiplexing circuits with common input select logic. Each circuit contains four inputs and fully buffered complementary outputs. In addition to multiplexer operation, the 93L09 can generate any two functions of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the 93L09 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output bus.

Features

- Multifunction capability
- On-chip select logic decoding
- Fully buffered complementary outputs

Connection Diagram

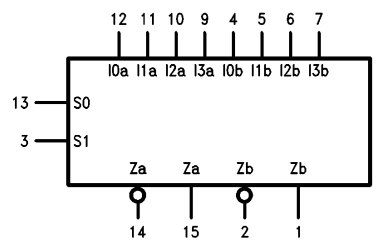
Dual-In-Line Package



TL/F/9602–1

Order Number 93L09DMQB or 93L09FMQB
See NS Package Number J16A or W16A

Logic Symbol



TL/F/9602–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
S0, S1	Common Select Inputs
I0a–I3a	Multiplexer A Inputs
Za	Multiplexer A Output
$\overline{Z}a$	Complementary Multiplexer A Output
I0b–I3b	Multiplexer B Inputs
Zb	Multiplexer B Output
$\overline{Z}b$	Complementary Multiplexer B Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L09 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, II = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	V
II	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
IIH	High Level Input Current	V_{CC} = Max, V_I = 2.4V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−400	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−10		−40	mA
I_{CC}	Supply Current	V_{CC} = Max			11.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay S_0 to Z_a		70 60	ns
t_{PLH} t_{PHL}	Propagation Delay S_0 to $\overline{Z}_a$		55 50	ns
t_{PLH} t_{PHL}	Propagation Delay I_0 to Z_a		70 65	ns
t_{PLH} t_{PHL}	Propagation Delay S_0 to $\overline{Z}_a$		40 60	ns

Functional Description

The 93L09 dual 4-input multiplexers are able to select two bits of either HIGH or LOW data or control from up to four sources, in one package. The 93L09 is the logical implementation of two-pole, four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

$$Za = I0a \bullet \overline{S1} \bullet \overline{S0} + I1a \bullet \overline{S1} \bullet S0 + I2a \bullet S1 \bullet \overline{S0} + I3a \bullet S1 \bullet S0$$

$$Zb = I0b \bullet \overline{S1} \bullet \overline{S0} + I1b \bullet \overline{S1} \bullet S0 + I2a \bullet S1 \bullet \overline{S0} + I3b \bullet S1 \bullet S0$$

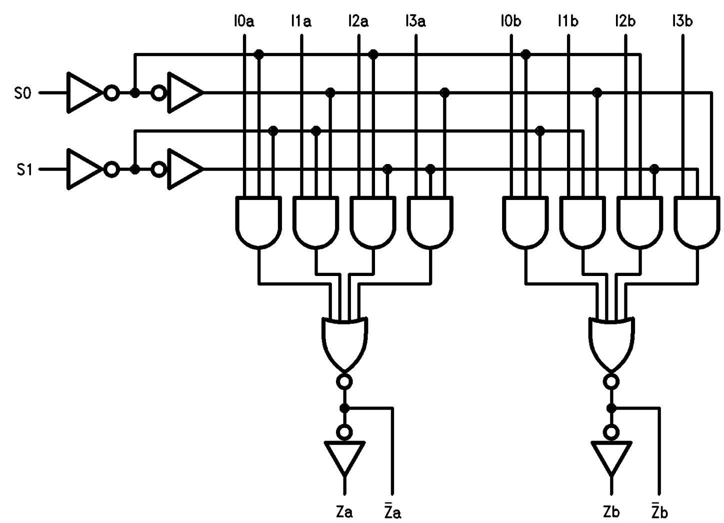
The 93L09 is frequently used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the select inputs. A less obvious application is as a function generator. The 93L09 can generate two functions of three variables. This is useful for implementing random gating functions.

Truth Table

Select Inputs		Inputs (a or b)				Outputs (a or b)	
S0	S1	I0	I1	I2	I3	Z	$\overline{Z}$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Immaterial

Logic Diagram



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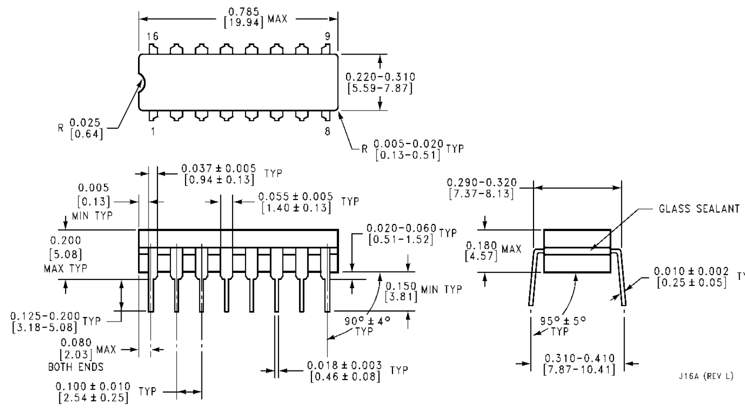
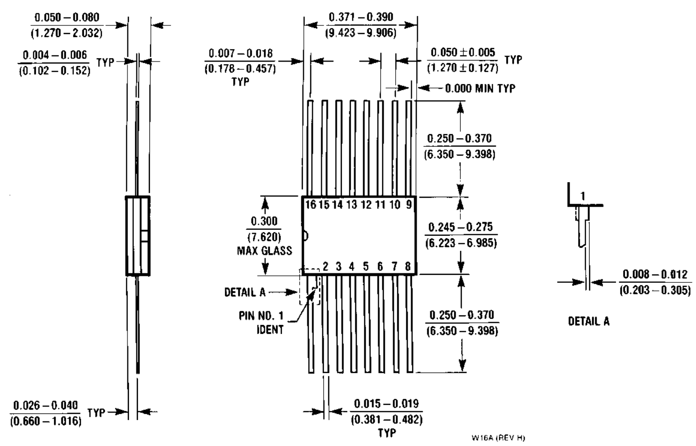
Physical Dimensions inches (millimeters)



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L09DMQB
NS Package Number J16A



16-Lead Ceramic Flat Package (W)
Order Number 93L09FMQB
NS Package Number W16A

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National Semiconductor

June 1989

93L10/93L16
BCD Decade Counter/4-Bit Binary Counter

General Description

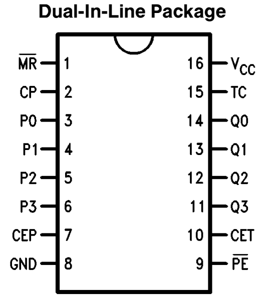
The 93L10 is a high speed synchronous BCD decade counter and the 93L16 is a high speed synchronous 4-bit binary counter. They are synchronously presettable, multifunctional MSI building blocks useful in a large number of counting, digital integration and conversion applications. Several states of synchronous operation are obtainable with no external gating packages required through an internal carry lookahead counting technique.

Features

- Synchronous counting and parallel entry
- Decoded terminal count
- Built-in Carry Circuitry
- Easy interfacing with DTL, LPDTL, and TTL families

Connection Diagram

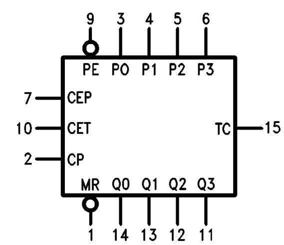
Dual-In-Line Package



TL/F/9603–1

Order Number 93L10DMQB, 93L10FMQB,
93L16DMQB or 93L16FMQB
See NS Package Number J16A or W16A

Logic Symbol



TL/F/9603–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
P0–P3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q0–Q3	Flip-Flop Outputs
TC	Terminal Count Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	$-55°C$ to $+125°C$
Storage Temperature Range	$-65°C$ to $+150°C$

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L10/93L16 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Voltage			-400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	-55		125	°C
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW P_n to CP	75 75			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW P_n to CP	10 10			ns
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW $\overline{PE}$ to CP	(Note 2) 53			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW $\overline{PE}$ to CP	7.0 (Note 2)			ns
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW CEP or CET to CP	26 (Note 1)			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW CEP or CET to CP	(Note 1) 10			ns
$t_w(H)$ $t_w(L)$	CP Pulse Width	25 25			ns
$t_w(L)$	$\overline{MR}$ Pulse Width LOW	65			ns
t_{rec}	Recovery Time, $\overline{MR}$ to CP	30			ns

Note 1: The Setup Time "$t_s(L)$" and Hold Time "$t_h(H)$" between the Count Enable (CEP and CET) and the Clock (CP) indicate that the HIGH-to-LOW transition of the CEP and CET must occur only while the Clock is HIGH for conventional operation.

Note 2: The Setup Time "$t_s(H)$" and Hold Time "$t_h(L)$" between the Parallel Enable ($\overline{PE}$) and Clock (CP) indicate that the LOW-to-HIGH transition of the $\overline{PE}$ must occur only while the Clock is HIGH for conventional operation.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			CET, CP, PE			40	
			P_n			13.3	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−400	μA
			CET, CP, PE			−800	
			P_n			−267	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max				27.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Count Frequency	13		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q		32 39	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		66 30	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC		35 30	ns
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q		72	ns

Functional Description

The 93L10 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it increments to state 0 (LLLL). The 93L16 counts modulo-16 in binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Four control inputs—Master Reset ($\overline{MR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 93L10 and 93L16 contain masterslave flip-flops which are ''next-state catching'' because of the JK feedback. This means that when CP is LOW, information that would change the state of a flip-flop, whether from the counting logic or the parallel entry logic if either mode is momentarily enabled, enters the master and is locked in. Thus to avoid inadvertently changing the state of a master latch, and the subsequent transfer of the erroneous information to the slave when the clock rises, it is necessary to insure that neither the counting mode, nor the parallel entry mode is momentarily enabled while CP is LOW.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state (9 for the decade counters, 15 for the binary counters—fully decoded in both types). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. These two schemes are shown in *Figures a* and *b*. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the state diagrams.

MULTISTAGE COUNTING

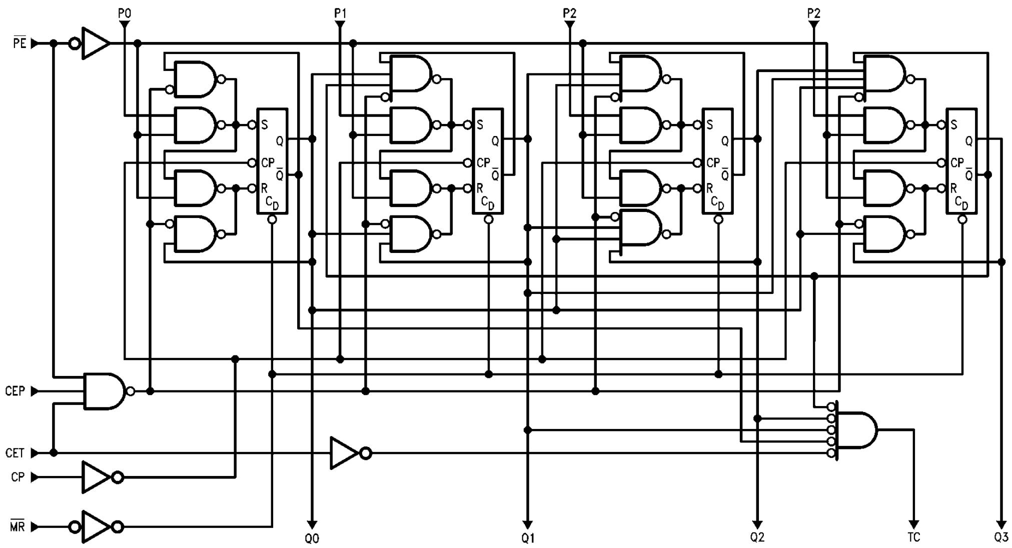
The '10/'16 counters may be cascaded to provide multistage synchronous counting. Two methods commonly used to cascade these counters are shown in *Figures a* and *b*.

In multistage counting, all less significant stages must be at their terminal count before the next more significant counter is enabled. The '10/'16 internally decodes the terminal count condition and ''ANDs'' it with the CET input to generate the terminal count (TC) output. This arrangement allows one to perform series enabling by connecting the TC output (enable signal) to the CET input of the following stage, *Figure a*. The setup requires very few interconnections, but has the following drawback: since it takes time for the enable to ripple through the counter stages, there is a reduction in maximum counting speed. To increase the counting rate, it is necessary to decrease the propagation delay of the TC signal, which is done in the second method.

The scheme illustrated in *Figure b* permits multistage counting, limited by the fan-out of the terminal count. The CEP input of the '10/'16 is internally ''ANDed'' with the CET input and as a result, both must be HIGH for the counter to be enabled. The CET inputs are connected as before except for the second stage. There the CET input is left floating and is therefore HIGH. Also, all CEP inputs are connected to the terminal output of the first stage. The advantage of this method is best seen by assuming all stages except the second and last are in their terminal condition. As the second stage advances to its terminal count, an enable is allowed to trickle down to the last counter stage, but has the full cycle time of the first counter to reach it. Then as the TC of the first stage goes active (HIGH), all CEP inputs are activated, allowing all stages to count on the next clock.

Logic Diagrams

93L10



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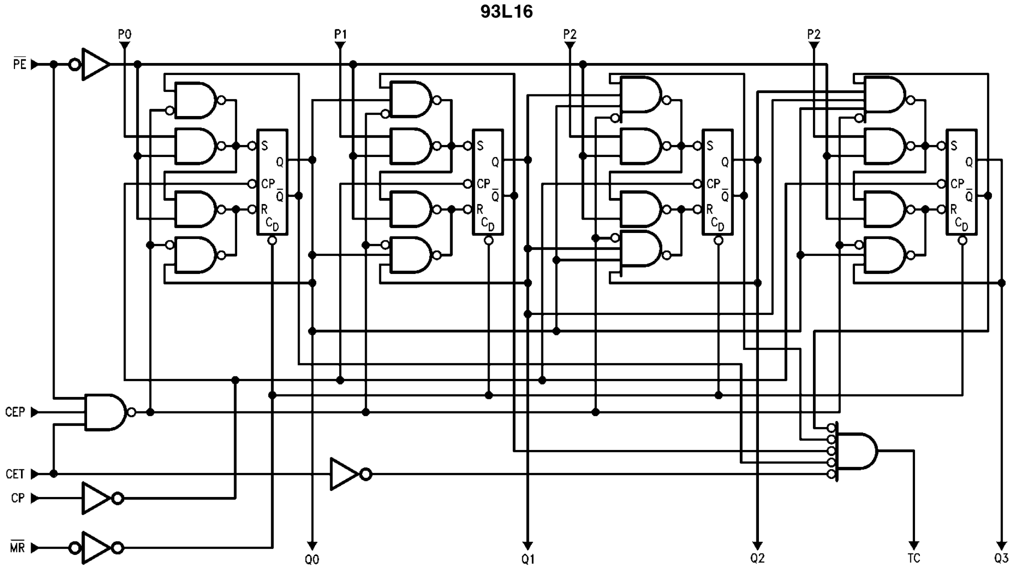
93L16



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Mode Select Table

Inputs					Response
$\overline{MR}$	$\overline{PE}$	CEP	CET	CP	
L	X	X	X	X	Clear; All Outputs LOW
H	L	X	X	$\uparrow$	Parallel Load; $P_n \rightarrow Q_n$
H	H	L	X	X	Hold
H	H	X	L	X	Hold; TC = LOW
H	H	H	H	$\uparrow$	Count Up

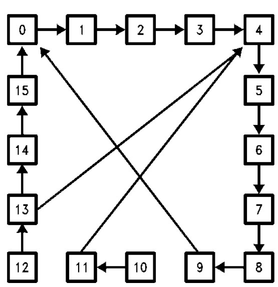
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Equations

Count Enable = MR • PE • CEP • CET
Terminal Count = CET • Q0 • Q1 • Q2 • Q3 ('16)
Terminal Count = CET • Q0 • $\overline{Q}$1 • $\overline{Q}$2 • Q3 ('10)

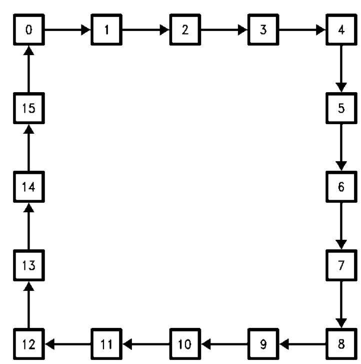
State Diagrams

93L10

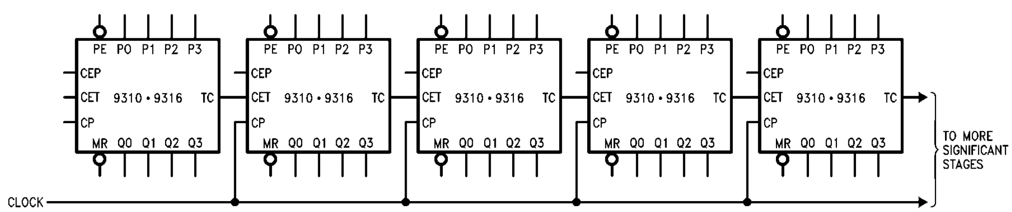


TL/F/9603-5

93L16

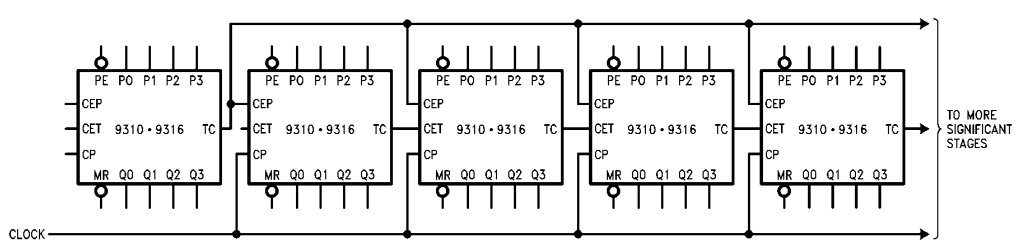


TL/F/9603-6



TL/F/9603-7

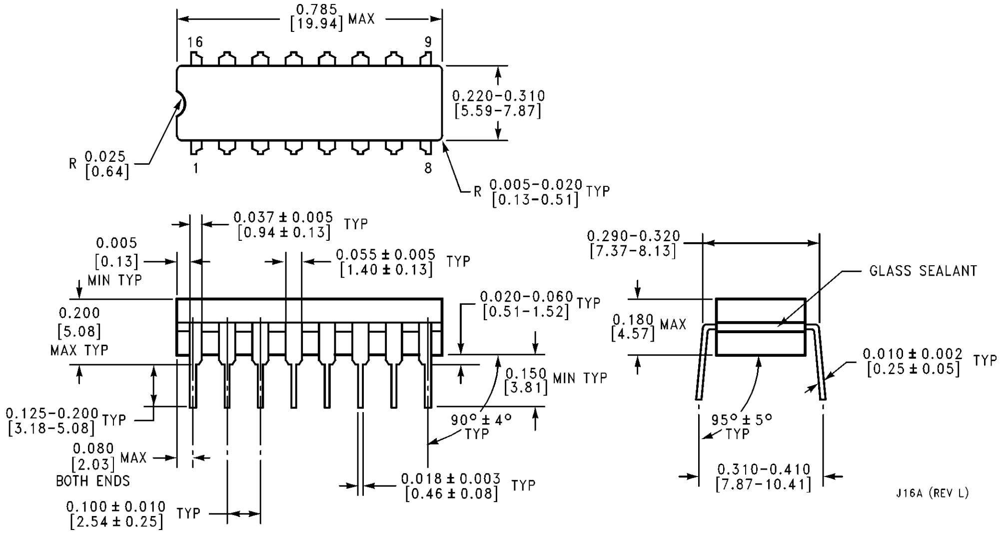
FIGURE a. Synchronous Multistage Counting Scheme (Slow)



TL/F/9603-8

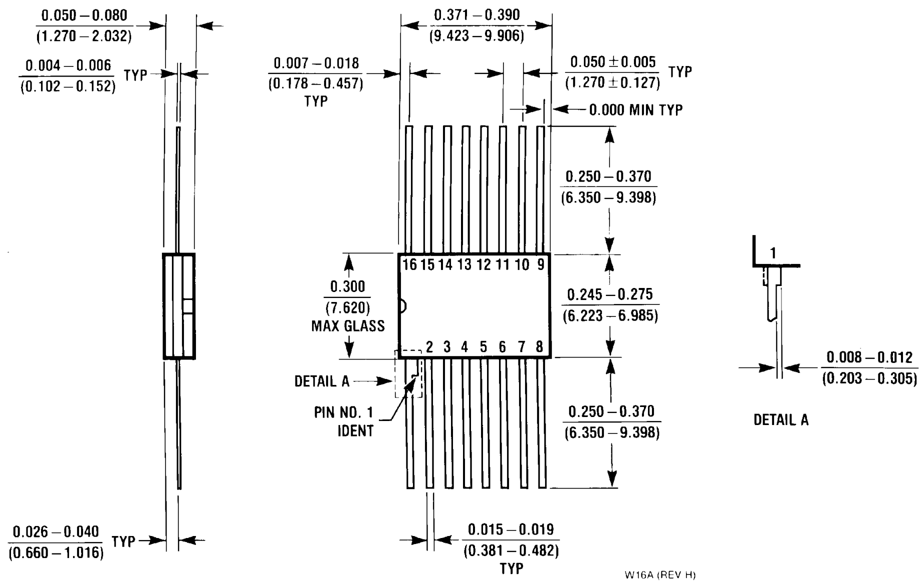
FIGURE b. Synchronous Multistage Counting Scheme (Fast)

Physical Dimensions inches (millimeters)



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L10DMQB or 93L16DMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 93L10FMQB or 93L16FMQB
NS Package Number W16A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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June 1989

93L12
8-Input Multiplexer

General Description

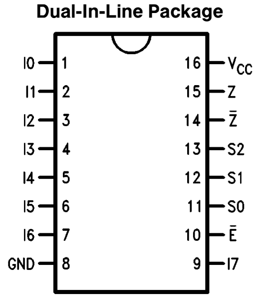
The 93L12 is a monolithic, high speed, 8-input digital multiplexer circuit. It provides, in one package, the ability to select one bit of data from up to eight sources. The 93L12 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

Features

- Multifunction capability
- On-chip select logic decoding
- Fully buffered complementary outputs

Connection Diagram

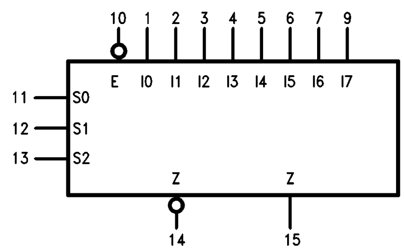
Dual-In-Line Package



TL/F/9610–1

Order Number 93L12DMQB or 93L12FMQB
See NS Package Number J16A or W16A

Logic Symbol



TL/F/9610–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
S0–S2	Select Inputs
$\overline{E}$	Enable Input (Active LOW)
I0–I7	Multiplexer Inputs
Z	Multiplexer Output
$\overline{Z}$	Complementary Multiplexer Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L12 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−400	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			13.3	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay S0 to Z		60 75	ns
t_{PLH} t_{PHL}	Propagation Delay S0 to $\overline{Z}$		70 50	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z		60 75	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$		70 45	ns
t_{PLH} t_{PHL}	Propagation Delay In to Z		70 65	ns
t_{PLH} t_{PHL}	Propagation Delay In to $\overline{Z}$		55 55	ns

Functional Description

The 93L12 is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of three Select inputs, S0, S1, S2. Both assertion and negation outputs are provided. The Enable input (E) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$
\begin{aligned}
Z = E \bullet (&I0 \bullet \overline{S0} \bullet \overline{S1} \bullet \overline{S2} + I1 \bullet S0 \bullet \overline{S1} \bullet \overline{S2} \\
&+ I2 \bullet \overline{S0} \bullet S1 \bullet \overline{S2} + I3 \bullet S0 \bullet S1 \bullet \overline{S2} \\
&+ I4 \bullet \overline{S0} \bullet \overline{S1} \bullet S2 + I5 \bullet S0 \bullet \overline{S1} \bullet S2 \\
&+ I6 \bullet \overline{S0} \bullet S1 \bullet S2 \\
&+ I7 \bullet S0 \bullet S1 \bullet S2).
\end{aligned}
$$

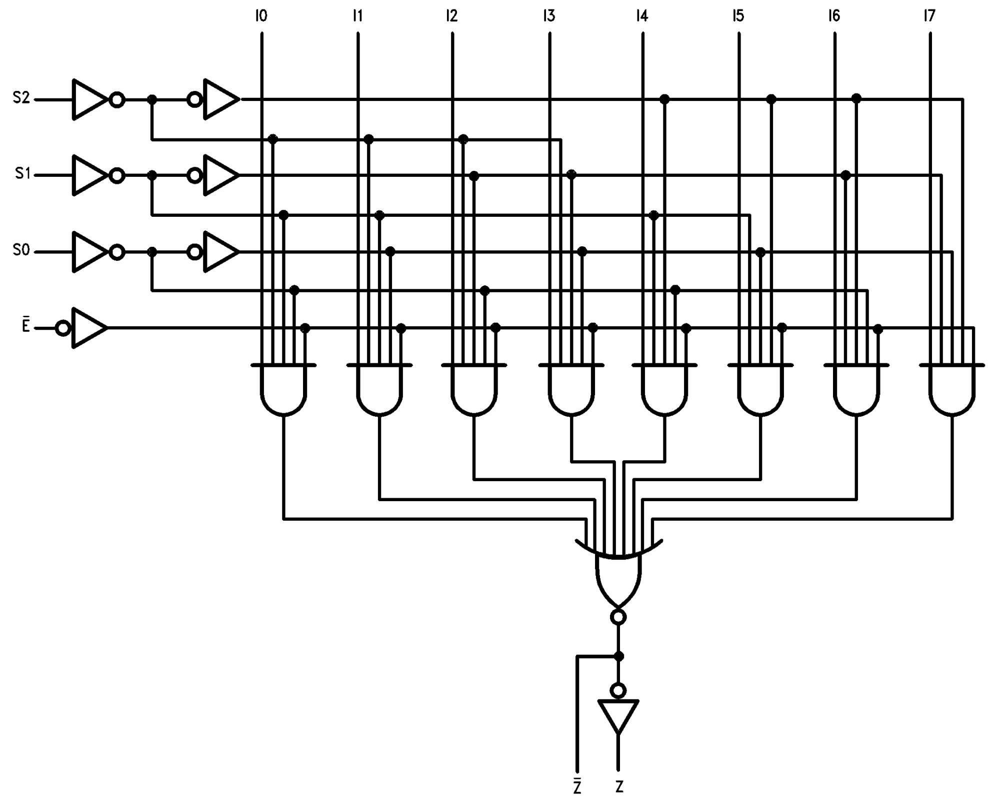
The 93L12 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 93L12 can provide any logic function of four variables and its negation. Thus any number of random logic elements used to generate unusual truth tables can be replaced by one 93L12.

Truth Table

Inputs												Outputs	
$\overline{E}$	S2	S1	S0	I0	I1	I2	I3	I4	I5	I6	I7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

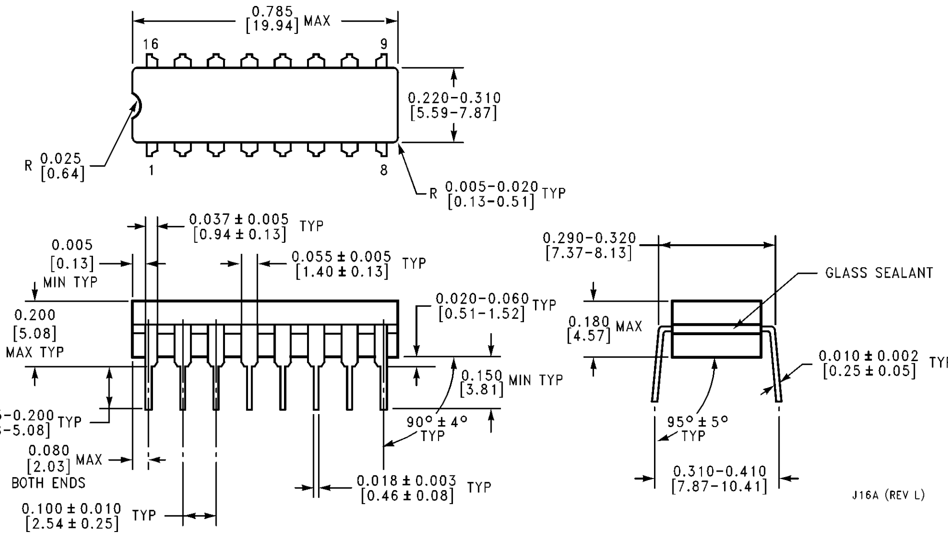
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



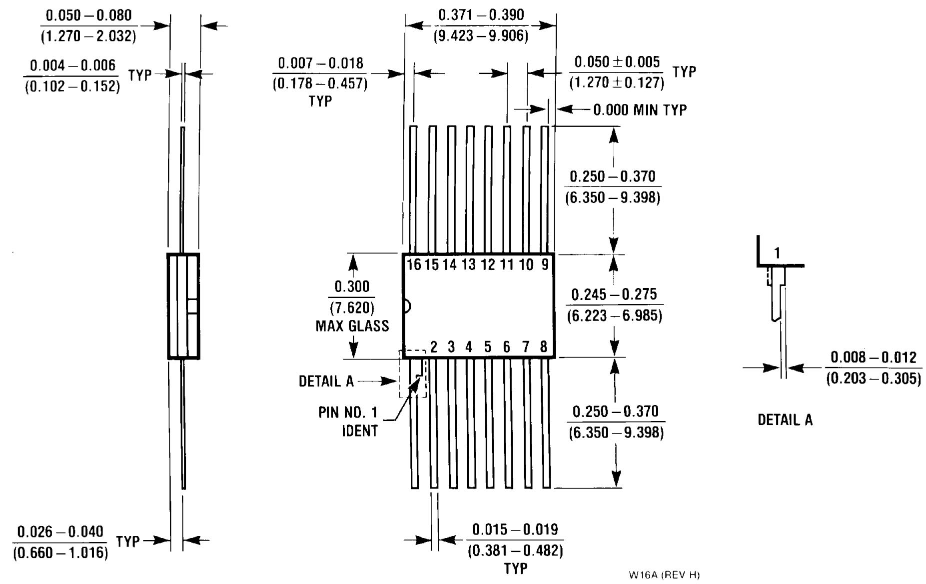
TL/F/9610–3

Physical Dimensions inches (millimeters)



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L12DMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 93L12FMQB
NS Package Number W16A

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National Semiconductor

June 1989

93L14 Quad Latch

General Description

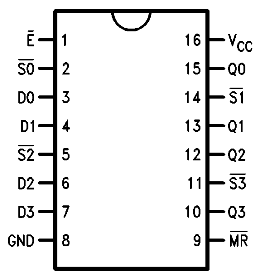
The 93L14 is a multifunctional 4-bit latch designed for general purpose storage applications in high speed digital systems. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good noise immunity.

Features

- Can be used as single input D latches or set/reset latches
- Active low enable gate input
- Overriding master reset

Connection Diagram

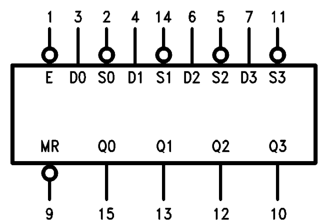
Dual-In-Line Package



TL/F/9612–1

Order Number 93L14DMQB or 93L14FMQB
See NS Package Number J16A or W16A

Logic Symbol



TL/F/9612–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
D0–D3	Data Inputs
$\overline{S0}$–$\overline{S3}$	Set Inputs (Active LOW)
$\overline{MR}$	Master Reset Input (Active LOW)
Q0–Q3	Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L14 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Voltage			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to $\overline{E}$	10 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to $\overline{E}$	0 10			ns
t_s (H)	Setup Time HIGH, D_n to $\overline{S}_n$	15			ns
t_h (L)	Hold Time LOW, D_n to $\overline{S}_n$	5			ns
t_w (L)	$\overline{E}$ Pulse Width LOW	30			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	25			ns
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}$	5			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			D_n			30	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−400	μA
			D_n			−600	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				16.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		45 36	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		30 30	ns
t_{PLH}	Propagation Delay, $\overline{MR}$ to Q_n		30	ns
t_{PHL}	Propagation Delay, $\overline{S}_n$ to Q_n		33	ns

Functional Description

The 93L14 consists of four latches with a common active LOW Enable input and active LOW Master Reset input. When the Enable goes HIGH, data present in the latches is stored and the state of the latch is no longer affected by the $\overline{S}_n$ and D_n inputs. The Master Reset when activated overrides all other input conditions forcing all latch outputs LOW. Each of the four latches can be operated in one of two modes:

D-TYPE-LATCH—For D-type operation the $\overline{S}$ input of a latch is held LOW. While the common Enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the Enable goes HIGH.

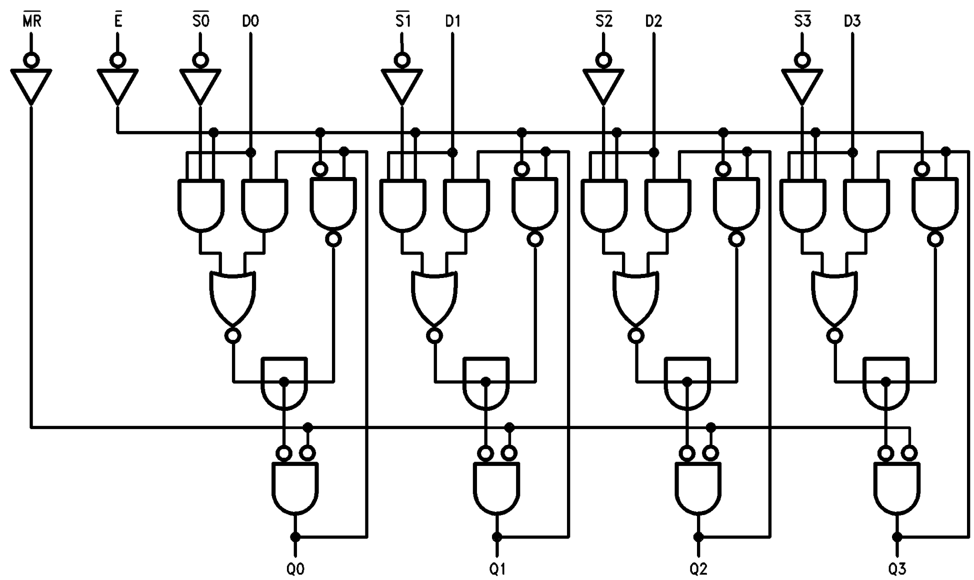
SET/RESET LATCH—During set/reset operation when the common Enable is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the $\overline{S}$ input if the D input is HIGH. If both $\overline{S}$ and D inputs are LOW, the D input will dominate and the latch wil be reset. When the Enable goes HIGH, the latch remains in the last state prior to disablement. The two modes of latch operation are shown in the Truth Table.

Truth Table

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_n	Operation
H	L	L	L	L	D Mode
H	L	H	L	L	
H	H	X	X	Q_{n-1}	
H	L	L	L	L	R/S Mode
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{n-1}	
H	H	X	X	Q_{n-1}	
L	X	X	X	L	RESET

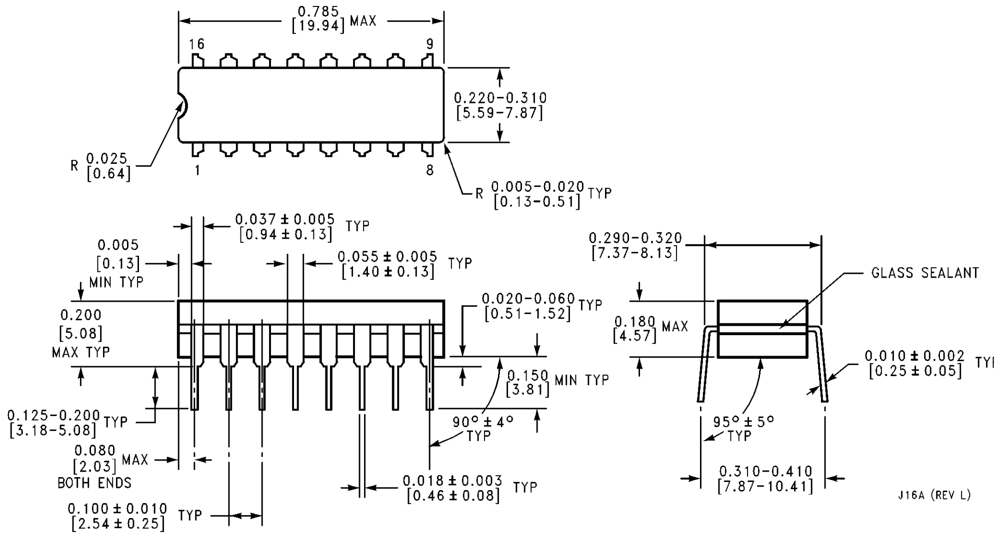
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Q_{n-1} = Previous Output State
Q_n = Present Output State

Logic Diagram



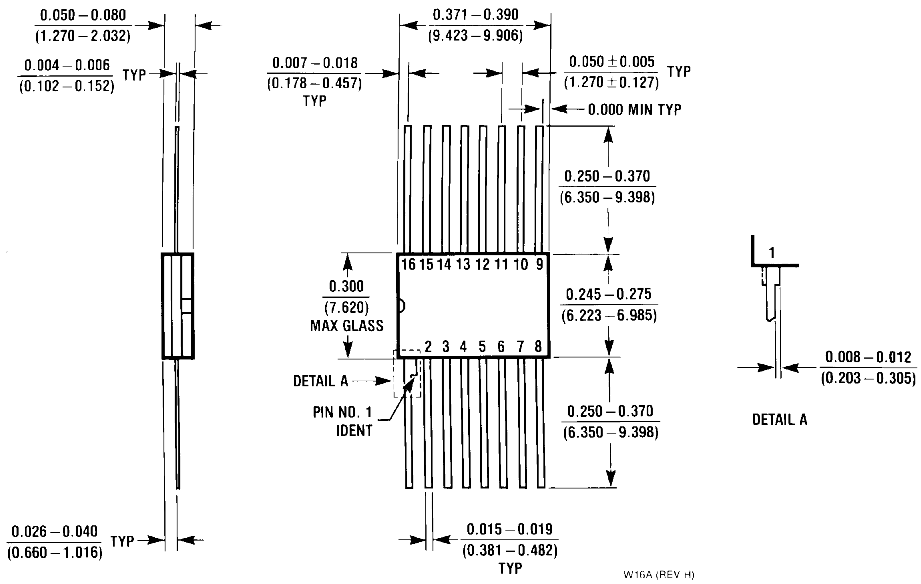
TL/F/9612–3

Physical Dimensions inches (millimeters)



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L14DMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 93L14FMQB
NS Package Number W16A

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National Semiconductor

June 1989

93L21 Dual 1-of-4 Decoder

General Description

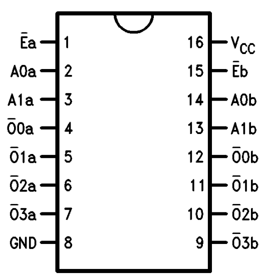
The 93L21 consists of two independent multipurpose decoders, each designed to accept two inputs and provide four mutually exclusive outputs. In addition an active LOW enable input, which gives demultiplexing capability, is provided for each decoder.

Features

- Multifunction capability
- Mutually exclusive outputs
- Demultiplexing capability
- Active low enable for each decoder

Connection Diagram

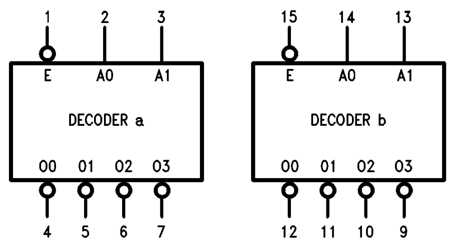
Dual-In-Line Package



TL/F/10197–1

Order Number 93L21DMQB or 93L21FMQB
See NS Package Number J16A or W16A

Logic Symbol



TL/F/10197–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
Ēa, Ēb	Enable Inputs (Active LOW)
A0a, A1a, A0b, A1b	Address Inputs
Ō0a–Ō3a Ō0b–Ō3b	Decoder Outputs (Active LOW)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L12 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating	−55		125	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, II = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	V
II	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
IIH	High Level Input Current	V_{CC} = Max, V_I = 2.4V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−400	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			13.2	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Functional Description

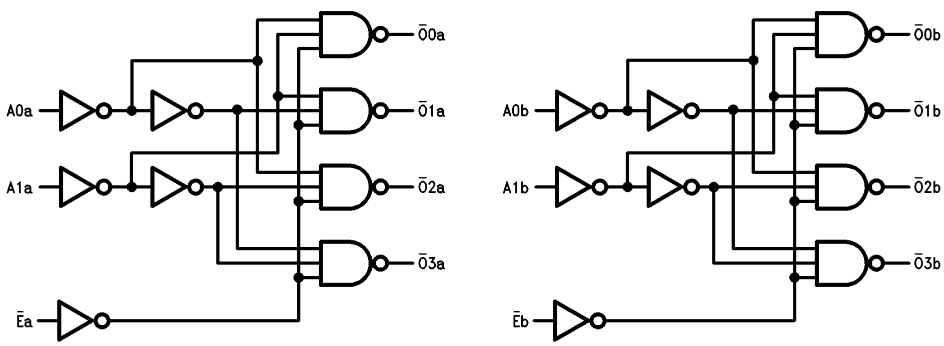
The 93L21 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs as shown in the logic symbol. Each decoder can be used as a 4-output demultiplexer by using the enable as a data input.

Truth Table (Each Decoder)

Inputs			Outputs			
$\overline{E}$	A0	A1	$\overline{O}0$	$\overline{O}1$	$\overline{O}2$	$\overline{O}3$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram

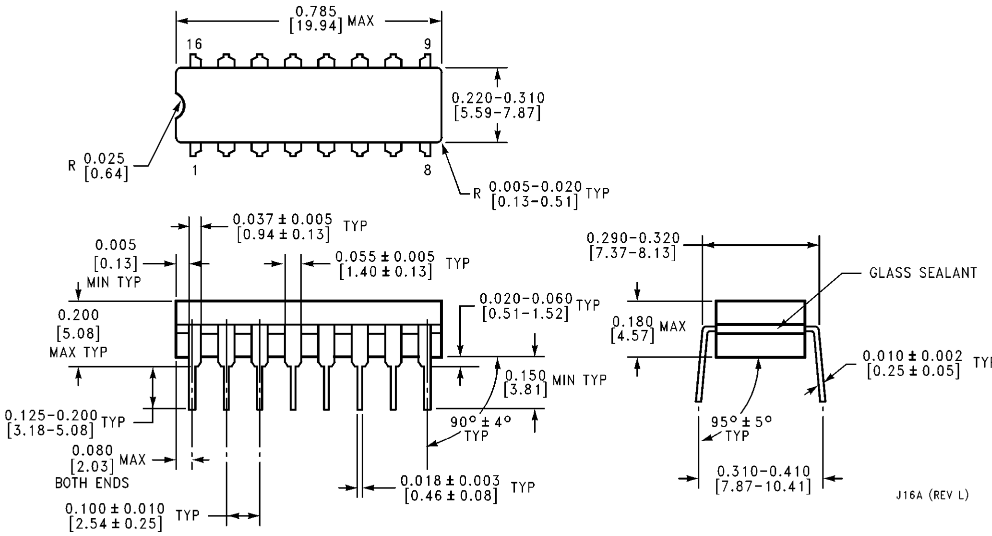


TL/F/10197–3

Switching Characteristics V_{CC} = +5.0V, T_A = +25°C (See Section 5 for test waveforms and output load.)

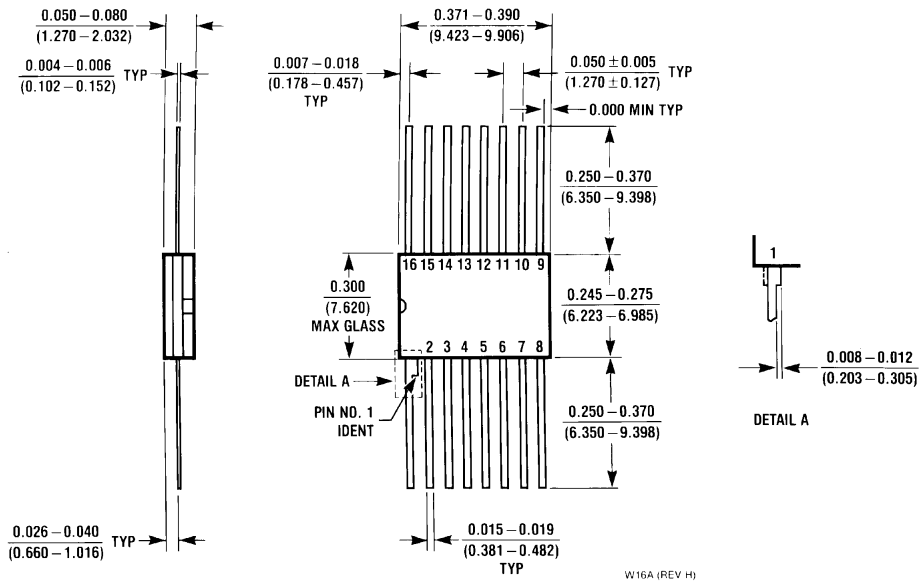
Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
tPLH tPHL	Propagation Delay An to $\overline{O}$n		50 65	ns
tPLH tPHL	Propagation Delay $\overline{E}$n to $\overline{O}$n		40 52	ns

Physical Dimensions inches (millimeters)



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L21DMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 93L21FMQB
NS Package Number W16A

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June 1989

93L22
Quad 2-Input Multiplexer

General Description

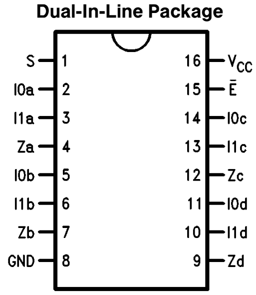
The 93L22 quad 2-input digital multiplexers consist of four multiplexing circuits with common select and enable logic; each circuit contains two inputs and one output.

Features

- Multifunction capability
- On-chip select logic decoding
- Fully buffered outputs

Connection Diagram

Dual-In-Line Package

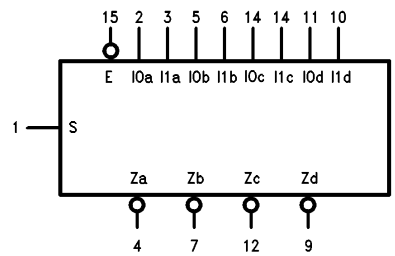


TL/F/10198–1

Order Number 93L22DMQB or 93L22FMQB
See NS Package Number J16A or W16A

Pin Names	Description
S	Common Select Input
$\overline{E}$	Enable Input (Active LOW)
I0a–I0d I1a–I1d	Multiplexer Inputs
Za–Zd	Multiplexer Outputs

Logic Symbol



TL/F/10198–2

V_{CC} = Pin 16
GND = Pin 8

Truth Table

Inputs				Output
$\overline{E}$	S	I0n	I1n	Zn
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L22 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	V
II	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
IIH	High Level Input Current	V_{CC} = Max, V_I = 2.4V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−400	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, (Note 2)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max			13.2	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
tPLH tPHL	Propagation Delay S to Zn		36 49	ns
tPLH tPHL	Propagation Delay I0 or I1 to Zn		30 22	ns
tPLH tPHL	Propagation Delay $\overline{E}$ to Zn		27 27	ns

Functional Description

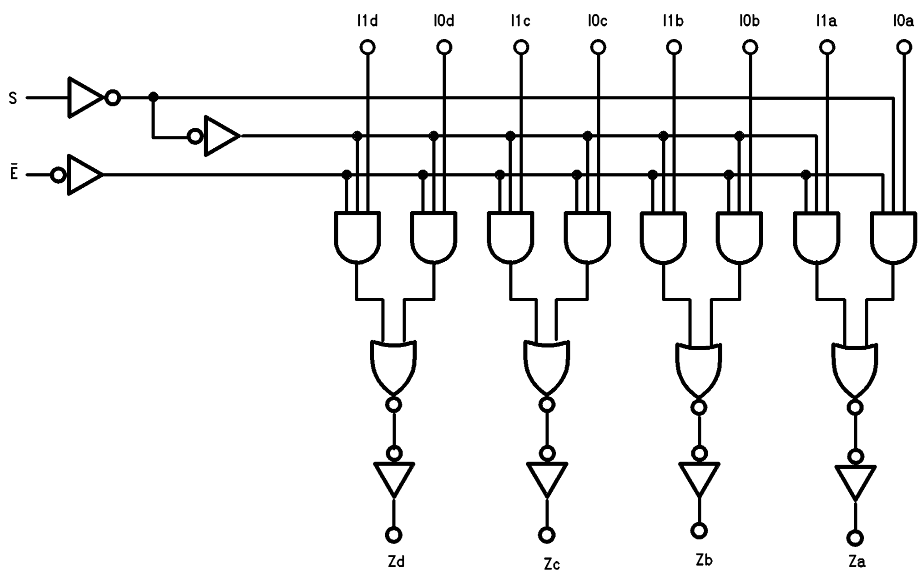
The 93L22 quad 2-input multiplexer provides the ability to select four bits of either data or control from two sources, in one package. The Enable input ($\overline{E}$) is active LOW. When not activated all outputs (Z_n) are LOW regardless of all other inputs.

The 93L22 quad 2-input multiplexer is the logical implementation of a four-pole, two position switch, with the position of the switch being set by the logic levels supplied to the one select input. The logic equations for the outputs are shown below:

$Za = E \bullet (I1a \bullet S + I0a \bullet \overline{S})$ $Zb = E \bullet (I1b \bullet S + I0b \bullet \overline{S})$
$Zc = E \bullet (I1c \bullet S + I0c \bullet \overline{S})$ $Zd = E \bullet (I1d \bullet S + I0d \bullet \overline{S})$

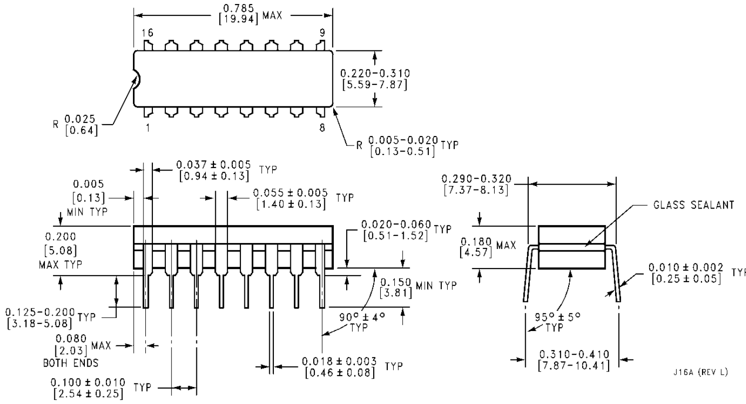
A common use of the 93L22 is the moving of data from a group of registers to four common output busses. The particular register from which the data comes is determined by the state of the select input. A less obvious use is as a function generator. The 93L22 can generate four functions of two variables with one variable common. This is useful for implementing random gating functions.

Logic Diagram

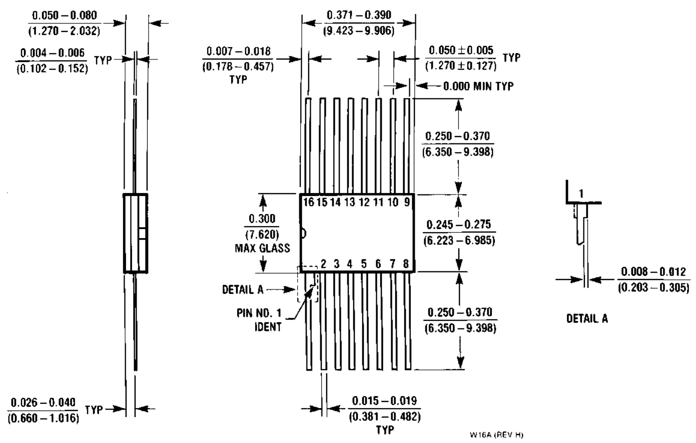


TL/F/10198–3

Physical Dimensions inches (millimeters)



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L22DMQB
NS Package Number J16A



16-Lead Ceramic Flat Package (W)
Order Number 93L22FMQB
NS Package Number W16A

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April 1998

93L24
5-Bit Comparator

General Description

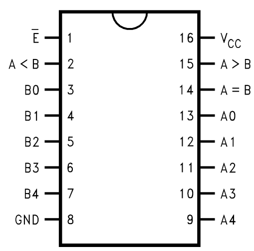
The 93L24 expandable comparator provides comparison between two 5-bit words and gives three outputs—“less than”, “greater than” and “equal to”. A HIGH on the active LOW Enable Input forces all three outputs LOW.

Features

- Three separate outputs: A<B, A>B, A=B
- Easily expandable
- Active low enable input

Connection Diagram

Dual-In-Line Package

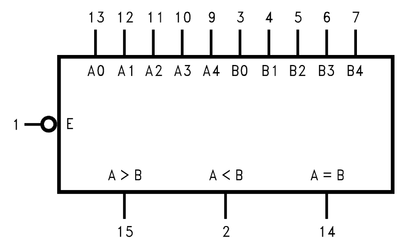


DS010199-1

Order Number 93L24DMQB or 93L24FMQB
See Package Number J16A or W16A

Pin Names	Description
Ē	Enable Input (Active LOW)
A0–A4	Word A Parallel Inputs
B0–B4	Word B Parallel Inputs
A<B	A Less than B Output (Active HIGH)
A>B	A Greater than B Output (Active HIGH)
A=B	A Equal to B Output (Active HIGH)

Logic Symbol



DS010199-2

V_{CC} = Pin 16
GND = Pin 8

Truth Table

Inputs			Outputs		
Ē	An	Bn	A<B	A>B	A=B
H	X	X	L	L	L
L	Word A = Word B		L	L	H
L	Word A > Word B		L	H	L
L	Word B < Word A		H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55˚C to +125˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	93L24 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	µA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max			21	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25˚C

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay		32	ns
t_{PHL}	$\overline{E}$ to A=B; $\overline{E}$ to A<B, A>B		35	
t_{PLH}	Propagation Delay		54	ns
t_{PHL}	An to A>B; Bn to A>B		75	
t_{PLH}	Propagation Delay		70	ns
t_{PHL}	An to A<B; Bn to A<B		77	
t_{PLH}	Propagation Delay		100	ns
t_{PHL}	An or Bn to A=B		102	

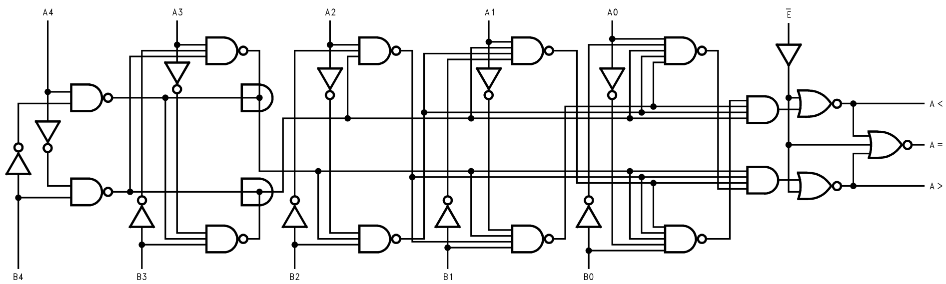
Functional Description

The 93L24 5-bit comparators use combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these ouptuts are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW Enable Input ($\overline{E}$).

Tying the A>B output from one device into an A input on another device and the A< B output into the corresponding B input permits easy expansion.

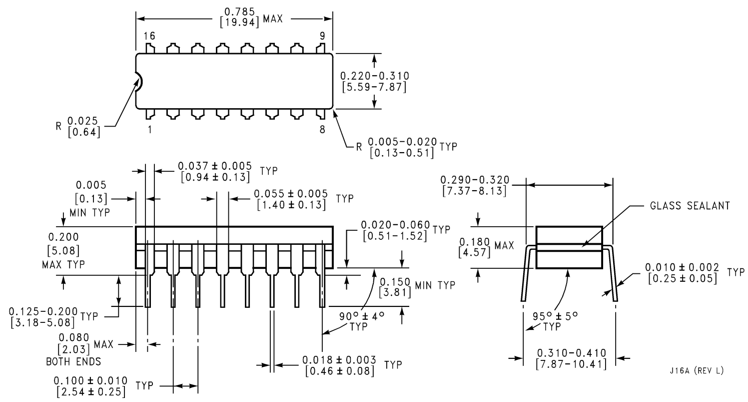
The A4 and B4 inputs are the most significant inputs and A0, B0 the least significant. Thus if A4 is HIGH and B4 is LOW, the A>B output will be HIGH regardless of all other inputs except $\overline{E}$.

Logic Diagram

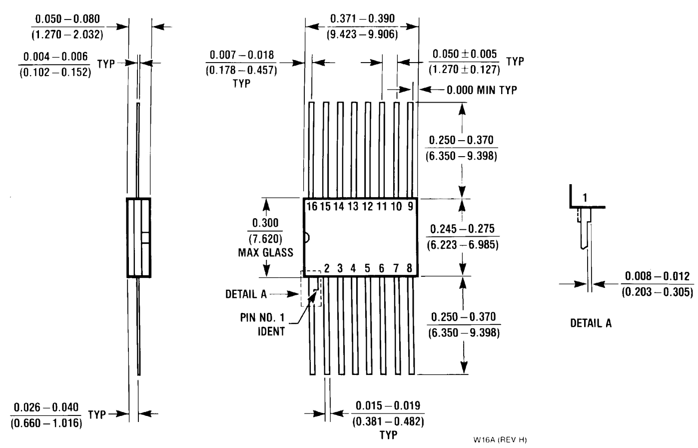


DS010199-3

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L24DMQB
Package Number J16A



16-Lead Ceramic Flat Package (W)
Order Number 93L24FMQB
Package Number W16A

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April 1998

93L28
Dual 8-Bit Shift Register

General Description

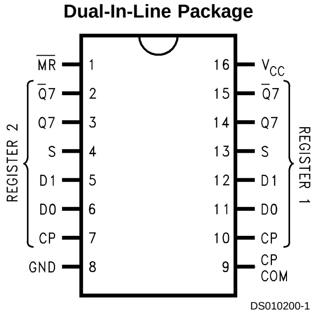
The 93L28 is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers. The multifunctional capability of this device is provided by several features: 1) additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources; 2) the clock of each register may be provided separately or together; 3) both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

Features

- 2-input multiplexer provided at data input of each register
- Gated clock input circuitry
- Both true and complementary outputs provided from last bit of each register
- Asynchronous master reset common to both registers

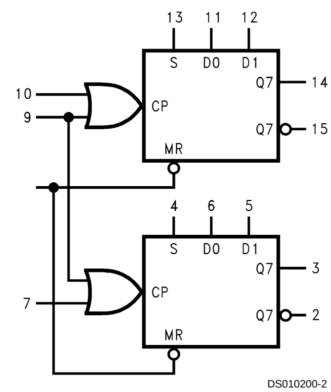
Connection Diagram

Dual-In-Line Package



Order Number 93L28DMQB or 93L28FMQB
See Package Number J16A or W16A

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
S	Data Select Input
D0, D1	Data Inputs
CP	Clock Pulse Input (Active HIGH)
	Common (Pin 9)
	Separate (Pins 7 and 10)
$\overline{MR}$	Master Reset Input (Active LOW)
Q7	Last Stage Output
$\overline{Q}7$	Complementary Output

 DS010200

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55˚C to +125˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	93L28 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	µA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	˚C
t_s(H) t_s(L)	Setup Time HIGH or LOW D_n to CP	30 30			ns
t_h(H) t_h(L)	Hold Time HIGH or LOW D_n to CP	0 0			ns
t_w(H) t_w(L)	Clock Pulse Width HIGH or LOW	55 55			ns
t_w(L)	$\overline{MR}$ Pulse Width with CP HIGH	60			ns
t_w(L)	$\overline{MR}$ Pulse Width with CP LOW	70			ns

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V	$\overline{MR}$, Dx			20	µA
			CP (7, 10)			30	
			S			40	
			CP Com			60	
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.3V	$\overline{MR}$, Dx			−400	µA
			CP (7, 10)			−600	
			S			−800	
			CP Com			−1200	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max				25.3	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25˚C (See Section 1 for test waveforms and output load)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Shift Right Frequency	5.0		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_7 or $\overline{Q}_7$		45 80	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_7		110	ns

Functional Description

The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW-to-HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH-to-LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal. Each 8-bit shift register has a 2-input multiplexer in front of the serial data input. The two data inputs D0 and D1 are controlled by the data select input (S) following the Boolean expression:

Serial data in: S_D = $\overline{S}$D0 + SD1

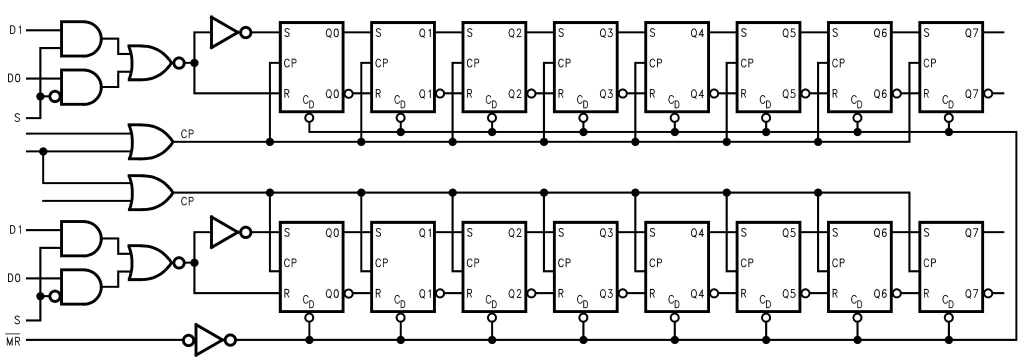
An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all 16 stages independently of any other input signal.

Shift Select Table

Inputs			Output
S	**D0**	**D1**	**Q7 (t_{n+8})**
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

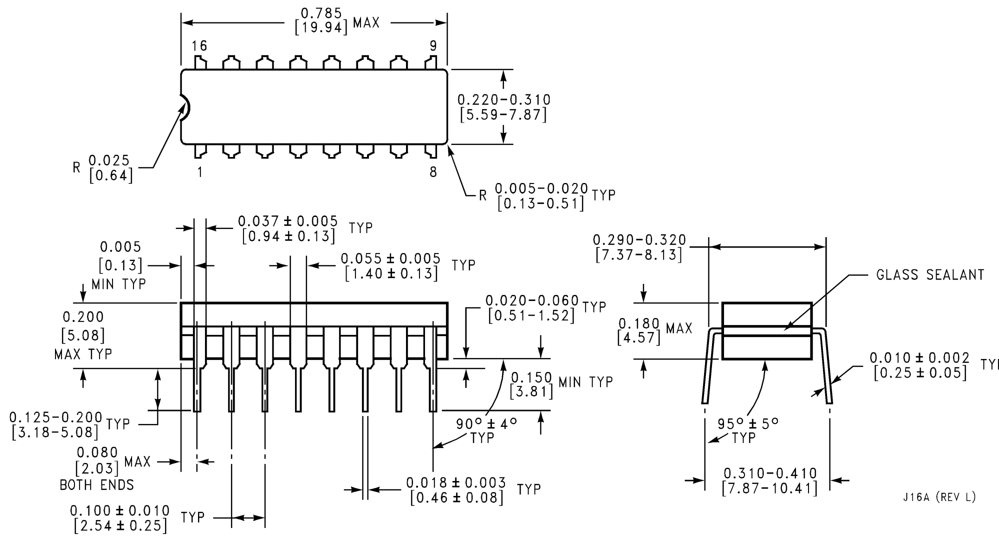
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
n+8 = Indicates state after eight clock pulse

Logic Diagram

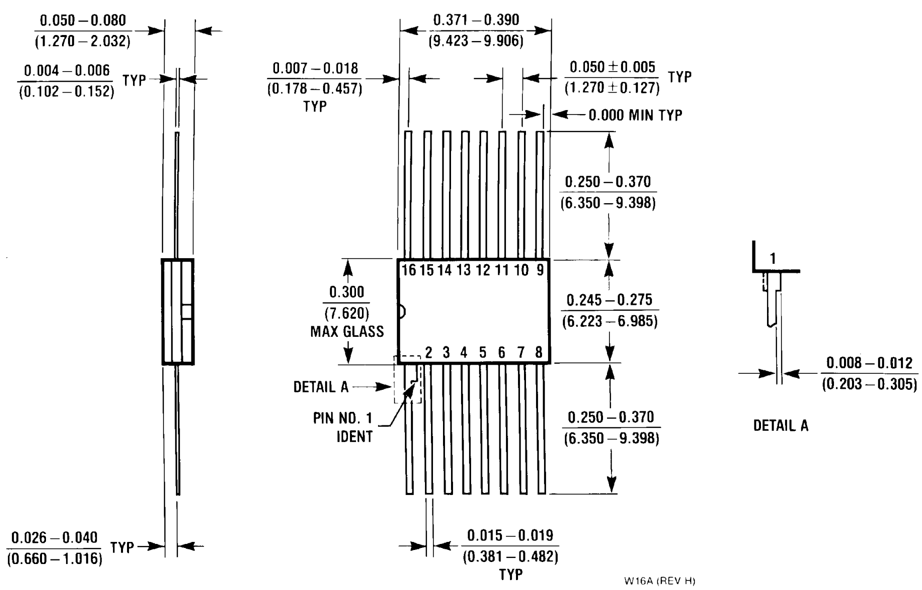


DS010200-3

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L28DMQB
Package Number J16A



16-Lead Ceramic Flat Package (W)
Order Number 93L28FMQB
Package Number W16A

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National Semiconductor

June 1989

93L34
8-Bit Addressable Latch

General Description

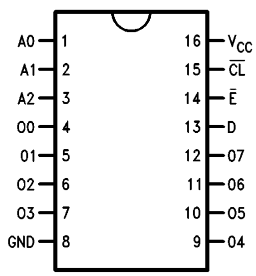
The 93L34 is an 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active LOW common clear for resetting all latches, as well as, an active LOW enable.

Features

- Serial to parallel capability
- Eight bits of storage with output of each bit available
- Random (addressable) data entry
- Active high demultiplexing or decoding capability
- Easily expandable
- Common conditional clear

Connection Diagram

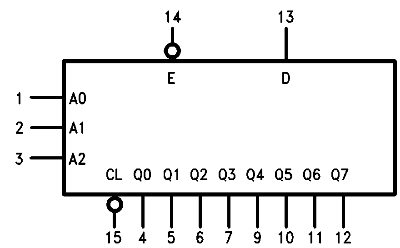
Dual-In-Line Package



TL/F/10201–1

Order Number 93L34DMQB or 93L34FMQB
See NS Package Number J16A or W16A

Logic Symbol



TL/F/10201–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A3	Address Inputs
D	Data Input
$\overline{E}$	Enable Input (Active LOW)
$\overline{CL}$	Clear Input (Active LOW)
Q0–Q7	Parallel Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L34 (Mil)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Voltage			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H)	Setup Time HIGH, D to $\overline{E}$	45			ns
t_h (H)	Hold Time HIGH, D to $\overline{E}$	−5			ns
t_s (L)	Setup Time LOW, D to $\overline{E}$	45			ns
t_h (L)	Hold Time LOW, D to $\overline{E}$	−7			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{E}$	10 10			ns
t_w (L)	$\overline{E}$ Pulse Width LOW	26			ns
t_w (L)	$\overline{CL}$ Pulse Width LOW	35			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			$\overline{E}$			30	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−0.4	mA
			$\overline{E}$			−0.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		45 42	ns
t_{PLH} t_{PHL}	Propagation Delay D to Q_n		65 45	ns
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n		66 66	ns
t_{PHL}	Propagation Delay $\overline{CL}$ to Q_n		55	ns

Functional Description

The 93L34 has four modes of operation which are shown in the Mode Select Table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the Data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the Enable should be held HIGH while the Address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the 93L34 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

Mode Select Table

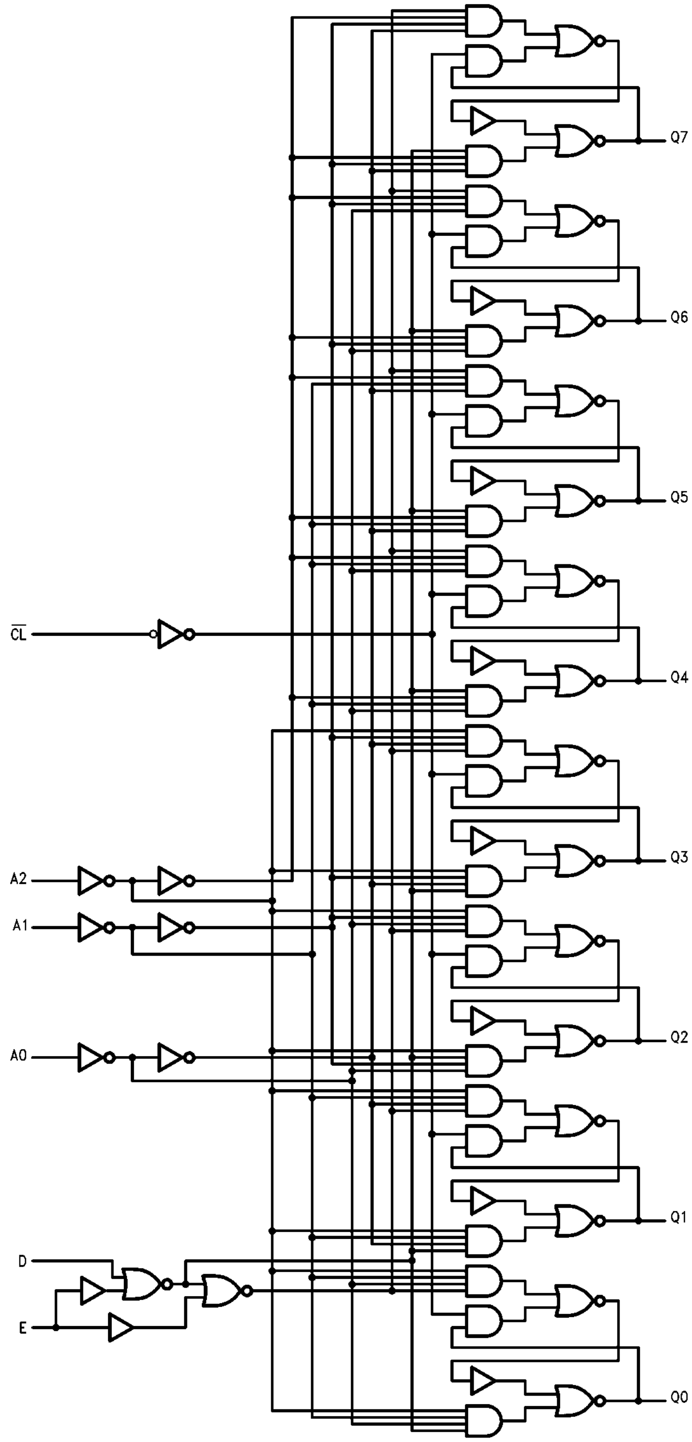
$\overline{E}$	$\overline{CL}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

Truth Table

Inputs					Outputs								Mode
$\overline{CL}$	$\overline{E}$	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	H	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	D	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	D	L	L	L	L	L	L	
L	L	L	H	L	L	L	D	L	L	L	L	L	
•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	
L	L	H	H	H	L	L	L	L	L	L	L	L	
H	H	X	X	X	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Memory
H	L	L	L	L	D	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Addressable
H	L	H	L	L	Qt−1	D	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Latch
H	L	L	H	L	Qt−1	Qt−1	D	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	
•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	
H	L	H	H	H	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	D	

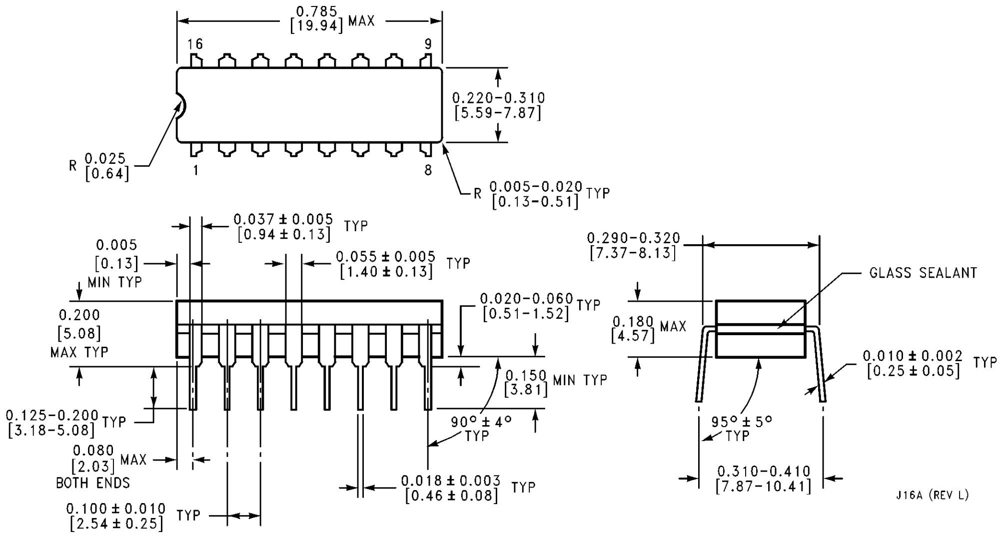
H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Qt−1 = Previous Output State

Logic Diagram



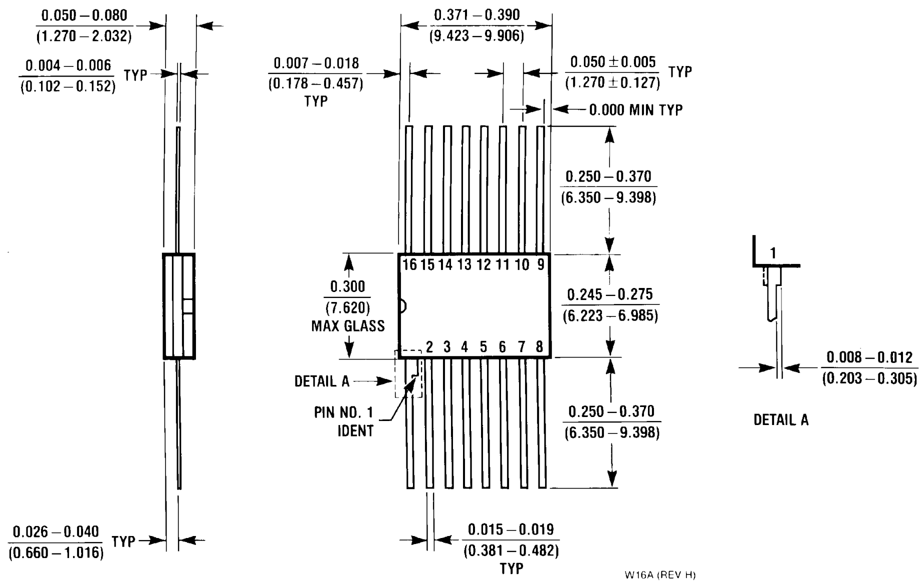
TL/F/10201–3

Physical Dimensions inches (millimeters)



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L34DMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 93L34FMQB
NS Package Number W16A

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March 1998

93L38
8-Bit Multiple Port Register

General Description

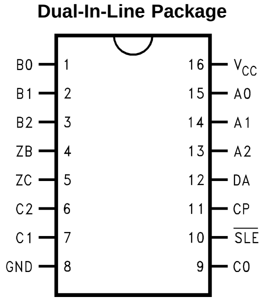
The 93L38 is an 8-bit multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously. The circuit uses TTL technology and is compatible with all TTL families.

Features

- Master/slave operation permitting simultaneous write/read without race problems
- Simultaneously read two bits and write one bit in any one of eight bit positions
- Readily expandable to allow for larger word sizes

Connection Diagram

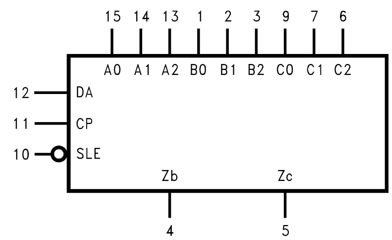
Dual-In-Line Package



DS010202-1

Order Number 93L38DMQB or 93L38FMQB
See Package Number J16A or W16A

Logic Symbol



DS010202-2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A2	Write Address Inputs
DA	Data Input
B0–B2	B Read Address Inputs
C0–C2	C Read Address Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{SLE}$	Slave Enable Input (Active LOW)
ZB	B Output
ZC	C Output

Absolute Maximum Ratings (Note 1)

Supply Voltage 7V
Input Voltage 5.5V
Operating Free Air Temperature Range
Military −55˚C to +125˚C
Storage Temperature Range −65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	93L38 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	µA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	˚C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_A to CP	30 22			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_A to CP	0 −4.0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to CP	0 0			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to CP	0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	40 30			ns

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature (unless othewise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			50	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			70	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with all outputs open and all input grounded.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25˚C

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay		68	ns
t_{PHL}	B_n or C_n or Z_n		95	
t_{PLH}	Propagation Delay		70	ns
t_{PHL}	D_A to Z_n		92	
t_{PLH}	Propagation Delay		65	ns
t_{PHL}	CP to Z_n		57	

Functional Description

The 93L38 8-bit multiple port register can be considered a 1-bit slice of eight high speed working registers. Data can be written into any one and read from any two of the eight locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous read/write activity from the same location. When the clock input (CP) is LOW data applied to the data input line (D_A) enters the selected master. This selection is accomplished by coding the three write input select lines (A0–A2) appropriately. Data is stored synchronously with the rising edge of the clock pulse.

The information for each of the two slaved (output) latches is selected by two sets of read address inputs (B0–B2 and C0–C2). The information enters the slave while the clock is HIGH and is stored while the clock is LOW. If Slave Enable is LOW ($\overline{SLE}$), the slave latches are continuously enabled. The signals are available on the output pins (Z_B and Z_C). The input bit selection and the two output bit selections can be accomplished independently or simultaneously. The data flows into the device, is demultiplexed according to the state of the write address lines and is clocked into the selected latch. The eight latches function as masters and store the input data. The two output latches are slaves and hold the data during the read operation. The state of each slave is determined by the state of the master selected by its associated set of read address inputs.

The method of parallel expansion is shown in *Figure 1*. One 93L38 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of n-bits each at one time, where n devices are connected in parallel.

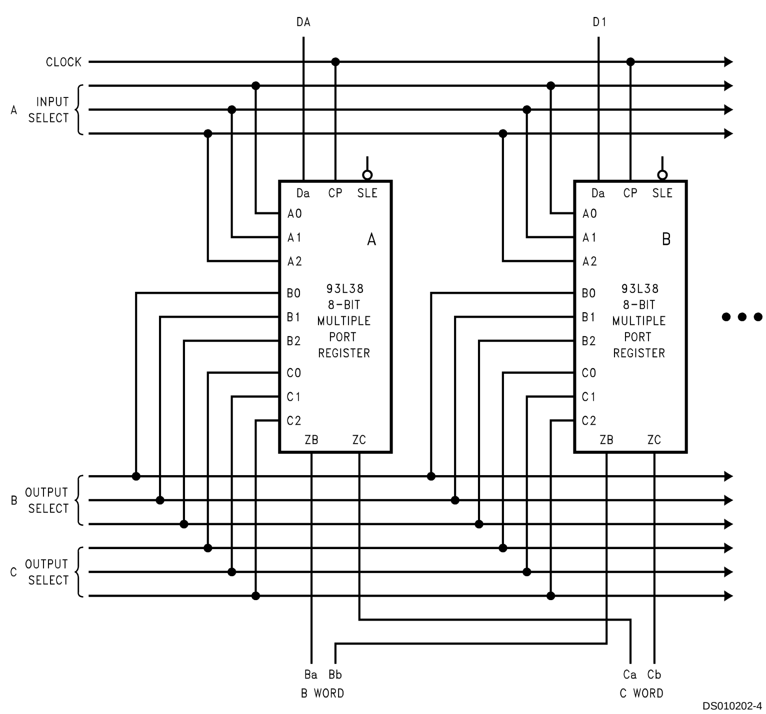
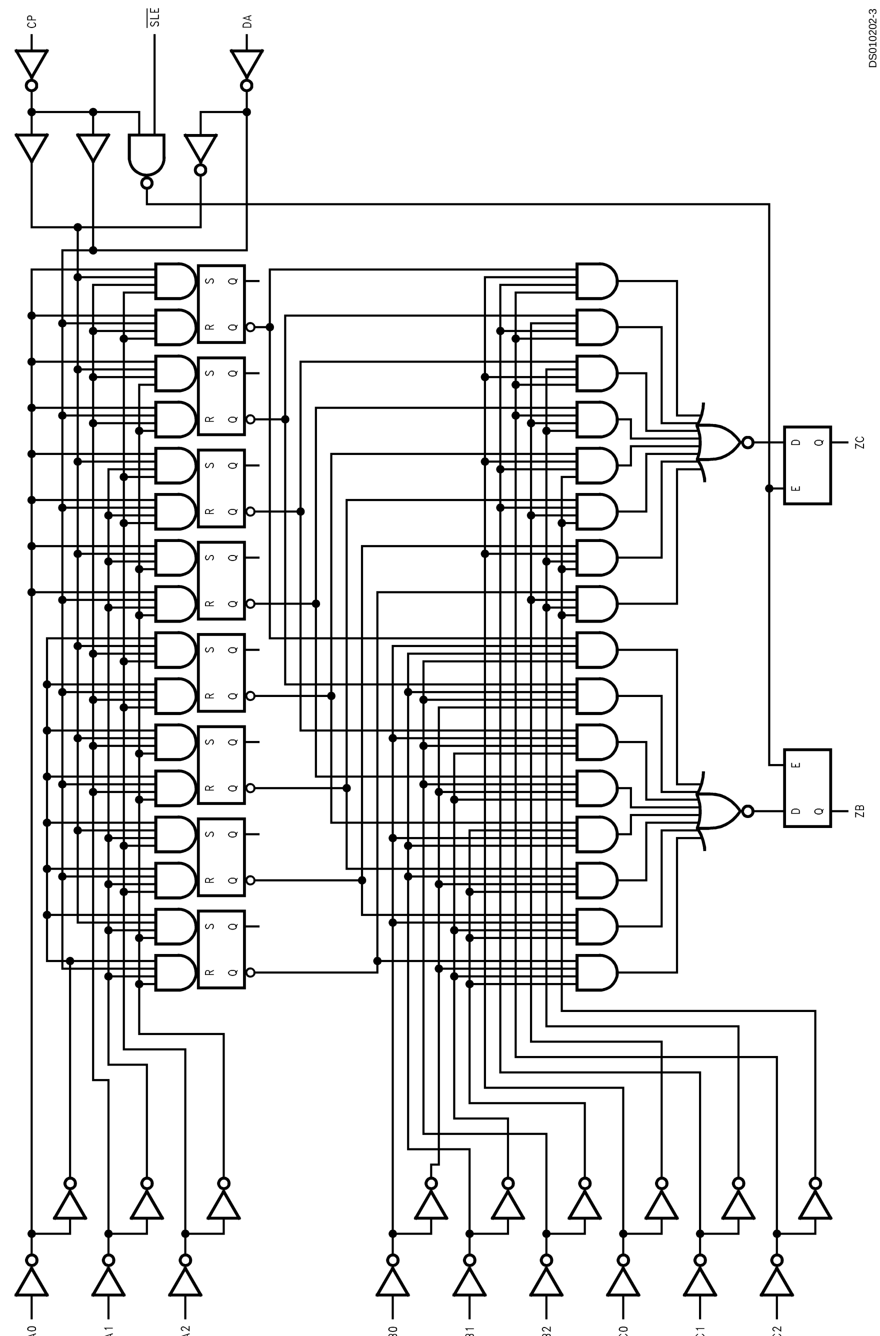
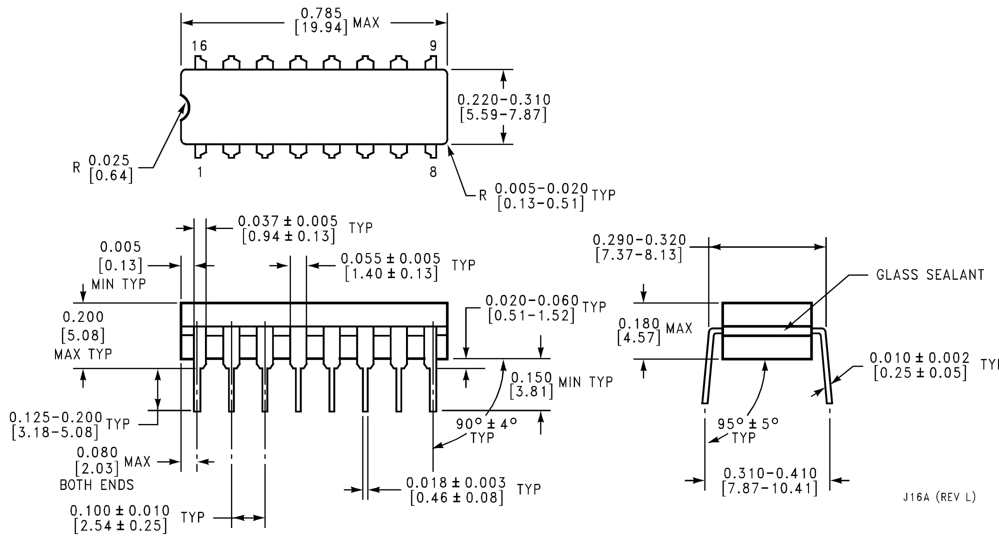


FIGURE 1. Parallel Expansion

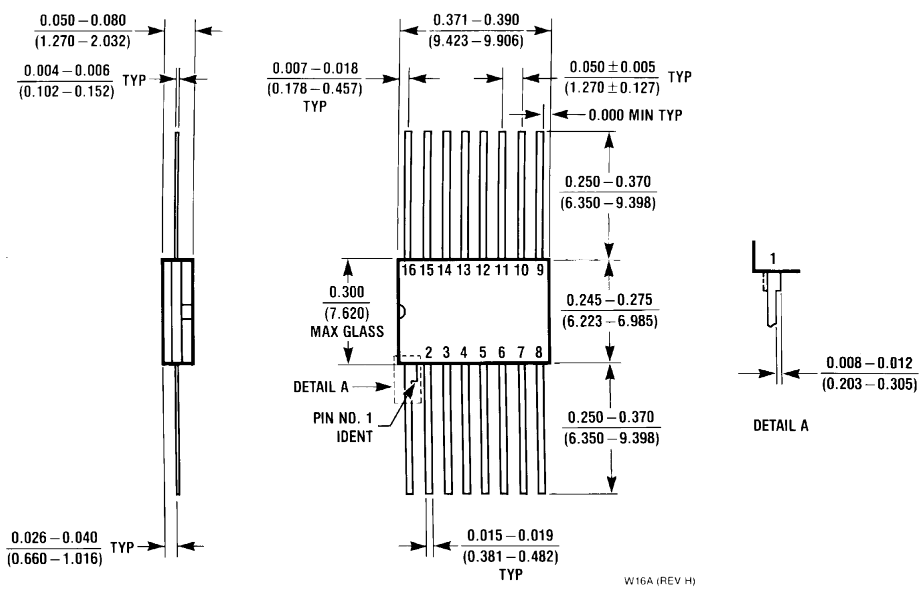
Logic Diagram



Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 93L38DMQB
Package Number J16A



16-Lead Ceramic Flat Package (W)
Order Number 93L38FMQB
Package Number W16A

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