Siliconix incorporated

DMCA1 DIE

N-Channel Lateral DMOS Quad FETs

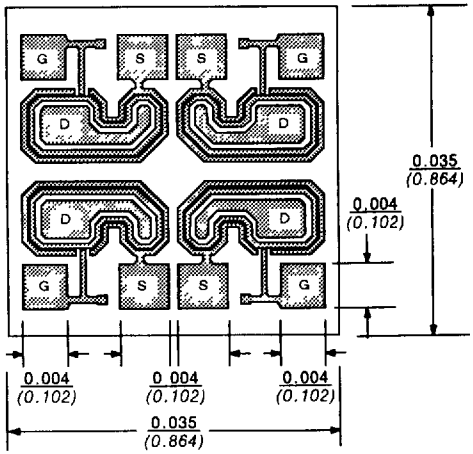
T-51-11

The Siliconix DMCA1 Die is a monolithic array of single-pole, single-throw analog switches designed for high-speed switching in audio, video and high-frequency applications in communications, instrumentation, and process control. Designed on the Siliconix DMOS process, the product is rated for analog signals of ± 10 V.

These bidirectional switches feature very low interelectrode capacitance and on-resistance to achieve low insertion loss, crosstalk, and feedthrough performance. The threshold voltage is 2 V maximum, simplifying driver requirements for low level signal applications.

For additional design information please consult the typical performance curves DMCA/B.

DMCA1CHP*
SD5000I SD5000N SD5001N SD5400CY SD5401CY
*Meets or exceeds specification for all part numbers listed below



Nominal Thickness
0.009 Inches
0.228 mm

DESIGNED FOR:

- Ultra-High Speed Switching
- High Gain Amplifiers

FEATURES

- < 1 ns Switching t_{ON}
  Ultra-Low Capacitance C_G < 3.5 pF
- g_{fs} (gain) > 10000 µmhos

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Source, Gate-Drain Voltage	V_{GS}, V_{GD}	30/–25	V
Drain-Substrate, Source-Substrate Voltage	V_{DB}, V_{SB}	25	
Drain-Source, Source-Drain Voltage	V_{DS}, V_{SD}	20	
Gate-Substrate Voltage	V_{GB}[1]	30/–0.3	
Drain Current	I_D	50	mA
Storage Temperature	T_{stg}	–65 to 150	°C

[1]This series features an internal zener diode for gate protection

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SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		30	20		V
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source OPEN		35	25		
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10$ µA, Drain OPEN		35	25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V, $V_{DS} = 20$ V		0.9			nA
Source-Drain Leakage	$I_{DS(OFF)}$	$V_{GD} = V_{BD} = -5$ V, $V_{DS} = 20$ V		1			
Gate Leakage	I_{GBS}	$V_{DB} = V_{GS} = 0$ V, $V_{GB} = 30$ V		10^{-5}			µA
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1$ µA, $V_{SB} = 0$ V		0.7	0.1	2.0	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V	58			Ω
			$V_{GS} = 10$ V	38			
			$V_{GS} = 15$ V	30			
			$V_{GS} = 20$ V	26			
Resistance Match		$I_D = 1$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V		1			
DYNAMIC							
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, $f = 1$ kHz		11			mS
Gate-Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, $f = 1$ MHz, $V_{GS} = V_{BS} = -15$ V		2.5			pF
Drain-Node Capacitance	$C_{(GD+DB)}$			1.1			
Source-Node Capacitance	$C_{(GS+SB)}$			3.7			
Reverse Transfer Capacitance	C_{rss}			0.2			
Crosstalk		f = 3 kHz, See Test Circuits in DMCA Performance Curves		-107			dB
SWITCHING							
Turn-On Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680$ Ω, $V_{IN} = 5$ V		0.5			ns
	t_r			0.6			
Turn-Off Time	$t_{d(OFF)}$			2			
	t_f			6			

NOTES:
a $T_A = 25°C$ unless otherwise noted.
b For design aid only, not subject to production testing.