Siliconix incorporated

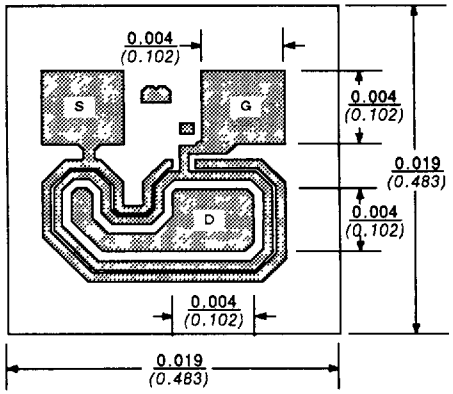
# DMCD1 DIE
# N-Channel Depletion-Mode Lateral DMOS FETs

T-35-25

The DMCD is a depletion-mode MOSFET which utilizes our lateral DMOS process to provide low capacitance, fast switching, and high operating frequency. This DMOS process effectively bridges the operating frequency gap between JFETs and costly gallium-arsenide devices.

| DMCD1CHP* |
|---|
| SD2100 |
| *Meets or exceeds specification for all part numbers listed below |

For additional design information please consult the typical performance curves DMCD.




Back of Chip is Substrate

Nominal Thickness
0.009 inches
0.228 mm

## DESIGNED FOR:

- High-Gain Amplification
- Analog Switching

## FEATURES

- High $g_{fs}$ > 10 mS (Typically)

5

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C Unless Otherwise Noted)

| PARAMETERS/TEST CONDITIONS | SYMBOL | LIMITS | UNITS |
|---|---|---|---|
| Gate-Drain Voltage | $V_{GD}$ | ±25 | V |
| Gate-Source Voltage | $V_{GS}$ | 25 | |
| Drain Current | $I_D$ | 50 | mA |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | -55 to 150 | °C |

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| SPECIFICATIONS[a] | | | | LIMITS | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | TEST CONDITIONS | | TYP[b] | MIN | MAX | UNIT |
| **STATIC** | | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DS}$ | $V_{GS} = V_{BS} = -5$ V, $I_D = 1$ µA | | 25 | 15 | | V |
| Gate Reverse Current | $I_{GSS}$ | $V_{GS} = \pm 25$ V, $V_{DS} = V_{BS} = 0$ V | | ±0.05 | | | nA |
| Saturation Drain Current | $I_{DSS}$ | $V_{DS} = 10$ V, $V_{GS} = V_{BS} = 0$ V | | 7 | 0.5 | 10 | mA |
| Gate Source Cutoff | $V_{GS(OFF)}$ | $V_{DS} = 10$ V, $I_D = 1$ µA, $V_{BS} = 0$ V | | -1.5 | | -2 | V |
| Gate-Source Voltage | $V_{GS}$ | $V_{DG} = 10$ V, $V_{BS} = 0$ V | $I_D = 5$ mA | -0.3 | | | |
| | | | $I_D = 10$ mA | 0 4 | | | |
| Drain-Source On-Resistance | $r_{DS(ON)}$ | $V_{BS} = 0$ V, $I_D = 100$ µA | $V_{GS} = 0$ V | 120 | | 200 | Ω |
| | | | $V_{GS} = 5$ V | 40 | | 50 | |
| **DYNAMIC** | | | | | | | |
| Forward Transconductance | $g_{fs}$ | $V_{DS} = 10$ V, $V_{GS} = V_{SB} = 0$ V | | 8000 | 1000 | | µS |
| Output Conductance | $g_{os}$ | f = 1 kHz | | 250 | | 500 | |
| Forward Transconductance | $g_{fs}$ | $V_{DG} = 10$ V, $V_{BS} = 0$ V | | 10000 | 7000 | | |
| Output Conductance | $g_{os}$ | $I_D = 10$ mA, f = 1 kHz | | 350 | | 500 | |
| Common-Source Input Capacitance | $C_{iss}$ | $V_{DS} = 10$ V, f = 1 MHz | | 5 | | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | $V_{GS} = V_{BS} = -5$ V | | 1 | | | |
| **SWITCHING** | | | | | | | |
| Turn-On Time | $t_{d(ON)}$ | $V_{DD} = 5$ V, $R_L = 680$ Ω | | 0.7 | | | ns |
| | $t_r$ | $V_{IN} = -4$ to $-2$ V | | 0.4 | | | |
| Turn-Off Time | $t_{d(OFF)}$ | | | 5 | | | |

NOTES:
a. $T_A = 25°C$ unless otherwise noted.
b. For design aid only, not subject to production testing.