

DN74LS112

Dual J-K Negative Edge-Triggered Flip-Flops (with Set and Reset)

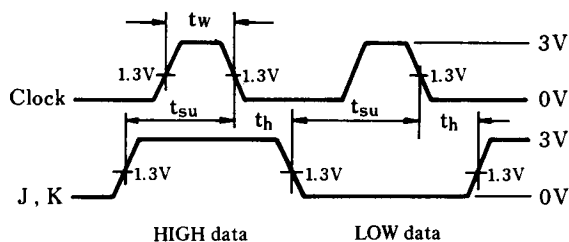
Description

DN74LS112 contains two negative-edge triggered J-K flip-flop circuits, each with independent clock-CP, J, K, and direct-coupled set and reset input terminals.

Features

- Negative-edge trigger
- Independent input and output terminals for each flip-flop
- Direct-coupled set and reset inputs
- Q and $\bar{Q}$ outputs
- Wide operating temperature range ($T_a = -20$ to $+75^\circ\text{C}$)

Timing definition



P-2



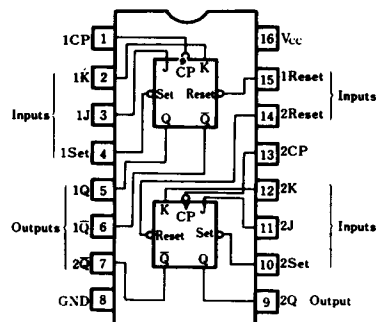
16-pin plastic DIL package

P-5



16-pin Panaflat package (SO-16D)

Pin configuration (top view)



Recommended operating conditions

Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			-400	μA
		I_{OL}			8	mA
Operating temperature range		T_{opr}	-20	25	75	$^\circ\text{C}$
Clock frequency		f_{clock}	0		30	MHz
Pulse width	Clock High	t_w	25			ns
	Set or Reset Low		25			ns
Set-up time	HIGH data	t_{su}	20 ↓			ns
	LOW data		20 ↓			ns
Hold time		t_h	5 ↓			ns

Notes 1. ↓: Indicates fall edge of standard clock pulse.

■ DC characteristics ($T_a = -20 \sim +75^\circ\text{C}$)

Parameter		Sym	Test conditions	Min	Typ*	Max	Unit
Input voltage		V_{IH}		2.0			V
		V_{IL}				0.8	V
Output voltage		V_{OH}	$V_{CC} = 4.75\text{V}$, $V_{IH} = 2\text{V}$ $V_{IL} = 0.8\text{V}$, $I_{OH} = -400\mu\text{A}$	2.7	3.4		V
		V_{OL1}	$V_{CC} = 4.75\text{V}$ $V_{IH} = 2\text{V}$		0.25	0.4	V
		V_{OL2}	$V_{IL} = 0.8\text{V}$		0.35	0.5	V
			$I_{OL} = 4\text{mA}$				
Input current	J-K	I_{IH}	$V_{CC} = 5.25\text{V}$ $V_I = 2.7\text{V}$			20	μA
	Reset					60	μA
	Set					60	μA
	Clock					80	μA
	J-K	I_{IL}	$V_{CC} = 5.25\text{V}$ $V_I = 0.4\text{V}$			-0.4	mA
	Reset					-0.8	mA
	Set					-0.8	mA
	Clock					-0.8	mA
	J-K	I_I	$V_{CC} = 5.25\text{V}$ $V_I = 7\text{V}$			0.1	mA
	Reset					0.3	mA
	Set					0.3	mA
	Clock					0.4	mA
Output short circuit current**		I_{OS}	$V_{CC} = 5.25\text{V}$, $V_O = 0\text{V}$	-15		-100	mA
Input clamp voltage		V_{IK}	$V_{CC} = 4.75\text{V}$, $I_I = -18\text{mA}$			-1.5	V
Supply current***		I_{CC}	$V_{CC} = 5.25\text{V}$		4.0	8.0	mA

* When constant at $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

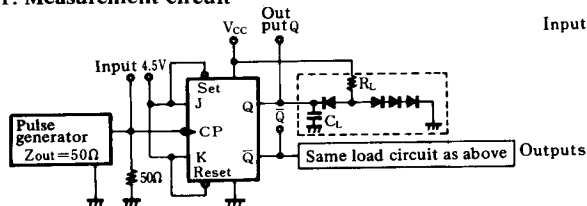
*** Measured with all outputs open, Q and $\bar{Q}$ outputs alternately HIGH, and clock inputs grounded.■ Switching characteristics ($V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	$f_{\max}$			$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$	30	45		MHz
Propagation delay time	t_{PLH}	Reset Set	Q, $\bar{Q}$			11	20	ns
	t_{PHL}	Clock				15	30	ns

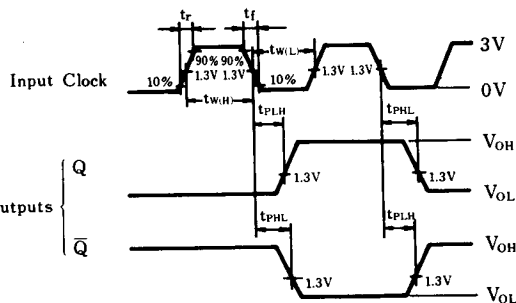
※ Switching parameter measurement information

[1] $f_{\max}$, t_{PLH} , t_{PHL} (Clock $\rightarrow$ Q, $\bar{Q}$)

1. Measurement circuit



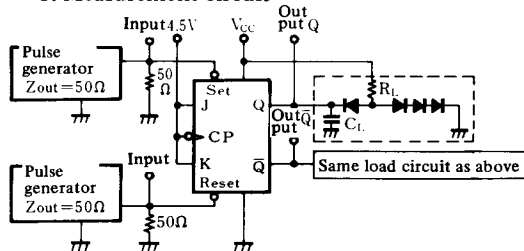
1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.



1. Clock input waveform: $t_r \leq 15\text{ns}$, $t_f \leq 6\text{ns}$, $\text{PRR} = 1\text{MHz}$, duty cycle 50%
2. When measuring $f_{\max}$, t_r and $t_f \leq 2.5\text{ns}$.

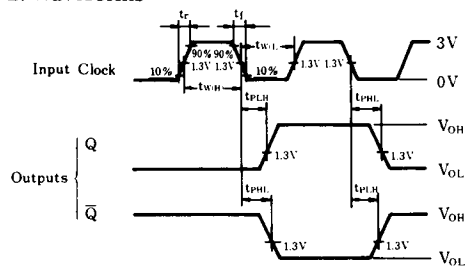
[2] t_{PLH} , t_{PHL} (Reset, Set $\rightarrow$ Q, $\bar{Q}$)

1. Measurement circuit



1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

2. Waveforms



Notes

1. Reset, Set Input waveform: $t_r \leq 15\text{ns}$, $t_f \leq 6\text{ns}$, $\text{PRR}=1\text{MHz}$

■ Truth tables

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	H	L	L	Q_0	$\bar{Q}_0$
H	H	H	H	L	H	L
H	H	H	L	H	L	H
H	H	H	H	H	Toggle	
H	H	H	X	X	Q_0	$\bar{Q}_0$

Notes

1. H: HIGH voltage level.
2. L: LOW voltage level.
3. $\downarrow$: Change from HIGH to LOW.
4. X: Either HIGH or LOW; doesn't matter.
5. Q_0 : Q level prior to determination of input condition shown in table.
6. $\bar{Q}_0$: $\bar{Q}$ level prior to determination of input condition shown in table.
7. Toggle: With $\downarrow$ change, outputs become complement of previous condition.
8. H*: When set and reset are LOW, Q and $\bar{Q}$ are HIGH; however, when set and reset simultaneously change to HIGH, requirements of Q and $\bar{Q}$ cannot be predicted.

■ Logic diagram (1/2)

