DN74LS241 N74LS241

Octal Buffers AND Line Drivers (with 3-state Outputs)

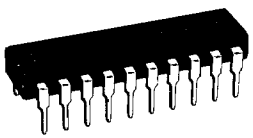
Description

DN74LS241 contains two buffer blocks, each with independent output-control inputs common to four circuits and 3-state non-inverted outputs.

Features

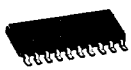
- Low input load coefficient (pnp input)
- Hysteresis (width = 400mV typical)
- Complementary output-control inputs ($\overline{G}_1$, and $\overline{G}_2$)
- High fan-out 3-state outputs (I_{OL} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range (Ta = −20 to +75°C)

P-3



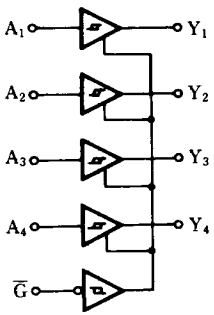
20-pin plastic DIL package

P-6

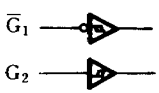


20-pin Panaflat package (SO-20D)

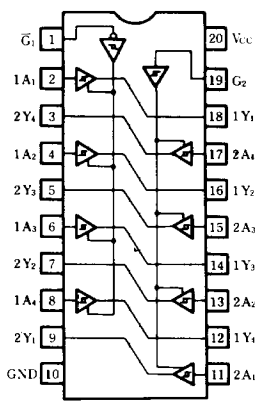
Logic diagram (1/2)



Note



Pin configuration (top view)



Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−15	mA
	I_{OL}			64	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Hysteresis		$V_T^+ - V_T^-$	$V_{CC} = 4.75V$		0.2	0.4		V
Output voltage		V_{OH1}	$V_{CC} = 4.75V$, $V_{IH} = 2V$ $V_{IL} = 0.5V$, $I_{OH} = -15mA$		2.0			V
		V_{OH2}	$V_{CC} = 4.75V$, $V_{IH} = 2V$ $V_{IL} = 0.8V$, $I_{OH} = -3mA$		2.4	3.4		V
		V_{OL1}	$V_{CC} = 4.75V$ $V_{IH} = 2V$ $V_{IL} = 0.8V$	$I_{OL} = 12mA$		0.25	0.4	V
		V_{OL2}		$I_{OL} = 24mA$		0.35	0.5	V
Output current		I_{OZH}	$V_{CC} = 4.75V$ $V_{IH} = 2V$ $V_{IL} = 0.8V$	$V_O = 2.7V$			20	μA
		I_{OZL}		$V_O = 0.4V$			−20	μA
Input current		I_{IH}	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		I_{IL}	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.2	mA
		I_I	$V_{CC} = 5.25V$, $V_I = 7V$				0.1	mA
Output short circuit current**		I_{OS}	$V_{CC} = 5.25V$, $V_I = 0V$		−15		−130	mA
Input clamp voltage		V_{IK}	$V_{CC} = 4.75V$, $I_I = -18mA$				−1.5	V
Supply current ***	All outputs HIGH	I_{CC}	$V_{CC} = 5.25V$			17	27	mA
	All outputs LOW					27	46	mA
	Disable output					32	54	mA

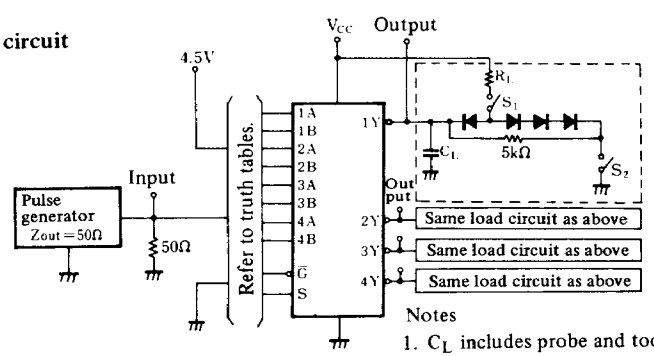
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.
*** I_{CC} is measured with all outputs open.

■ Switching characteristics ($V_{CC} = 5V$, $Ta = 25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L = 45pF$ $R_L = 667Ω$		12	14	ns
	t_{PHL}			12	18	ns
Output enable time	t_{ZL}			20	30	ns
	t_{ZH}			15	23	ns
Output disable time	t_{LZ}	$C_L = 5pF$ $R_L = 667Ω$		15	25	ns
	t_{HZ}			10	18	ns

※ Switching parameter measurement information

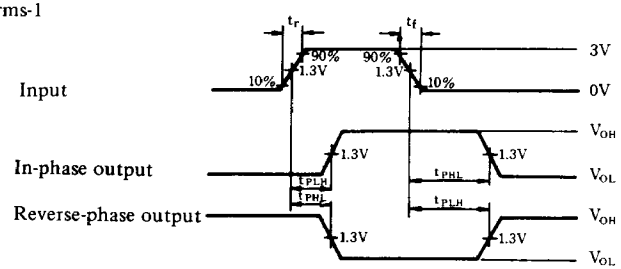
1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.
2. Diodes are all MA161 or equivalent.

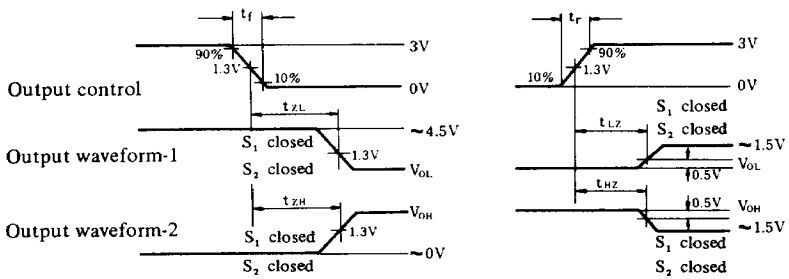
2. Waveforms

Waveforms-1



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.

Waveforms-2



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 6$ns, PRR = 1MHz, duty cycle = 50%.
2. Except when the output is disabled by the output control, output waveform-1 occurs as a result of internal conditions such as a LOW voltage level.
3. Except when the output is disabled by the output control, output waveform-2 occurs as a result of internal conditions such as a HIGH voltage level.
4. When measuring t_{PLH} and t_{PHL}, S_1 and S_2 are closed.

■ Truth tables

Inputs			Outputs
$\overline{G}_1$	G_2	A	Y
H	L	×	Z
L	H	H	H
L	H	L	L

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. Z: High impedance.