National Semiconductor

DP8342/NS32442
High-Speed 8-Bit Serial Transmitter/Encoder

General Description

The DP8342/NS32442 generates a complete encoding of parallel data for high speed serial transmission. It generates a five bit starting sequence, three bit code violation, followed by a syn bit and eight bit per byte of data plus a parity bit. A three-bit ending code signals the termination of the transmission. The DP8342/NS32442 adapts to generalized high speed serial data transmission as well as the coax lines at a maximum data rate of 3.5 MHz.

The DP8342/NS32442 and its complementary chip, the DP8343 (receiver/decoder) have been designed to provide maximum flexibility in system designs. The separation of the transmitter receiver functions provides convenient addition of more receivers at one end of a biphase line without the need of unused transmitters. This is specifically advantageous in control units where typical biphase data is multiplexed over many biphase lines and the number of receivers generally exceeds the number of transmitters.

Features

- Eight bits per data byte transmission
- Single-byte or multi-byte transmission
- Internal parity generation (even or odd)
- Internal crystal controlled oscillator used for the generation of all required chip timing frequencies
- Clock output directly drives receiver (DP8343) clock input
- Input data hold register
- Automatic clear status response feature
- Line drivers at data outputs provide easy interface to bi-phase coax line or general transmission media
- <2 ns driver output skew
- Bipolar technology provides TTL input/output compatibility
- Data outputs power up/down glitch free
- Internal power up clear and reset
- Single +5V power supply

Connection Diagram

Dual-In-Line Package

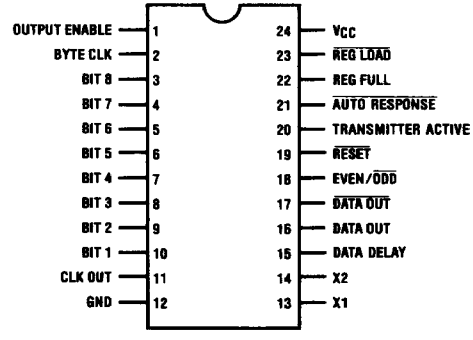

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FIGURE 1

Order Number DP8342J, NS32442J
or DP8342J, NS32442N
See NS Package Number J24A or N24A

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Block Diagram

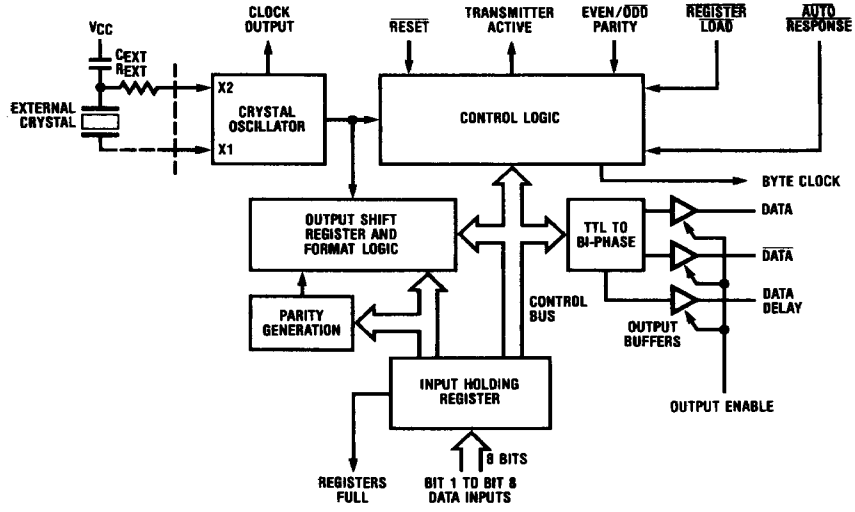

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FIGURE 2

Functional Description

Figure 2 is a block diagram of the DP8342/NS32442 Biphase Transmitter/Encoder. The transmitter/encoder contains a crystal oscillator whose input is a crystal with a frequency eight (8) times the data rate. A Clock Output is provided to drive the DP8342/NS32442 receiver/decoder Clock Input and other system components at the oscillator frequency. Additionally, the oscillator drives the control logic and output shift register/format logic blocks.

Data is parallel loaded from the system data bus to the transmitter/encoder's input holding register. This data is in turn loaded by the transmitter/encoder to its output shift register if this register was empty at the time of the load. During this load, message formatting and parity are generated. The formatted message is then shifted out at the bit rate frequency to the TTL to Biphase block which generates the proper data bit formatting. The data outputs, DATA, $\overline{\text{DATA}}$, and DATA DELAY provide for flexible interface to the transmission medium with little or no external components.

The control Logic block interfaces to all blocks to insure proper chip operation and sequencing. It controls the type of parity generation through the Even/$\overline{\text{Odd}}$ Parity input. An additional feature provided by the transmitter/encoder is the Reset and Output-TRI-STATE® capability. Another feature of the DP8342/NS32442 is the Byte Clock output which keeps track of the number of bytes transferred.

The transmitter/encoder is also capable of internal TT/AR ($\overline{\text{Transmission}}$ Turnaround/Auto Response). When the $\overline{\text{Auto-Response}}$ ($\overline{\text{AR}}$) input is forced to the logic "0" state, the transmitter/encoder responds with clean status (all zeros on data bits).

Operation of the transmitter/encoder is automatic. After the first data byte is loaded, the Transmitter Active output is set and the transmitter/encoder immediately formats the input data and serially shifts it out its data outputs. If the message is a mutli-byte message, the internal format logic will modify the message data format for multibyte as long as the next byte is loaded to the input holding format logic will modify the message data format for multibyte as long as the next byte is loaded to the input holding register before the last data bit of the previous data byte is transferred out of the internal output shift register. After all data is shifted out of the transmitter/encoder the Transmitter Active output will return to the inactive state.

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Detailed Pin/Functional Description

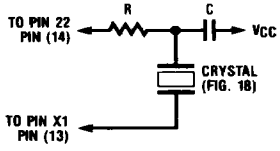
CRYSTAL INPUTS X1 AND X2

The oscillator is controlled by an external, parallel resonant crystal connected between the X1 and X2 pins. Normally, a fundamental mode crystal is used to determine the operating frequency of the oscillator; however, over-tone mode crystals may be used.

CRYSTAL SPECIFICATIONS (PARALLEL RESONANT)

Type	<20 MHz AT-cut or > 20 MHz BT-cut
Tolerance	0.005% at 25°C
Stability	0.01% from 0°C to +70°C
Resonance	Fundamental (Parallel)
Maximum Series Resistance	Dependent on Frequency (For 20 MHz, 50Ω)
Load Capacitance	15 pF

Connection Diagram



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Freq	R	C
10 MHz–20 MHz	500Ω	30 pF
>20 MHz	120Ω	15 pF

If the DP8342/NS32442 transmitter is clocked by a system clock (crystal oscillator not used), pin 13 (X1 input) should be clock directly using a Schottky series (74S) circuit. Pin 14 (X2 input) may be left open. The clocking frequency must be set at eight times the data bit rate. Maximum input frequency is 28 MHz.

CLOCK OUTPUT

The Clock Output is a buffered output derived directly from the crystal oscillator block and clocks at the oscillator frequency. It is designed to directly drive the DP8343 receiver/decoder Clock Input as well as other system components.

REGISTERS FULL

This output is used as a flag by the external operating system. A logic "1" (active state) on this output indicates that both the internal output shift register and the input holding register contain active data. No additional data should be loaded until this output returns to the logic "0" state (inactive state).

TRANSMITTER ACTIVE

This output will be in the logic "1" state while the transmitter/encoder is about to transmit or is in the process of transmitting data. Otherwise, it will assume the logic "0" state indicating no data presently in either the input holding or output shift registers.

$\overline{\text{REGISTER LOAD}}$

The Register Load input is used to load data from the Data Inputs to the input holding register. The loading function is level sensitive, the data present during the logic "0" state of this input is loaded, and the input data must be valid before the logic "0" to logic "1" transition. It is after this transition that the transmitter/encoder begins formatting of data for serial transmission.

$\overline{\text{AUTO RESPONSE}}$ (TT/AR)

This input provides for automatic clear data transmission (all bits in logic "0") without the need of loading all zero's. When a logic "0" is forced on this input the transmitter/encoder immediately responds with transmission of "clean status". When this input is in the logic "1" state the transmitter/encoder transmits data entered on the Data Inputs.

EVEN/$\overline{\text{ODD}}$ PARITY

This input sets the internal logic of the DP8342/NS32442 transmitter/encoder to generate either even or odd parity for the data byte in the bit 10 position. When this pin is in the logic "0" state odd parity is generated. In the logic "1" state even parity is generated. This feature is useful when the control unit is performing a loop back check and at the same time the controller wishes to verify proper data transmission with its receiver/decoder.

SERIAL OUTPUTS—DATA, $\overline{\text{DATA}}$, AND DATA DELAY

These three output pins provide for convenient application of data to the Bi-Phase transmission line. The Data outputs are a direct bit representation of the Biphase data while the Data Delay output provides the necessary increment to clearly define the four (4) DC levels of the pulse. The DATA and $\overline{\text{DATA}}$ outputs add flexibility to the DP8342/NS32442 transmitter/encoder for use in high speed differential line driving applications. The typical DATA to $\overline{\text{DATA}}$ skew is 2 ns.

$\overline{\text{RESET}}$

When a logic "0" is forced on this input, all outputs except Clock Output are latched low.

OUTPUT ENABLE

When a logic "0" is forced on this input the three serial data outputs are in the high impedence state.

BYTE CLOCK

This pin registers a pulse at the end of each byte transmission. The number of pulses registered corresponds to the number of bytes transmitted.

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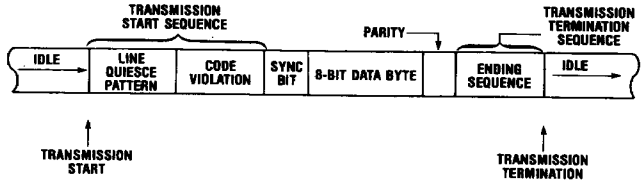
Message Format

Single Byte Transmission



Multi-Byte Transmission

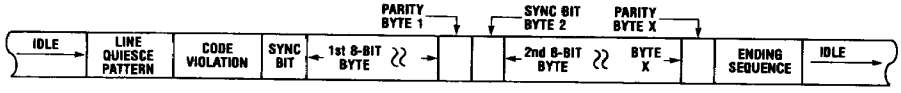


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FIGURE 3

Functional Timing Waveforms

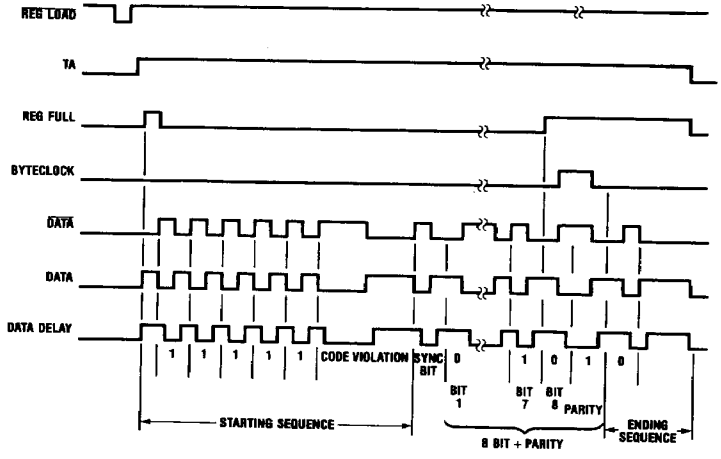

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FIGURE 4. Overall Timing Waveforms for Single Byte

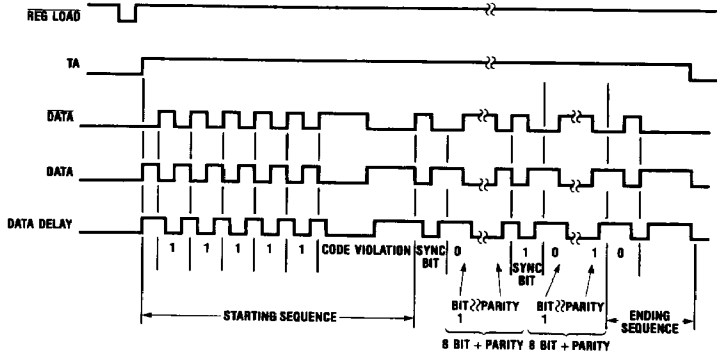

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FIGURE 5. Overall Timing Waveforms for Multi-Byte

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Output Voltage	5.25V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Maximum Power Dissipation* at 25°C

Cavity Package	2237 mW
Dual-In-Line package	2500 mW

*Derate cavity package 14.9 mW/°C above 25°C; derate dual in line package 20 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})	4.75	5.25	V
Ambient Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage (All Inputs Except X1 and X2)		V_{CC} = 5V	2.0			V
V_{IL}	Logic "0" Input Voltage (All Inputs Except X1 and X2)		V_{CC} = 5V			0.8	V
V_{CLAMP}	Input Clamp Voltage (All Inputs Except X1 and X2)		I_{IN} = −12 mA		−0.8	−1.2	V
I_{IH}	Logic "1" Input Current	Register Load Input	V_{CC} = 5.25V, V_{IN} = 5.25V		0.3	120	μA
		All Others Except X1 and X2			0.1	40	μA
I_{IL}	Logic "0" Input Current	Register Load Input	V_{CC} = 5.25V, V_{IN} = 0.5V		−15	−300	μA
		All Inputs Except X1 and X2			−5	−100	μA
V_{OH1}	Logic "1" All Outputs Except CLK OUT, DATA, $\overline{DATA}$, and DATA DELAY		I_{OH} = −100 μA, V_{CC} = 4.75V	3.2	3.9		V
			I_{OH} = −1 mA	2.5	3.4		V
V_{OH2}	Logic "1" for CLK OUT, DATA, $\overline{DATA}$, and DATA DELAY Outputs		V_{CC} = 4.75V, I_{OH} = −10 mA	2.6	3.0		V
V_{OL1}	Logic "0" All Outputs Except CLK OUT, DATA, $\overline{DATA}$, and DATA DELAY		V_{CC} = 4.75V, I_{OL} = 5 mA		0.35	0.5	V
V_{OL2}	Logic "0" for CLK OUT, DATA $\overline{DATA}$, and DATA DELAY Outputs		V_{CC} = 4.75V, I_{OL} = 20 mA		0.4	0.6	V
I_{OS1}	Output Short Circuit Current for All Except CLK OUT, DATA, $\overline{DATA}$, and DATA DELAY Outputs		(Note 5) V_{OUT} = 0V	−10	−30	−100	mA
I_{OS2}	Output Short Circuit Current DATA, $\overline{DATA}$, and DATA DELAY Outputs		(Note 5) V_{OUT} = 0V	−50	−140	−350	mA
I_{OS3}	Output Short Circuit Current for CLK OUT		(Note 5) V_{OUT} = 0V	−30	−90	−200	mA
I_{CC}	Power Supply Current		V_{CC} = 5.25V		170	250	mA

Timing Characteristics V_{CC} = 5V ±5%, T_A = 0°C to 70°C, Oscillator Frequency = 28 MHz (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	$\overline{REG\ LOAD}$ to Transmitter Active (TA) Positive Edge	Load Circuit 1 *Figure 6*		60	90	ns
t_{pd2}	$\overline{REG\ LOAD}$ to Register Full; Positive Edge	Load Circuit 1 *Figure 6*		45	75	ns
t_{pd3}	TA to Register Full; Negative Edge	Load Circuit 1 *Figure 6*		40	70	ns
t_{pd4}	Positive Edge of $\overline{REG\ LOAD}$ to Positive Edge of DATA	Load Circuit 2 *Figure 9*		50	80	ns
t_{pd5}	$\overline{REG\ LOAD}$ to $\overline{DATA}$; Positive Edge	Load Circuit 2 *Figure 9*		280	380	ns
t_{pd6}	$\overline{REG\ LOAD}$ to DATA DELAY; Positive Edge	Load Circuit 2 *Figure 9*		150	240	ns

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Timing Characteristics (Continued)

V_{CC} = 5V ±5%, T_A = 0°C to 70°C, Oscillator Frequency = 28 MHz (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd7}	Positive Edge of $\overline{DATA}$ to Negative Edge of DATA DELAY	Load Circuit 2 *Figure 9*		70	85	ns
t_{pd8}	Positive Edge of DATA DELAY to Negative Edge of $\overline{DATA}$	Load Circuit 2 *Figure 9*		80	95	ns
t_{pd9}, t_{pd10}	Skew between DATA and $\overline{DATA}$	Load Circuit 2 *Figure 9*		2	6	ns
t_{pd11}	Negative Edge of $\overline{Auto\ Response}$ ($\overline{AR}$) to Positive Edge of TA	Load Circuit 1 *Figure 10*		70	100	ns
t_{pd12}	Maximum Time Delay to Load Second Byte after Positive Edge of REG FULL	Load Circuit 1 *Figure 8*, (Note 7)			4 × T − 50	ns
t_{pd13}	X1 to CLK OUT; Positive Edge	Load Circuit 2 *Figure 11*		21	30	ns
t_{pd14}	X1 to CLK OUT; Negative Edge	Load Circuit 2 *Figure 11*		23	33	ns
t_{pd15}	Negative Edge of $\overline{AR}$ to Positive Edge of REG FULL	Load Circuit 1 *Figure 10*		45	75	ns
t_{pd16}	Skew between TA and REG FULL during $\overline{Auto\ Response}$	Load Circuit 1 *Figure 10*		50	80	ns
t_{pd17}	$\overline{REG\ LOAD}$ to REG FULL; Positive Edge for Second Byte	Load Circuit 1 *Figure 7*		45	75	ns
t_{pd18}	REG FULL to BYTE CLK; Negative Edge	Load Circuit 1 *Figure 7*		60	90	ns
t_{pd19}	REG FULL to BYTE CLK; Positive Edge	Load Circuit 1 *Figure 7*		145	180	ns
t_{ZH}	Output Enable to DATA, $\overline{DATA}$, or DATA DELAY outputs: HiZ to High	CL = 50 pF *Figures 16, 17*		25	45	ns
t_{ZL}	Output Enable to DATA, $\overline{DATA}$, or DATA DELAY Outputs; HiZ to High	CL = 50 pF *Figures 16, 17*		15	30	ns
t_{HZ}	Output Enable to DATA, $\overline{DATA}$, or DATA DELAY Outputs; High to HiZ	CL = 15 pF *Figures 16, 17*		65	100	ns
t_{LZ}	Output Enable to DATA, $\overline{DATA}$, or DATA DELAY Outputs; Low to HiZ	CL = 15 pF *Figures 16, 17*		45	70	ns
t_{pw1}	$\overline{REG\ LOAD}$ Pulse Width	*Figure 12*	40			ns
t_{pw2}	First REG FULL Pulse Width (Note 6)	Load Circuit 1 *Figure 7*, (Note 7)		8 × T + 60	8 × T + 100	ns
t_{pw3}	REG FULL Pulse Width Prior to Ending Sequence (Note 6)	Load Circuit 1 *Figure 7*		5 × B		ns
t_{pw4}	Pulse Width for $\overline{Auto\ Response}$	*Figure 10*	40			ns
t_{pu5}	Pulse Width for BYTE CLK	Load Circuit 1 *Figure 7*, (Note 7)		8 × T + 30	8 × T + 80	ns
t_s	Data Setup Time prior to $\overline{REG\ LOAD}$ Positive Edge; Hold Time = 0 ns	*Figure 12*		15	23	ns
t_{r1}	Rise Time for DATA, $\overline{DATA}$, and DATA DELAY Output Waveform	Load Circuit 2 *Figure 13*		7	13	ns
t_{f1}	Fall Time for DATA, $\overline{DATA}$, and DATA DELAY Output Waveform	Load Circuit 2 *Figure 13*		5	11	ns
t_{r2}	Rise Time for TA and REG FULL	Load Circuit 1 *Figure 14*		20	30	ns
t_{f2}	Fall Time for TA and REG FULL	Load Circuit 1 *Figure 14*		15	25	ns

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Timing Characteristics (Continued)

V_{CC} = 5V ±5%, T_A = 0°C to 70°C, Oscillator Frequency = 28 MHz (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{MAX}	Data Rate Frequency (Clock Input must be 8× this Frequency)		DC		3.5	Mbits/s
C_{IN}	Input Capacitance—Any Input	(Note 4)		5	15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute basis.

Note 4: Input capacitance is guaranteed by periodic testing. f_{TEST} = 10 kHz at 300 mV, T_A = 25°C.

Note 5: Only one output should be shorted at a time.

Note 6: T = 1/(Oscillator Frequency). Unit for T should be in ns. B = 8T.

Note 7: Oscillator Frequency Dependent.

Timing Waveforms (Continued)

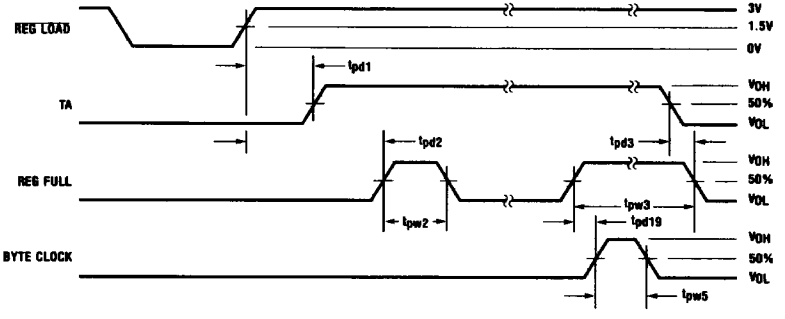

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FIGURE 6. Single Byte Transfer

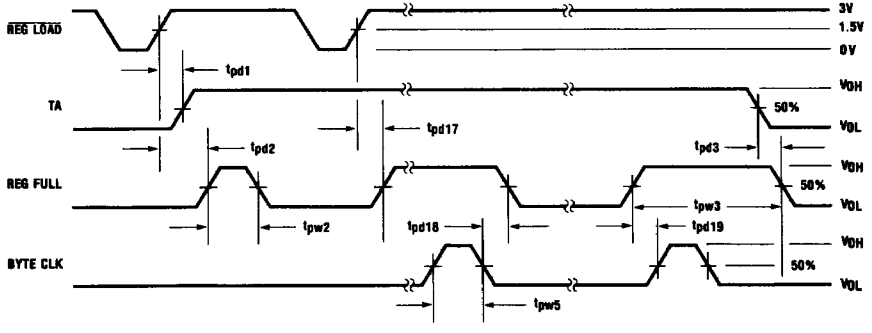

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FIGURE 7. Two-Byte Transfer

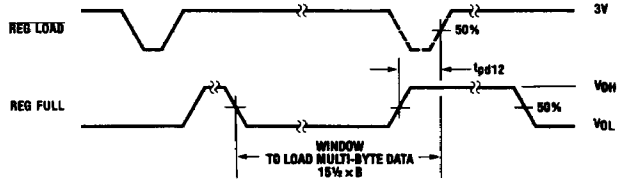

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FIGURE 8. Maximum Window to Load Multi-Byte Data

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Functional Timing Waveforms (Continued)

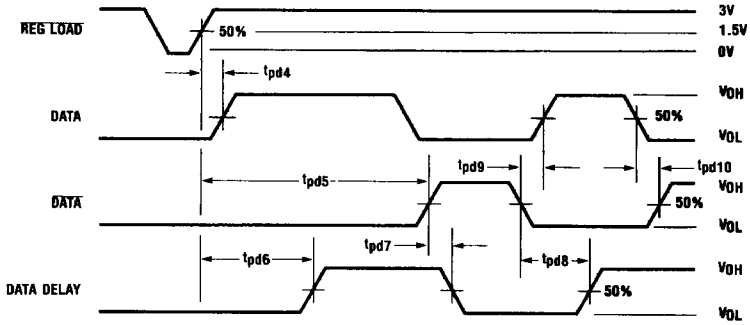

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FIGURE 9. Three Serial Outputs

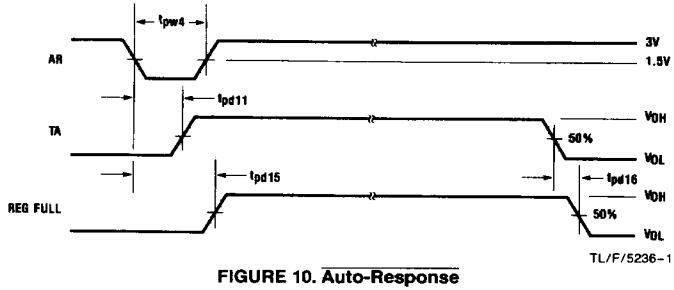

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FIGURE 10. Auto-Response

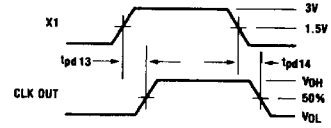

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FIGURE 11. Clock Pulse

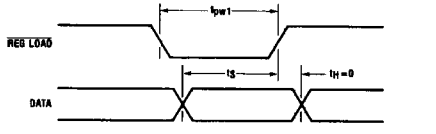

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FIGURE 12. REG LOAD

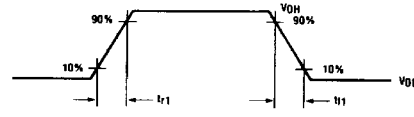

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FIGURE 13. Output Waveform for DATA, DATA, DATA DELAY (Load Circuit 2)

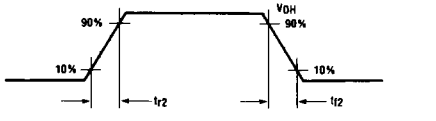

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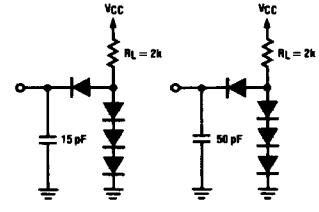
FIGURE 14. Rise and Fall Time Measurement for TA and REG FULL



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Load Circuit 1 **Load Circuit 2**

FIGURE 15. Test Load Circuits

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Timing Waveforms (Continued)

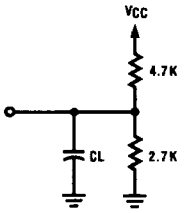

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FIGURE 16. Load Circuit for Output TRI-STATE Test

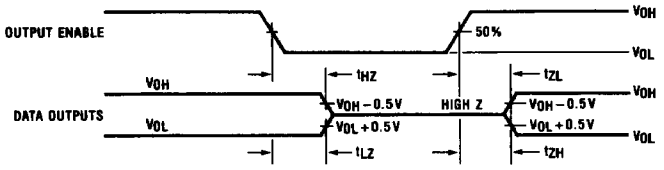

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FIGURE 17. TRI-STATE Test

Typical Applications

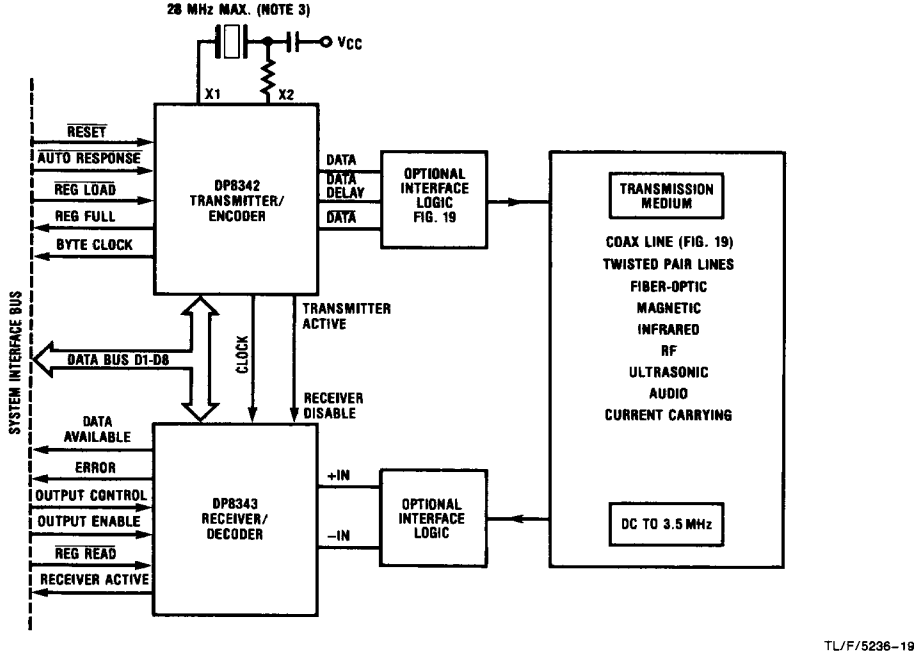

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FIGURE 18

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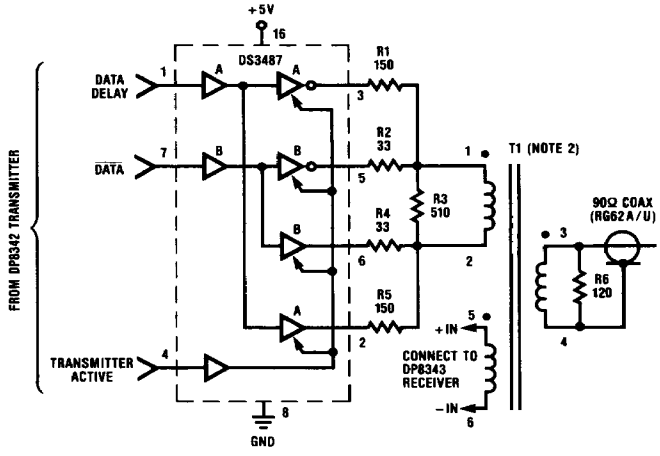
Typical Applications (Continued)

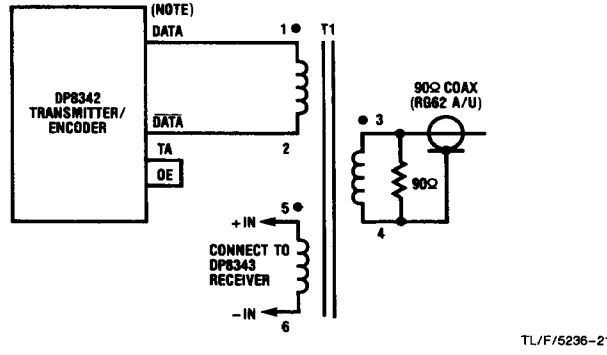


Note 1: Resistance values are in Ω, ±5%, ¼W.

Note 2: T1 is a 1:1:1 pulse transformer, L = 500 μH for 18 MHz to 28 MHz system clock. Pulse Engineering Part No. 5762; Technitrol Part No. 11LHA, Valor Electronics Part No. CT1501, or equivalent transformer.

Note 3: Crystal manufacturer Midland Ross Corp. NEL Unit Part No. NE-18A at 28 MHz.

FIGURE 19. Interface Logic for a Coax Transmission Line



Note: Data rates up to 3.5 Mbits/s at 5000' still apply.

FIGURE 20. Direct Interface for a Coax Transmission Line (Non-IBM Voltage Levels)

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