National Semiconductor

Dynamic Memory Support
PRELIMINARY

DP84332 Dynamic RAM Controller Interface Circuit for the 8086 and 8088 CPUs

General Description

The DP84332 dynamic RAM controller interface is a Programmable Array Logic* (PAL) device which allows for easy interface between the DP8408 dynamic RAM controller and the 8086 and 8088 microprocessors. No wait states are required for memory access. Memory refreshing may be hidden (no wait states) or forced (up to three wait states).

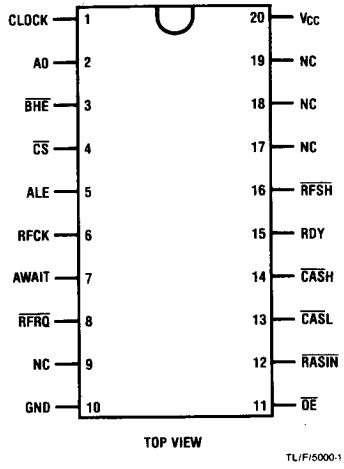
The DP84332 supplies all the control signals needed to perform memory read, write, and refresh. Logic is also included to insert a wait state when using slow memory.

Features

- Low parts count controller for the DP8408/DP8409
- Works with 8086 systems configured in min or max mode
- Performs hidden refresh using the DP8408 dynamic RAM controller
- Compatible with both the 8086 and 8088 microprocessors
- Capable of working at all CPU clock frequencies up to 8 MHz
- Standard National Semiconductor PAL part (DMPAL16R8)
- PAL logic equations can be modified by the user for his specific application and programmed into any of the PALs in the National Semiconductor family, including the new high speed PALs.

Connection Diagram

Dual-In-Line Package

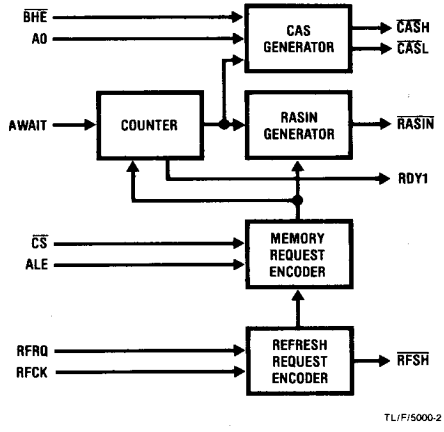


TOP VIEW

TL/F/5000-1

Order Number DP84322N-3
NS Package Number N20A

Block Diagram



TL/F/5000-2

*PAL is a registered trademark of Monolithic Memories, Inc.

Recommended Operating Conditions (Commercial)

	Min	Typ	Max	Units
V_{CC}, Supply Voltage	4.75	5.00	5.25	V
I_{OH}, High Level Output Current			−3.2	mA
I_{OL}, Low Level Output Current			24 (Note 2)	mA
T_A, Operating Free Air Temperature	0		75	°C

Electrical Characteristics over recommended operating temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max			0.5	V
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 2.4V, V_{IL} = 0.8V			100	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 0.4V, V_{IL} = 0.8V			−100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−250	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max		150	225 (Note 1)	mA

DP84332-3 Switching Characteristics over recommended ranges of temperature and V_{CC}

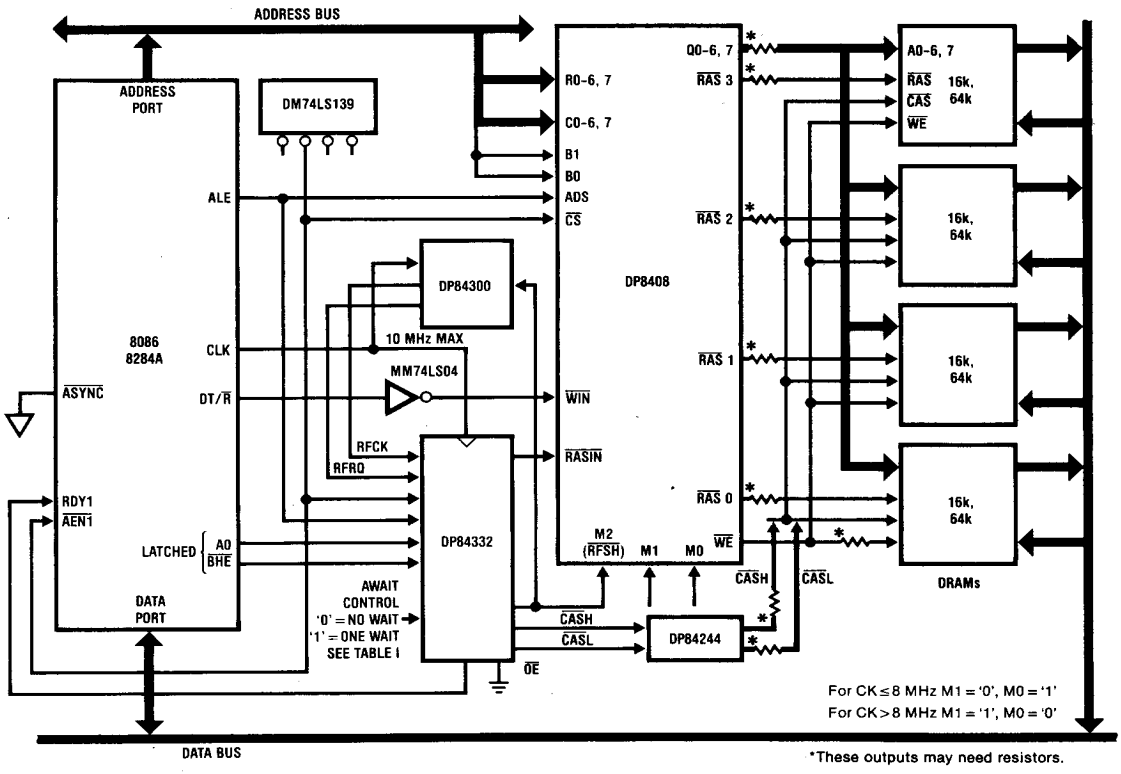
Symbol	Parameter		Conditions R_L = 667Ω	Commercial T_A = 0°C to +75°C V_{CC} = 5.0V ± 5%			Units
				Min	Typ	Max	
t_{PD}	Clock to Output		C_L = 45 pF		15	25	ns
t_{PZX}	Pin 11 to Output Enable		C_L = 45 pF		15	25	ns
t_{PXZ}	Pin 11 to Output Disable		C_L = 5 pF		15	25	ns
t_W	Width of Clock	High		25			ns
		Low		25			ns
t_{su}	Set-Up Time			40			ns
t_H	Hold Time			0	−15		ns

Note 1: I_{CC} = max at minimum temperature.

Note 2: One output at a time; otherwise 16 mA.

System Block Diagram

Interfacing the DP8408 to an 8086 System



Mnemonic Description

INPUT SIGNALS

CLOCK	The CLOCK signal determines the timing of the outputs and should be connected directly to the 8086 clock.
A0, $\overline{BHE}$	These inputs come from the 8086 CPU. They must remain stable during the memory cycle for proper operation of the $\overline{CAS}$ outputs.
$\overline{CE}$	Chip enable. This input is used to select the memory and enable the hidden refresh logic.
ALE	Address latch enable. This input is used to indicate the beginning of a memory cycle.
RFCK	Refresh clock. The period of this input determines the refresh interval. The duty cycle of this clock will determine the length of time that the circuit will attempt a hidden refresh.
AWAIT	When connected to V_{CC}, the DP84332 will insert an extra wait state in selected memory cycles.
$\overline{RFRQ}$	Refresh request. This input requests the DP84332 to perform a refresh. The state of the RFCK input will determine what type of refresh will be performed.

OUTPUT SIGNALS

$\overline{RASIN}$	This output provides a memory cycle start signal to the DP8408, and provides $\overline{RAS}$ timing during refresh.
$\overline{CASH}$, $\overline{CASL}$	These signals are the separate $\overline{CAS}$s needed for byte writing. Their presence is controlled by $\overline{BHE}$ and A0 respectively.
RDY	This output is used to insert a wait state into the 8086 memory cycles when selected and during a forced refresh cycle where the 8086 attempts to access the memory. The 8284A clock circuit should be configured so that ASYNC is enabled.
RFSH	This output controls the mode of the DP8408 dynamic RAM controller. When low, it switches the DP8408 into an all $\overline{RAS}$ refresh mode. This signal is also used to reset the refresh request logic.

Functional Description

A memory cycle starts when chip select ($\overline{CS}$) and address latch enable (ALE) are true. RASIN is supplied from the DP84332 to the DP8408 dynamic RAM controller, which then supplies a RAS signal to the selected dynamic RAM bank. After the necessary row address hold time, the DP8408 switches the address outputs to the column address. The DP84332 then supplies the required $\overline{CAS}$ signals ($\overline{CASH}$, $\overline{CASL}$) to the RAM. For byte operations, only one $\overline{CAS}$ will be activated. To differentiate between a read and a write, the DT/$\overline{R}$ signal from the CPU is inverted and supplied by the DP8408 to the memory array.

A refresh cycle is started by one of two conditions. One is when a refresh is requested (RFRQ is true), refresh clock (RFCK) is high, and a non-selected memory cycle is started (CE is not true, ALE is high). This is called hidden refresh because it is transparent to the CPU. In this case, the address supplied to the memories comes from the refresh counter in the DP8408, and no $\overline{CAS}$ signals are generated from the DP84332. The second form of refresh occurs when a refresh is requested, refresh clock is low, and there is no memory cycle in progress. This is called forced refresh, because the CPU will be forced to wait during the next memory cycle to allow for the refresh to be performed. In this case, a refresh is performed as before, but any attempt to access memory is delayed by wait states until after the refresh is finished. In either case, the refresh request is cleared by the refresh line ($\overline{RFSH}$) which also goes to the DP8408.

In a standard memory cycle, the access can be slowed down by one clock cycle to accommodate slower memories. This extra wait state will not appear during the hidden refresh cycle, so faster devices on the CPU bus will not be affected.

With higher speed systems, memory speed requirements will affect the performance of the system. Table I shows memory speed requirements at three different CPU clock speeds.

TABLE I. MEMORY SPEED REQUIREMENTS

CPU Clock Frequency	t_{CAC}		t_{RAH}
	No Wait States	1 Wait State	
8 MHz	≤105 ns	≤223 ns	≤30 ns
5 MHz	≤170 ns	≤370 ns	≤30 ns

t_{CAC} = access time from $\overline{CAS}$ including delay through buffers (DP84244)
t_{RAH} = row address hold time from $\overline{RAS}$

System Description

For memory operation, the DP84332 can be directly connected between the control signals from the CPU chip set and the DP8408 dynamic RAM controller. Each $\overline{CAS}$ output of the DP84332 is capable of driving eight memory devices. If additional drive is required, a DP84244 buffer can be used to increase the fanout to the full capabilities of the DP8408 (eight memories per output of the DP84244).

The 84332 is a standard National Semiconductor PAL part (DMPAL16R8). The user can modify the PAL equations to support his particular application. The 84332 logic equations, function table (functional test) and logic diagram can be seen at the end of this data sheet.

Refresh Request Logic

To generate the refresh request for the DP84332, external circuitry is required. *Figure 1* shows how this can be implemented, using standard SSI and MSI logic. A DM74LS393 counter is used to time the period between refresh cycles, while the DM74LS74 flip-flop is used to record the need of a new refresh. A better solution is to use the 24-pin DP84300 programmable refresh timer, as shown in *Figure 2*. This part allows a maximum amount of time for a hidden refresh to occur before lowering the refresh clock output, and implements the refresh request logic.

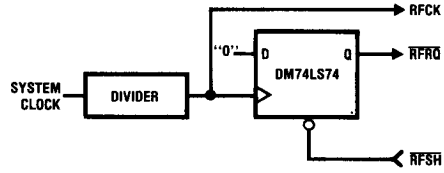


FIGURE 1. Using a Flip-Flop and a Counter for Refresh Request Logic

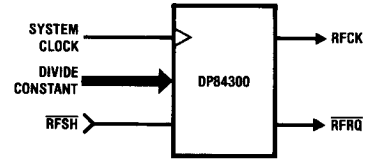
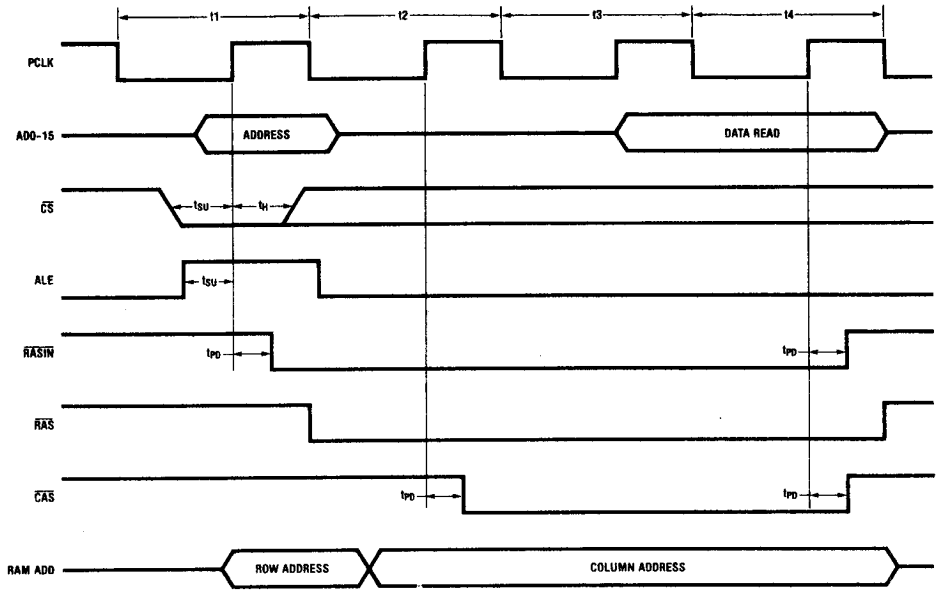


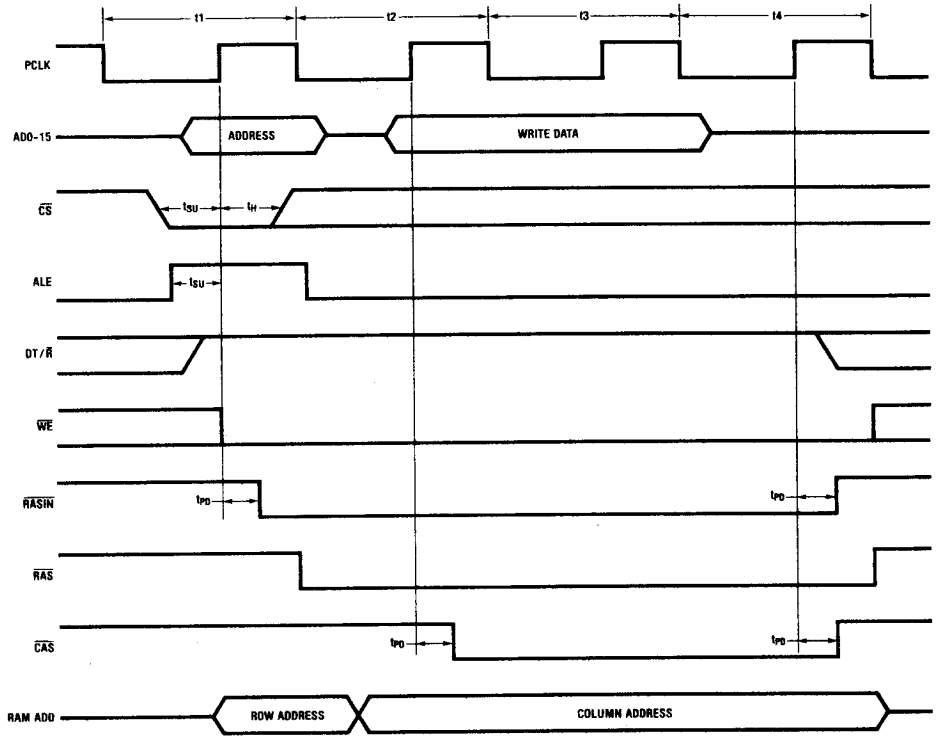
FIGURE 2. Using the DP84300 Refresh Counter for Refresh Request Logic

Timing Diagrams

Read Timing

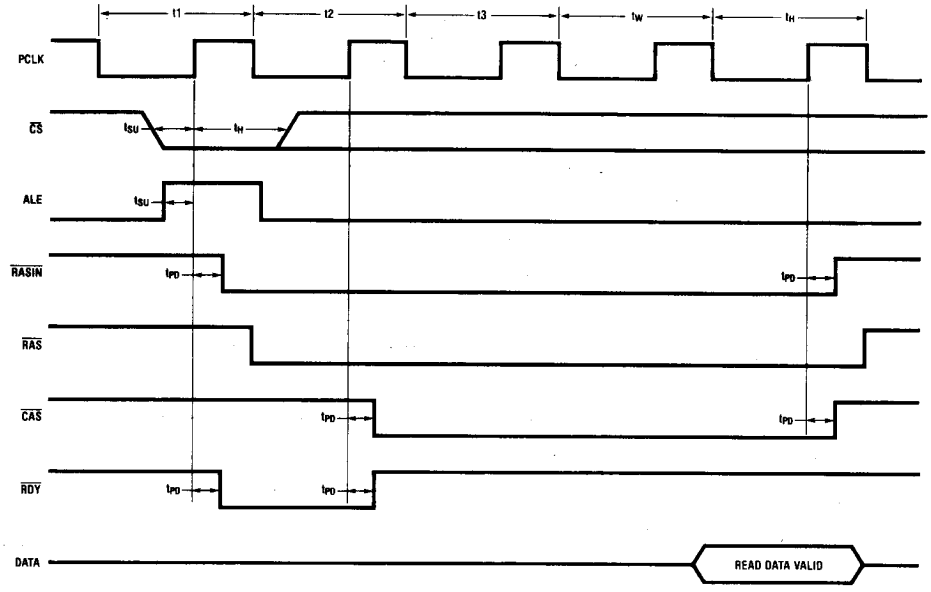


Write Timing

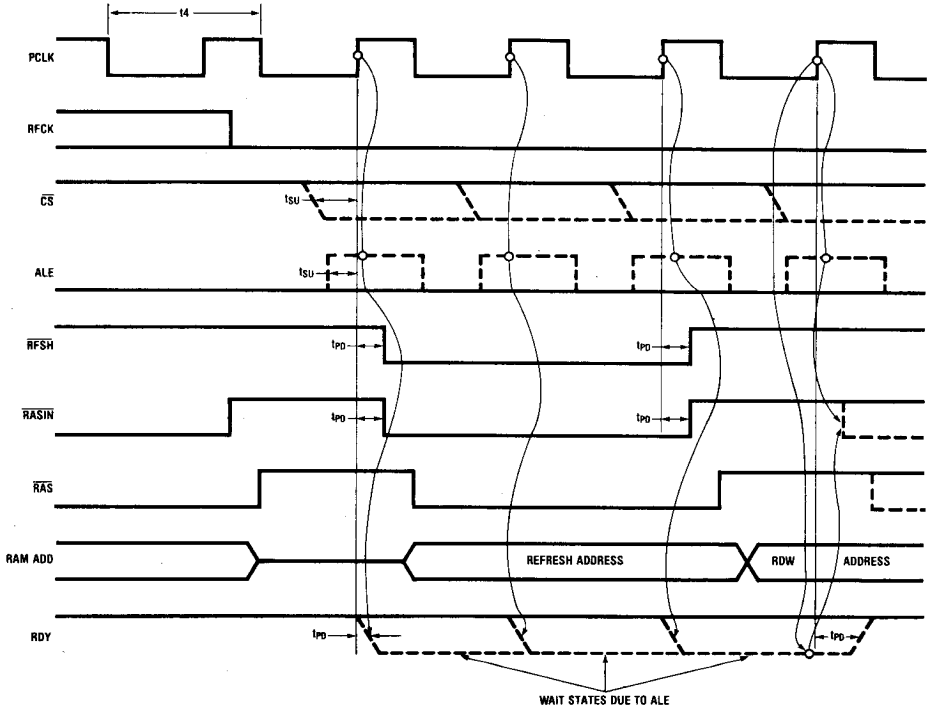


Timing Diagrams (Continued)

Memory Cycle with 1 Wait State

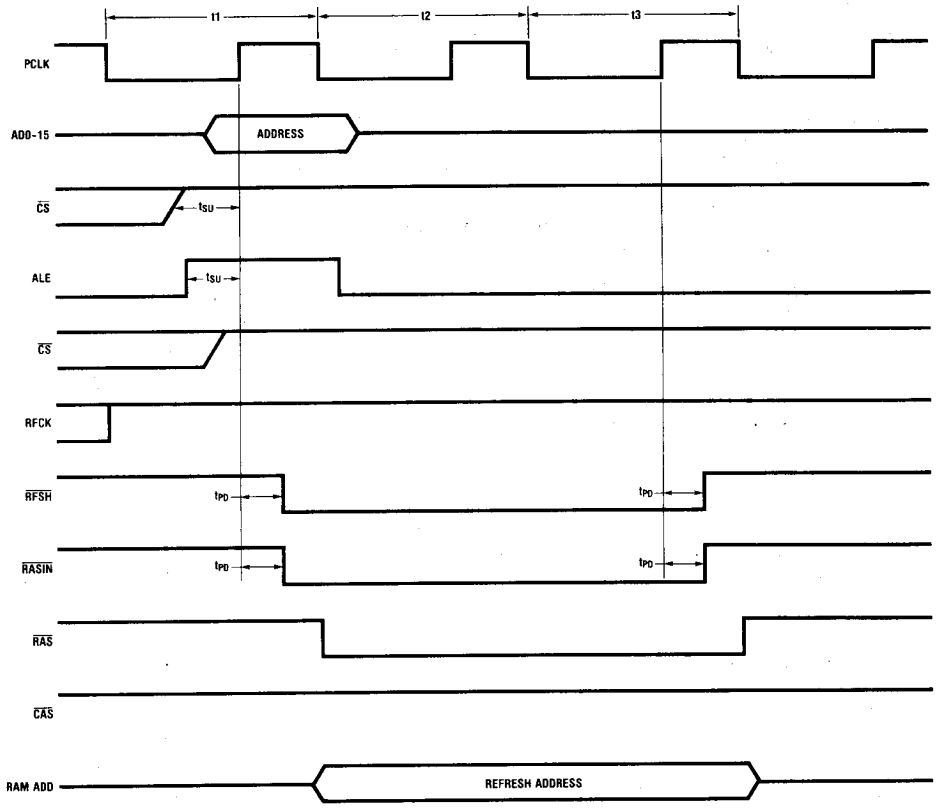


Forced Refresh



Timing Diagrams (Continued)

Transparent Refresh



16R8
DP84332
Dynamic RAM Controller Interface for the 8086-8408 System
CK A0 /BHE /CS ALE RFCK WAIT /RFRQ NC GND /OE /RASIN /CA /CB
RDY /RFSH /A /B /MRQ VCC

MRQ: = /RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • RFRQ • CS • ALE • /RFCK +
MRQ • RASIN +
RASIN • /CA • /CB • RDY • RFSH • /A • /MRQ • CS • ALE

B: = RASIN • /CA • /CB • RFSH • /A • /B +
RASIN • /CA • /CB • /RDY • /RFSH • /A • /B • WAIT +
RASIN • RDY • /RFSH • A • /B

A: = RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /WAIT +
RASIN • RDY • /RFSH • /A • B +
RASIN • RDY • /RFSH • A • /B

RFSH: = /RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • RFRQ • /CS • ALE • RFCK +
/RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • RFRQ • /RFCK +
RASIN • /CA • /CB • RFSH • /A • /B

/RDY: = /RASIN • /CA • /CB • RDY • /RFSH • /A • /B • MRQ • RFRQ • CS • ALE • /RCFK +
RASIN • /CA • /CB • RDY • RFSH • /A • /MRQ • CS • ALE +
/RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • /RFRQ • CS • ALE • WAIT +
/RASIN • /CA • /CB • /RDY • /RFSH • /A • /B • MRQ • /RFRQ • WAIT +
RASIN • /CA • /CB • /RDY • RFSH • /A +
/RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • RFRQ • CS • ALE • RFCK • WAIT

CB: = RASIN • /CA • /CB • /RFSH • /A • /B • BHE +
RASIN • CB • RDY • /RFSH • /A • B • WAIT +
RASIN • CB • RDT • /RFSH • A • /B

CA: = RASIN • /CA • /CB • /RFSH • /A • /B • /A0 +
RASIN • CA • RDY • /RFSH • /A • B • WAIT +
RASIN • CA • RDY • RFSH • A • /B

RASIN: = /RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • /RFRQ • CS • ALE +
/RASIN • /CA • /CB • /RDY • /RFSH • /A • /B • MRQ • /RFRQ +
RASIN • /CA • /CB • /RFSH • /A • /B +
RASIN • RDY • /RFSH • /A • B • WAIT +
/RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • RFRQ • ALE • RFCK +
/RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • RFRQ • /RFCK +
RASIN • /CA • /CB • RFSH • /A • /B +
RASIN • RDY • /RFSH • A • /B

Function Table

CK	A0	$\overline{BHE}$	$\overline{CS}$	ALE	RFCK	WAIT	$\overline{RFRQ}$	$\overline{OE}$	$\overline{RASIN}$	$\overline{CA}$	$\overline{CB}$	RDY	$\overline{RFSH}$	$\overline{A}$	$\overline{B}$	$\overline{MRQ}$
C	L	L	H	L	H	L	H	L	X	X	X	X	X	X	X	X
C	L	L	H	L	H	L	H	L	H	H	H	H	H	H	H	H
C	X	X	L	H	X	L	H	L	L	H	H	H	H	H	H	H
C	L	H	L	L	X	L	H	L	L	L	H	H	H	L	H	H
C	L	H	L	L	X	L	H	L	L	L	H	H	H	L	L	H
C	X	X	H	L	H	L	H	L	H	H	H	H	H	H	H	H
C	X	X	L	H	X	H	H	L	L	H	H	L	H	H	H	H
C	H	H	L	L	X	H	H	L	L	H	H	H	H	H	L	H
C	H	H	L	L	X	H	H	L	L	H	H	H	H	L	L	H
C	H	H	L	L	X	H	H	L	L	H	H	H	H	L	L	H
C	X	X	H	L	H	H	H	L	H	H	H	H	H	H	H	H
C	X	X	H	H	H	X	L	L	L	H	H	H	L	H	H	H
C	X	X	H	L	X	X	X	L	L	H	H	H	L	H	L	H
C	X	X	X	L	X	X	H	L	H	H	H	H	H	H	H	H
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C	X	X	L	H	L	X	L	L	L	H	H	L	L	H	H	L
C	H	L	L	L	X	X	X	L	L	H	H	L	L	H	L	L
C	H	L	L	L	X	X	H	L	H	H	H	L	H	H	H	L
C	H	L	L	L	X	L	H	L	L	H	H	H	H	H	H	H
C	H	L	L	L	X	L	H	L	L	H	H	L	H	L	H	H
C	H	L	L	L	X	L	H	L	L	H	L	H	H	L	H	H
C	X	X	L	L	X	L	H	L	H	H	H	H	H	L	H	H
C	X	X	X	L	L	X	L	L	L	H	H	H	L	H	H	H
C	X	X	L	H	X	H	X	L	L	H	H	L	H	H	H	L
C	L	L	L	L	X	H	X	L	H	H	H	L	H	H	L	L
C	L	L	L	L	X	H	H	L	L	H	H	L	H	H	H	H
C	L	L	L	L	X	H	H	L	L	L	L	H	H	H	L	H
C	L	L	L	L	X	H	H	L	L	L	L	H	H	L	H	H
C	X	X	L	L	X	H	H	L	H	H	H	H	H	H	H	H
C	X	X	L	H	H	L	L	L	L	H	H	H	H	H	H	H
C	H	L	L	L	X	L	X	L	L	H	L	H	H	L	H	H
C	H	L	L	L	X	L	X	L	L	H	H	H	H	L	H	H
C	X	X	L	L	X	L	X	L	H	H	H	H	H	H	H	H
C	X	X	L	H	H	H	L	H	L	L	L	L	L	L	L	L
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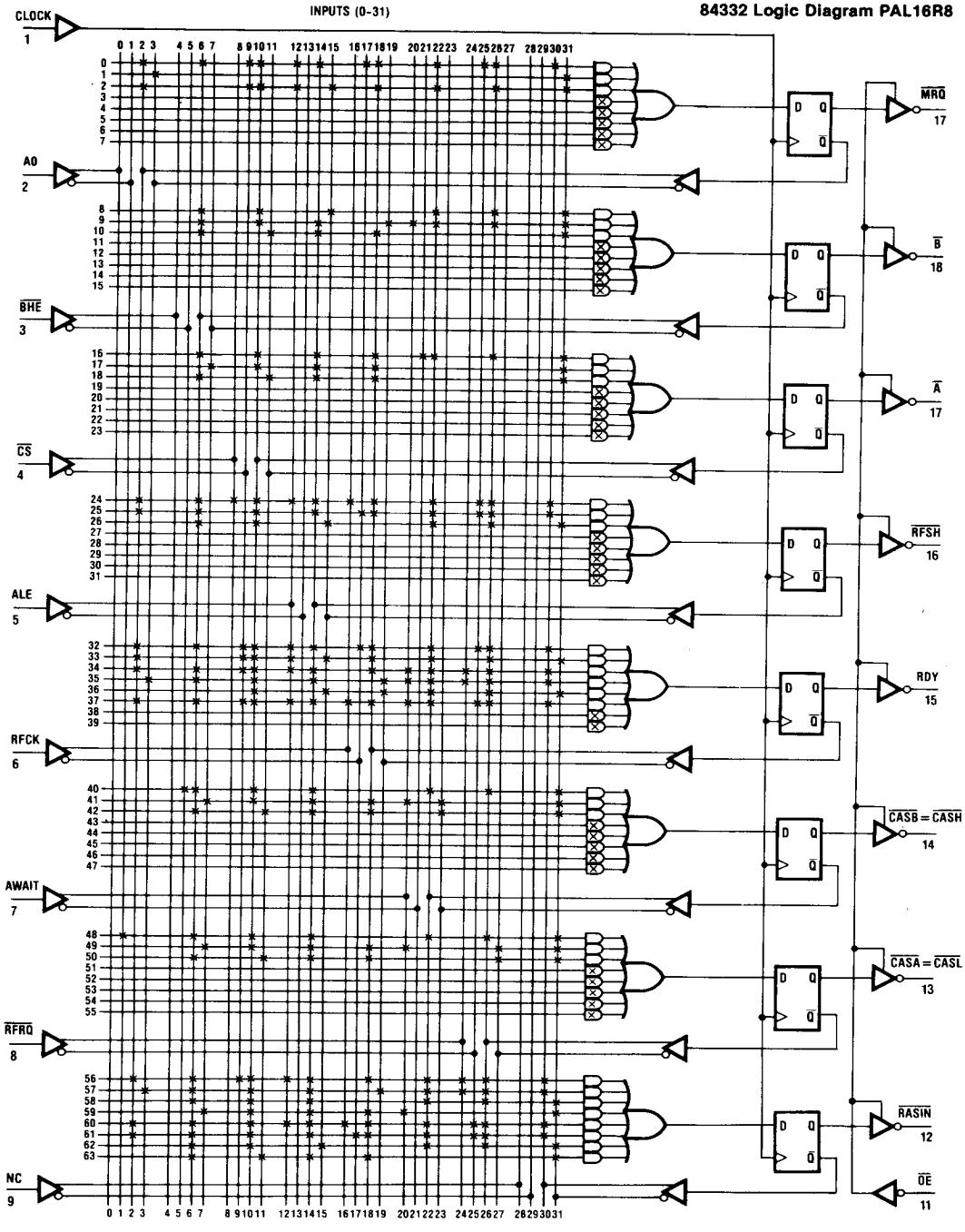

8086 PAL