National Semiconductor

DP8460 Data Separator/DP8450 Data Synchronizer

General Description

The DP8460 Data Separator is designed for application in disk drive memory systems, and depending on system requirements, may be located either in the drive or in the controller. It receives digital pulses from a pulse detector circuit (such as the DP8464 Disk Pulse Detector), if the DP8460 is situated in the drive, or from an ST506 type interface if it is situated in the controller. After locking on to the frequency of these input pulses, it separates them into synchronized data and clock signals. If the input pulses are MFM encoded data, the data is made available as decoded NRZ data to be deserialized directly by a controller (such as the DP8466 Disk Data Controller). If a run-length-limited code is used, the synchronized data output is available to allow external circuitry to perform the data decoding function. All of the digital input and output signals are TTL compatible and only a single +5V supply is required. The chip is housed in a standard narrow 24-pin dual-in-line package (DIP) and is fabricated using Advanced Schottky bipolar analog and digital circuitry. This high speed I.C. process allows the chip to work with data rates up to 15Mbit/sec.

The DP8460 features a phase-lock-loop (PLL) consisting of a pulse gate, phase comparator, charge pump, buffering amplifier, and voltage-controlled-oscillator (VCO). Pins are provided for the user to select the values of the external filtering components required for the pulse gate and amplifier, the frequency setting components required for the VCO, and two current setting resistors for the charge pump. The DP8460 has been designed to lock on to the incoming preamble data pattern within the first two bytes, using a high rate of charge pump current. Once lock-on has been achieved, the charge pump switches to a lower rate (both rates being determined by the external resistors) to maintain stability for the remainder of the read operation. At this time the READ CLOCK output switches, without glitching, from half the 2f-CLOCK frequency to half the VCO CLOCK frequency. After lock-on, with soft sectored disks, the MISSING CLOCK DETECTED output indicates when a missing clock in an address mark field occurs so the controller can align byte boundaries to begin deserialization of the incoming data.

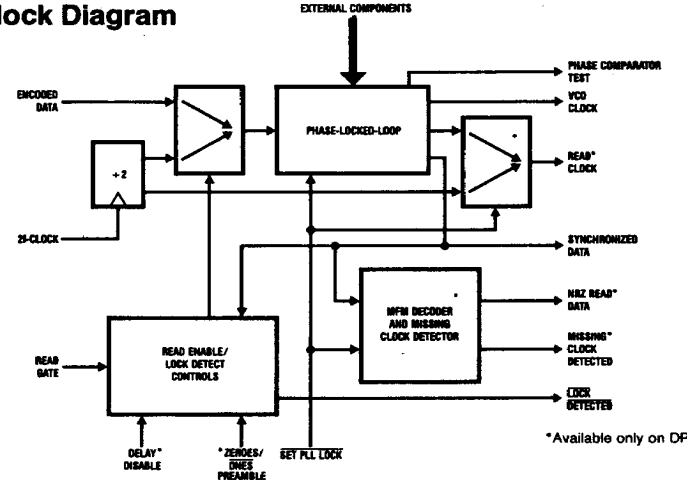
The DP8450 incorporates just the data synchronization function of the DP8460. The READ CLOCK generating circuitry along with the MFM Decoder, Missing Clock Detector, and Read Enable Delay, is not included in the DP8450 which is packaged in a 20 pin DIP.

Users who do not need these functions and are only interested in using the SYNCHRONIZED DATA OUTPUT along with the VCO OUTPUT might consider the DP8450 as an alternative to the DP8460.

Features

- Operates at data rates up to 15Mbit/sec
- Separates MFM data into read clock and serial NRZ data
- 4 byte preamble-lock indication capability
- Preamble recognition of MFM encoded "0"s or "1"s
- User-determined PLL loop filter network
- PLL charge pump has two user-determined tracking rates
- External control of track rate switchover
- No glitch on READ CLOCK at switchover
- Synchronized data provided as an output (for RLL codes)
- ORed phase comparator outputs for monitoring bit-shift
- Missing clock detected for soft sectored disks
- Less then ½W power consumption
- Standard narrow 24-pin DIP
- Single +5V supply

Simplified Block Diagram

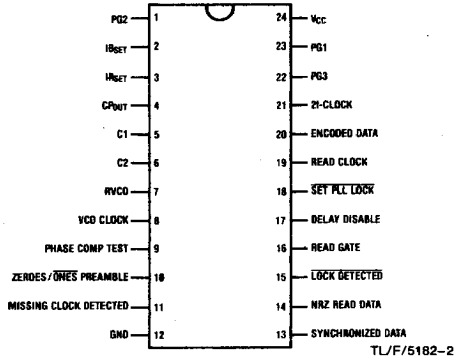


*Available only on DP8460

TL/F/5182–1

Connection Diagram

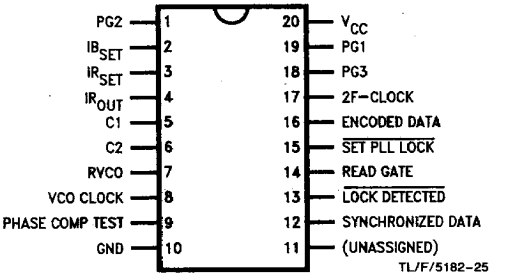
DP8460 Dual-In-Line Package



TL/F/5182-2

Top View

DP8450 Dual-In-Line Package



TL/F/5182-25

Top View

PIN DEFINITIONS: *

Power Supply

24 V_{CC} +5V ±5%

12 Ground

TTL Level Logic Inputs

16 READ GATE: This is an active high input signal that sets the DP8460 Data Separator into the Read Mode.

17 DELAY DISABLE: This input determines the delay from READ GATE going high to the time the DP8460 enters the Read Mode. If DELAY DISABLE is set high, this delay is within one cycle of the 2f-CLOCK signal. If DELAY DISABLE is set low, the delay is thirty two-cycles of the 2f-CLOCK, as shown in *Figure 1*.

18 SET PLL LOCK: This input allows the user to determine when the on-chip PLL will go into the low track rate. A high level at this input results in the PLL being in the high track rate. If this input is connected to the LOCK DETECTED output, the PLL will go into the low track rate mode immediately after lock is detected.

10 ZEROES/ONES PREAMBLE: A high level on this input enables the circuit to recognize an All Zeros data preamble. A low level results in the recognition of an All Ones data preamble.

20 ENCODED DATA: This input is connected to the output of the head amplifier/pulse-detecting network located in the disk drive. Each positive edge of the ENCODED DATA waveform identifies a change of flux on the disk. In the case of MFM encoded data, the input will be raw MFM.

21 2f-CLOCK: This is a system clock input, which is either a signal generated from the servo track (for systems utilizing servo tracks), or a signal buffered from a crystal. 2f CLOCK MUST ALWAYS BE APPLIED TO THIS INPUT FOR PROPER OPERATION.

TTL Level Logic Outputs

8 VCO CLOCK: This is the output of the on-chip VCO, transmitted from an Advanced Schottky-TTL buffer. It is synchronized to the MFM data output and, if needed, it can be used as the 2f-CLOCK for encoding MFM when writing to the disk.

15 LOCK DETECTED: This output goes active low only after both PLL Lock has occurred and the preamble pattern has been recognized. It remains low until READ GATE goes inactive

14 NRZ READ DATA: This is the NRZ decoded data output, whose leading edges coincide with the trailing edge of READ CLOCK.

13 SYNCHRONIZED DATA: This output is the same encoded data that is input to the chip, but is synchronous with the negative edge of the VCO CLOCK.

11 MISSING CLOCK DETECTED: When a missing clock is detected, this output will be a single pulse (of width equal to one cycle of READ CLOCK) occurring as shown in *Figure 2*.

19 READ CLOCK: This is half VCO CLOCK frequency when SET PLL LOCK is low; it is half 2f-CLOCK frequency at all other times. A deglitcher is utilized to ensure that no short clock periods occur during either switchover.

9 PHASE COMP TEST: This output is the logical "OR" of the Phase Comparator outputs, and may be used for the testing of the disk media.

Analog Signals

23, 22, PG1, PG3: The external capacitors and resistor of the Pulse Gate filter are connected to these pins. PG1 should be connected directly to the ground pin, pin 12.

1 PG2: This is the Pulse Gate current supply.

3 IRSET: The current into the rate set pin (V_{BE}/R_{Rate}) is half the charge pump output current for the low tracking rate.

2 IBSET: The current into the boost set pin (V_{BE}/R_{Boost}) is half the amount by which the charge pump current is increased for the high tracking rate. (I_{HIRATE} = I_{RATE} Set + I_{BOOST} Set).

4 CPOUT: CHARGE PUMP OUT/BUFFER AMP IN is available for connection of external filter components, for the phase-lock-loop. In addition to being the charge pump output node, this pin is also the noninverting input to the op-amp of the Buffer Amplifier.

7 RVCO: The current into this pin determines the operating currents within the VCO.

5, 6 VCO C1, C2: An external capacitor connected across these pins sets the nominal VCO frequency.

* Pin number designations apply only to the DP8460. See Connection Diagram for DP8450.

Absolute Maximum Ratings

Supply Voltage	7V	Input Current	
TTL Inputs	7V	(CPOUT, IRSET, IBSET, RVCO)	2mA
Output Voltages	7V	Storage Temperature	−65°C to 150°C

Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75	5.00	5.25	V
T_A	Ambient Temperature		0	25	70	°C
I_{OH}	High Logic Level Output Current	V_{CO} Clock Others			−2000 −400	μA
I_{OL}	Low Logic Level Output Current	V_{CO} Clock Others			20 8	mA
f_{DATA}	Input Data Rate		2.0		15	Mbit/sec
t_{WCK}	Width of 2f-CLOCK, High or Low		10			ns
t_{WPD}	Width of ENCODED DATA Pulse (Note 2)	High	5 ns + 0.10t			ns
		Low	0.4t			
V_{IH}	High Logic Level Input Voltage		2			V
V_{IL}	Low Logic Level Input Voltage				0.8	V
t_{SETUP} (Read Gate)	Mininum amount of time which a positive edge of read gate must precede a negative edge of V_{CO} (Pin 8)		20			ns
t_{HOLD} (Read Gate)	Minimum time required for a positive edge of read gate to be held after a negative edge of V_{CO} (Pin 8)		10			ns

DC Electrical Characteristics Over Recommended Operating Temperature Range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min., I_{OH} = Max.	V_{CC}−2V	V_{CC}−1.6V		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min., I_{OL} = Max.			0.5	V
I_{IH}	High Level Input Current	V_{CC} = Max., V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max., V_I = 0.4V			−200	μA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.125V[1]	−20		−110	mA
I_{CC}	Supply Current	V_{CC} = Max.			100	mA
I_{OUT}	Charge Pump Output Current	$I_{RSET} = V_{BE}/R_{RATE}$ $I_{BSET} = V_{BE}/R_{BOOST}$	−10% −10%	$1.7 \times I_{RSET}$ $1.8 \times (I_{RSET} + I_{BSET})$	+10% +10%	mA

1. This value has been chosen to produce a current that closely approximates one-half of the true short-circuit output current. I_{OS}.
2. t is defined as the period of the encoded data.

AC Electrical Characteristics (Over Recommended V_{CC} and Operating Temperature Range.)

(All Parts unless stated otherwise) ($t_R = t_F = 2.0$ ns, $V_{IH} = 3.0V$, $V_{IL} = 0V$)

Symbol	Parameter	Min	Typ	Max	Units
t_{READ}	Positive READ CLOCK transitions from READ GATE set active until PLL Lock sequence begins (DELAY DISABLE low)		16	17	—
t_{READ}	Positive READ CLOCK transitions from READ GATE set active until PLL Lock sequence begins (DELAY DISABLE high)		1	1	—
$t_{DECODE\ NRZ}$	Number of READ CLOCK cycles required to output each decoded MFM data bit[4]	—	2	3	T-clock
$t_{TRANSMIT\ MFM}$	Positive READ CLOCK transitions required to transmit input MFM to output	1	2	3	—
$t_{READ\ ABORT}$	Number of READ CLOCK cycles after READ GATE set low to read operation abort			2	T-clock
t_{WINDOW}	Variance of center of decode window from nominal[7,8] DP8460-4			10	ns
$\phi_{LINEARITY}$	Phase range for charge pump output linearity[2]	$-\pi$		$+\pi$	Radians
K_1	Phase Comparator — Charge Pump gain constant[5] ($N = f_{VCO}/f_{INPUT\ DATA}$ $2 \le N \le 4$ for MFM)		$\frac{1.78V_{BE}}{N2\pi R}$		Amps/rad
$V_{CONTROL}$	Charge pump output voltage swing from nominal		± 100		mV
K_{VCO} ($=A \times K_2$)	VCO gain constant (ω_{VCO} = VCO center frequency in rad/s)[6]	$\frac{1.20\omega_C}{V_{BE}}$	$\frac{1.40\omega_C}{V_{BE}}$	$\frac{1.60\omega_C}{V_{BE}}$	rad/sec. V
f_{VCO}	VCO center frequency variation over temperature and V_{CC}	-5		$+5$	%
$f_{MAX\ VCO}$	VCO maximum frequency	50			MHz
t_{HOLD}	Time READ CLOCK is held low during changeover after lock detection has occurred[3]			1½	T-clock
t_{PHL}	Prop. delay. V_{CO} negative edge to synchronized data negative edge			30	ns
t_{PLH}	Prop. delay. V_{CO} negative edge to synchronized data positive edge			25	ns

1. A sample calculation of frequency variation vs. control voltage: $V_{IN} = \pm 0.1V$;

$$K_{VCO} = \frac{\omega OUT}{V_{IN}} = \frac{0.4\omega_C}{0.2V} = \frac{2.0\omega_C}{V}\ \frac{(rad/sec)}{(volt)}$$

2. $-\pi$ to $+\pi$ with respect to 2f VCO CLOCK
3. T-clock is defined as the time required for one period of the READ CLOCK to occur.
4. This number remains fixed after PLL Lock occurs.
5. With respect to VCO CLOCK; $I_{PUMP\ OUT} = 1.7\ I_{SET}$

$$I_{SET} = \frac{V_{BE}}{R_{SET}}$$

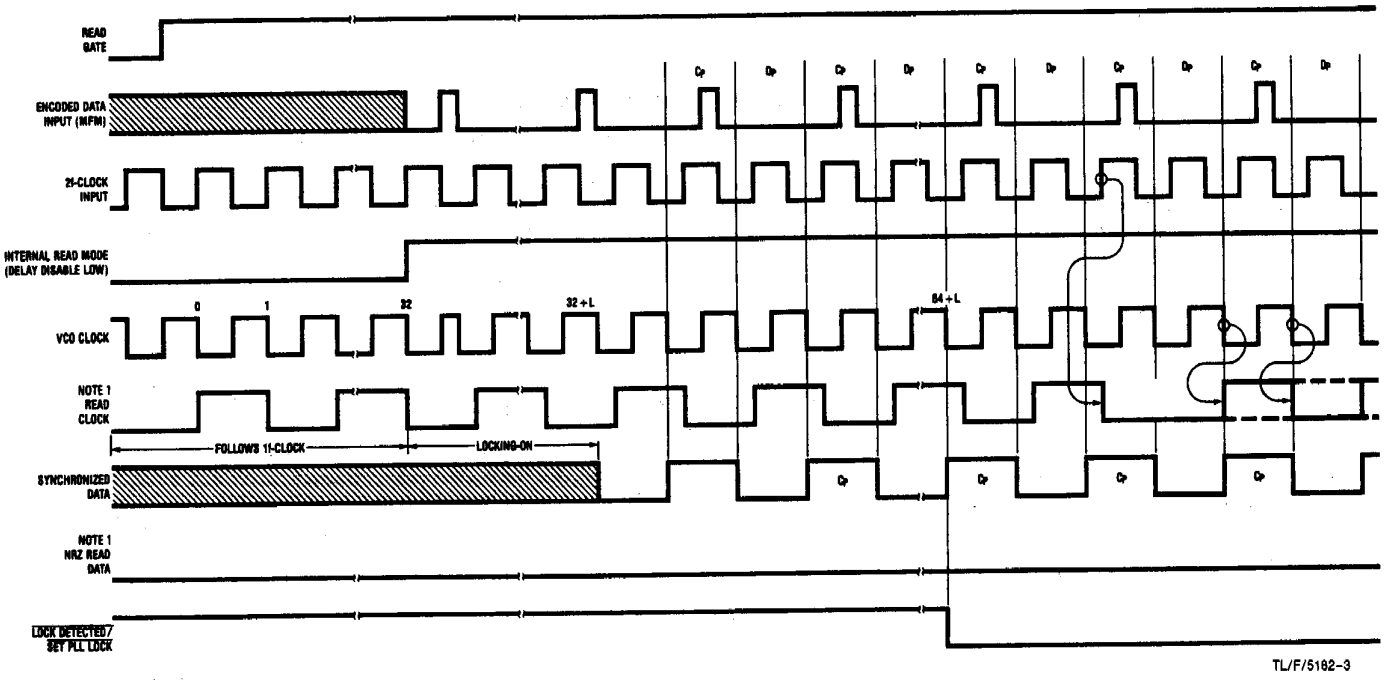
6. Although specified as the VCO gain constant, this is the gain from the Buffer Amplifier input to the VCO output.
7. τ is defined as the period of the incoming data stream.
8. This specification is guaranteed only for the conditions under which the parts were tested. However, significant variation from the formula is not expected for other data rates and filters. The filter values below were chosen for operation in an automatic test system (static window) environment. Different criteria may apply for choosing filter values in a disk system. See p. 15-17 for sample calculations of other filter values:

		Filter				
Part Type	Data Rate Tested	C_1	C_2	R_1	R_{RATE}	R_{BOOST}
DP8450-4	5 MBit/sec	0.02 μF	150 pF	200Ω	750Ω	1.6K
DP8460-4	5 MBit/sec	0.02 μF	150 pF	200Ω	750Ω	1.6K

External Component Selection (All Parts)[1]

Symbol	Component	Min	Typ	Max	Unit
R_{VCO}	VCO Frequency Setting Resistor[2]	990		1010	Ω
C_{VCO}	VCO Frequency Setting Capacitor[3,4]	28		245	pF
R_{RATE}	Charge Pump I_{RATE} Set Resistor[6]	0.4		4.0	kΩ
R_{BOOST}	Charge Pump (High Rate) I_{BOOST} Resistor[6]	0.5		∞	kΩ
C_R	I_{RATE} Bypass Capacitor[5]	.01			μF
C_B	I_{BOOST} Bypass Capacitor[5]	.01			μF

1. External component values for the Loop Filter and Pulse Gate are given on p. 16 and p. 13 respectively.
2. A 1% Component Tolerance is Required.
3. These MIN and MAX values correspond to the MAX and MIN data rates respectively.
4. The Component Tolerance is system dependent on how much center frequency deviation can be tolerated.
5. Component Tolerance 15%.
6. The minimum value of the parallel combination of R_{RATE} and R_{BOOST} is 400Ω.



NOTE 1. Not included on the DP8450.

C_P, D_P = preamble clock and preamble data bits respectively.

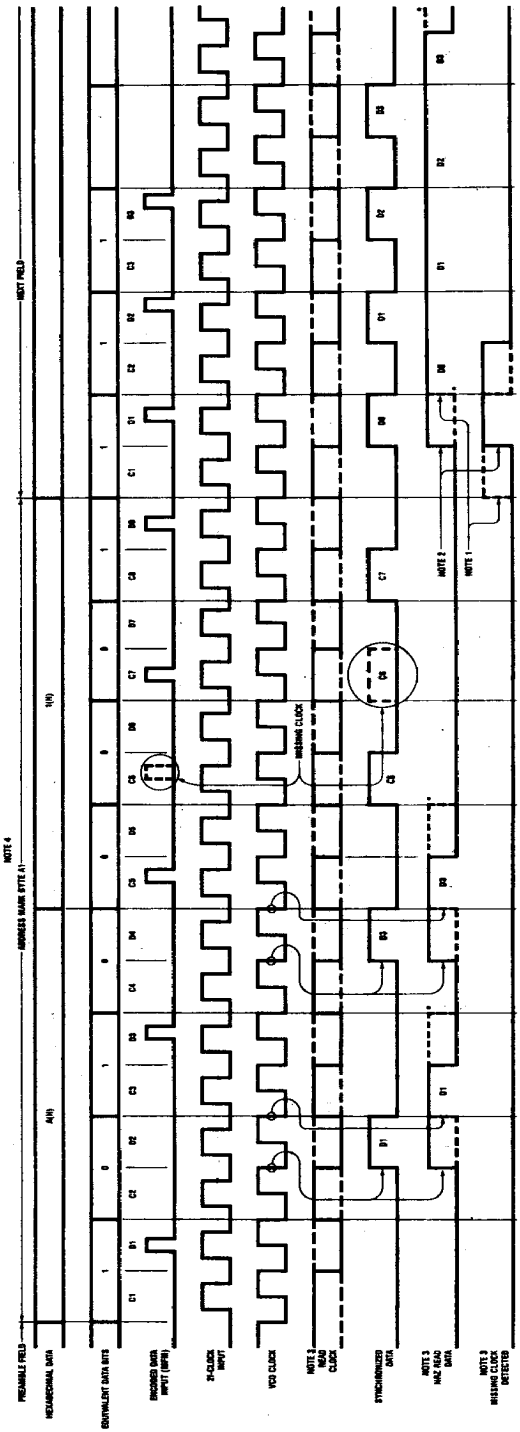
L = Number of 2f-clock cycles required for VCO to lock (typically ≈ 20 2f-clock cycles), but determined by external component values

At 32 + L, VCO has just locked.

At 64 + L, circuit has confirmed lock (has been in lock for 16 MFM clock bits). This sequence shows the MFM all-zeros preamble pattern.

For DP8450 DELAY DISABLE does not exist and part functions as if this input is always high.

FIGURE 1. Lock-on Sequence Waveform Diagram



* READ CLOCK and NRZ READ DATA may be delayed by one VCO clock period depending on the phase of the internal clock at activation of READ GATE input.

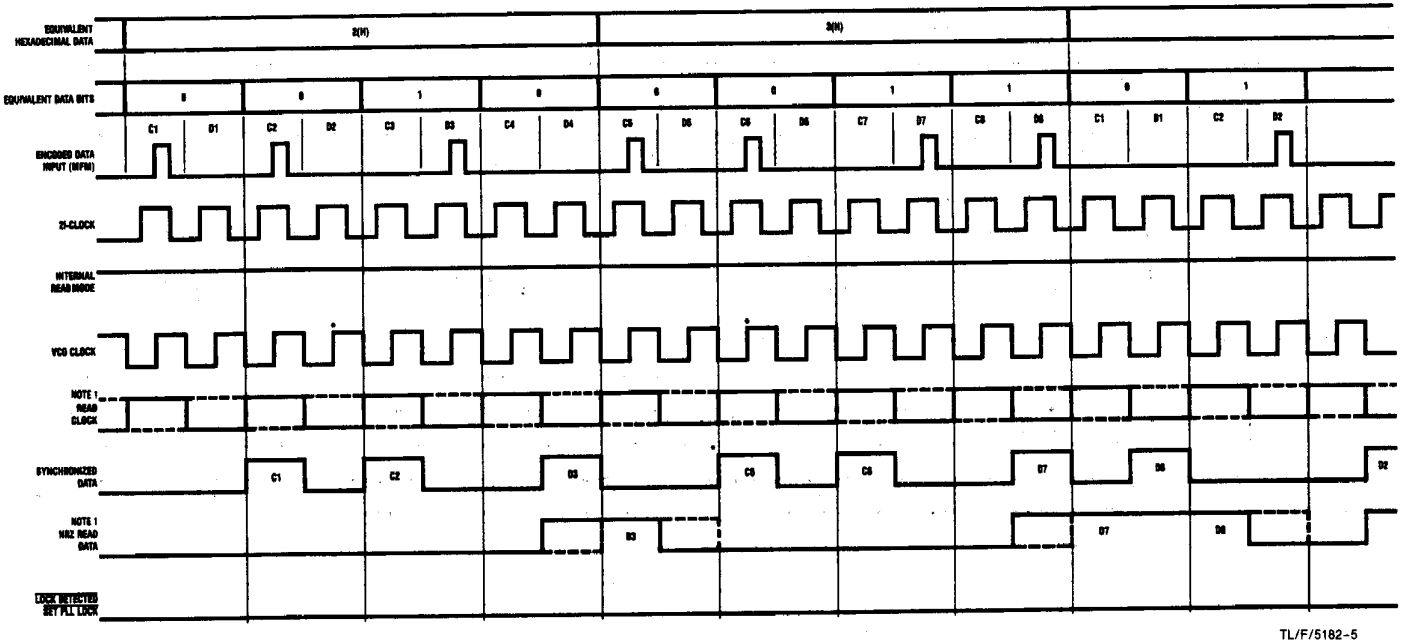
① MISSING CLOCK DETECTED is one READ CLOCK period ahead of the chip issuing D8 on the NRZ READ DATA output when READ CLOCK is delayed by one VCO clock period

② MISSING CLOCK DETECTED is synchronous with the chip issuing D8 on the NRZ READ DATA Output when READ CLOCK is not delayed

③ Not included on the DP8450

④ The A_1 byte is shown, however, any missing clock bit between two adjacent clock bits will be detected.

FIGURE 2. Missing Clock Detection Waveform Diagram

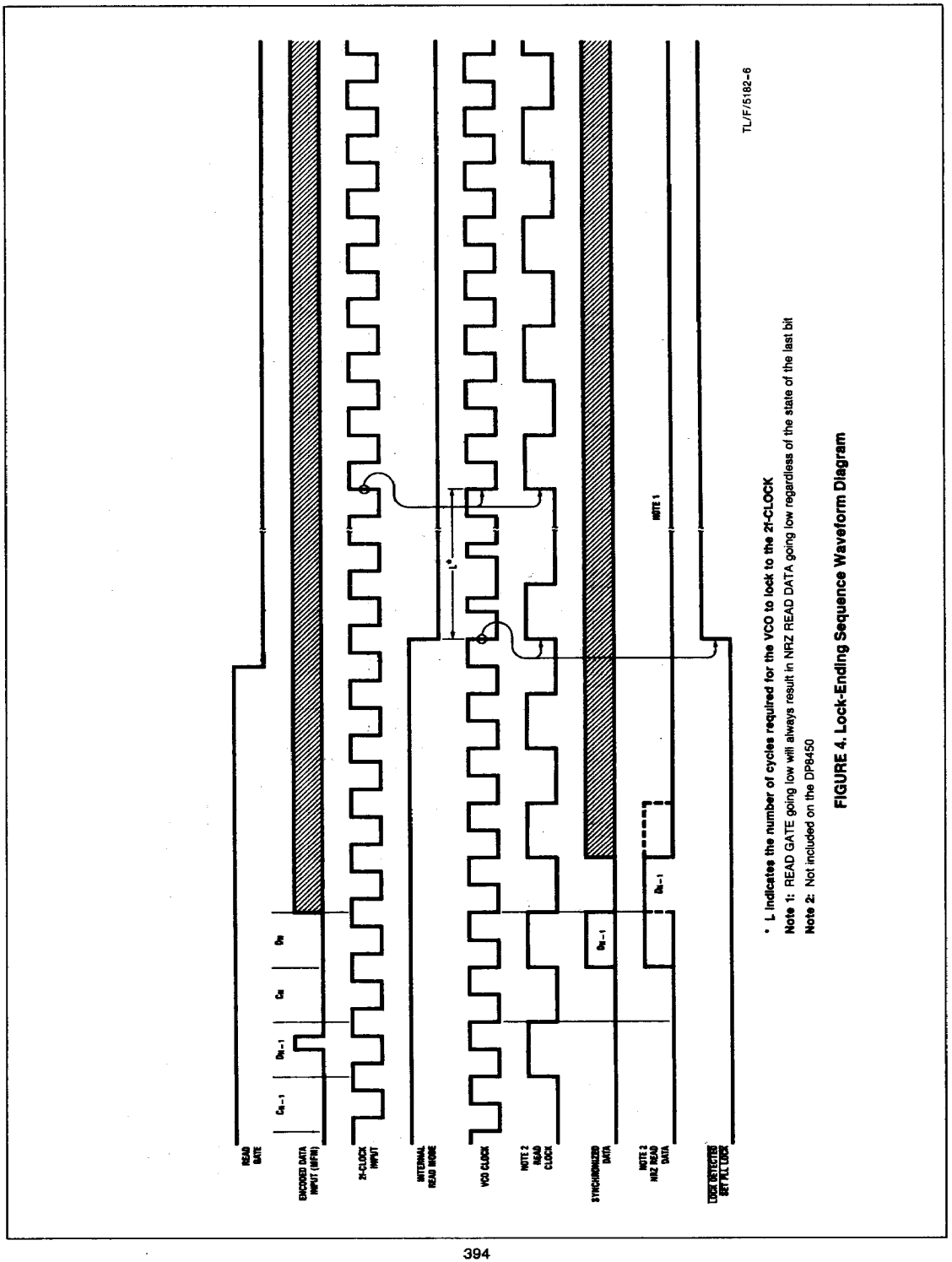


TL/F/5182–5

* READ CLOCK and NRZ READ DATA may be delayed by one VCO clock period with respect to Synchronized Data depending on the phase of the internal clock at activation of READ GATE Input.

Note 1. Not included on the DP8450.

FIGURE 3. Locked-on Waveform Diagram



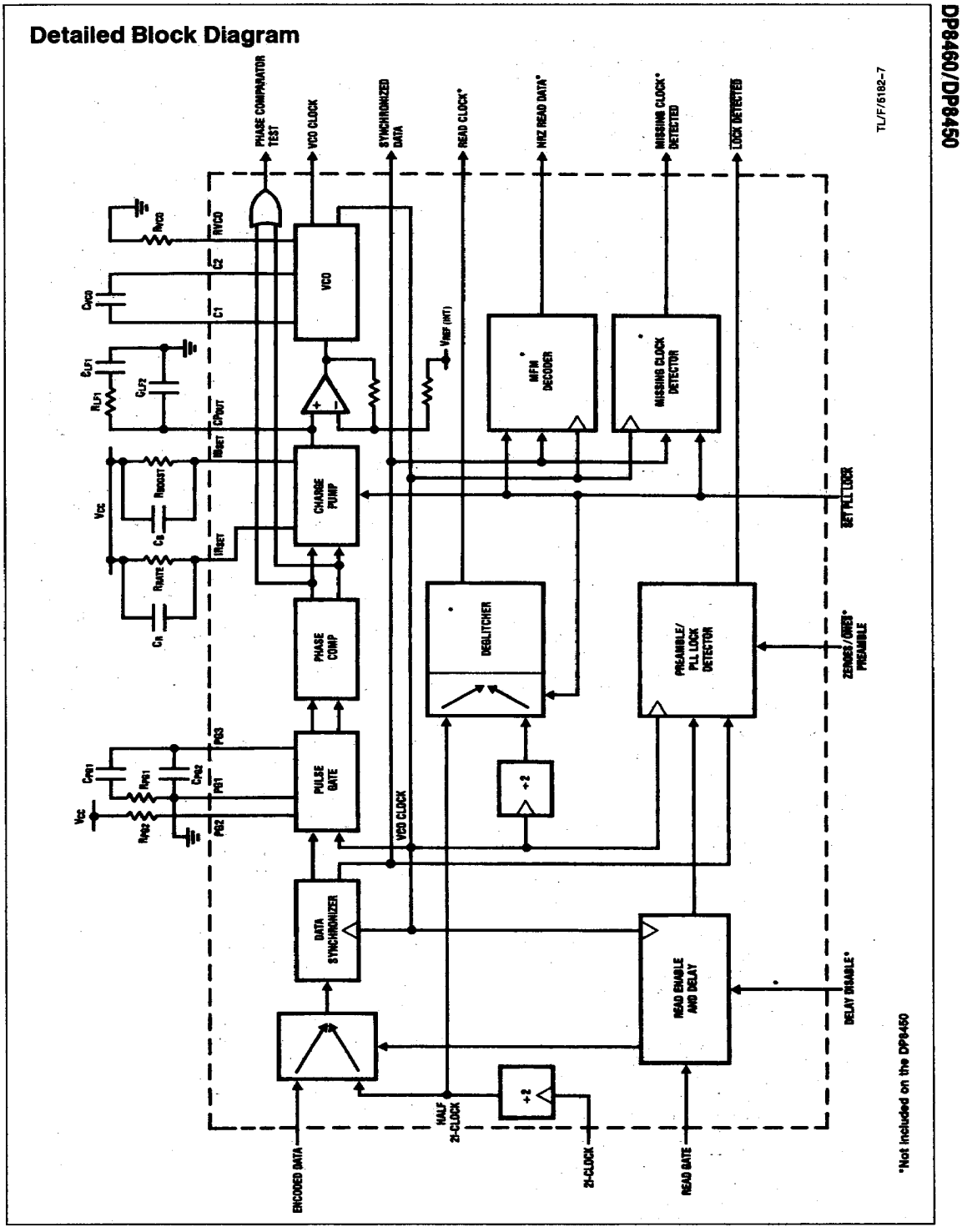
* L indicates the number of cycles required for the VCO to lock to the 21-CLOCK

Note 1: READ GATE going low will always result in NRZ READ DATA going low regardless of the state of the last bit

Note 2: Not included on the DP8450

FIGURE 4. Lock-Ending Sequence Waveform Diagram

Detailed Block Diagram



CIRCUIT OPERATION

When the READ GATE input goes high, the DP8460 Data Separator enters the read mode after a period determined by the state of the DELAY DISABLE pin. This may be either one or thirty two 2f-CLOCK cycles. Referring to *Figure 1*, once in the read mode, the phase-locked-loop reference signal is switched from 2f-CLOCK input to the ENCODED DATA input. The PLL, initially in the high-tracking rate mode, then attempts to lock onto the incoming encoded data stream. By careful selection of the loop filter components, this can be within 2 bytes. Preamble pattern recognition then can begin. As soon as two bytes of the selected preamble are detected, (the selection is determined by the ZEROES/ONES PREAMBLE pin) the LOCK DETECTED output goes low. In a typical MFM disk drive application, the LOCK DETECTED output is directly connected to the SET PLL LOCK input. With this connection, track rate selection, clock output switchover, and data output enabling will occur after four consecutive preamble bytes have been fed into the chip, from the time the read mode began.

A low level on the SET PLL LOCK causes the PLL Charge Pump to switch from the high to low tracking rate. At the same time the source of the READ CLOCK signal is switched from half the frequency of the 2f-CLOCK to half the VCO clock. The MFM decoder also becomes enabled and begins to output decoded NRZ data. If the preamble is being decoded, and it is a zeroes data preamble, the NRZ READ DATA output will remain low until the end of the preamble. It will then output NRZ data some 2f-CLOCK periods after the preamble field has ended, as shown in *Figures 2* and *3*.

Figure 4 shows the sequence when READ GATE goes low, signifying the end of a read operation. The PLL reference signal is switched back to half the 2f-CLOCK and the LOCK DETECTED output (and therefore the SET PLL LOCK input) goes high. The PLL then returns to the high tracking rate, and the output signals return to their initial conditions. 2f CLOCK MUST ALWAYS BE APPLIED TO THE DP8460 FOR PROPER OPERATION.

CIRCUIT DESCRIPTION

1. Read Enable and Delay: If the DELAY DISABLE input is connected low, then thirty two 2f-CLOCK cycles after READ GATE goes active, the DP8460 will go into the read mode. If the DELAY DISABLE input is connected high, the chip will go into the read mode one 2f-CLOCK cycle after READ GATE goes active. This feature allows the user to choose the time at which the PLL Lock Sequence begins and thus accommodates systems with short preambles. This circuitry is not in the DP8450 and it will perform as if the DELAY DISABLE input is HIGH.

2. Pulse Gate, including Input Multiplexer and Data Synchronizer: The Input Multiplexer selects the input to the phase-lock-loop. When the Read Gate is low, the Input Multiplexer feeds the 2f-CLOCK divided by two into the Pulse Gate. The Pulse Gate allows a reference signal from the VCO into the Phase Comparator only when a signal from the 2f-CLOCK divided by two occurs. In the read mode, the Input Multiplexer switches to the ENCODED DATA signal. The VCO CLOCK then begins to synchronize with the ENCODED DATA signal. The Pulse Gate allows a reference signal from the VCO into the Phase Comparator only when a ENCODED DATA bit is valid. The Pulse Gate utilizes a scheme which delays the incoming data by one-half the period of the 2f-CLOCK. This optimizes the position of the decode window and allows input jitter up to ± half the 2f-CLOCK period, assuming no error in the decode window position. The decode window error can be determined from the specification in the Electrical Characteristics Table.

3. Phase Comparator: The Phase Comparator receives its inputs from the Pulse Gate, and is edge-triggered from these inputs to provide charge-up and charge-down outputs.

4. Charge Pump: The high speed charge pump consists of a switchable constant current source and sink. The charge pump constant current is set by connecting external resistors to V_{CC} from the charge current rate set (IRSET) and current boost set (IBSET) pins. Before lock is indicated, the PLL is in the fast tracking rate and both resistors determine the current. In the slow tracking rate after lock-on, only the IRSET resistor determines the charge pump current. The output of the charge pump feeds into external filter components and the Buffer Amplifier.

5. Buffer Amplifier: The input of the Buffer Amplifier is internally connected to the charge pump's constant current source/sink output as well as the external Loop Filter components. The Buffer Amplifier is configured as a high input impedance amplifier which allows for the connection of external PLL filter components to the Charge Pump output pin CPOUT. The output of the Buffer Amplifier is internally connected to the VCO control input.

6. VCO: The Voltage-Controlled-Oscillator requires a resistor from the RVCO pin to ground and a capacitor between pins C1 and C2, to set the center frequency. The VCO frequency can be varied from nominal by approximately ±20%, as determined by its control input voltage.

7. PLL Lock-on/Preamble Pattern Detector: To recognize preamble, the preamble pattern from the disk must consist exclusively of either data bit zeroes (encoded into ..10.. MFM clock pulses) when the ZEROES/ONES PREAMBLE pin is set high, or data bit ones (encoded into ..01.. MFM clock pulses) when set low. The preamble pattern must be long enough to allow the PLL to lock, and subsequently for the Preamble Pattern Detector circuit to detect two complete bytes.

Once the chip is in the read mode, the VCO proceeds to lock on to the incoming data stream. The Preamble Pattern Detector then searches for a continuous pattern of 10101010101010101010101010101010 (16 consecutive pulses at the data rate) to indicate lock has been achieved. The LOCK DETECTED output then goes low.

Any deviation from the above-mentioned one-zero pattern at any time before PLL Lock is detected will reset the PLL Lock Detector. The lock detection procedure will then start again.

8. MFM Decoder: The MFM Decoder receives synchronized MFM data from the Pulse Gate and converts it to NRZ READ DATA. For run-length-limited codes the MFM Decoder and Missing Clock Detector will not be used.

9. Missing Clock Detector: This block is only required for soft-sectored drives, and is used to detect a missing clock violation of the MFM pattern. The missing clock is inserted when writing to soft-sectored disks to indicate the location of the Address Mark in both the ID and the Data fields of each sector. Once PLL Lock has been indicated, the Missing Clock Detector circuit is enabled. MISSING CLOCK DETECTED will go active only if the incoming data pattern contains one suppressed clock bit framed by two adjacent clock bits. The output signal goes high for one cycle of READ CLOCK.

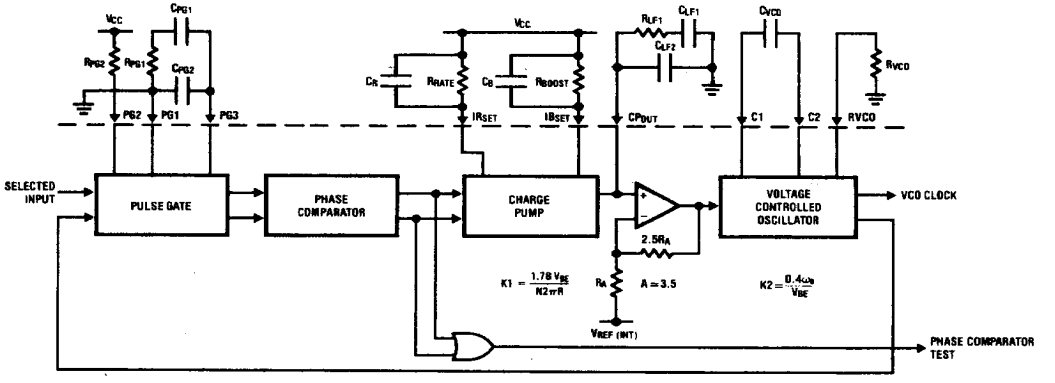
10. Clock Multiplexer and Deglitcher: When the $\overline{\text{SET PLL LOCK}}$ input changes state this circuit switches the source of the READ CLOCK signal between the half 2f-CLOCK frequency and the half VCO CLOCK frequency. A deglitcher circuit is utilized to ensure that no short clock periods occur during either switchover.

BIT JITTER TOLERANCE

The DP8460 −4 part will be used in most low data rate applications. As an example, at the 5Mbit/sec data rate of most 5¼ inch drives, T = 200 ns so that from the Electrical Characteristics Table, t_{WINDOW} = (8 + (1% of 200 ns)) or 10 ns. The chip therefore contributes up to 10 ns of window error, out of the total allowable error of 50 ns (half the 2f-clock period of 100 ns). This allows the disk drive to have a margin of 40 ns of jitter on the transition position before an error will occur.

ANALOG CONNECTIONS TO THE DP8460

External passive components are required for the Pulse Gate, Charge Pump, Loop Filter and VCO as shown in *Figure 5*. The information provided here is for guidelines only. The user should select values according to his own system requirements. Phase-Locked Loops are complex circuits that require detailed knowledge of the specific system. Factors such as loop gain, stability, response to change of signal, lock-on time, etc are all determined by the external components. In many disk systems these factors are critical, and National Semiconductor recommends the designer be knowledgeable of phase-locked-loops, or seek the advice of an expert. Inaccurate design will probably result in excessive disk error rates. The phase-locked-loop in the DP8460 has many advantages over all but the most sophisticated discrete designs, and if the component values are selected correctly, it will offer significant performance advantages. This should result in a reduction of disk error rates over equivalent discrete designs.



TL/F/5182–8

FIGURE 5. Phase-Locked-Loop Section DP8460/DP8450

Pulse Gate

There are four external components connected to the Pulse Gate as shown in *Figure 6* with the associated internal components. The values of R_{PG1}, R_{PG2}, C_{PG1}, and C_{PG2} are dependent on the data rate. R_{PG1} is proportional to the data rate, while R_{PG2}, C_{PG1} and C_{PG2} are inversely proportional. Table I shows component values for the data rates given. Component values are calculated by selecting R_{PG2} from Table I. Next calculate

$$C_{PG1} = \left(\frac{2.12 \times 10^5}{890 + R_{PG2}}\right)\left(\frac{1}{100 \times R_S}\right)^2$$

$$C_{PG2} = \frac{1}{10} C_{PG1}, \text{ and } R_{PG1} = \left(\frac{890 + R_{PG2}}{2.38 \times 10^5}\right)(100 \times R_S).$$

In the above equations R_S is the rotational speed and, for 3600 RPM, R_S = 60Hz. A rotational speed of 3600 RPM was assumed for the calculations in Table I. For data rates not listed, R_{PG2} may be approximated as $(30\ k\Omega/f_{DATA}) - 1.20\ k\Omega = R_{PG2}$ where f_{DATA} is the data rate in Megabits/second.

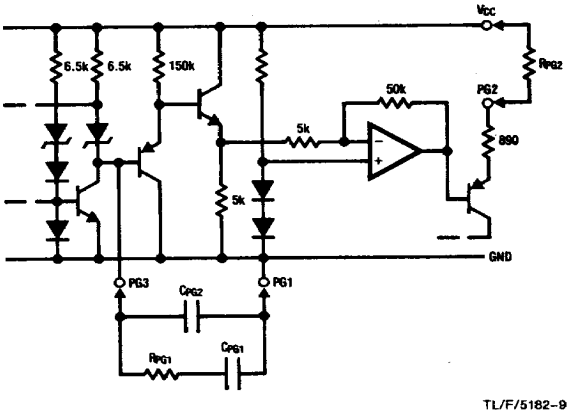
Data Rate	R_{PG2}	R_{PG1}	C_{PG1}	C_{PG2}
2Mbit/sec	15 kΩ	430Ω	.39 μF	.039 μF
5Mbit/sec	4.7 kΩ	150Ω	1 μF	.1 μF
10Mbit/sec	1.8 kΩ	68Ω	2.2 μF	.22 μF
15Mbit/sec	750Ω	39Ω	3.9 μF	.39 μF

TABLE I. Pulse Gate Component Selection Chart
Components with 10% tolerance will suffice

Charge Pump

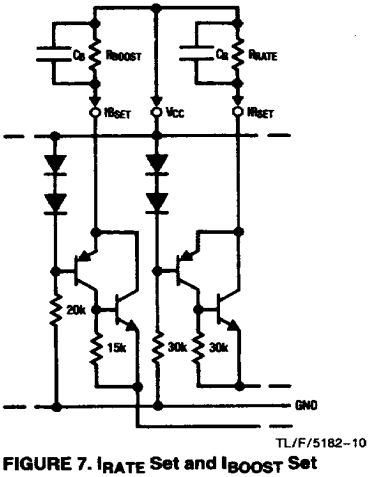
Resistors R_{RATE} and R_{BOOST} determine the charge pump current. The Charge Pump bidirectional output current is approximately (within ±10%) 1.7 × the input current. In the high tracking rate with $\overline{\text{SET PLL LOCK}}$ high, the input current is $I_{BSET} + I_{RSET}$, ie, the sum of the currents through R_{BOOST} and R_{RATE} from V_{CC}. In the low tracking rate, with $\overline{\text{SET PLL LOCK}}$ low, this input current is I_{RSET} only.

A recommended approach would be to select R_{RATE} first. The External Component Limits table allows R_{RATE} to be 1.2 kΩ to 6.5 kΩ, so for simplicity select R_{RATE} = 1.5 kΩ. A typical loop gain change of 2:1 for high to low tracking rate would require $R_{BOOST} = R_{RATE}$ or 1.5 kΩ. Referring to *Figure 7* the input current is effectively V_{BE} / R_{RATE} in the low tracking rate, where V_{BE} is an internal voltage. This means that the current into or out of the loop filter is approximately 1.7 V_{BE} / R_{RATE}, or in this example approximately 0.85 mA. Note that although it would seem the overall gain is dependent on V_{BE}, this is not the case. The VCO gain is altered internally by an amount inversely proportional to V_{BE}, as detailed in the section on the Loop Filter. This means that as V_{BE} varies with temperature or device spread, the gain will remain constant for a particular fixed values of R_{RATE} and R_{BOOST}. This alleviates the need for potentiometers to select values for each device. The tolerance required for these two resistors will depend on the total loop gain tolerance allowed, but 5% would be typical. Also V_{CC} by-pass capacitors are required for these two resistors. A value of .01 μF is suitable for each.



TL/F/5182–9

FIGURE 6. Pulse Gate Controls



TL/F/5182–10

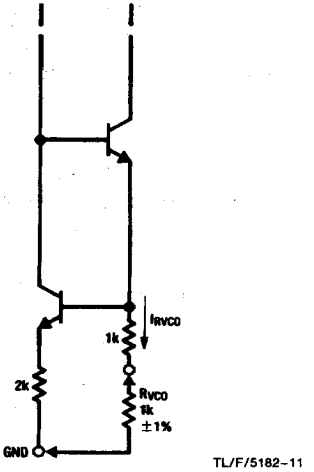
FIGURE 7. I_{RATE} Set and I_{BOOST} Set

VCO

The value of F_{VCO} is fixed at 1 kΩ ±1% in the External Component Limits table. *Figure 8* shows how R_{VCO} is connected to the internal components of the chip. This value was fixed at 1 kΩ to set the VCO operating current such that optimum performance of the VCO is obtained for production device spreads. This means fixed value components will be adequate to set the VCO center frequency for production runs. The value of C_{VCO} can therefore be determined from the VCO frequency f_{VCO}, using the equation: $C_{VCO} = [1/(R_{VCO})(f_{VCO})] - 5$ pF where f_{VCO} is twice the input data rate. As an example, for a 5Mbit/sec data rate, $f_{VCO} = 10$ Mhz, requiring that $C_{VCO} = 95$ pF. The amount of tolerance a particular design can afford on the center frequency will determine the capacitor tolerance. The capacitor is connected to internal circuitry of the chip as shown in *Figure 9*.

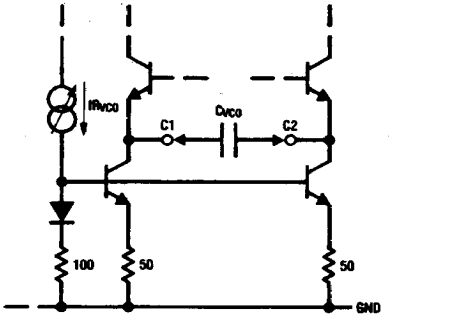
As the data rate increases and C_{VCO} gets smaller, the effects of unwanted parasitic capacitances influence the frequency. As a guide the graph of *Figure 10* shows approximately the value of C_{VCO} for a given data rate.

The center frequency may be checked by applying pulses at the ENCODED DATA input with READ GATE set high. The input frequency should be varied above and below the chosen center frequency until the VCO stops tracking. Typically this will be 20% either side of the center frequency.



TL/F/5182–11

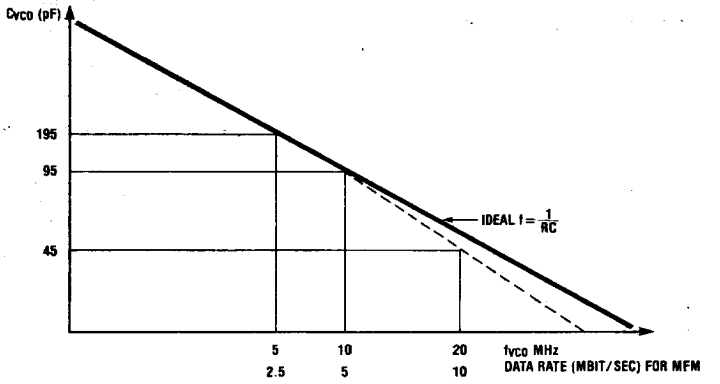
FIGURE 8. VCO Current Setting Resistor



TL/F/5182–12

FIGURE 9. VCO Capacitor

$$C_{VCO} = \left(\frac{1}{R_{VCO}\, f_{VCO}}\right) - 5\ \text{pF}$$



TL/F/5182–13

FIGURE 10. VCO Capacitor Value for Disk Data Rates

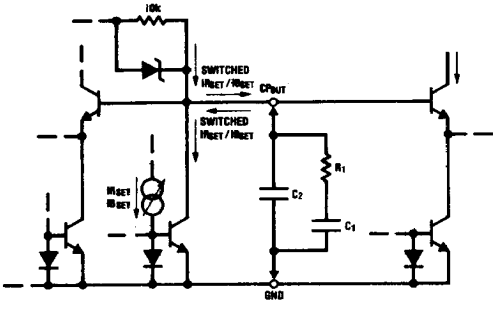
Loop Filter

The input current into the Buffer Amplifier is offset by a matched current out of the Charge Pump, and even so is much less than the switching current in or out of the Charge Pump. It can therefore be assumed that all the Charge Pump switching current goes into the Loop Filter components R_1 and C_1 and C_2. The tolerance of these components should be the same as R_{RATE} and R_{BOOST}, and will determine the overall loop gain variation. The three components connected to the Charge Pump output are shown in *Figure 11*. Note the return current goes to analog GND, which should be electrically very close to the GND pin itself.

The value of capacitor C_1 basically determines loop stability the larger the value the longer the loop takes to respond to an input change. If C_1 is too small, the loop will track any jitter on the ENCODED DATA input and the VCO output will follow this jitter, which is undesirable. The value of C_1 should therefore be large enough so that the PLL is fairly immune to phase jitter but not large enough that the loop won't respond to longer term data rate changes that occur on the disk drive.

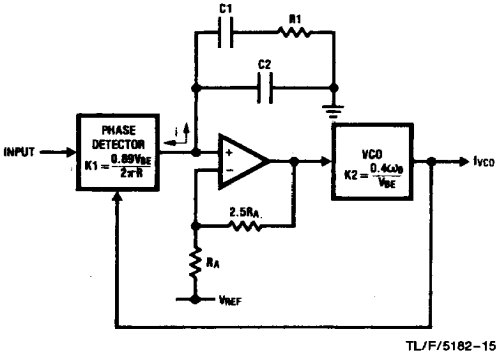
The damping resistor R_1 is required to damp any oscillation on the VCO input that would otherwise occur due to step function changes on the input. A value of R_1 that would give a phase margin of around 45 degrees would be a reasonable starting point.

The main function of the capacitor C_2 is to integrate the effects of the VCO frequency on the VCO input voltage. Typically its value will be less than one tenth of C_1.



TL/F/5182–14

FIGURE 11. Charge Pump Out



TL/F/5182–15

FIGURE 12. Loop Response Components

Figure 12 shows the relevant phase-locked-loop blocks that determine system response, namely the Phase Detector, Filter/Buffer Amplifier, and VCO. The Phase Detector (Phase Comparator and Charge Pump) produces an aggregate output current i which is proportional to the phase difference between the input signal and the VCO signal. The constant

$$(K_1)\ \text{is}\ \frac{.89\ V_{BE}}{2\pi R}\ \text{amps per radian.}$$

R is either R_{RATE} or $R_{RATE} \parallel R_{BOOST}$. This aggregate current feeds into or out of the filter impedance (Z), producing a voltage to the VCO that regulates the VCO frequency. The VCO gain constant is 0.4 ω_{VCO}/V_{BE} radians per second per volt. Under steady state conditions, i will be zero and there will be no phase difference between the input signal and the VCO. Any change of input signal will produce a change in VCO frequency that is determined by the loop gain equation. This equation is determined from the gain constants K_1, A and K_2 and the filter v/i response.

The impedance Z of the filter is:

$$\frac{1}{sC_2} \parallel \left(\frac{1}{sC_1} + R_1\right) = \frac{1 + sC_1R_1}{sC_1\left(1 + \frac{C_2}{C_1} + sC_2R_1\right)}$$

If $C_2 \ll C_1$ then the impedance Z approximates to:

$$\frac{1 + sC_1R_1}{sC_1\,(1 + sC_2R_1)}$$

The overall loop gain is then $G(s) = \frac{K_1AK_2}{s} \times \frac{1+sC_1R_1}{sC_1(1+sC_2R_1)}$

The Overall Closed Loop Gain is:

$$\frac{\phi_{OUT}}{\phi_{IN}} = \frac{G_{(K)}\,F(s)}{s + G_{(K)}\,F(s)}$$

Let $G_{(K)} = K_1\,A\,K_2$

$$F(s) = \frac{1+SC_1R_1}{SC_1\,(1+SC_2R_1)}$$

Substituting, We Get

$$\frac{\phi_{OUT}}{\phi_{IN}} = \frac{G_{(K)}\,(SC_1R_1+1)}{S^3\,R_1\,C_1\,C_2 + S^2\,C_1 + GK\,(SC_1R_1+1)}$$

$$= \frac{(G_{(K)}/C_1)(SR_1C_1+1)}{S^3R_1C_2+S^2+SG_{(K)}R_1+G_{(K)}/C_1}$$

If $C_2 << C_1$, we can ignore the 3rd Order Component introduced by C_2 then:

$$\frac{\phi_{OUT}}{\phi_{IN}} = \frac{(G_{(K)}/C_1)(SR_1C_1+1)}{S^2+SG_{(K)}R_1+G_{(K)}/C_1}$$

This is a second Order Loop and can be solved as follows:

$$S^2 + SG_{(K)}R_1 + G_{(K)}/C_1 = S^2 + 2\delta\,\omega_nS + \omega_n{}^2$$

$$\therefore\ C_1 = \frac{G_{(K)}}{\omega_n{}^2}$$

$$R_1 = \frac{2\delta\omega_n}{G_{(K)}}$$

$\delta = 0.707$ For Critically Damped Response

From the above equations:

$$\omega = \sqrt{\frac{G(K)}{C1}}$$

$$G(K) = K1 \times A \times K2 =$$

$$\frac{0.89V_{BE}}{2\pi R} \times \frac{0.4\omega V_{CO}}{V_{BE}} \times 3.5$$

MFM encoded data has a two to one frequency range within the data field. The expression

$$K = \frac{0.89V_{BE}}{2\pi R}$$

is valid when the MFM data pattern is at its maximum frequency. In order to make this equation more general, it may be written as follows:

$$K = \frac{1.78V_{BE}}{2\pi RN}$$

where N is defined as the V_{CO} frequency divided by the encoded data frequency, or, N is equal to

$$\frac{F_{VCO}}{F_{DATA}}$$

(N = 2 for maximum data rate and N = 4 for minimum data rate). Now G(K) can be written as follows:

$$G(K) = \frac{1.78V_{BE}}{2\pi RN} \times \frac{0.4\omega_{VCO}}{V_{BE}} \times 3.5 = \frac{2.5F_{VCO}}{RN}$$

$$\omega n = \sqrt{\frac{2.5F_{VCO}}{C1RN}}$$

$R = R_{RATE}$ in the low track rate

$R = R_{RATE} // R_{BOOST}$ in the high track rate

From the above equations:

$$\omega n = \frac{R1 \times G(K)}{2\delta}$$

$$G(K) = C1(\omega n^2)$$

$$\delta = \text{eta (damping factor)} = \frac{R1 \times \omega n \times C1}{2}$$

The damping factor should approach, but not fall below, 0.5 when ωn is minimum. Response to bit shift is minimized when the damping factor is small; however, if the damping factor drops much below 0.5, the system tends to be oscillatory (underdamped).

Additionally, loop performance is poor (excessive phase acquisition times) if the damping factor becomes significantly greater than 1.0. Any increase in loop bandwidth (due to R decreasing in the high track rate) produces a proportional increase in the damping factor, and this should be limited to the point where the maximum damping factor does not significantly exceed 1.0. With the damping factor range established, loop design can now proceed.

A 1550 Krads/sec bandwidth in the non read mode results in a wide capture range; a 4% frequency difference between the crystal and recorded data would not cause an acquisition problem. (This bandwidth may seem excessive to some and if the user does not think it is necessary, he may design his filter with a more desirable bandwidth. For an in-depth discussion of this point, it is suggested that the applicaton note "Phase Locked Loop Filter Design For Disk Data Separators" be read.)

This design example assumes that the SET PLL LOCK pin is tied to the PLL LOCK DETECTED pin. This results in the track rate being switched from high to low after two bytes of preamble are detected. As an alternative, the SET PLL LOCK pin may be tied to an inverted READ GATE signal, resulting in the track rate switching immediately to low when READ GATE is asserted. This is discussed further in the above mentioned application note.

In the non read mode or high track rate.

$$\omega n = \sqrt{\frac{2.5F_{VCO}}{C1RN}}$$

Choose $R = R_{RATE} // R_{BOOST} = 425$

In the non-read mode N = 2

$$1550 \text{ Krads/sec} = \sqrt{\frac{2.5 \times 10^7}{C1 \times 425 \times 2}}$$

$$C1 = 0.012\ \mu F$$

In the preamble, after two bytes are detected and PLL LOCK DETECT goes low

$$\omega n = \sqrt{\frac{2.5F_{VCO}}{C1RN}}$$

$R = R_{RATE} = 850$

N = 2

ωn = 1107 Krads/sec

Again, in the data field, the minimum data frequency is equal to one half the preamble frequency. This means that N = 4 in the bandwidth equation. This reduces the bandwidth to:

$$\omega n(\text{min}) = \frac{1}{\sqrt{2}} \times 1107 \text{ Krads/sec} = 783 \text{ Krads/sec}$$

Before, we stated that the minimum value of d should be 0.5; knowing ωn(min) we can now solve for R1

$$\delta = \omega n \times R1 \times C1 \times \tfrac{1}{2}$$

choose δ(min) = 0.55

$$R1 = \frac{2\delta}{\omega n \times C1}$$

R1 = 117 choose 120

The maximum damping value occurs in the high track rate;

$$\delta(\text{max}) = \omega n(\text{max}) \times R1 \times \frac{C1}{2}$$

$$= 1550 \text{ Krads/sec} \times 120 \times \frac{0.012\ \mu F}{2}$$

δ(max) = 1.12

The maximum damping value in the read mode is as follows:

$$\delta(\text{max-read}) = 1107 \text{ Krads/sec} \times 120 \times \frac{0.012\ \mu F}{2}$$

δ(max-read) = 0.80

The continuous behavior (non-quantized) approximation used to predict loop performance assumes that the phase detector output is constantly proportional to the input phase difference. In reality, the phase detector output is a pulse applied for a period of time equal to the phase difference. The function of C2 is to smooth the phase detector output (VCO control voltage) over each cycle. C2 also adds a second pole to the filter transfer function. This pole should be far enough outside the loop bandwidth (at least one order of magnitude) that its phase and amplitude contribution is negligible in the loop bandwidth. If:

$$C2 = \frac{C1}{50} = 240 \text{ pF choose } 300 \text{ pF}$$

The final loop component is R_{BOOST}. Since R_{RATE} and the parallel combination of R_{RATE} and R_{BOOST} are known, we can calculate R_{BOOST}.

$$R_{BOOST} = \frac{(Rp)\ (R_{RATE})}{(R_{RATE} - Rp)} = 850$$

The above filter values and those for other bandwidths are listed on following page.

Data Rate (NRZ)	Non-Read ωn(max) rads/sec	δ	Read ωn(min) rads/sec	δ	Charge Pump[1] R_{RATE} ohms	R_{BOOST} ohms	Loop Filter[2] R1 ohms	C1 μF	C2 pF
5 Mbit/sec	1550k	1.12	783k	0.55	850	850	120	0.012	300
5 Mbit/sec	903k	0.99	435k	0.48	1500	1300	100	0.022	390
5 Mbit/sec	659k	1.55	248k	0.52	1500	590	69	0.068	1500

1. Component tolerances are system dependent; they depend on how much loop gain deviation can be tolerated.
2. Component tolerances are typically 5% but they depend on the amount of Loop Bandwidth tolerance that can be accepted.

The calculated values are only a guide, the user should then empirically test the loop and determine stability, lock-on time, jitter tolerance, etc.

The desired Bode plot of gain and phase is shown in *Figure 13*, with 20-dB/decade slope at ω_0 for stability at unity gain.

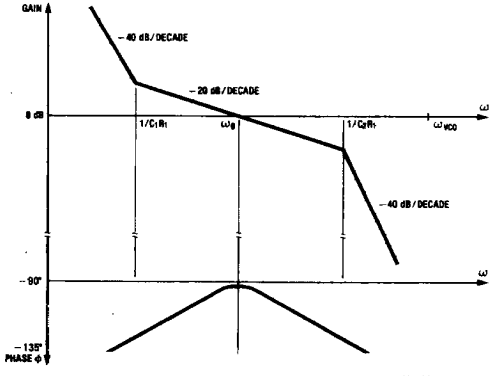
Note that capacitor C_2 affects the amount by which the Charge Pump switching current affects the filter voltage. Obviously as C_2 is increased in value ripple will decrease, but the closer the −40dB/decade slope gets to ω_0 on the Bode plot the more unstable the loop will be. Thus if C_2 is made too large the loop will oscillate.

Resistor R_1 determines where the low-frequency end −40 dB/decade slope changes into the −20 dB/decade slope. The wider the −20 dB/decade slope is around unity gain, the more stable the loop becomes. If R_1 is too large it will reduce the impact of C_1, while too small a value will increase instability. The capacitor C_1 strongly effects the response of the loop. Too high a value will slow down the response time, but make the PLL less prone to jitter or frequency shift whereas too low a value will improve response time while tending to increase the PLL's reaction to jitter.

Other filter combinations may be used, other than R_1 in series with C_1, all in parallel with C_2. For example the filter shown in *Figure 14* will also perform similarly, and in fact for some systems it will yield superior performance.

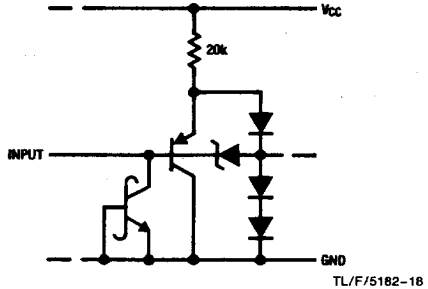
DIGITAL CONNECTIONS TO THE DP8460

Figure 17 shows a connection diagram for the DP8460 in a typical application. All logic inputs and outputs are TTL compatible as shown in *Figure 15* and *16*. The VCO CLOCK output is 74AS compatible and can therefore drive up to 40 74AS (or 74F) inputs, or 10 74S inputs, or 100 74ALS inputs, or 50 of 74LS inputs. All other outputs are 74ALS compatible and so will drive up to 16 74AS inputs, or 4 74S inputs, or 40 74ALS inputs or 20 74LS inputs. All inputs are 74ALS compatible and therefore can be driven easily from any 74 series devices. The raw MFM from the pulse detector in the drive is connected to the ENCODED DATA input.



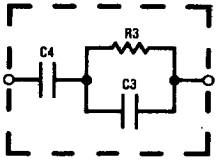
TL/F/5182–16

FIGURE 13. Bode Plot of Loop Response



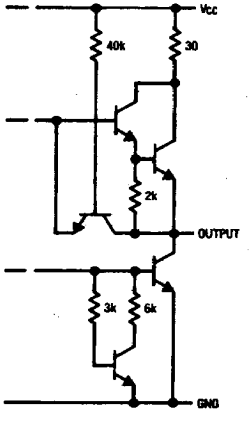
TL/F/5182–18

FIGURE 15. Logic Inputs



TL/F/5182–17

FIGURE 14. Alternate Loop Filter Configuration



TL/F/5182–19

FIGURE 16. Logic Outputs

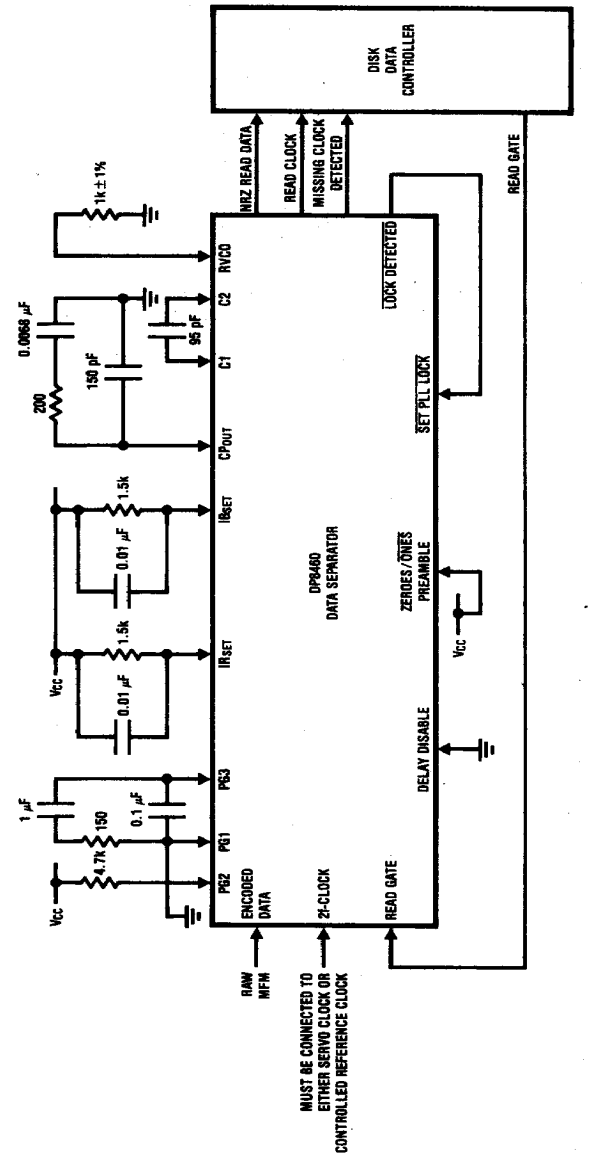


FIGURE 17. Typical Connection to DP8460 for:
1) MFM Data Input, 5Mbit/sec Data Rate
2) 32 Bit Delay to Enable
3) All Zeroes (NRZ) Preamble

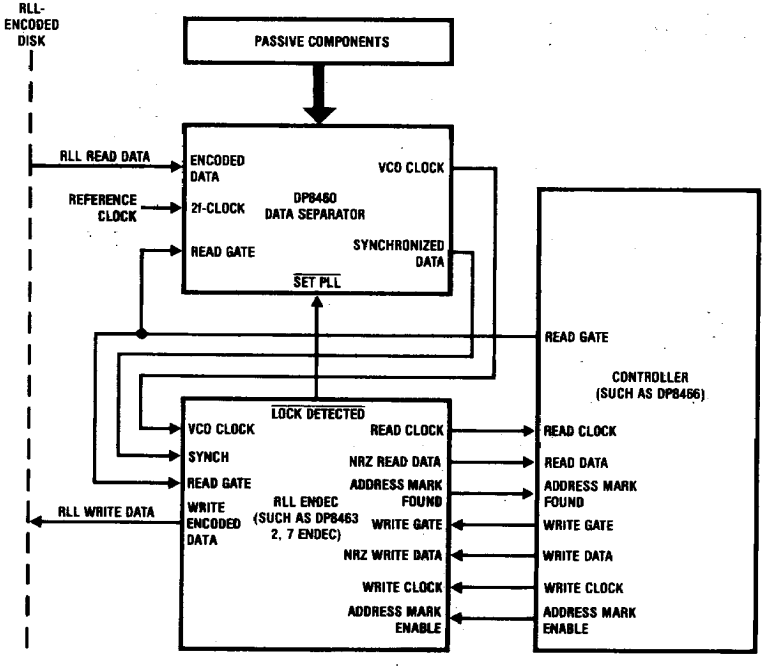
The DELAY DISABLE input determines whether attempting lock-on will begin immediately after READ GATE is set or after 2 bytes. Typically in a hard-sectored drive, READ GATE is set active as the sector pulse appears, meaning a new sector is about to pass under the head. Normally the preamble pattern does not begin immediately, because gap bytes from the preceding sector usually extend just beyond the sector pulse. Allowing 2 bytes to pass after the sector pulse helps ensure that the PLL will begin locking on to preamble, and will not be chasing non-symmetrical gap bits. Attempting to lock-on to a fixed . . . .1010. . . . preamble pattern speeds up lock-on, and after another two bytes the PLL will nominally have locked-on. Thus DELAY DISABLE should be set low for this kind of disk drive.

For soft sectored drives, the controller normally will not wait for the index pulse before it attempts lock-on, so that READ GATE may go active at any time. Chances are the head will not be over a preamble field and therefore there is no need to wait 2 bytes before attempting lock-on. DELAY DISABLE can therefore be set high. If a non-preamble field is passing by as READ GATE goes active, the DP8460 will not indicate lock, and no data decoding will occur nor will MISSING CLOCK DETECTED go active. Normally, if lock-on has not been achieved after a certain time limit, the controller will de-activate READ GATE and then try again.

For MFM encoded disk drives, the $\overline{\text{LOCK DETECTED}}$ output will be connected back to the $\overline{\text{SET PLL LOCK}}$ input. As the PLL achieves lock-on, the DP8460 will automatically switch to the slower tracking rate and decoded data will appear at the NRZ READ DATA output. Also the READ CLOCK output will switch from half the 2f-clock frequency to the disk data rate frequency. If a delay is required before the changeover occurs, a time delay may be inserted between the two pins.

Some drives have an all-ONES data preamble instead of all-ZEROES and the DP8460 must be set to the type being used before it can properly decode data. The ZEROES/$\overline{\text{ONES}}$ PREAMBLE input selects which preamble type the chip is to lock-on to.

If the drive uses a run-length-limited (RLL) code such as '2, 7', instead of MFM, the phase-locked-loop function of the DP8460 may still be used. *Figure 18* shows how the DP8460 may be connected to a RLL ENDEC circuit. The RLL ENDEC performs encoding of NRZ data to RLL encoded data, and RLL encoded data back to NRZ data. The RLL ENDEC can use the SYNCHRONIZED DATA output of the DP8460 along with VCO CLOCK to lock-on to the preamble and then decode data. Once lock-on has been detected, the RLL ENDEC can set the $\overline{\text{SET PLL LOCK}}$ input of the DP8460 low so that the tracking rate can be changed.



TL/F/5182–21

FIGURE 18. DP8460 with Run-Length-Limited (RLL) Codes

APPLICATIONS OF THE DP8460 DATA SEPARATOR

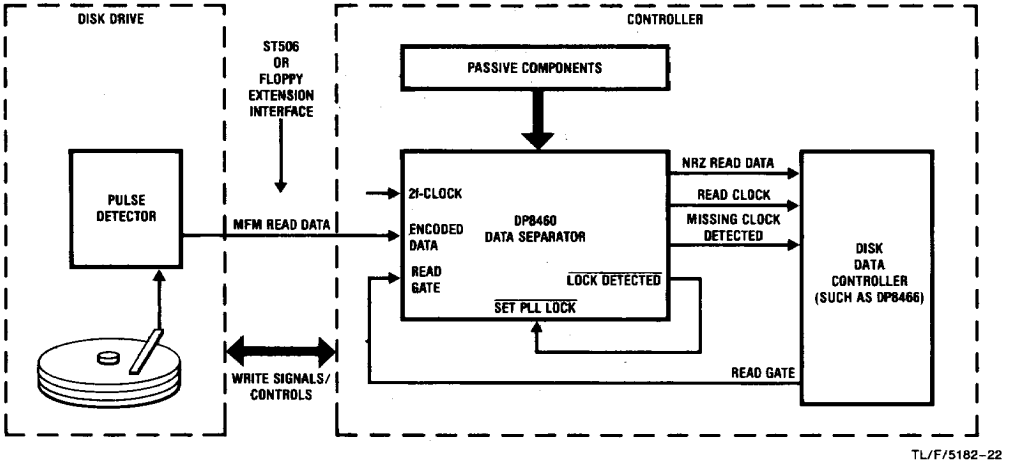
The DP8460 is the first integrated circuit to place on one chip a PLL with features that offer the improved speed and reliability required by the disk industry. Not only does the chip simplify disk system design, but also provides fast lock-on to the incoming preamble. Once locked on, the loop is set into a more stable mode. This inherent loop stability allows for a sizeable amount of jitter on the data stream, such as is encountered in many disk systems. Once in the stable tracking rate, the SYNCHRONIZED DATA output represents the incoming ENCODED DATA and is synchronous with VCO CLOCK. If the disk is MFM encoded, then the chip can decode the synchronized data into NRZ READ DATA and READ CLOCK. These are available as outputs from the chip allowing the NRZ READ DATA to be deserialized using the READ CLOCK.

The DP8460 is capable of operating at up to 15Mbits/sec data rates and so is compatible with a wide assortment of disk drives. The faster data rates of the 8-inch and 14-inch disk drives will mandate the selection of either the DP8460–3 or –2 parts with their narrower window margins on the incoming data stream. This will also be the case when 5¼-inch drives achieve higher data rates. Some 8-inch and 14-inch disk drives incorporate the functions of the DP8460, but use many discrete ICs. In these cases, replacing these components with the DP8460 will offer reduced P.C. board area, lower cost, and improved performance while simplifying circuit testing.

Most 5¼-inch and many 8-inch and 14-inch disk drives manufactured at present do not incorporate any of the functions of the DP8460. This is so primarily because the PLL function is difficult to design and implement and requires circuitry which covers a large area of the printed circuit card. This is undesirable both from the drive size aspect and from the cost aspect (the cost includes soldering, testing, and adjusting the components). Consequently, most smaller disk drives output MFM encoded data so that the phase-locked-loop and data separation have to be performed by the controller. The DP8460 will therefore replace these functions in controller designs, as shown in *Figure 19*.

System design criteria may now change because the DP8460 is a one-chip solution, requiring only a few external passive components with fixed values. It operates from a +5V supply, consumes about 0.5W, and is housed in a narrow 24-pin package. The circuitry has been designed so that the external resistors and capacitors need not be adjustable; the user chooses the values according to the disk drive requirements. Once selected, they will be fixed for that particular drive type. These features make it possible to transfer these functions to the disk drive, as shown in *Figure 20*. Apart from a slight increase in board area, the advantages outweigh the disadvantages. First, the components selected are fixed for each type of drive and this facilitates the problem of interchangeability of drives. At present, controllers are adjusted to function with each specific drive; with the DP8460 in the drive, component adjustment will no longer be required. Second there is often a problem of reliability of data transfer. Because the MFM data is clock encoded, this signal is susceptible to noise, bit shift, etc. Soft errors will sometimes occur when the incoming disk data bit position is outside the Pulse Gate window as it is being synchronized to the VCO clock in the phase-locked-loop. Obviously, the nearer the PLL is to the MFM source, the less chance there is that errors will occur. Thus placing the DP8460 in the drive will increase the reliability of data transfer within the system.

A third advantage is data rate upgrading. Most 5¼-inch drives have 5Mbit/sec data rate because the early drives were made with this data rate. This meant the controllers had to be designed with PLLs which operate at this data rate. It is therefore difficult for drive manufacturers to introduce new drives that are not compatible with existing controllers. Since no new standard data rate has emerged, they must continue to produce drives at this data rate to be compatible with the controllers on the market. With the DP8460 in the drive, and its associated components set for the drive's data rate, it no longer becomes a problem to increase the data rate, assuming the controllers digital circuitry can accommodate the change. This will allow the manufactures to increase the bit density and therefore the capacity of their drives.



TL/F/5182–22

FIGURE 19. DP8460 In the Controller

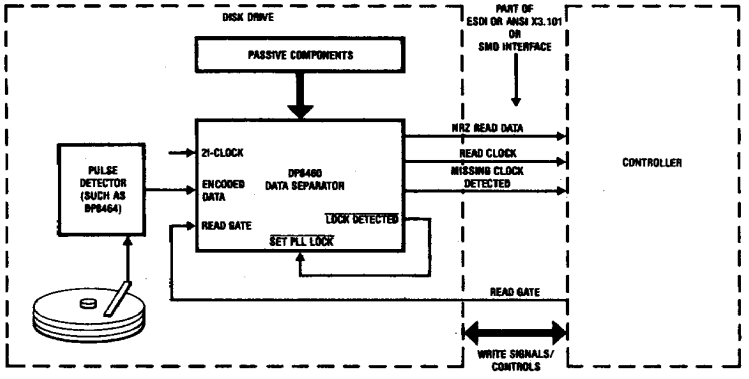


FIGURE 20. DP8460 in the Disk Drive

PRECAUTIONS IN BREADBOARDING AND PCB LAYOUT

The DP8460 contains a high performance analog PLL and certain precautions must be taken when breadboarding or designing a PCB layout. The following guidelines should be adhered to when working with the DP8460:

1) Do not wire wrap.
2) Keep component lead lengths short, place components as close to pins as possible.This applies to R1, C1, R2, C_{VCO}, R_{RATE}, R_{BOOST}, C_{RATE}, C_{BOOST}, RPG1, RPG2, and CPG1.
3) Provide a good ground plane and use a liberal amount of supply bypassing. The quieter a PLL's environment, the happier it is.
4) Avoid routing any digital leads within the vicinity of the analog leads and components.

We have used a PC board approach to breadboarding the DP8460 that gives us an excellent ground plane and keeps component lead lengths very short. With this setup we have found very stable and reliable operation. Illustrations of component layout is shown in *Figure 21*. Note that the board layout is a recommendation not a requirement.

ADDITIONAL NOTES

1. PG1 should be grounded to improve noise immunity.
2. 2F clock must be applied at all times; without the 2F clock, the pulse gate circuitry will not operate properly making it impossible to lock onto the incoming data stream.
3. The programming capacitor for the V_{CO} can be calculated as:

$$C_{VCO} = 1/(f_{VCO} * R_{VCO}) - 5\ pF$$

The 5 pF value is due to parasitic and pin to pin capacitance.

4. Care must be taken in final PC board layout to minimize pin to pin capacitance, particularly in multi-layer printed circuit boards.
5. Additional design information is available in the application note "Designing with the DP8460", Dec. 1984. It provides simple solutions to potential application problems.

DP8460 Data Separator Pin Connection Diagram

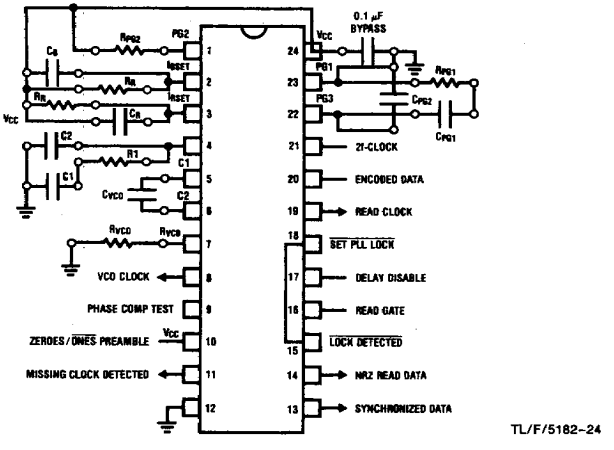


FIGURE 21. Recommended Component Layout