National Semiconductor

PRELIMINARY
February 1994

DP84650R/DP84651R/DP84652R Read/Multiwrite™ Preamplifiers

General Description

The DP84650R/1R/2R devices are 5V, high performance, two or four channel, low power, read preamplifiers/write current drivers designed for two-terminal recording head applications. An idle mode is available which conserves power to a level of 0.5 mW (typically) when activated. The device can be switched into a Multiwrite™ mode, allowing all channels to write at the same time. The write data inputs for the DP84650R have been designed to accept both PECL and TTL inputs for maximum user flexibility. Power supply fault protection is included to disable the write current generator whenever the supply voltage is below 4V.

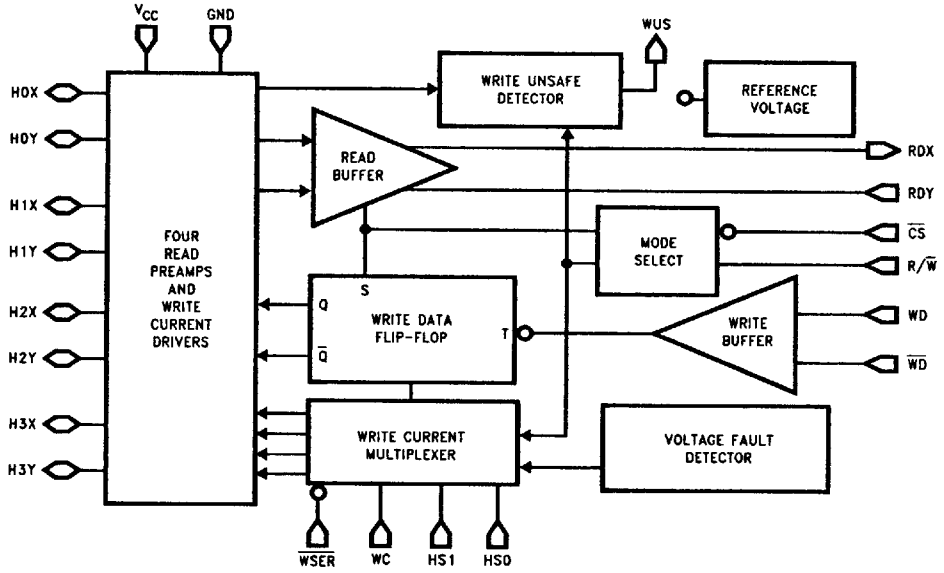
A mirror image pinout for the DP84651R is available to simplify flex circuit layout in multiple disk head applications.

Upon request, other options such as different read gain, damping, and packaging are available.

Features

- Low input capacitance: 12 pF typical
- Low input noise: 0.49 nV/$\sqrt{\text{Hz}}$ typical
- Low power: 100 mW typical in read mode
- Very low idle power: 0.5 mW typical
- TTL and PECL compatible WD input
- Programmable write current source (1–40 mA)
- Low power supply protection in write mode
- Head short to ground protection
- DP84650RM-4/2 are plug compatible to VTC VM7154/7152
- Single 5V power supply

Circuit Block Diagram



TL/F/11947–1

Multiwrite™ is a trademark of National Semiconductor Corporation.

 TL/F/11947

RRD-B20M24/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	7V
Digital Input Voltage	−0.3 to (V_{CC} + 0.3)V
Maximum Head Port Voltage	−0.3 to (V_{CC} + 0.3)V
Maximum Output Current (RDX, RDY)	−10 mA
Maximum Output Write Current	60 mA
ESD Susceptibility (Note 2)	2000V
Storage Temperature Range	−65°C to +150°C

Note 1. Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" tables are not guaranteed at these ratings. The Recommended Operating Conditions table will define the conditions for actual device operation.

Note 2. Human body model is used. (120 pF through 1.5 kΩ)

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.5	5	5.5	V
Operating Free Air Temperature Range (T_A)	0		70	°C

DC Electrical Characteristics

Guaranteed over operating conditions (see table) unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units	Test
I_{CCR}	Supply Current (Read Mode)	$\overline{CS}$ = LOW, R/$\overline{W}$ = HIGH		20	28	mA	(Note A)
I_{CCW}	Supply Current (Write Mode)	$\overline{CS}$ = R/$\overline{W}$ = LOW, $\overline{WSER}$ = HIGH		20 + 1.1(I_W)	27 + 1.1(I_W)	mA	(Note A)
I_{CCI}	Supply Current (Idle Mode)	$\overline{CS}$ = HIGH		0.1	0.2	mA	(Note A)
I_{CCS}	Supply Current (Multiwrite Mode)	$\overline{CS}$ = R/$\overline{W}$ = LOW, $\overline{WSER}$ = LOW		40 + 4.3(I_W)	60 + 4.3(I_W)	mA	(Note A)
PD_R	Power Dissipation (Read Mode)	$\overline{CS}$ = LOW, R/$\overline{W}$ = HIGH		100	154	mW	(Note A)
PD_W	Power Dissipation (Write Mode)	$\overline{CS}$ = LOW, R/$\overline{W}$ = LOW		100 + 5.5(I_W)	150 + 6(I_W)	mW	(Note A)
PD_I	Power Dissipation (Idle Mode)	$\overline{CS}$ = HIGH		0.5	1.1	mW	(Note A)
PD_S	Power Dissipation (Multiwrite Mode)	$\overline{CS}$ = R/$\overline{W}$ = LOW, $\overline{WSER}$ = LOW		200 + 22(I_W)	330 + 24(I_W)	mW	(Note A)
$V_{IH(TTL)}$	TTL Input High Voltage		2		V_{CC} + 0.3	V	(Note A)
$V_{IL(TTL)}$	TTL Input Low Voltage		−0.3		0.8	V	(Note A)
$I_{IH(TTL)}$	TTL Input High Current		−100		100	μA	(Note A)
$I_{IL(TTL)}$	TTL Input Low Current		−100		100	μA	(Note A)
$V_{IH(WD)}$	PECL Input High Voltage	DP84650R only	V_{CC} − 1		V_{CC} − 0.7	V	(Note A)
$V_{IL(WD)}$	PECL Input Low Voltage	DP84650R only	V_{CC} − 1.9		V_{CC} − 1.6	V	(Note A)
$I_{IH(WD)}$	PECL Input High Current	DP84650R only		40	100	μA	(Note A)
$I_{IL(WD)}$	PECL Input Low Current	DP84650R only		30	80	μA	(Note A)

Note 1. Typical values are specified at 25°C and 5V supply.

Note A. This parameter is guaranteed by outgoing testing.

AC Electrical Characteristics

Guaranteed over operating conditions (see table) unless otherwise specified.
I_W = 20 mA, L_h = 1 μH, R_h = 30Ω and f(data) = 5 MHz unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units	Test
td_{RW}	Time Delay Switching from Read to Write Modes	R/$\overline{W}$ Transition to 90% of Write Current, I_W > 5 mA			0.35	μs	(Note A)
td_{RWL}	Time Delay Switching from Read to Write Modes	R/$\overline{W}$ Transition to 90% I_{WRITE}, 1 mA < I_W < 5 mA			2	μs	(Note A)
td_{WR}	Time Delay Switching from Write to Read Modes	R/$\overline{W}$ Transition to 90% of 100 mV Read Signal Envelope			1	μs	(Note A)
td_{SELECT}	Time Delay Switching from Idle to Either Read or Write Modes	$\overline{CS}$ Negative Transition to 90% I_{WRITE} or 90% of 100 mV, 10 MHz Signal Envelope			0.6	μs	(Note A)
td_{IDLE}	Time Delay Switching from Either Read or Write to Idle Mode				0.6	μs	(Note A)
td_{HEAD}	Time Delay Switching from One Head to Another	HS0/HS1 to 90% of 100 mV, 10 MHz Read Signal Envelope			0.6	μs	(Note A)
td_{UNSAFE}	WUS Safe to Unsafe Write Condition Delay Time	WD Negative Transition to WUS Positive Transition	1	2	3.6	μs	(Note A)
td_{SAFE}	WUS Unsafe to Safe Write Condition Delay Time	WD Negative Transition to WUS Negative Transition			0.6	μs	(Note A)
td_{HDI}	Time Delay from WD to a Current Direction Change in a Head Output	Measurements Made from 50% Points, L_h = 0		10	20	ns	(Note A)
ASY_{HD}	Head Current Asymmetry	WD has 1 ns $t_{r/f}$ Times, L_h = 0			0.5	ns	(Note B)
$t_{r/f(HD)}$	Head Current Rise and Fall Times	Measurements Made from 10%–90% Points, L_h = 0			6	ns	(Note B)
$t_{r/f(loaded)}$	Head Current Rise and Fall Times	Measurements Made from 10%–90% Points		10	16	ns	(Note B)

Note 1. Typical values are specified at 25°C and 5V supply.

Note A. This parameter is guaranteed by outgoing testing.

Note B. The limit values have been determined by characterization data. No outgoing tests are performed.

DC and AC Electrical Characteristics

READ MODE guaranteed over operating conditions (see table) unless otherwise specified. Read characteristics: C_L (RDX, RDY) < 20 pF, R_L (RDX, RDY) = 1 kΩ

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units	Test
A_V	Differential Voltage Gain	V_{IN} = 1 mV_{PP} @ 1 MHz (Note 2)	250	300	350	V/V	(Note A)
V_N	Input Noise Voltage	BW = 15 MHz, $L_h = R_h = 0$		0.49	0.65	$nV/\sqrt{Hz}$	(Note B)
C_I	Differential Input Capacitance	V_{IN} = 1 mV_{PP}, f = 5 MHz		12	17	pF	(Note B)
R_I	Differential Input Resistance	f = 5 MHz, V_{IN} = 1 mV_{PP}	720	1250		Ω	(Note A)
V_{IRANGE}	Input Voltage Dynamic Range	f = 5 MHz, (Note 3)	4	6		mV_{PP}	(Note A)
$V_{O(OFF)}$	Output Offset Voltage		−150		150	mV	(Note A)
$R_{O(SE)}$	Single Ended Output Resistance	f = 5 MHz			40	Ω	(Note B)
I_{OUT}	Output Current	AC Coupled Load, RDX to RDY	1.5	2		mA	(Note A)
$V_{O(CM)}$	Common Mode Output Voltage at RDX, RDY Pins		2	V_{CC} − 2.4	3.5	V	(Note A)
BW_{1dB}	Voltage Bandwidth—1 dB	V_{IN} = 1 mV_{PP}, Z_{source} < 5Ω	40	60		MHz	(Note B)
BW_{3dB}	Voltage Bandwidth—3 dB	V_{IN} = 1 mV_{PP}, Z_{source} < 5Ω	80	100		MHz	(Note B)
CMRR	Common Mode Rejection Ratio	V_{CM} = 100 mV_{PP} @ 5 MHz	60	90		dB	(Note A)
PSRR	Power Supply Rejection Ratio	ΔV_{CC} = 100 mV_{PP} @ 5 MHz	60	90		dB	(Note A)
CSRR	Channel Separation	Unselected Channel 100 mV_{PP}	50	60		dB	(Note A)

Note 1. Typical values are specified at 25°C and 5V supply.

Note 2. Various gain options exist from 160 to 300. See order information.

Note 3. The dynamic input voltage range limit is defined as the point where the gain falls to 90% of its small signal gain value.

Note A. This parameter is guaranteed by outgoing testing.

Note B. The limit values have been determined by characterization data. No outgoing tests are performed.

DC and AC Electrical Characteristics

WRITE MODE guaranteed over operating conditions (see table) unless otherwise specified. Write characteristics: I_W = 20 mA, L_h = 1 μH, R_h = 30Ω

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units	Test
K_W	Write Current Constant	$K_W = A_{WC} \times V_{WC}$	46	50	54	V	(Note A)
K_{WI}	Write Current Constant	DP84651R only	23	25	27	V	(Note A)
A_{WC}	I_{WC} to I_{HEAD} Current Gain	R_H = 40Ω	18.4	20	21.6	mA	(Note A)
I_{HM}	Write Current Matching	I_H = 20 mA, R_H = 40Ω, (Note 2)	−10		+10	%	(Note A)
V_{WC}	Write Current Pin Voltage	1 mA < I_W < 40 mA	2.3	2.5	2.7	V	(Note A)
V_{WCI}	Write Current Pin Voltage	DP84651R only	1.15	1.25	1.35	V	(Note A)
V_H	Differential Head Voltage Swing		5	6.5		V_{PP}	(Note A)
$I_{H(NS)}$	Unselected Head Current	I_H = 20 mA			100	μA	(Note A)
R_{DAMP}	Damping Resistance			300		Ω	(Note A)
I_H	Head Write Current Range	(Note 3)	1		40	mA	(Note A)
V_{CCF}	V_{CC} Shut-Off Voltage	I_W < 0.2 mA	3.6		4.2	V	(Note A)
V_{OLWUS}	WUS Low Level Output Voltage	I_{LOAD} < 2 mA			0.5	V	(Note A)
I_{LKWUS}	WUS High Level Output Leakage Current	$V_{OH} = V_{CC}$			100	μA	(Note A)
C_D	Differential Head Load Capacitance				15	pF	(Note B)
f_W	WD Transition Frequency		1			MHz	(Note A)
$t_{PWH(WD)}$	WD Pulse Width (HIGH)		5			ns	(Note B)
$t_{PWL(WD)}$	WD Pulse Width (LOW)		5			ns	(Note B)

Note 1. Typical values are specified at 25°C and 5V supply.

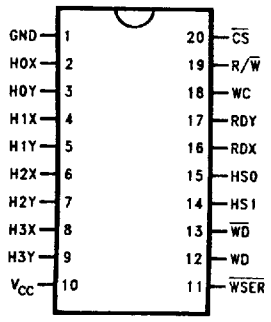
Note 2. Write current matching applies between any two heads and for both Multiwrite and normal write operating modes

Note 3. The capability to Multiwrite at high write currents is dependent upon the supply impedance. It is advisable to decouple the device supply pins for maximum performance in the Multiwrite mode.

Note A. This parameter is guaranteed by outgoing testing.

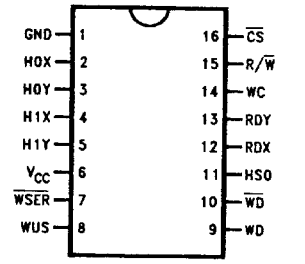
Note B. The limit values have been determined by characterization data. No outgoing tests are performed.

Connection Diagrams



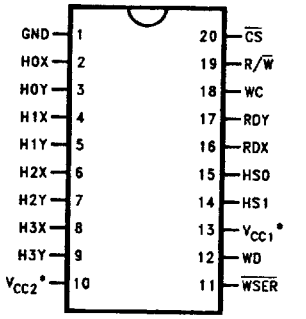
TL/F/11947–2

DP84650R (4-Channel)
See NS Package Number M20B or MSA20



TL/F/11947–3

DP84650R (2-Channel)
See NS Package Number M16B



TL/F/11947–4

DP84651R/652R
See NS Package Number M20B or MSA20

*V_{CC1} not internally shorted to V_{CC2}

Pin Descriptions

Name	Type	Description
V_{CC}	Power Supply	Power supply pin (5V ±10%)
WD, $\overline{WD}$	Input (PECL or TTL)	These differential ECL inputs (PECL) control the direction of current flow through the XY head connections. A negative transition on WD toggles the head current between the X and Y head connections. If $\overline{WD}$ is not used (floated or low), then WD functions with TTL voltage levels.
HS0, HS1	Input (TTL)	Logic levels are applied to these pins to select 1 of 4 heads (see Table II).
R/$\overline{W}$	Input (TTL)	A logic high level selects the read mode while a low logic level selects the write mode. The $\overline{CS}$ pin must be at a low logic level for this operation to be active (see Table III).
$\overline{CS}$	Input (TTL)	A high logic level disables the operation of the device and puts the read data outputs (RDX, RDY) into a high impedance state.
H0X, H0Y through H3X–H3Y	Outputs	X and Y connections to the read/write heads.
$\overline{WSER}$	Input (TTL)	The logic level on this pin selects between the Multiwrite mode and the standard write mode. When at a logic high or open circuit, the device functions in a normal write mode with the selected head controlled by the HS0 and HS1 pins. When at a logic low, all four heads will write at one time, irrespective of the levels on the HS0 and HS1 pins. This pin is only active in the write mode.
RDX, RDY	Output	Differential read data outputs.
WC	Output	A resistor is connected from this pin to ground to control the magnitude of the write current (see formula in WRITE MODE description).
WUS	Output (TTL)	A low level voltage indicates a safe writing condition exists. Since this is an open collector output, a pull-up resistor (to V_{CC}) is required for proper operation.
GND	Ground	Device ground.

Basic Circuit Operation

The DP84650R/651R/652R can address up to four two-terminal thin-film or metal-in-gap (MIG) heads, providing the write current drive in the write mode or read data amplification in the read mode.

Head selection is controlled by the logic states on two pins, HEAD SELECT 0 (HS0) and HEAD SELECT 1 (HS1). Table II defines the results of each combination of these two pins. These pins have internal pull-down current so that head 0 is selected if an open condition exists on these pins.

TABLE II. Head Selection

HS1	HS0	Head Selected
0	0	0
0	1	1
1	0	2
1	1	3

The selection of device mode (write, read or idle) is also controlled by two pins, CHIP SELECT ($\overline{CS}$) and READ/$\overline{WRITE}$ (R/$\overline{W}$). Table III defines the results of each combination of these two pins. These pins have internal pull-up resistors so that the idle condition is selected if an open condition exists on these pins.

TABLE III. Mode Selection

$\overline{CS}$	R/$\overline{W}$	Mode Selected
0	0	WRITE
0	1	READ
1	0	IDLE
1	1	IDLE

WRITE MODE

The write mode is entered by setting both $\overline{CS}$ and R/$\overline{W}$ to logical low values. To enable the standard write mode (only one head enabled), the $\overline{WSER}$ pin is set to a logic high level or open circuit (see Table IV). In the write mode, the device acts as a current switch which toggles between the X and Y sides of the selected head on each high-to-low logic level transition of the WRITE DATA (WD) input. When entering the write mode from the read mode, the write data flip-flop is initialized to pass current into the X side of the selected head. The magnitude of the write current is set by an external resistor, R_{WRITE}, connected between the WC pin and ground. The relationship between the write current and the write resistor is:

$$I_{WRITE} = A_{WC} \times \frac{V_{WC}}{R_{WRITE}}$$

where A_{WC} is the current gain (see DC and AC Electrical Characteristics Write Mode table).

The portion of the write current that passes through the head (I_h) is defined as:

$$I_h = \frac{I_{WRITE}}{1 + R_h/R_d}$$

where: R_h = the sum of the head and external wire resistance and R_d = the damping resistance (if any). $R_d = \infty$ for no damping.

MULTIWRITE MODE

In the Multiwrite mode, all channels of the device will write the same data with the same write current. The $\overline{WSER}$ pin selects the Multiwrite mode when at a low logic level and overrides any settings on the HS0/HS1 pins (see Table IV). If left floating, $\overline{WSER}$ has an internal pull-up resistor to ensure normal write operation. In the read and idle modes, $\overline{WSER}$ is disabled and has no effect.

TABLE IV. Read and Write Mode Selection

R/$\overline{W}$	$\overline{WSER}$	HS1	HS0	Result
1	X	0	0	Read Channel 0
1	X	0	1	Read Channel 1
1	X	1	0	Read Channel 2
1	X	1	1	Read Channel 3
0	0	X	X	Write All Channels
0	1	0	0	Write Channel 0
0	1	0	1	Write Channel 1
0	1	1	0	Write Channel 2
0	1	1	1	Write Channel 3

Basic Circuit Operation (Continued)

POWER SUPPLY FAULT AND WRITE UNSAFE DETECTION

A power supply fault detection circuit is provided on chip. This circuit will disable the write current generator during device power-up, power-down or when a power supply fault occurs. This will prevent the possibility of writing bad data onto the media.

When entering the write mode, the write unsafe detector circuitry is enabled. This circuit issues a high level output at the WRITE UNSAFE (WUS) output when any of the following conditions exist:

1. Write data input frequency is too low.
2. The device is in the read mode.
3. The chip is disabled.
4. No write current exists.
5. The head is an open circuit.

The WUS pin is an open-collector output and requires an external pull-up resistor. After a fault condition has been removed, two negative transitions of the WD pin are required to clear the write unsafe circuitry.

IDLE MODE

The idle mode is entered by applying a logical high level to the $\overline{CS}$ pin. In this mode the RDX and RDY outputs are in a high impedance state and the device is disabled. This will reduce the power consumption to a minimum value when the device is not needed, which is particularly important for battery applications.

READ MODE

The read mode is entered by setting $\overline{CS}$ to a low logic level and R/$\overline{W}$ to a high logic level. In this mode the write current generator is disabled and a low noise differential amplifier is enabled. The amplified head read-back signal is available at the RDX and RDY pins. These outputs are differential emitter-followers and should be AC coupled to the load.

During the write or idle modes, the read amplifier is disabled and the RDX, RDY outputs are forced to a high impedance state. This allows these outputs to be wire-ORed with outputs from other devices to support multiple read/write applications.

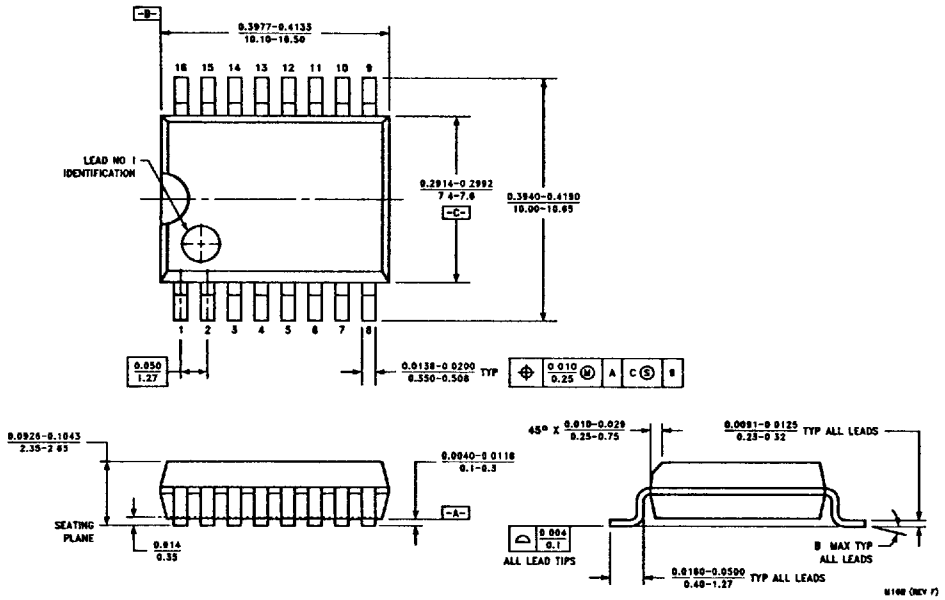
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

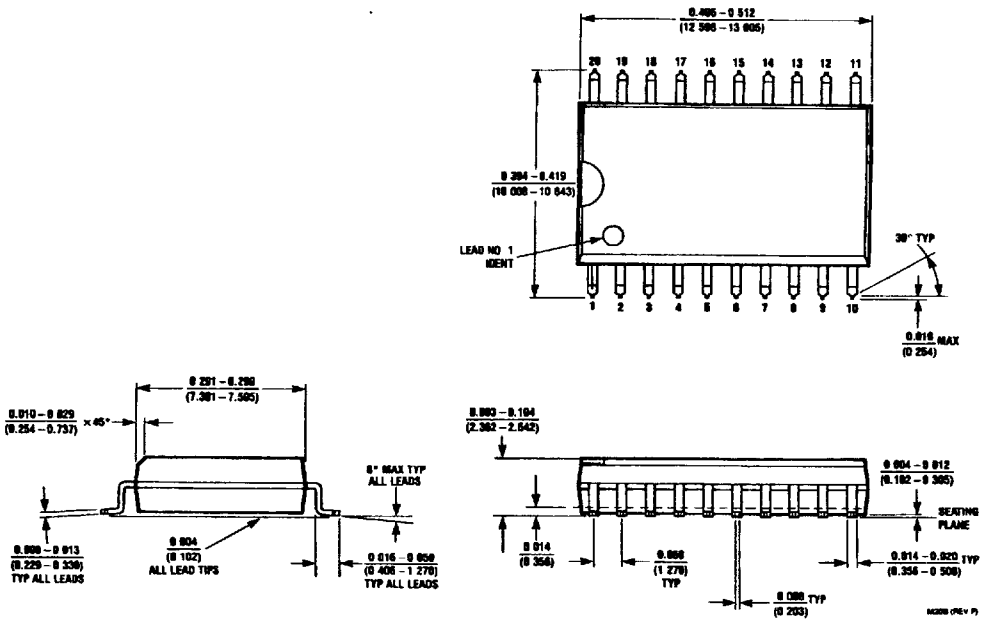
DP 846 XY R ZW- N I

- DP — Manufacturer's ID
- 846 — Product Prefix
- XY — Preamplifier Part Number
  - X = 0 5V, Conventional Preamplifier
  - X = 3 3V–5V, Conventional Preamplifier
  - X = 4 3V–5V, Multiwrite Preamplifier
  - X = 5 5V, Multiwrite Preamplifier
  - Y = 0 Read Gain of 300
  - Y = 5 Read Gain of 200
- R — R = Internal Damping Resistor; Blank = No Internal Damping Resistor
- ZW- — Package Information
  - M = Plastic Small Outline
  - MS = Shrink Small Outline
- N — Number of Channels
  - N = 2
  - N = 4
- I — Mirror Image

Physical Dimensions inches (millimeters)



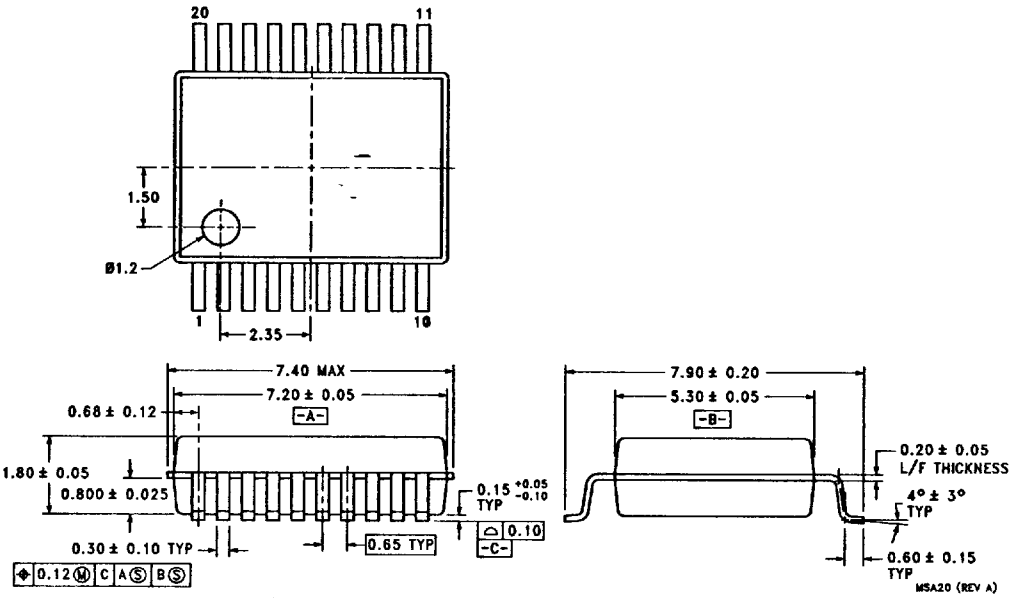
16-Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16B



20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)

Lit. # 103130-001



20-Lead Molded Shrink Small Outline Package, EIAJ, Type II
NS Package Number MSA20

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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