

# DP8472/DP8474 Floppy Disk Controller PLUS

## General Description

The DP8472 and DP8474 are complete floppy disk drive controllers. They are software compatible with the  $\mu$ PD765A but also include many additional enhancements. This includes an internal analog data separator, internal write precompensation, a motor on/off control, internal disk I/O drivers, low power mode, and some software enhancements that simplify the programming.

A high performance analog data separator is included in the DP8472/74. The data rate is programmable up to 1.25 Mbyte/sec. The data separator requires only four external passive components. Due to internal calibration, no trims or adjustments are necessary.

The internal write precompensation can be programmed to shift the data written to the disk drive early or late between 0 ns and 464 ns.

The Head Load and Head Unload timers can be redefined as Motor On and Motor Off timers. This allows interfacing to 8", 5¼", and 3½" disk drives.

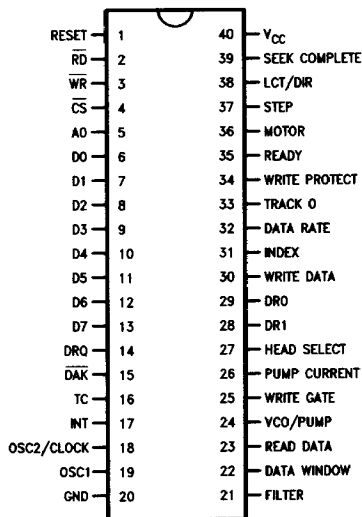
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## Features

- Internal analog data separator
- Internal write precompensation
- Software compatible with the  $\mu$ PD765
- CMOS
- Software selectable data rate (125 kbits–1.25 Mbit/sec)
- No trimmable components required
- Improved DMA timing
- 8 mA disk output buffers
- Low Power mode
- Implied seeks on read and write commands
- Can disable polling mode
- Can redefine timers for motor on/off
- Seek Complete input pin for buffered seeks
- Demultiplexed drive select outputs (DP8474)
- Extended track range (up to 4096 tracks)
- Format with IBM® or ISO (3½") standards

## Connection Diagrams

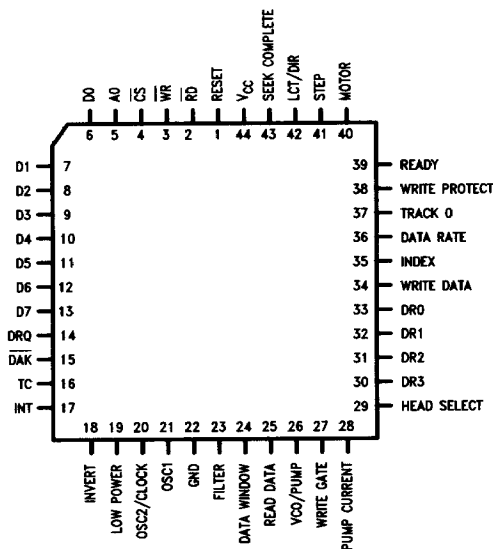
Dual-In-Line Package



Top View

TL/F/8592-1

Plastic Leaded Chip Carrier Package



Top View

TL/F/8592-2

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## General Description (Continued)

A power down mode can be enabled from software or the controller can power down automatically when it is idle. This will reduce the power consumption.

The output pins to the disk drive on the DP8474 can sink up to 8 mA. The inputs and outputs can also be active high or active low. If 1 k $\Omega$  termination resistors are used, the disk drive can be connected directly to the controller without any external buffers. The input pins are Schmitt trigger type inputs.

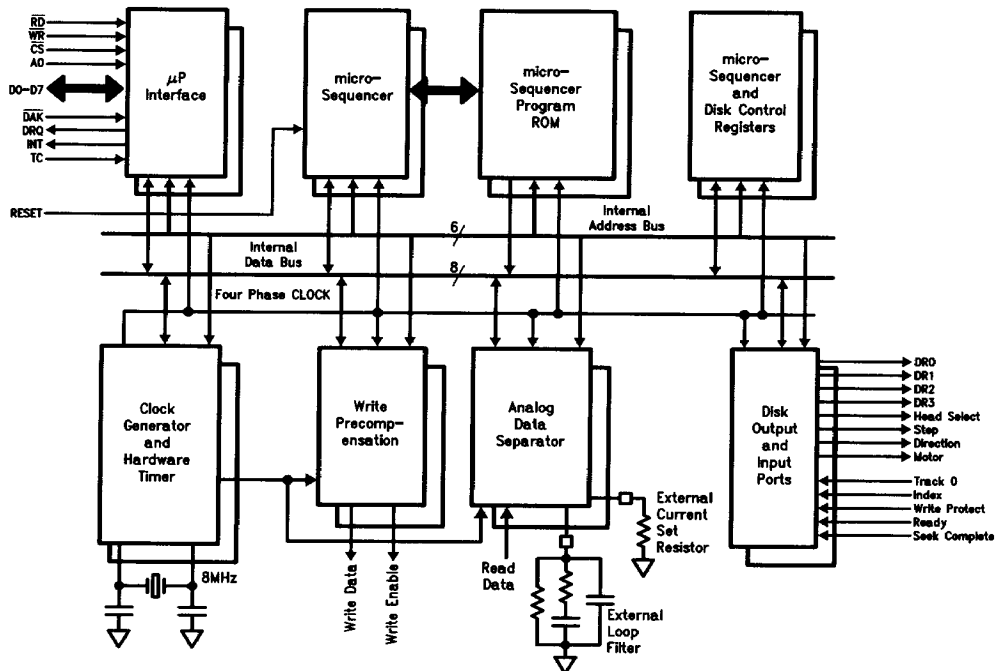
Other enhancements that may be enabled or disabled include implied seeks that will automatically move the drive

head to the correct position in many commands. Another enhancement is the ability to disable the polling mode. Also, the motor multiplexing scheme may be programmed so that the controller knows whether all the drive motors are on at the same time or if only one is on at a time.

If the command used to control these new features is not accessed, the controller will use default modes that are compatible with software written for the  $\mu$ PD765.

There are two different package types. The DP8472 is a 40-pin DIP package. The DP8474 is a 44-pin PLCC package with some additional features.

## Block Diagram



TL/F/8592-3

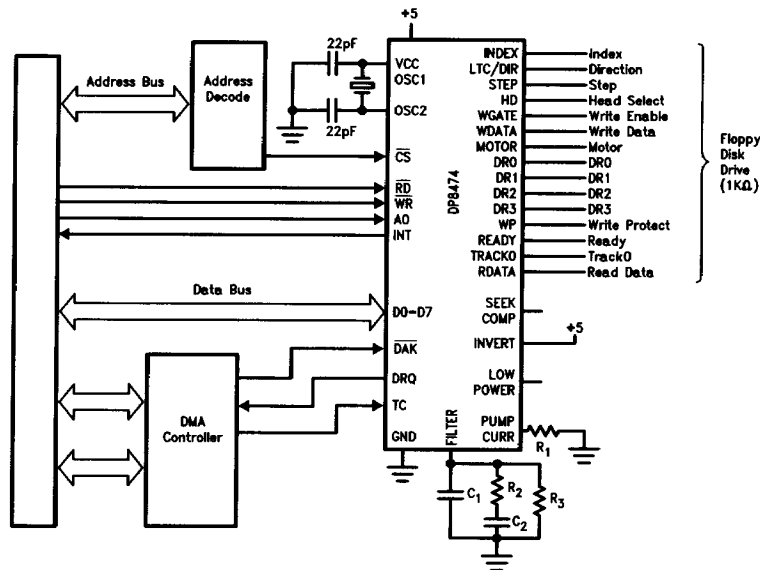
## Pin Descriptions

Symbol	DP8472 DIP Pin No.	DP8474 PLCC Pin No.	Function
RESET	1	1	Active high input that resets the controller to the idle state and resets all the output lines to the disk drive to their disabled state. Resets the Mode Command registers to their default values. Resets the Present Track registers to zero. Should be asserted at power up. To prevent glitches activating the reset sequence, a small capacitor (1000 pF) should be attached to this pin.
RD	2	2	Active low input to signal a read from the controller to the microprocessor.
WR	3	3	Active low input to signal a write from the microprocessor to the controller.
CS	4	4	Active low input to enable the RD and WR inputs for non-DMA transfers. DAK should not be asserted while CS is asserted.
A0	5	5	Address line from the microprocessor. This determines which register the microprocessor is accessing: Data (high) or Status (low) Register. Don't care during DMA transfers.
D0-D7	6-13	6-13	Bi-directional data lines to the microprocessor.
DRQ	14	14	Active high output to signal the DMA controller that a data transfer is needed.
DAK	15	15	Active low input to acknowledge the DMA request and enable the RD and WR inputs. CS should not be asserted while DAK is asserted.
TC	16	16	Active high input to indicate the termination of a DMA transfer.
INT	17	17	Active high output to signal that an operation requires the attention of the microprocessor. The action required depends on the current function of the controller.
INVERT		18	(DP8474 only.) This input determines the polarity of the disk drive interface lines (input and output). Low indicates normal push-pull output signals with the polarity as described in the pin description. High indicates active low 8 mA open drain outputs. The DP8472 has this signal tied low internally.
LOW POWER		19	(DP8474 only.) This active high output indicates when the controller is in its low power mode. This can be connected to a disk drive that has a low power input signal.
CLK/OSC2	18	20	An external crystal or the output of an external clock is attached here. The normal frequency is 8 MHz.
OSC1	19	21	An external crystal is attached here or it is grounded if an external clock is being used.
GROUND	20	22	This pin is the analog and digital ground for the controller.
FILTER	21	23	This pin is the output of the charge pump and is also the input to the VCO. A simple filter is attached to this pin. See Table II.
DATA WINDOW	22	24	This input pin is not used and should be tied to the same state as the INVERT pin. For the DP8472, this pin should be tied low.
READ DATA	23	25	The raw data read from the disk is connected here. Affected by the INVERT pin.
VCO/PUMP	24	26	This output is the NOR of the internal Pump Up and Pump Down signals. This can be used for diagnostic purposes.
WRITE GATE	25	27	This active high output enables the write circuitry of the selected disk drive. This output has been designed to prevent glitches during power up and power down. Affected by the INVERT pin.

## Pin Descriptions (Continued)

Symbol	DP8472 DIP Pin No.	DP8474 PLCC Pin No.	Function
PUMP CURRENT	26	28	A resistor is attached to this pin to set the charge pump current. The other end of the resistor is tied to ground. See Table II.
HEAD SELECT	27	29	This output determines which disk drive head is active. Low = Head 0, High = Head 1. Affected by the INVERT pin.
DR1 DR0	28 29		(DP8472 only.) Active high outputs that indicate in binary form which disk drive is active.
DR3 DR2 DR1 DR0		30 31 32 33	(DP8474 only.) Active high outputs to select which disk drive is active. These pins are the demultiplexed DR0, DR1 pins described above. Affected by the INVERT pin.
WRITE DATA	30	34	This is the active high write precompensated serial data output to be written onto the selected disk drive. Affected by the INVERT pin.
INDEX	31	35	This active high input signals the beginning of a track. Affected by the INVERT pin.
DATA RATE	32	36	This input selects the data rate used if the Mode command is not issued since the last reset. High indicates 500 kbits/sec (MFM), Low indicates 250 kbits/sec (Based on 8 MHz clock). The data rate may be overridden in software through the Mode command. This pin also affects the times programmed with the Specify command. The times are doubled if this pin is low. This doubling is not overridden by the Mode Command.
TRACK 0	33	37	This active high input tells the controller that the head is at track zero of the selected disk drive. Affected by the INVERT pin.
WRITE PROTECT	34	38	This active high input indicates that the disk is write protected. Any command that writes to the disk drive is not permitted when a disk is write protected. Affected by the INVERT pin.
READY	35	39	This active high input indicates that the selected disk drive is ready. If the disk drive does not support a Ready signal, this pin should be tied high. See also the ANR and POL bits in the Mode command. Affected by the INVERT pin.
MOTOR	36	40	Active high output to turn on the disk drive motor for 5¼" drives. May also be used to load the head of an 8" drive. Affected by the INVERT pin.
STEP	37	41	This active high output will produce a pulse at a software programmable rate to move the head during a Seek or Recalibrate. Affected by the INVERT pin.
LCT/DIR	38	42	When in the seek mode, this output will determine the direction of the head movement (high = step in, low = step out). When in the write or read modes, this output will be high when the head of the selected disk drive is on a track number that is greater than or equal to a software programmable number. Otherwise, it will be low. Affected by the INVERT pin.
SEEK COMPLETE	39	43	This active high input from the disk drive indicates that a buffered seek operation is complete. This input may be tied high if drive does not support buffered seeks. Affected by the INVERT pin.
V <sub>CC</sub>	40	44	This pin is the 5V supply for both the analog and digital circuitry.

## Typical Application



TL/F/8592-4

## Functional Description

The DP8472/74 contains virtually all the logic necessary to connect a  $\mu$ P system to a floppy disk drive. There are only two registers to access in the controller: the Main Status Register and the Data Register. The read only Main Status Register is used to detect the current status of the controller.

The Data Register is used for many things. Commands and command parameters are programmed through the Data Register. While reading or writing to a disk, the data is transferred through the Data Register. Finally, the result of a command after it is finished is read from the Data Register.

### COMMAND SEQUENCE

The disk controller can perform many commands. There are three phases for every command executed.

**Command Phase:** The  $\mu$ P writes a series of bytes to the Data Register. These bytes indicate the command desired and the particular parameters required for the command.

**Execution Phase:** The disk controller performs the desired command. Some commands require the  $\mu$ P to read or write data to or from the Data Register during this time. Reading data from a disk is an example of this.

**Result Phase:** The  $\mu$ P reads a series of bytes from the Data Register. These bytes indicate whether the command executed properly and other status information.

Each command requires a set of bytes to be written to the disk controller in the Command Phase. All the bytes must be written in the order specified in the Command Description Table. The Execution Phase starts immediately after the last byte in the Command Phase is written.

After the end of the Execution Phase, all the Result Phase bytes must be read from the disk controller. The bytes are read in the order specified in the Command Description Table.

A new command may be initiated by writing the Command Phase bytes after the last byte from the Result Phase has been read.

### MAIN STATUS REGISTER (A0 = 0)

The read only Main Status Register indicates the current status of the disk controller. The Main Status Register is always available to be read. One of its functions is to control the flow of data to and from the Data Register. The Main Status Register indicates when the disk controller is ready to send or receive data. It should be read before each byte is transferred to or from the Data Register except during a DMA transfer. No delay is required when reading this register after a data transfer.

#### Main Status Register

- D7 Request for Master:** Indicates that the Data Register is ready to send or receive data from the  $\mu$ P. This bit is cleared immediately after a byte transfer and will become set again as soon as the disk controller is ready for the next byte.
- D6 Data Direction:** Indicates whether the controller is expecting a byte to be written to (0) or read from (1) the Data Register.
- D5 Non-DMA Execution:** Bit is set only during the Execution Phase of command if it is in the non-DMA mode. In other words, if this bit is set, the multiple byte data transfer (in the Execution Phase) must be monitored by the  $\mu$ P either through interrupts, or software polling as described under Interrupt Mode.

## Functional Description (Continued)

- D4 Command in Progress:** Bit is set after the first byte of the Command Phase is written. Bit is cleared after the last byte of the Result Phase is read. If there is no result phase in a command, the bit is cleared after the last byte of the Command Phase is written.
- D3 Drive 3 Seeking:** Set after the last byte of the Command Phase of a Seek or Recalibrate command is issued for drive 3. Cleared after reading the first byte in the Result Phase of the Sense Interrupt Command for this drive.
- D2 Drive 2 Seeking:** Same as above for drive 2.
- D1 Drive 1 Seeking:** Same as above for drive 1.
- D0 Drive 0 Seeking:** Same as above for drive 0.

### PROCESSOR INTERFACE

Bytes are transferred to and from the disk controller in different ways for the different phases in a command. During the Command Phase and the Result Phase, bytes are transferred to and from the Data Register. The Main Status Register is monitored by the software to determine when a data transfer can take place. Bit 6 of the Main Status Register must be cleared and bit 7 must be set before a byte can be written to the Data Register during the Command Phase. Bits 6 and 7 of the Main Status Register must both be set before a byte can be read from the Data Register during the Result Phase.

If there is information to be transferred during the Execution Phase, there are three methods that can be used. The DMA mode is used if the system has a DMA controller. This allows the  $\mu$ P to do other things during the Execution Phase data transfer. If DMA is not used, an interrupt can be issued for each byte transferred during the Execution Phase. If interrupts are not used, the Main Status Register can be polled to indicate when a byte transfer is required.

### DMA MODE

If the DMA mode is selected (from the Specify Command), a DMA request will be generated in the Execution Phase when each byte is ready to be transferred. The DMA controller should respond to the DMA request with a DMA acknowledge and a RD or WR strobe. The DMA request will be cleared by the active edge of the DMA acknowledge. After the last byte is transferred, an interrupt is generated. This indicates the beginning of the Result Phase. The interrupt will be cleared by reading the first byte in the Result Phase.

### INTERRUPT MODE

If the non-DMA mode is selected, an interrupt will be generated in the Execution Phase when each byte is ready to be transferred. The Main Status Register should be read to verify that the interrupt is for a data transfer. Bits 5 and 7 of the Main Status Register will be set. The interrupt will be cleared when the byte is transferred to or from the Data Register. The  $\mu$ P should transfer the byte within the time allotted by Table I. If the byte is not transferred within the time allotted, an Overrun Error will be indicated in the Result Phase when the command terminates at the end of the current sector.

An interrupt will also be generated after the last byte is transferred. This indicates the beginning of the Result Phase. Bits 7 and 6 of the Main Status Register will be set and bit 5 will be clear. This interrupt will be cleared by reading the first byte in the Result Phase.

**TABLE I. Maximum Time Allowed to Service an Interrupt or DRQ in Execution Phase**

Data Rate	Clock Frequency	Time to Service
125	8 MHz	62.0 $\mu$ s
250	8 MHz	30.0 $\mu$ s
500	8 MHz	14.0 $\mu$ s
1000	8 MHz	6.0 $\mu$ s
1250	10 MHz	4.4 $\mu$ s
2500	20 MHz	2.2 $\mu$ s

For any clock frequency, time = (8/Data Rate) - (16/clock)

Time from rising edge of DRQ or INT to trailing edge of  $\overline{\text{DAR}}$  or RD or WR

### SOFTWARE POLLING

If the non-DMA mode is selected and interrupts are not suitable, the  $\mu$ P can poll the Main Status Register during the Execution Phase to determine when a byte is ready to be transferred. In the non-DMA mode, bit 7 of the Main Status Register reflects the state of the interrupt pin. Otherwise, the data transfer is similar to the Interrupt Mode described above.

### DATA RATE

The data rate is determined by three factors; the crystal frequency, the data rate pin, and the data rate programmed via the Mode command. Normally an 8 MHz crystal is used as the clock. If this is the case, the data rate pin can be used to select between 250 kbits/sec or 500 kbits/sec (MFM). If a different value crystal frequency is used, the data rate for MFM is given by the formulas:

$$\text{data rate} = f / 32 \text{ bits/sec (Data rate pin low)}$$

$$\text{data rate} = f / 16 \text{ bits/sec (Data rate pin high)}$$

The Mode command can be used to select the data rate via software. This method gives better flexibility than the data rate pin. With an 8 MHz clock, the following MFM data rates can be selected: 250, 500, or 1000 kbits/sec. Other data rates can also be used by simply changing the crystal frequency as described in the Mode command.

It is important to note that the internal data separator will not function correctly above a data rate of 1.25 Mbits/sec. The write precompensation logic will also fail above this data rate.

### Data Separator

The internal data separator consists of a high performance analog PLL. The PLL synchronizes the raw data signal read from the disk drive. The synchronized signal is used to separate the encoded clock and data pulses. The data pulses are grouped into bytes and then sent to the  $\mu$ P.

The PLL consists of three main components, a phase comparator, a filter, and a voltage controlled oscillator (VCO). The basic operation of a PLL is fairly straightforward. The phase comparator detects the difference between the phase of the VCO output and the phase of the raw data being read from the disk. This phase difference is converted to a current which either charges or discharges an external

## Data Separator (Continued)

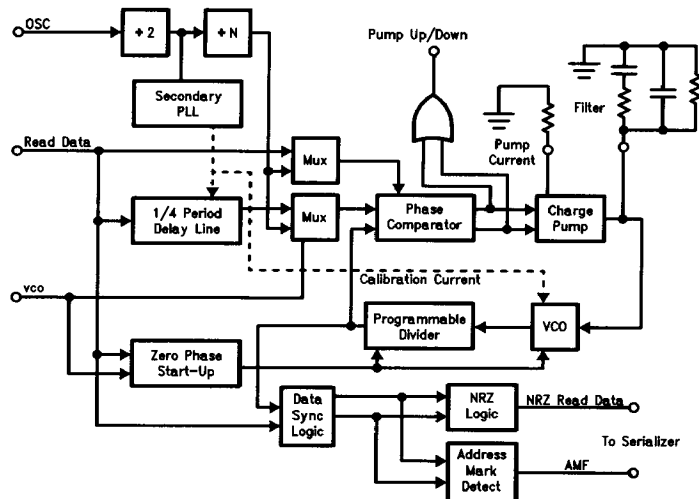


FIGURE 1. Data Separator Block Diagram

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filter. The resulting voltage of the filter changes the frequency of the VCO in an attempt to reduce the phase difference between the two signals. A PLL is "locked" when the frequency of the VCO is exactly the same as the average frequency of the data read from the disk. This is somewhat of a simplified view because it ignores such topics as loop stability, acquisition time, and filter values. A block diagram of the data separator is shown in Figure 1.

The quarter period delay line is used to determine the center of each bit cell. It is important that this delay line be as accurate as possible. A typical data separator would normally require an external trim to adjust the delay. An external trim is not required for the DP8472/74 however. A secondary PLL is used to automatically calibrate the quarter period delay line. The secondary PLL also calibrates the center frequency of the VCO.

### PLL Filter Design

The information in this section provides information to enable design of the data separator's external filter and charge pump set resistor. Table II shows some typical filter component values, but if a custom filter is desired, the following parameters must be considered:

**R<sub>1</sub>:** Charge pump current setting resistor. The range of R<sub>1</sub> is 3 kΩ–12 kΩ.

$$I_{PUMP} = \frac{2.5 \cdot 1.2}{R_1}$$

**C<sub>2</sub>:** Filter capacitor in series with R<sub>2</sub>. With pump current determines loop bandwidth.

**R<sub>2</sub>:** Filter resistor. Determines the PLL damping factor.

**R<sub>3</sub>:** Pulldown resistor. Improves PLL performance and bit jitter tolerance.

**C<sub>1</sub>:** This filter capacitor improves the performance of the PLL by providing additional filtering of bit jitter and noise.

**K<sub>VCO</sub>:** The ratio of the change in the frequency of the VCO output due to a voltage change at the VCO input.  $K_{VCO} \approx 25 \text{ Mrad/s/V}$ . The VCO is followed by a divider to achieve the desired frequency for each data rate. VCO center frequency is 4 MHz.

**K<sub>PLL</sub>:** This is the gain of the internal PLL circuitry, and is the product of  $V_{REF} K_{VCO} K_P$ . This value is specified in the Phase Locked Loop Characteristics table.

**$\omega_n$ :** This is the bandwidth of the PLL, and is given by,

$$\omega_n = \sqrt{\frac{K_{PLL}}{2\pi C_2 N R_1}}$$

where N is the number of VCO cycles between two phase comparisons. The value of N for the various data rates are shown in Table III.

**$\zeta$ :** The damping factor is set between 0.7 and 1.2 and is given by,

$$\zeta = \frac{\omega_n R_2 C_2}{2}$$

TABLE II. Recommended Filter Values

	250	500	1000	kbit/sec
R1	5.6k	5.6k	5.6k	Ω
R2	470	560	560	Ω
C1	0.001	0.001	0.0005	μF
C2	0.042	0.033	0.012	μF
R3	200k	150k	none	Ω

## Data Separator (Continued)

The trade off, when choosing filter components is between acquisition time while the PLL is locking and jitter immunity while reading data. To select the proper components for a standard floppy disk application the following procedure can be used:

1. Choose FM or MFM, and data rate. Determine N from Table III. Determine preamble length (MFM = 12). The PLL should lock within  $\frac{1}{2}$  the preamble time.
2. Determine loop bandwidth ( $\omega_n$ ) required.
3. Set the charge pump resistor  $R_1$ .
4. Calculate  $C_2$  using:

$$C_2 = \frac{K_{PLL}}{2\pi \omega_n^2 N R_1}$$

5. Choose  $R_2$  using:

$$R_2 = \frac{2\xi}{\omega_n C_2}$$

6. Select  $C_1$  to be about 1/20th of  $C_2$ .

The above procedure will yield adequate loop performance. If optimum loop performance is required, or if the nature of the loop performance is very critical, then some additional consideration must be given to choosing  $\omega_n$  and the damping factor. Refer to the DP8473 Data Separator application note (AN505) for more details.

TABLE III. Programmable Divider Factor

Programmed Data Rate (FM/MFM)	N
1 Mbit/sec	4
500 Kbit/sec	8
250 Kbit/sec	16

## OTHER FEATURES

### Drive Polling

If the Polling Mode is enabled (power on default), the disk controller will poll the drives continuously while it is in the idle state. The idle state is after the last byte of the Result Phase has been read and the Motor pin has become inactive, but before the first byte of the next command has been written. The disk controller will select each drive and check to see if the ready signal has changed states since the last time it checked. If a drive has changed its ready state, an interrupt is generated by the controller. The Sense Interrupt command should be used to identify and clear this interrupt. After a reset, the controller assumes that the disk drives are not ready. Therefore, if the Ready pin is tied high (or low if INVERT is used), the  $\mu P$  should issue four Sense Interrupt commands to clear the Ready Changed interrupts. The Polling Mode can be enabled and disabled through the Mode Command.

### Low Power Mode

In the Low Power Mode the crystal oscillator is turned off. When the oscillator is turned off the controller draw less current. The internal circuitry is disabled while the oscillator is off because the internal circuitry is driven from this clock. The oscillator will turn back on automatically after it detects  $\overline{CS}$  and  $\overline{RD}$  or  $\overline{CS}$  and  $\overline{WR}$  being activated. It may take a few milliseconds for the oscillator to stabilize and the  $\mu P$  will be prevented from trying to access the Data Register during this time through the normal Main Status Register protocol. The Request for Master bit in the Main Status Register will be inactive.

### Buffered Seeks

A seek complete signal is available on any disk drive that supports buffered seeks. This input on the controller is included to accommodate this signal. If the disk drive used does not have this signal available, simply tie this input high (or low if INVERT is used).

Sometimes, after a reset, the controller will consistently return an error in the Result Phase after an FM read command. If this occurs, simply reset the controller and retry the operation. This may have to be done more than once, as many as five times. Resetting and repeating will prevent soft errors from being reported prematurely. This technique is used by MS-DOS. FM mode is not tested by National Semiconductor.



# Command Description Table

## READ DATA

Command Phase

MT	MFM	SK	0	0	1	1	0
IPS	0	0	0	0	HD	DR1	DR0

Track Number
Drive Head Number
Sector Number
Number of Bytes per Sector
End of Track Sector Number
Intersector Gap Length
Data Length

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

## READ DELETED DATA

Command Phase

MT	MFM	SK	0	1	1	0	0
IPS	0	0	0	0	HD	DR1	DR0

Track Number
Drive Head Number
Sector Number
Number of Bytes per Sector
End of Track Sector Number
Intersector Gap Length
Data Length

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

## READ A TRACK

Command Phase

0	MFM	SK	0	0	0	1	0
IPS	0	0	0	0	HD	DR1	DR0

Track Number
Drive Head Number
Sector Number
Number of Bytes per Sector
End of Track Sector Number
Intersector Gap Length
Data Length

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

## WRITE DATA

Command Phase

MT	MFM	SK	0	0	1	0	1
IPS	0	0	0	0	HD	DR1	DR0

Track Number
Drive Head Number
Sector Number
Number of Bytes per Sector
End of Track Sector Number
Intersector Gap Length
Data Length

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

## WRITE DELETED DATA

Command Phase

MT	MFM	SK	0	1	0	0	1
IPS	0	0	0	0	HD	DR1	DR0

Track Number
Drive Head Number
Sector Number
Number of Bytes per Sector
End of Track Sector Number
Intersector Gap Length
Data Length

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

## FORMAT A TRACK

Command Phase

0	MFM	0	0	1	1	0	1
0	0	0	0	0	HD	DR1	DR0

Number of Bytes per Sector
Number of Sectors per Track
Intersector Gap Length
Data Pattern

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

# Command Description Table (Continued)

## SCAN EQUAL

Command Phase

MT	MFM	SK	1	0	0	0	1
IPS	0	0	0	0	HD	DR1	DR0

Track Number
Drive Head Number
Sector Number
Number of Bytes per Sector
End of Track Sector Number
Intersector Gap Length
Sector Step Size

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

## SCAN LOW OR EQUAL

Command Phase

MT	MFM	SK	1	1	0	0	1
IPS	0	0	0	0	HD	DR1	DR0

Track Number
Drive Head Number
Sector Number
Number of Bytes per Sector
End of Track Sector Number
Intersector Gap Length
Sector Step Size

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

## SCAN HIGH OR EQUAL

Command Phase

MT	MFM	SK	1	1	1	0	1
IPS	0	0	0	0	HD	DR1	DR0

Track Number
Drive Head Number
Sector Number
Number of Bytes per Sector
End of Track Sector Number
Intersector Gap Length
Sector Step Size

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

## READ ID

Command Phase

0	MFM	0	0	1	0	1	0
IPS	0	0	0	0	HD	DR1	DR0

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

## SENSE INTERRUPT

Command Phase

0	0	0	0	1	0	0	0
---	---	---	---	---	---	---	---

Result Phase

Status Register 0
Present Track Number
Bits 6-11 of PTN 0 0 0 0 0

## SENSE DRIVE STATUS

Command Phase

0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	HD	DR1	DR0

Result Phase

Status Register 3
-------------------

## SET TRACK

Command Phase

0	R/W	1	0	0	0	0	1
0	0	1	1	0	MSB	DR1	DR0

New Track Number

Result Phase

Value
-------

## SEEK

Command Phase

0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	0	DR1	DR0

New Track Number

Bits 8-11 of Track 0 0 0 0 0
------------------------------

## RECALIBRATE

Command Phase

0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	DR1	DR0

## SPECIFY

Command Phase

0	0	0	0	0	0	0	1	1
---	---	---	---	---	---	---	---	---

Step Rate Time

Motor Off Time

Motor On Time

DMA

## MODE

Command Phase

0	0	0	0	0	0	0	0	1
TMR	IAF	IPS	DMC	LOW	PWR	POL	ETR	

Low Current & Precomp Track #

DRE	ANR	0	WLD	Head Settle
1	0	Data Rt	Write Precomp	

**Notes:** Grey boxes indicate bytes that are written or read only while in the extended track range mode.

MT—Multi-Track

SK—Skip

IPS—Implied Seek

HD—Head #

DR—Drive Select

TMR—Timer mode

IAF—Index address field

IPS—Implied Seek

DMC—Drive motor configuration

POL—Polling mode

ETR—Extended track range

DRE—Software data rate enable

ANR—Abort not ready

WLD—Wildcard in Scan Command

MSB—Selects MSB of Track Register

## Result Phase Status Registers

The Result Phase of a command contains bytes that hold status information. The formats of these bytes are the same for each command and are described below. Do not confuse these internal register bytes with the Main Status Register which is a read-only register that is always available. The Result Phase status registers are read from the Data Register only during the Result Phase.

### STATUS REGISTER 0 (ST0)

#### D7, D6 Interrupt Code:

- 00 = Normal Termination of Command. Command was completed and properly executed.
- 01 = Abnormal Termination of Command. Execution of Command was started, but was not successfully completed.
- 10 = Invalid Command Issue. Command issued was not recognized as a valid command.
- 11 = Ready changed state during the polling mode.

**D5 Seek End:** Seek or Recalibrate Command completed. (Used during Sense Interrupt command.)

**D4 Equipment Check:** After a Recalibrate Command, Track 0 signal failed to occur. (Used during Sense Interrupt command.)

#### D3 Not Ready:

Read, Write, Format, or Scan commands:

Only set if ANR bit (Mode command) is enabled. If POL bit (Mode command) is not set, Ready pin was not true for more than 5 disk revolutions during a command. If POL bit is set, Ready pin was not true at some time during a command.

Sense Interrupt command:

Inverse state of Ready pin if Invert pin is low.

Actual state of Ready pin if Invert pin is high.

**D2 Head Address:** (at end of Execution Phase).

**D1, D0 Drive Select:** (at end of Execution Phase).

- 00 = Drive 0 selected.
- 01 = Drive 1 selected.
- 10 = Drive 2 selected.
- 11 = Drive 3 selected.

### STATUS REGISTER 1 (ST1)

**D7 End of Track:** Controller transferred the last byte of the last sector without the TC pin becoming active. The last sector is the End Of Track Sector Number programmed in the Command Phase.

**D6 Not Used:** 0.

**D5 CRC Error:** If bit 5 of ST2 is clear and this bit is set, then there was a CRC error in the Address Field of the correct sector. If bit 5 of ST2 is set, then there was a CRC error in the Data Field.

**D4 Over Run:** Controller was not serviced by the  $\mu$ P soon enough during a data transfer in the Execution Phase.

**D3 Not Used:** 0.

**D2 No Data:** Three possible problems: 1) Controller cannot find the sector specified in the Command Phase during the execution of a Read, Write, or Scan command. An address mark was found, however, so it is not a blank disk. 2) Controller cannot read any Address Fields without a CRC error during Read ID command. 3) Controller cannot find starting sector during execution of Read A Track command.

**D1 Not Writable:** Write Protect pin is active when a Write or Format command is issued.

**D0 Missing Address Mark:** If bit 0 of ST2 is clear, then the disk controller cannot detect any Address Field Address Mark after two disk revolutions. If bit 0 of ST2 is set, then the disk controller cannot detect the Data Field Address Mark.

### STATUS REGISTER 2 (ST2)

**D7 Not Used:** 0.

**D6 Control Mark:** Controller tried to read a sector which contained a deleted data address mark during execution of Read Data or Scan commands. Or, if a Read Deleted Data command was executed, a regular address mark was detected.

**D5 CRC Error in Data Field:** Controller detected a CRC error in the Data Field. Bit 5 of ST1 is also set.

**D4 Wrong Track:** Only set if desired sector not found and the track number recorded on any sector of the current track is different from that stored in the Track Register (but is not track FF hex).

**D3 Scan Equal Hit:** "Equal" condition satisfied during any Scan Command.

**D2 Scan Not Satisfied:** Controller cannot find a sector on the track which meets the desired condition during Scan Command.

**D1 Bad Track:** Only set if the desired sector is not found and the track number recorded on any sector on the track is different from that stored in the Track Register and the recorded track number is FF(hex).

**D0 Missing Address Mark in Data Field:** Controller cannot find a Data Field Address Mark of the desired sector during a Read or Scan command. Bit 0 of ST1 is also set.

### STATUS REGISTER 3 (ST3)

**D7 Not used:** 0

**D6 Write Protect Status**

**D5 Ready Status**

**D4 Track 0 Status**

**D3 Not used:** 0

**D2 Head Select Status**

**D1,D0 Drive Selected:**

- 00 = Drive 0 selected.
- 01 = Drive 1 selected.
- 10 = Drive 2 selected.
- 11 = Drive 3 selected.

## Command Description

### READ DATA

The Read Data op-code is written to the data register followed by 8 bytes as specified in the Command Description Table. After the last byte is written, the controller turns on the correct drive and starts looking for the sector specified. Once the sector is found the controller sends the data to the  $\mu$ P. After one sector is finished, the Sector Number is incremented by one and this new sector is searched for. If MT (Multi-Track) is set, both sides of one track can be read. Starting on side zero, the sectors are read until the sector number specified by End of Track Sector Number is reached. Then side one is read, starting with sector number one.

The Read Data command continues to read until the TC pin is set. This means that the DMA controller should be programmed to transfer the correct number of bytes. TC could be controlled by the  $\mu$ P and be asserted when enough bytes are received. An alternative to these methods of stopping the Read Data command is to program the End of Track Sector Number to be the last sector number that needs to be read. The controller will stop reading the disk with an error indicating that it tried to access a sector number beyond the end of the track.

The Number of Data Bytes per Sector parameter is defined in Table IV. If this is set to zero, the Data Length parameter determines the number of bytes that the controller transfers to the  $\mu$ P. If the data length specified is smaller than 128, the controller still reads the entire 128 byte sector and checks the CRC, though only the number of bytes specified by the Data Length parameter are transferred to the  $\mu$ P. Data Length should not be set to zero. If the Number of Bytes per Sector parameter is not zero, the Data Length parameter has no meaning and should be set to FF(hex).

After the last byte of the Command Phase is written and if the ANR and POL bits are both enabled (from the Mode command), the controller will check the state of both Ready and Seek Complete. If either is not valid, the command will be aborted with a Not Ready error.

Otherwise, the Motor On pin will be asserted. If the selected drive was previously off, the Motor On Timer will be enabled.

If the Implied Seek Mode is enabled by both the Mode command and the IPS bit in this command, a Seek will be performed to the track number specified in the Command Phase. The controller will also wait the Head Settle time if the implied seek is enabled.

The controller will wait for the Motor On Timer to time out, if it was enabled. If the ANR is set, the controller will wait up to five disk revolutions for the Ready and Seek Complete pins to become valid. If they don't become valid during this period, the command will be aborted with a Not Ready error. If ANR is not set, Ready and Seek Complete are ignored.

After all these conditions are met, the controller searches for the specified sector by comparing the track number, head number, sector number, and number of bytes/sector given in the Command Phase with the appropriate bytes read off the disk in the Address Fields.

If the correct sector is found, but there is a CRC error in the Address Field, bit 5 of ST1 (CRC Error) is set and an abnormal termination is indicated. If the correct sector is not found, bit 2 of ST1 (No Data) is set and an abnormal termination is indicated. In addition to this, if any Address Field track number is FF, bit 1 of ST2 (Bad Track) is set; or if any Address Field track number is different from that specified in the Command Phase, bit 4 of ST2 (Wrong Track) is set.

After finding the correct sector, the controller reads that Data Field. If a Deleted Data Mark is found and the SK bit is set, the sector is not read, bit 6 of ST2 (Control Mark) is set, and the next sector is searched for. If a deleted data mark is found and the SK bit is not set, the sector is read, bit 6 of ST2 (Control Mark) is set, and the read terminates with a normal termination. If a CRC error is detected in the Data Field, bit 5 is set in both ST1 and ST2 (CRC Error) and an abnormal termination is indicated.

If no problems occur in the read command, the read will continue from one sector to the next in logical order (not physical order) until either TC is set or an error occurs.

If a disk has not been inserted into the disk drive, there are many opportunities for the controller to appear to hang up. It does this if it is waiting for a certain number of disk revolutions for something. If this occurs, the controller can be forced to abort the command by writing a byte to the Data register. This will place the controller into the Result Phase.

An interrupt will be generated when the Execution Phase of the Read Data command terminates. The values that will be read back in the Result Phase are shown in Table V. If an error occurs, the result bytes will indicate the sector being read when the error occurred.

TABLE IV. Sector Size Selection

Bytes/Sector Code	Number of Bytes in Data Field
0	128
1	256
2	512
3	1024
4	2048
5	4096
6	8192

## Command Description (Continued)

**TABLE V. Result Phase Termination Values with No Error**

MT	HD	Last Sector	ID Information at Result Phase			
			Track	Head	Sector	B/S
0	0	< EOT	NC	NC	S+1	NC
0	0	= EOT	T+1	NC	1	NC
0	1	< EOT	NC	NC	S+1	NC
0	1	= EOT	T+1	NC	1	NC
1	0	< EOT	NC	NC	S+1	NC
1	0	= EOT	NC	1	1	NC
1	1	< EOT	NC	NC	S+1	NC
1	1	= EOT	T+1	0	1	NC

EOT = End of Track Sector Number from Command Phase

NC = No Change in Value

S = Sector Number last operated on by controller

T = Track # programmed in Command Phase

### READ DELETED DATA

This command is the same as the Read Data command except for its treatment of a Deleted Data Mark. If a Deleted Data Mark is read, the sector is read normally. If a Regular Data Mark is found and the SK bit is set, the sector is not read, bit 6 of ST2 (Control Mark) is set, and the next sector is searched for. If a Regular Data Mark is found and the SK bit is not set, the sector is read, bit 6 of ST2 (Control Mark) is set, and the read terminates with a normal termination.

### WRITE DATA

The Write Data command is very similar to the Read Data command except that data is transferred from the  $\mu$ P to the disk rather than the other way around. If the controller detects the Write Protect signal, bit 1 of ST1 (Not Writable) is set and an abnormal termination is indicated.

### WRITE DELETED DATA

This command is the same as the Write Data command except a Deleted Data Mark is written at the beginning of the Data Field instead of the normal Data Mark.

### READ A TRACK

This command is similar to the Read Data command except for the following. The controller starts at the index hole and reads the sectors in their physical order, not their logical order.

Even though the controller is reading sectors in their physical order, it will still perform a comparison of the header ID bytes with the data programmed in the Command Phase. The exception to this is the sector number. Internally, this is initialized to a one, and then incremented for each successive sector read. Whether or not the programmed Address Field matches that read from the disk, the sectors are still read in their physical order. If a header ID comparison fails, bit 2 of ST1 (No Data) is set, but the operation will

continue. If there is a CRC error in the Address Field or the Data Field, the read will also continue.

The command will terminate when it has read the number of sectors programmed in the EOT parameter.

### READ ID

This command will cause the controller to read the first Address Field that it finds. The Result Phase will contain the header bytes that are read. There is no data transfer during the Execution Phase of this command. An interrupt will be generated when the Execution Phase is completed.

### FORMAT A TRACK

This command will format one track on the disk. After the index hole is detected, data patterns are written on the disk including all gaps, address marks, Address Fields, and Data Fields. The exact details of the number of bytes for each field is controlled by the parameters given in the Format A Track command, and the IAF (Index Address Field) bit in the Mode command. The exact format is shown in the Track Format figure at the end of this data sheet. The Data Field consists of the Fill Byte specified in the command, repeated to fill the entire sector.

To allow for flexible formatting, the  $\mu$ P must supply the four Address Field bytes (track, head, sector, # bytes) for each sector formatted during the Execution Phase. In other words, as the controller formats each sector, it will request four bytes through either DMA requests or interrupts. This allows for non-sequential sector interleaving. Some typical values for the programmable GAP size are shown in Table VI.

The Format Command terminates when the index hole is detected a second time, at which point an interrupt is generated. Only the first three status bytes in the Result Phase are significant.

## Command Description (Continued)

**TABLE VI. Gap Length for Various Sector Sizes and Disk Types**

Mode	Sector Size	Sector Code	EOT	Gap	Format Gap
<b>8" Drives (360 RPM, 500 kb/s)</b>					
FM	128	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
<b>5¼" Drives (300 RPM, 250 kb/s)</b>					
FM	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
<b>3½" Drives (300 RPM, 250 kb/s)</b>					
FM	128	00	0F	07	1B
	256	01	09	0E	2A
	512	02	05	1B	3A
MFM	256	01	0F	0E	36
	512	02	09	1B	54
	1024	03	05	35	74

**Note:** Format Gap is the gap length used only for the Format Command.

### SCAN COMMANDS

The Scan Commands allow data read from the disk to be compared against data sent from the  $\mu P$ . The disk will be read at the same time that the  $\mu P$  writes data to the controller. There are three Scan Commands to choose from:

Scan Equal	Disk Data = $\mu P$ Data
Scan Less Than Or Equal	Disk Data $\leq$ $\mu P$ Data
Scan Greater Than Or Equal	Disk Data $\geq$ $\mu P$ Data

Each sector is interpreted with the most significant bytes first. If the Wildcard mode is enabled from the Mode command, an FF(hex) from either the disk or the  $\mu P$  is used as a don't care byte that will always match equal. After each sector is read, if the desired condition has not been met, the

next sector is read. The next sector is defined as the current sector number plus the Sector Step Size specified. The Scan command will continue until the scan condition has been met, or the End of Track Sector Number has been reached, or if TC is asserted.

If the SK bit is set, sectors with deleted data marks are ignored. If all sectors read are skipped, the command will terminate with D3 of ST2 set (Scan Equal Hit). The result phase of the command is shown in Table VII.

### SEEK

There are two ways to move the disk drive head to the desired track number. Method One is to enable the Implied Seek Mode. This way each individual Read or Write command will automatically move the head to the track specified in the command.

Method Two is using the Seek command. If the extended track range mode is enabled, a fourth byte must be issued during the Command Phase which specifies the four most significant bits of the desired track number. Otherwise, only three bytes should be issued.

During the Execution Phase of the Seek Command, the track number to seek to is compared with the present track number and a step pulse is produced to move the head one track closer to the desired track number. This is repeated at the rate specified by the Specify Command until the head reaches the correct track. At this point an interrupt is generated and a Sense Interrupt Command is required to clear the interrupt.

During the Execution Phase of the Seek Command the only indication via software that a Seek Command is in progress is bits 0-3 (Drive Busy) of the Main Status Register. Bit 4 of the Main Status Register (Controller Busy) is not set. This allows a Seek Command to be issued for another drive even while the first drive is still seeking. This is called a Multiple Seek. All four drives may be seeking at the same time. No other command except the Seek Command or the Sense Interrupt Command should be issued while a Seek Command is in progress.

If the extended track range mode is enabled, a fourth byte should be written in the Command Phase to indicate the four most significant bits of the desired track number. Otherwise, only three bytes should be written.

**TABLE VII. Scan Command Termination Values**

Command	Status Register 2		Conditions
	D2	D3	
Scan Equal	0	1	Disk = $\mu P$
	1	0	Disk $\neq$ $\mu P$
Scan Low or Equal	0	1	Disk = $\mu P$
	0	0	Disk < $\mu P$
	1	0	Disk > $\mu P$
Scan High or Equal	0	1	Disk = $\mu P$
	0	0	Disk > $\mu P$
	1	0	Disk < $\mu P$

## Command Description (Continued)

### RECALIBRATE

The Recalibrate Command is very similar to the Seek Command. It is used to step a drive head out to track zero. Step pulses will be produced until the track zero signal from the drive becomes true. If the track zero signal does not go true before 255 step pulses are issued, an error is generated. If the extended track range mode is enabled, an error is not generated until 4095 pulses are issued.

Multiple recalibrations may be issued just like the Seek Command. No other command except the Recalibrate Command or the Sense Interrupt Command should be issued while a Recalibrate Command is in progress.

### SENSE INTERRUPT STATUS

An interrupt is generated by the controller when any of the following conditions occur:

- Upon entering the Result Phase of:
  - Read Data command
  - Read Deleted Data command
  - Write Data command
  - Write Deleted Data command
  - Read a Track command
  - Read ID command
  - Format command
  - Scan commands
- During data transfers in the Execution Phase while in the Non-DMA mode
- Ready signal from a drive changes state
- Seek or Recalibrate Command termination

An interrupt generated for reasons 1 or 2 above occurs during normal command operations and are easily discernible by the  $\mu$ P. During an execution phase in Non-DMA Mode, bit 5 (Execution Mode) in the Main Status Register is set to 1. Upon entering Result Phase this bit is set to 0. Reasons 1 and 2 do not require the Sense Interrupt Status command. The interrupt is cleared by reading or writing information to the data register.

Interrupts caused by reasons 3 and 4 are identified with the aid of the Sense Interrupt Status command. This command resets the interrupt when the command byte is written. Use bits 5, 6, and 7 of ST0 to identify the cause of the interrupt as shown in Table VIII.

Issuing a Sense Interrupt Status Command without an interrupt pending is treated as an invalid command.

If the extended track range mode is enabled, a third byte should be read in the Result Phase which will indicate the four most significant bits of the Present Track Number. Otherwise, only two bytes should be read.

### SPECIFY

The Specify command sets the initial values for each of the three internal timers. The timers have two modes as shown in Table IX. The timer modes are programmed from the Mode command. Mode One should be used if the controller is being interfaced to 8" drives. This mode could be interpreted as defining the timers to be Head Load and Head Unload timers. Mode Two should be used if a drive motor is being turned off and on as in a 5 $\frac{1}{4}$ " drive. The Motor On Time defines the time between when the Motor On signal is asserted and the start of the Read or Write operation. The Motor Off Time defines the time from the end of the Execution Phase of a command to when the Motor On pin is deasserted. The Step Rate Time defines the time interval between adjacent step pulses during a Seek, Implied Seek, or Recalibrate command.

The times stated in the table are affected by the Data Rate pin. If the pin is high, the table is correct. If the pin is low, the times in the table should be doubled.

The choice of DMA or Non-DMA operation is made by the Non-DMA bit. When this bit is 1 then Non-DMA mode is selected, and when this bit is 0, the DMA mode is selected. This command does not generate an interrupt.

TABLE VIII. Status Register 0 Termination Codes

Status Register 0			Cause
Interrupt Code		Seek End	
D7	D6	D5	
1	1	0	Ready Line Changed State
0	0	1	Normal Seek Termination
0	1	1	Abnormal Seek Termination

TABLE IX. Motor On/Off and Head Load/Unload Timer Definitions

Timer	Mode 1		Mode 2	
	Value	Range	Value	Range
Step Rate	(16-N) ms	1-16 ms	(16-N) ms	1-16 ms
Motor Off	N $\times$ 16 ms	0-240 ms	N $\times$ 512 ms	0-7.68 sec
Motor On	N $\times$ 2 ms	0-254 ms	N $\times$ 32 ms	0-4.064 sec

Note: Double all times if Data Rate pin is low.

## Command Description (Continued)

### SENSE DRIVE STATUS

This two-byte command obtains the status of the Drives. Status Register 3 is returned in the result phase and contains the drive status. This command does not generate an interrupt.

### MODE

This command is used to select the special features of the controller. The "" indicates the default which is used after being reset. This reset default has been chosen to be compatible with the  $\mu$ PD765. This command does not generate an interrupt.

- \* TMR = 0** Timers for motor on and motor off are defined for Mode 1 (see Specify command).
- TMR = 1** Timers for motor on and motor off are defined for Mode 2 (see Specify command).
- \* IAF = 0** The controller will format tracks with the Index Address Field included. (Exact IBM standard.)
- IAF = 1** The controller will format tracks without including the Index Address Field. This may increase the storage capability of each track. (ISO standard.)
- \* IPS = 0** The implied seek bit in the commands is ignored.
- IPS = 1** The implied seek bit in the commands is enabled so that if the bit is set in the command, a Seek will be performed automatically.
- \* DMC = 0** Only the motor of the drive selected is assumed on. This means that whenever a new drive is selected, the Motor On time is enabled.
- DMC = 1** All drive motors are assumed to be on when any motor is turned on. This eliminates the Motor On time when switching from one drive to another before the Motor Off time expires.
- LOW = \*00:** Completely disables the low power mode.
- PWR 01:** Go into low power mode automatically 500 ms after all drive motors are off. Will remain in this automatic mode until next Mode command.
- 10:** Go into low power mode now. Low power mode will be disabled again at next chip access.
- 11:** Not used.
- POL = 0** Disable polling mode. See Table X.
- \* POL = 1** Enable polling mode.
- \* ETR = 0** Header format is the IBM System 34 (double density) or System 3740 (single density).

**ETR = 1** Header format is the same as above but there are 12 bits of track number. The most significant bits of the track number are in the upper four bits of the head number byte.

**Low Current and Precomp Track #:** Track number to enable the low current output pin and to enable write precompensation. When the controller is writing to track numbers with a value which is less than this value, write precompensation is disabled and the low current output pin is deasserted. Default is track zero.

**\* DRE = 0** The data rate is determined by the Data Rate pin.

**DRE = 1** The data rate is determined by the bits set in the DATA RT field.

**ANR** (Abort Not Ready) The state of this bit, in conjunction with the POL bit, determines how the controller treats the drive ready signal. Table X describes how the controller responds to the Ready pin depending on the state of POL and ANR. Default is ANR = 1.

**\* WLD = 0** An FF(hex) from either the  $\mu$ P or the disk during a Scan Command is interpreted as a wildcard character that will always match true.

**WLD = 1** The Scan commands do not recognize FF(hex) as a wildcard character.

**Head Settle:** Time allowed for head to settle after an Implied Seek. Time =  $N \times 4$  ms, (0-60 ms). (Based on 8 MHz clock).

TABLE X. Polling and Abort Modes

POL	ANR	Comments
0	0	Do not check ready ever. All commands execute whether ready is true or not.
0	1	Wait up to 5 revs for ready. If ready is not true, wait up to 5 disk revolutions and if still not ready, abort the command.
1	0	Poll, but do not abort. All commands execute whether ready is true or not, but polling continues and ready change INTs are still issued.
1	1	Poll, and abort immediately if drive not ready (default).



## Command Description (Continued)

**DATA RT** After a Reset, the data rate is determined by the Data Rate pin. If the DRE bit is set, the data rate is determined by these two bits as shown in Table XI.

**Write Precomp** The value of these four bits determines the amount of write precompensation used when writing to the disk drive as shown in Table XII. The default value is based on the data rate used and can be found in Table XI.

### SET TRACK

This command is used to inspect or change the value of the internal Present Track Register. This could be useful for disk mistracking errors, where the real current track could be read through the Read ID command, and then the Set Track Command can set the internal present track register to the correct value.

The first byte of the command contains the command opcode and the R/W bit. If the R/W bit is low, a track register is to be read. In this case, the result phase contains the value in the internal register specified, and the third byte of the command is a dummy byte.

If the R/W bit is high, data is written to a track register. In this case the 3rd byte of the command phase is forced into the specified internal register, and the result phase contains the new byte value written.

The particular track register chosen to operate on is determined by the least significant 3 bits of the second byte of the command. The two LSB's select the drive (DR1, DR0), and the next bit (MSB) determines whether the least significant byte (MSB = 0) or the most significant byte (MSB = 1) of the track register is to be read/written. When not in the extended track range mode, only the LSB track register need be updated. In this instance, the MSB bit is set to 0.

This command does not generate an interrupt.

### INVALID COMMAND

If an invalid command (i.e., a command not defined) is received by the controller, the controller will respond with ST0 in the Result Phase. The controller does not generate an interrupt during this condition. Bits 6 and 7 in the Main Status Register are both set to one's, indicating to the processor that the controller is in the Result Phase and the contents of ST0 must be read. When the system reads ST0 it will find an 80 (hex) indicating an invalid command was received.

In some applications the user may use this command as a No-Op command to place the controller in a standby or no operation state. Simply issue an illegal command and delay reading the result phase until the controller is needed for another command. During this time, the Controller will not poll the drives.

TABLE XI. Data Rate Selection Table

Data Rate	FM		MFM		Default Precomp	
	f = 8 MHz	variable	f = 8 MHz	variable	f = 8 MHz	Binary
00	125K	1X	250K	2X	266 ns	0111
01	250K	2X	500K	4X	151 ns	0100
10	500K	4X	1000K	8X	75 ns	0010

Note: X = (f/64) bits/sec, where f = clock frequency.

TABLE XII. Write Precompensation Selection Table

Write Pre-Comp	Amount of Precompensation	
	f = 8 MHz	Variable
0 0 0 0	none	0X
0 0 0 1	36 ns	1X
0 0 1 0	75 ns	2X
0 0 1 1	116 ns	3X
0 1 0 0	151 ns	4X
0 1 0 1	179 ns	5X
0 1 1 0	229 ns	6X
0 1 1 1	266 ns	7X
1 0 0 0	286 ns	8X
1 0 0 1	338 ns	9X
1 0 1 0	357 ns	10X
1 0 1 1	411 ns	11X
1 1 0 0	429 ns	12X
1 1 0 1	464 ns	13X
1 1 1 0	Illegal Default	
1 1 1 1		

Note 1: X = 2/(7f) ns, where f = clock frequency.

Note 2: At a data rate of 1 Mbit/sec, only 0-107 ns are valid.

Note 3: These are typical values.

**Absolute Maximum Ratings** (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-0.5V to $V_{CC}$ + 0.5V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to $V_{CC}$ + 0.5V
Storage Temperature Range ( $T_{STG}$ )	-65°C to + 150°C
Power Dissipation ( $P_D$ )	500 mW
Lead Temperature ( $T_L$ )	
(Soldering 10 seconds)	260°C

**Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	4.75	5.25	V
Operating Temperature Range ( $T_A$ )	10	+70	°C
ESD Tolerance: $C_{ZAP} = 100$ pF			
$R_{ZAP} = 1500$ $\Omega$	1500		V

**DC Electrical Characteristics**  $V_{CC} = 5V \pm 10\%$  (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
$V_{IH}$	High Level Input Voltage		2.0		V
$V_{IL}$	Low Level Input Voltage			0.8	V
$I_{IN}$	Input Current (all pins) (Invert pin only)	$V_{IN} = V_{CC}$ or GND		$\pm 1.0$ $\pm 10$	$\mu A$ $\mu A$
$I_{CC}$	Average Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$ $f = 8.0$ MHz		40.0	mA
$I_{CC}$	Average Supply Current in Low Power Mode	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$		2.0	mA

 **$\mu P$  INTERFACE (D0-D7, INT, DRQ)**

$V_{OH}$	High Level Output Voltage	$I_{OUT} = -20$ $\mu A$ $I_{OUT} = -2.0$ mA	$V_{CC} - 0.1$ 3.5		V V
$V_{OL}$	Low Level Output Voltage	$I_{OUT} = 20$ $\mu A$ $I_{OUT} = 2.0$ mA		0.1 0.4	V V
$I_{OZ}$	Output TRI-STATE® Leakage Current	$V_{OUT} = V_{CC}$ or GND		$\pm 10.0$	$\mu A$

**OSCILLATOR (OSC2/CLK)**

$V_{IH}$	High Level Input Voltage	OSC1 = GND	2.4		V
$V_{IL}$	Low Level Input Voltage	OSC1 = GND		0.4	V
$I_{IN}$	Input Current	$V_{IN} = V_{CC}$ or GND		$\pm 1.6$	mA

**DISK INTERFACE (Read Data, Write Gate, Head Select, D0-D3, Write Data, Index, Track 0, Write Protect, Ready, Motor, Step, LCR/DIR, Seek Complete)**

$V_{OH}$	High Level Output Voltage (Invert pin low)	$I_{OUT} = -20$ $\mu A$ $I_{OUT} = -2.0$ mA	$V_{CC} - 0.1$ 3.5		V V
$V_{OL}$	Low Level Output Voltage	LCT/DIR $I_{OUT} = 20$ $\mu A$ $I_{OUT} = 16.0$ mA Others $I_{OUT} = 20$ $\mu A$ $I_{OUT} = 8.0$ mA		0.1 0.4 0.1 0.4	V V V V
$I_{LKG}$	Output High Leakage Current (Invert pin high)	$V_{OUT} = V_{CC}$ or GND		$\pm 10$	$\mu A$
$V_H$	Input Hysteresis		250 Typical		mV

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

# Phase Locked Loop Characteristics $V_{CC} = 5V \pm 5\%$ , $F_{XTAL} = 8\text{ MHz}$ unless otherwise specified

Symbol	Parameter	Conditions	Typ		Units
$V_{REF}$	SETCUR Pin Reference Voltage	$R_1 = 5.6\text{ k}\Omega$ , $V_{CC} = 5.0V$	1.1		V
$K_{VCO}$	VCO Gain (Note 1)	$t_{DATA} = 1\text{ }\mu s \pm 10\%$	25		Mrad/s/V
$R_1$	Recommended Pump Resistor Range		3–12		k $\Omega$
$K_{P(UP)}$	Charge Pump Up Current Gain ( $I_{REF}/I_{P(UP)}$ ) (Note 2)	$R_1 = 5.6\text{ k}\Omega$	2.50		(none)
$K_{P(DOWN)}$	Charge Pump Down Current Gain ( $I_{REF}/I_{P(DOWN)}$ ) (Note 2)	$R_1 = 5.6\text{ k}\Omega$	2.25		(none)
$K_{PLL}$	Internal Phase Locked Loop Gain (Note 3)	$R_1 = 5.6\text{ k}\Omega$	75 70		Mrad Mrad
$T_{SW}$	Static Window (Note 4)	$R_1 = 5.6\text{ k}\Omega$ 250 kb/s 500 kb/s 1.0 Mb/s	Early	Late	ns ns ns
			1075	872	
			530	440	
			259	234	
$T_{DW}$	Dynamic Window Margin (Note 5)	(Note)	65		%

**Note 1:** The VCO gain is measured at the 1.0 Mb/s data rate by forcing the data period over a range from 900 ns to 1100 ns, and measuring the resulting voltage on the filter pin. The best straight line gain is fit to the measured points.

**Note 2:** This is the current gain of the charge pump, which is defined as the output current divided by the current through  $R_1$ .

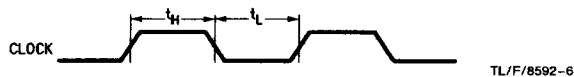
**Note 3:** This is the product of  $V_{REF} \times K_P \times K_{VCO}$ . The total variation in this specification indicates the total loop gain variation contributed by the internal circuitry. The  $K_{VCO}$  portion of this specification is measured at the 1.0 Mb/s data rate by forcing the data period over a range from 900 ns to 1100 ns, and measuring the resultant  $K_{VCO}$ .  $K_P$  is measured by forcing the Filter pin to 2.1V and measuring the ratio of the charge pump current over the input current.

**Note 4:** This part is guaranteed to correctly decode a single shifted clock pulse at the end of a long series of non-shifted preamble bits as long as the single shifted pulse is shifted less than the amount specified in  $T_{SW}$ . The length of the preamble is long enough for the PLL to lock. The filter components used are in Table II.

**Note 5:** Measurements made with a repeating "DB6" data pattern with reverse write precompensation, using recommended filter values. 25°C, 5.0V, 0% MSV.

# AC Electrical Characteristics $V_{CC} = 5V \pm 5\%$ , $C_L = 100\text{ pF}$ (unless otherwise specified)

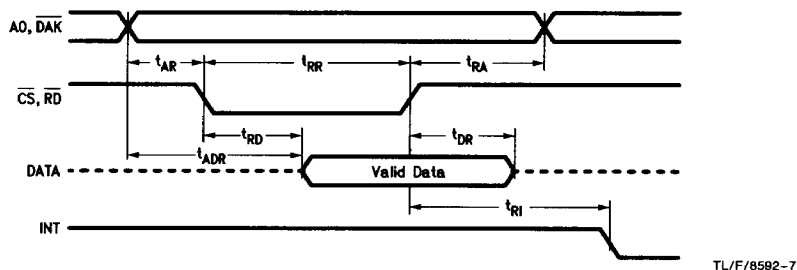
## CLOCK TIMING



Symbol	Parameter	Min	Max	Units
$F_{XTAL}$	Crystal or External Clock Frequency	4.0	8.0	MHz
$t_H$	Clock High Time	40		ns
$t_L$	Clock Low Time	40		ns
$t_{RW}$	Reset Pulse Width	100		ns

**Note 1:** The internal data separator will operate from 4–10 MHz. For frequencies from 1–4 MHz and 10–20 MHz, an external data separator and write precompensation circuit must be used.

## MICROPROCESSOR READ TIMING

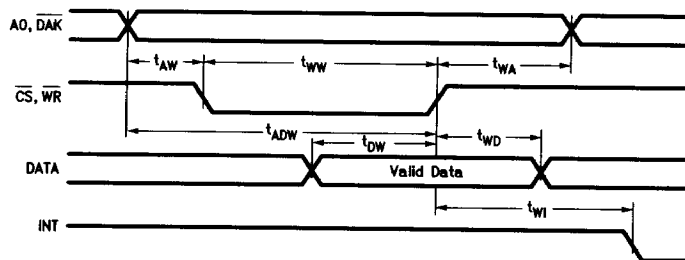


Symbol	Parameter	Min	Max	Units
$t_{AR}$	Address Valid to Read Strobe	10		ns
$t_{RA}$	Address Hold from Read Strobe	0		ns
$t_{RR}$	Read Strobe Width	75		ns
$t_{RD}$	Read Strobe and Chip Select to Data Valid		80	ns
$t_{ADR}$	Address Valid to Read Data		90	ns
$t_{DR}$	Data Hold from Read Strobe to High Impedance (TRI-STATE Note)	5	100	ns
$t_{RI}$	Clear INT from Read Strobe		65	ns

**TRI-STATE Note:** This limit includes the RC delay inherent in our test method. This signal will typically turn off within 15 ns, enabling other devices to drive this signal with no contention.

# AC Electrical Characteristics $V_{CC} = 5V \pm 5\%$ , $C_L = 100\text{ pF}$ (unless otherwise specified)

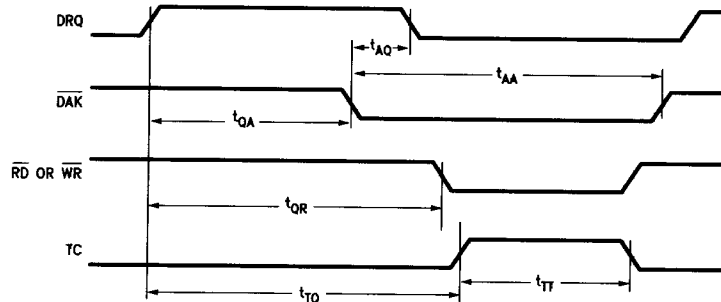
## MICROPROCESSOR WRITE TIMING



TL/F/8592-8

Symbol	Parameter	Min	Max	Units
$t_{AW}$	Address Valid to Leading Edge of Write Strobe	10		ns
$t_{WA}$	Address Hold from Write Strobe	0		ns
$t_{WW}$	Write Strobe Width	30		ns
$t_{ADW}$	Address Valid to Trailing Edge of Write Strobe	45		ns
$t_{DW}$	Data Setup to End of Write Strobe	20		ns
$t_{WD}$	Data Hold from Write Strobe	12		ns
$t_{WI}$	Clear INT from Write Strobe		65	ns

## DMA TIMING



TL/F/8592-9

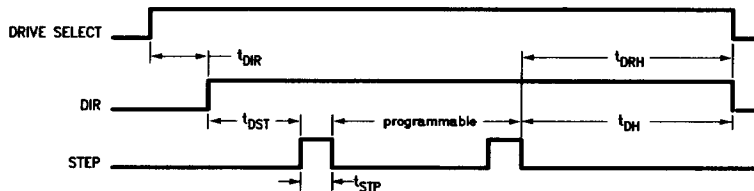
Symbol	Parameter	Min	Max	Units
$t_{AQ}$	End of DRQ from DAK		115	ns
$t_{QA}$	DAK assertion from DRQ	10		ns
$t_{AA}$	DAK Pulse Width	75		ns
$t_{QR}$	DRQ to Read or Write Strobe	10		ns
$t_{TQ}$	Time after last DRQ that TC must be asserted		Note 1	$\mu\text{s}$
$t_{TT}$	TC Strobe Width	50		ns

**Note:** During a DMA transfer, DAK is sufficient to acknowledge a data transfer. RD or WR is necessary only if data is to be presented to the data bus. Also, the DAK signal must go to a high level before the rising edge of DRQ to insure valid DMA transfers.

**Note 1:** The maximum  $t_{TQ}$  is equal to  $((1/\text{data rate} \times 8) - 1) \mu\text{s}$ . Data rate is the exact data transfer rate being used.

# AC Electrical Characteristics $V_{CC} = 5V \pm 5\%$ , $C_L = 100\text{ pF}$ (unless otherwise specified)

## DRIVE TRACK ACCESS TIMING



TL/F/8592-10

Symbol	Parameter	Min	Max	Units
$t_{DIR}$	Drive Select Setup Prior to Direction (Note 1)	6		$\mu\text{s}$
$t_{DRH}$	Drive Select Hold from End of Step (Note 1)	3		$\mu\text{s}$
$t_{DST}$	Direction Setup Prior to Step (Note 1)	6		$\mu\text{s}$
$t_{DH}$	Direction Hold from End of Step (Note 1)	3		$\mu\text{s}$
$t_{STP}$	Step Pulse Width (Note 1)	4		$\mu\text{s}$
$t_{IW}$	Index Pulse Width	500		ns

**Note 1:** Specification based on  $f = 8\text{ MHz}$ . Specification will vary with frequency as,  $t_f = t_{8.0}/f$ .

**Note:** Signals shown for non-Invert mode.

## READ DATA TIMING



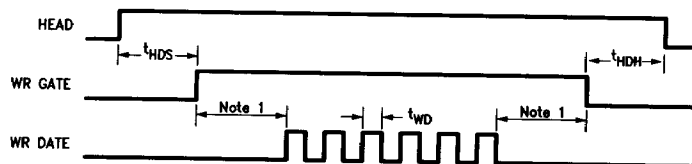
TL/F/8592-11

Symbol	Parameter	Min	Max	Units
$t_{RD}$	Read Data Pulse Width	25		ns

**Note:** Signals shown for non-Invert mode.

# AC Electrical Characteristics $V_{CC} = 5V \pm 5\%$ , $C_L = 100\text{ pF}$ (unless otherwise specified)

## DRIVE WRITE TIMING



TL/F/8592-12

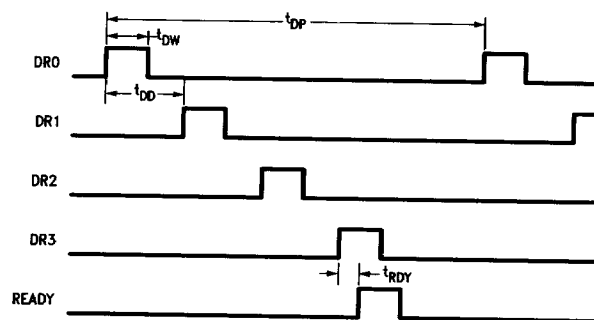
Symbol	Parameter	Min	Max	Units
$t_{HDS}$	Head Setup Time (Note 2)	50		$\mu\text{s}$
$t_{HDH}$	Head Hold Time (Note 2)	15		$\mu\text{s}$
$t_{WD}$	Write Data Pulse Width (Note 2)	100	900	ns

**Note 1:** Whenever WG is asserted, the Write Data line is active. At the end of each Write, one dummy byte is written before WG is deasserted.

**Note 2:** Specification based on  $f = 8\text{ MHz}$ . Specification will vary with frequency as,  $t_f = t_{8.0} (8.0/f)$ .

**Note 3:** Signals shown for non-Invert mode.

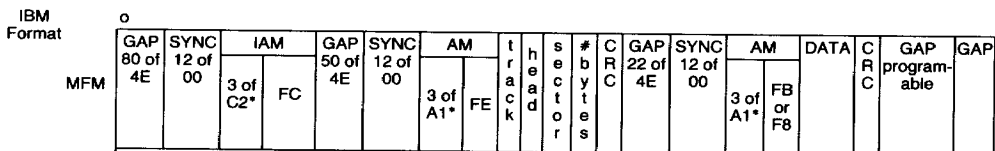
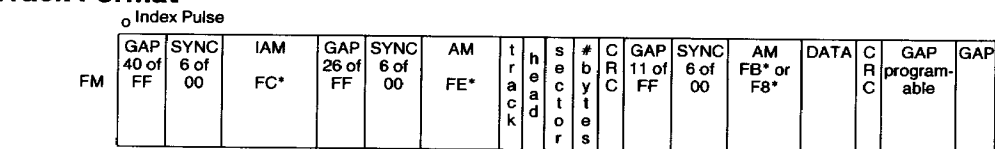
## POLLING MODE TIMING



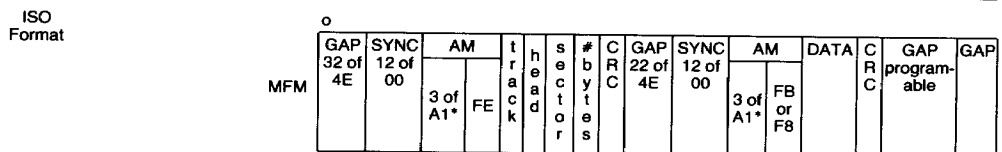
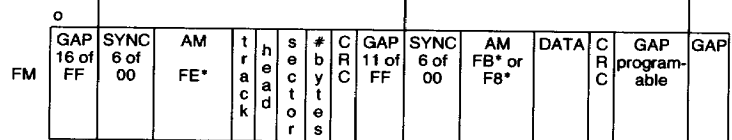
TL/F/8592-13

Symbol	Parameter	Max	Typical	Units
$t_{DP}$	Period of Polling Cycle		1	ms
$t_{DW}$	Drive Select Pulse Width		15	$\mu\text{s}$
$t_{DD}$	Time between Drive Selects		15	$\mu\text{s}$
$t_{RDY}$	READY Valid after Drive Select	4		$\mu\text{s}$

# Track Format



← Index Address Field →      ← Address Field →      ← Data Field →  
 Repeated for each sector



## Notes:

FE\* = Data pattern of FE, Clock pattern of C7  
 FC\* = Data pattern of FC, Clock pattern of D7  
 FB\* = Data pattern of FB, Clock pattern of C7  
 F8\* = Data pattern of F8, Clock pattern of C7  
 A1\* = Data pattern of A1, Clock pattern of 0A  
 C2\* = Data pattern of C2, Clock pattern of 14

All byte counts in decimal.

All byte values in hex.

CRC uses standard polynomial  $x^{16} + x^{12} + x^5 + 1$ .

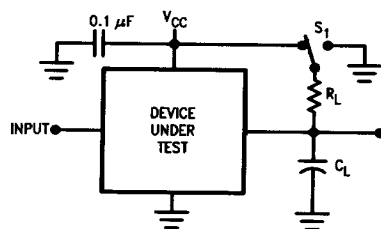
## AC Timing Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	6 ns
Input and Output Reference Levels	1.3V
TRI-STATE Reference Levels	High Level -0.5V
	Low Level +0.5V
Output Load	(see figure)

CAPACITANCE  $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$

Parameter	Description	Typ	Max	Units
$C_{IN}$	Input Capacitance	7	12	pF
$C_{OUT}$	Output Capacitance	7	12	pF

Note: This parameter is sampled and not 100% tested.



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## Notes:

$C_L = 100\text{ pF}$ , includes scope and jig capacitance.

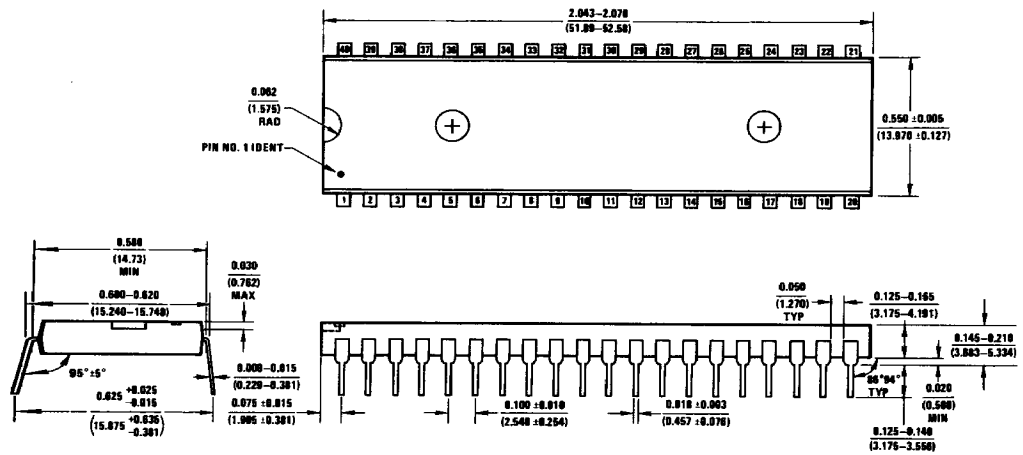
$R_L = 2.2\text{ k}\Omega$

$S_1 = V_{CC}$  for high impedance to active low and active low to high impedance measurements.

$S_1 = \text{GND}$  for high impedance to active high and active high to high impedance measurements.



# Physical Dimensions inches (millimeters)



**Dual-In-Line Package**  
**Order Number DP8472N**  
**NS Package Number N40A**

N40A (REV E)

