

LOGIC

DEVICES INCORPORATED

LPR520/521**4 x 16-bit Multilevel Pipeline Register****FEATURES**

- Four 16-bit Registers
- Implements Double 2-Stage Pipeline or Single 4-Stage Pipeline Register
- Hold, Shift, Load Instructions
- Separate Data In and Data Out Pins
- High Speed, Low Power CMOS Technology
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
 - 40-pin Plastic DIP
 - 40-pin Sidebrazed, Hermetic DIP
 - 44-pin Plastic LCC, J-Lead
 - 44-pin Ceramic LCC (Type C)

DESCRIPTION

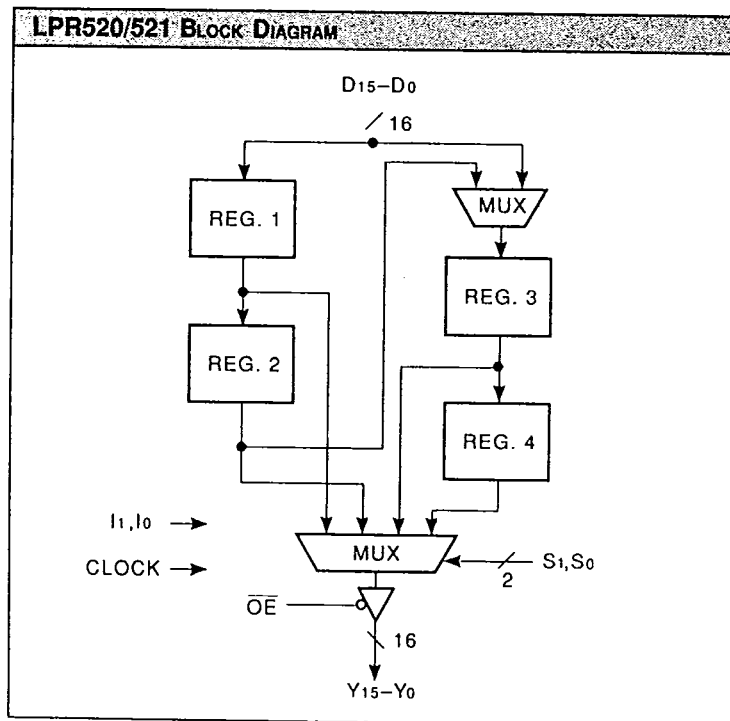
The Logic Devices LPR520 and LPR521 are functionally compatible with the Advanced Micro Devices AM29520 and AM29521 but are 16 bits wide. They are implemented in low power CMOS.

The LPR520 and LPR521 contain four registers which can be configured as two independent, 2-level pipelines or as one 4-level pipeline.

The Instruction pins, I₀ and I₁, control the loading of the registers. For either device, the registers may be configured as a four-stage delay line, with data loaded into R₁ and shifted sequentially through R₂, R₃, and R₄. Also, for the LPR520, data may be loaded from the inputs into either R₁

or R₃ with only R₂ or R₄ shifting. The LPR521 devices differ from the LPR520 in that R₂ and R₄ remain unchanged during this type of data load, as shown in Tables 1 and 2. Finally, I₀ and I₁ may be set to prevent any register from changing.

The S₀ and S₁ select lines control a 4 to 1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allows simultaneous write and read operations on different registers.

LPR520/521 BLOCK DIAGRAM**TABLE 1**

I ₁	I ₀	L29C520 Instruction
L	L	D→R ₁ R ₁ →R ₂ R ₂ →R ₃ R ₃ →R ₄
L	H	HOLD HOLD D→R ₃ R ₃ →R ₄
H	L	D→R ₁ R ₁ →R ₂ HOLD HOLD
H	H	ALL REGISTERS ON HOLD

TABLE 2

I ₁	I ₀	L29C521 Instruction
L	L	D→R ₁ R ₁ →R ₂ R ₂ →R ₃ R ₃ →R ₄
L	H	HOLD HOLD D→R ₃ HOLD
H	L	D→R ₁ HOLD HOLD HOLD
H	H	ALL REGISTERS ON HOLD

TABLE 3

S ₁	S ₀	Reg. Selected
L	L	Reg 4
L	H	Reg 3
H	L	Reg 2
H	H	Reg 1



DEVICES INCORPORATED

40E D ■ 5565905 0001510 9 ■ LDI
LOGIC DEVICES INC

LPR520/521

4 x 16-bit Multilevel Pipeline Register

MAXIMUM RATINGS Above which useful life may be impaired (Notes 1, 2, 3, 8)

T-46-09-09

Storage temperature	-65°C to +150°C
Operating ambient temperature	-55°C to +125°C
V _{CC} supply voltage with respect to ground	-0.5 V to +7.0 V
Input signal with respect to ground	-3.0 V to +7.0 V
Signal applied to high impedance output	-3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V _{CC} ≤ 5.25 V
Active Operation, Military	-55°C to +125°C	4.50 V ≤ V _{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _{OH}	Output High Voltage	I _{OH} = -2.0 mA	2.4			V
V _{OL}	Output Low Voltage	I _{OL} = 8.0 mA			0.5	V
V _{IH}	Input High Voltage		2.0		V _{CC}	V
V _{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I _{IX}	Input Current	Ground ≤ V _{IN} ≤ V _{CC} (Note 12)			±20	μA
I _{OZ}	Output Leakage Current	Ground ≤ V _{OUT} ≤ V _{CC} (Note 12)			±20	μA
I _{OS}	Output Short Current	V _{OUT} = Ground, V _{CC} = Max (Notes 4, 8)			-250	mA
I _{CC1}	V _{CC} Current, Dynamic	(Notes 5, 6)		10	40	mA
I _{CC2}	V _{CC} Current, Quiescent	(Note 7)			1.0	mA

4 x 16-bit Multilevel Pipeline Register

SWITCHING CHARACTERISTICS

(T-46-09-09)

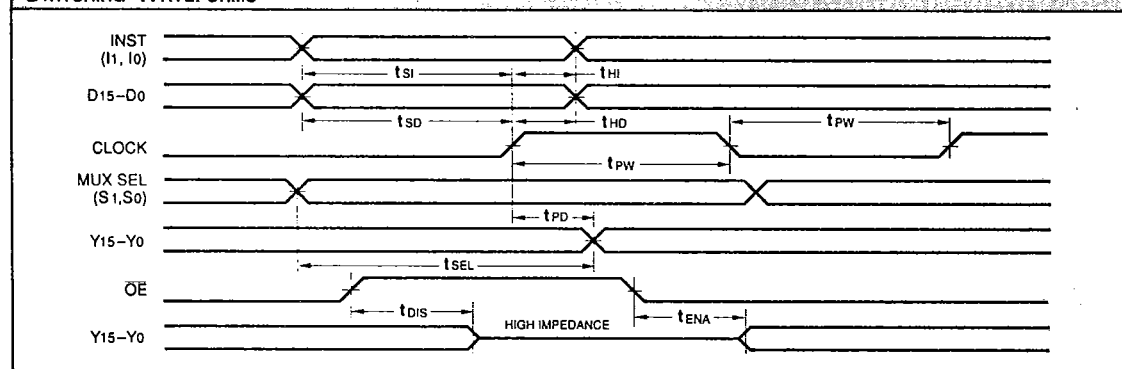
COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)

Symbol	Parameter	LPR520/521-					
		25		22		15	
		Min	Max	Min	Max	Min	Max
t _{PD}	CLK to Y ₁₅ -Y ₀		25		22		15
t _{SEL}	S ₁ ,S ₀ to Y ₁₅ -Y ₀		25		20		15
t _{SD}	D ₁₅ -D ₀ to CLK Setup	13		10		6	
t _{HD}	CLK to D ₁₅ -D ₀ Hold	3		3		1	
t _{SI}	I ₁ ,I ₀ to CLK Setup	13		10		6	
t _{HI}	CLK to I ₁ ,I ₀ Hold	3		3		1	
t _{DIS}	$\overline{OE}$ to Output Disable (Note 11)		25		15		12
t _{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		21		15
t _{PW}	Clock Pulse Width	10		10		8	

MILITARY OPERATING RANGE (-55°C to +125°C) Notes 9, 10 (ns)

Symbol	Parameter	LPR520/521-					
		30		24		18	
		Min	Max	Min	Max	Min	Max
t _{PD}	CLK to Y ₁₅ -Y ₀		30		24		18
t _{SEL}	S ₁ ,S ₀ to Y ₁₅ -Y ₀		30		22		18
t _{SD}	D ₁₅ -D ₀ to CLK Setup	15		10		8	
t _{HD}	CLK to D ₁₅ -D ₀ Hold	5		3		2	
t _{SI}	I ₁ ,I ₀ to CLK Setup	15		10		8	
t _{HI}	CLK to I ₁ ,I ₀ Hold	5		3		2	
t _{DIS}	$\overline{OE}$ to Output Disable (Note 11)		20		16		13
t _{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		22		16
t _{PW}	Clock Pulse Width	15		10		9	

SWITCHING WAVEFORMS



4 x 16-bit Multilevel Pipeline Register

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.
2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.
3. This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at GND - 0.6 V.
4. Duration of the output short circuit should not exceed 30 seconds.
5. Supply current for a given application can be accurately approximated by:

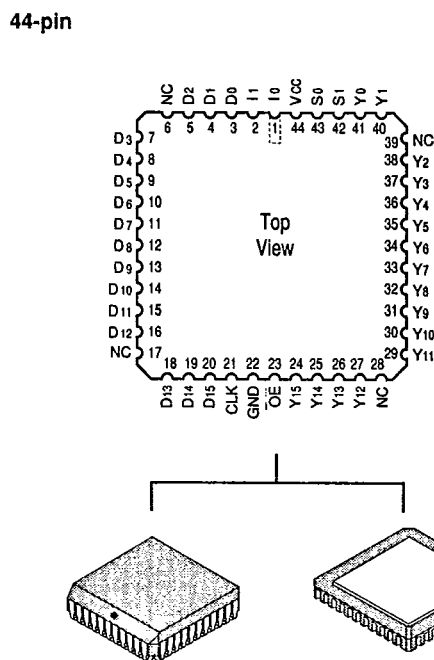
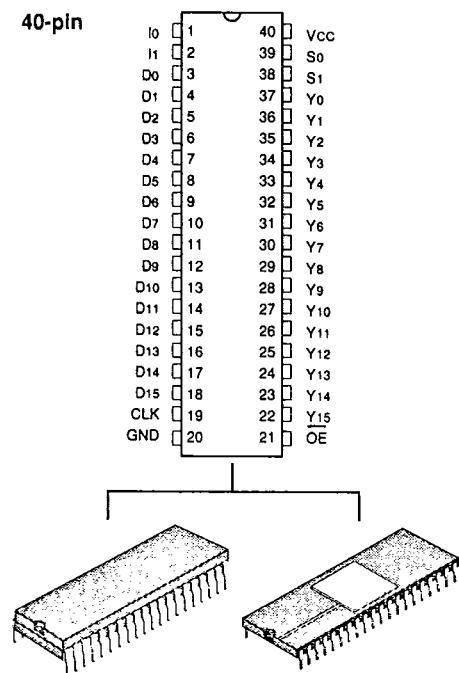
$$\frac{NCV^2F}{4}$$
 where
 N = total number of device outputs
 C = capacitive load per output
 V = supply voltage
 F = clock frequency
6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.
7. Tested with all inputs within 0.1 V of VCC or Ground, no load.
8. These parameters are guaranteed but not 100% tested.
9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified IOH and IOL at an output voltage of VOH min and VOL max respectively. Alternatively, a diode bridge with upper and lower current sources of IOH and IOL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and t_{DISABLE} measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
11. Transition is measured ±200 mV from steady-state voltage with specified loading.
12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.
- a. A 0.1 μF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.
- b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.
- c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

4 x 16-bit Multilevel Pipeline Register

ORDERING INFORMATION

T-46-09-09



Speed	Plastic DIP (P3)	Sidebraze Hermetic DIP (D3)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — COMMERCIAL SCREENING			
25 ns 22 ns 15 ns	LPR520PC or LPR521PC	$\begin{cases} 25 \\ 22 \\ 15 \end{cases}$ LPR520DC or LPR521DC	$\begin{cases} 25 \\ 22 \\ 15 \end{cases}$ LPR520JC or LPR521JC	$\begin{cases} 25 \\ 22 \\ 15 \end{cases}$ LPR520KC or LPR521KC
	-55°C to +125°C — COMMERCIAL SCREENING			
30 ns 24 ns 18 ns		$\begin{cases} 30 \\ 24 \\ 18 \end{cases}$ LPR520DM or LPR521DM		$\begin{cases} 30 \\ 24 \\ 18 \end{cases}$ LPR520KM or LPR521KM
	-55°C to +125°C — EXTENDED SCREENING			
30 ns 24 ns 18 ns		$\begin{cases} 30 \\ 24 \\ 18 \end{cases}$ LPR520DME or LPR521DME		$\begin{cases} 30 \\ 24 \\ 18 \end{cases}$ LPR520KME or LPR521KME
	-55°C to +125°C — MIL-STD-883 COMPLIANT			
30 ns 24 ns 18 ns		$\begin{cases} 30 \\ 24 \\ 18 \end{cases}$ LPR520DMB or LPR521DMB		$\begin{cases} 30 \\ 24 \\ 18 \end{cases}$ LPR520KMB or LPR521KMB

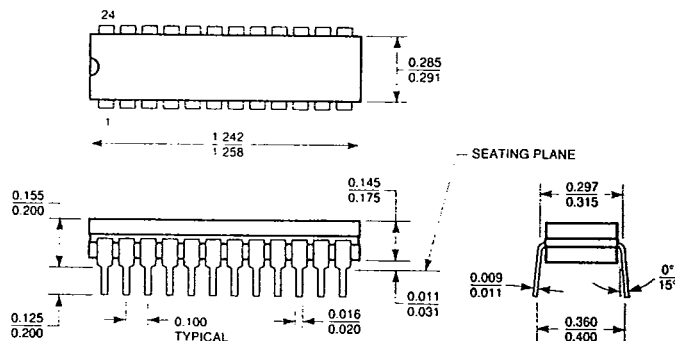


Mechanical Drawings

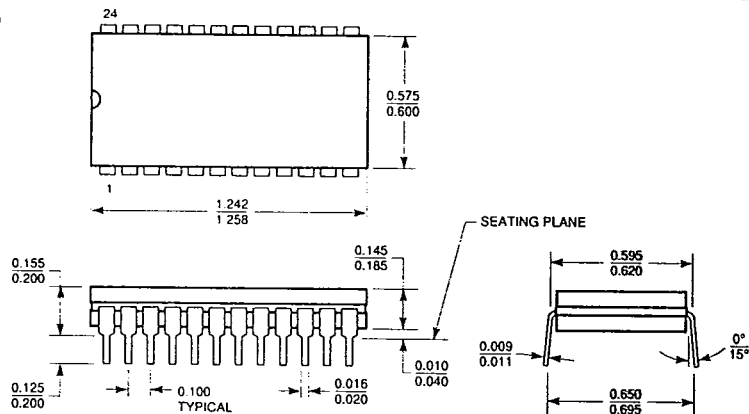
CerDIP — TYPE C

C1 — 24-pin CerDIP
(0.3" Wide)

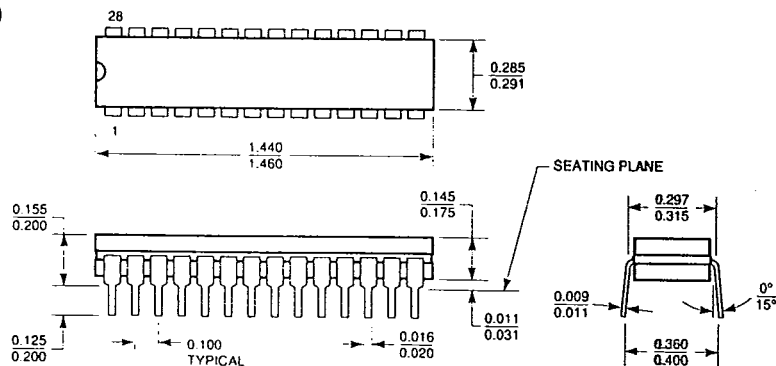
T-90-20

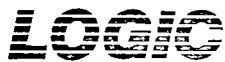


C4 — 24-pin CerDIP
(0.6" Wide)



C5 — 28-pin CerDIP
(0.3" Wide)



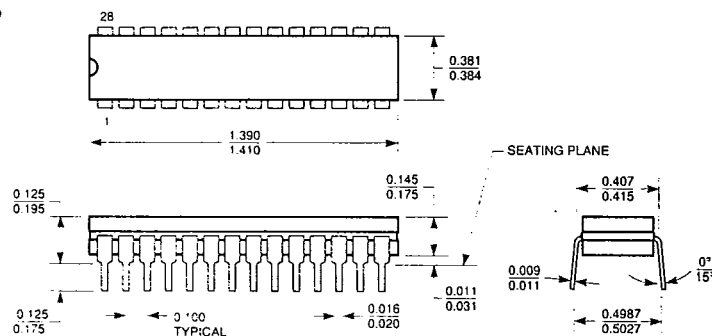


Mechanical Drawings

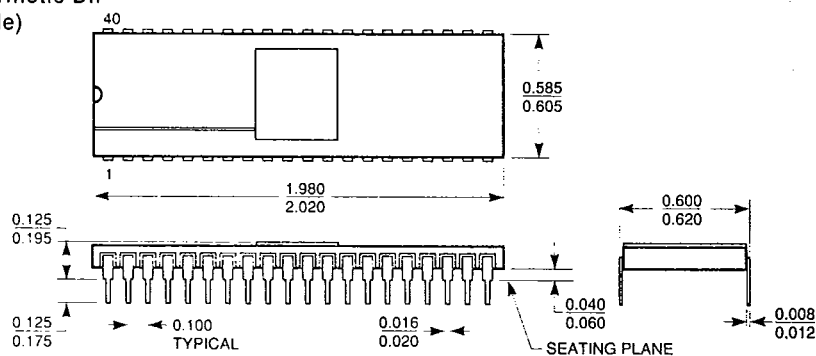
DEVICES INCORPORATED

T-90-20

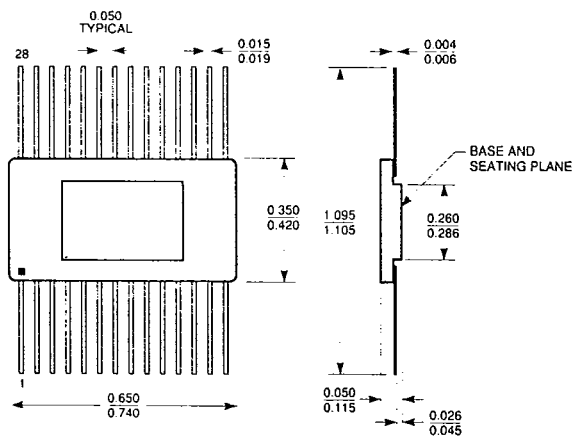
CERDIP — TYPE C

C10 — 28-pin CerDIP
(0.4" Wide)

SIDE BRAZE, HERMETIC DIP — TYPE D

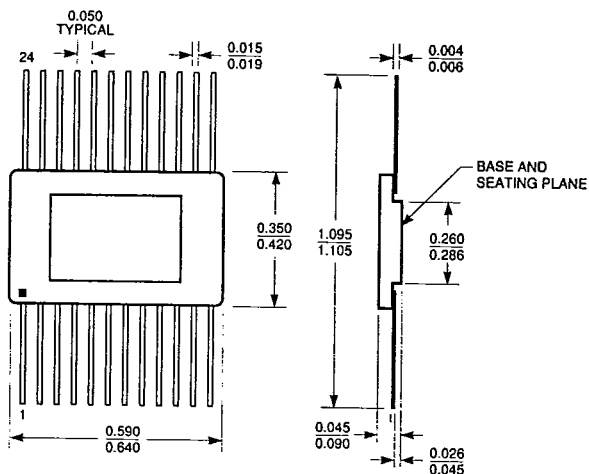
D3 — 40-pin Hermetic DIP
(0.6" Wide)

CERAMIC FLAT PACK — TYPE F

F1 — 24-pin Ceramic
Flat Pack

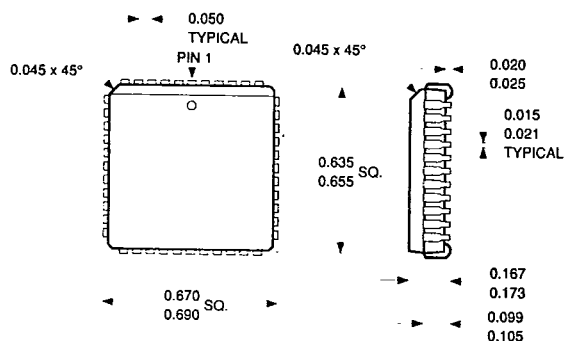
CERAMIC FLAT PACK — TYPE F

F2 — 28-pin Ceramic Flat Pack

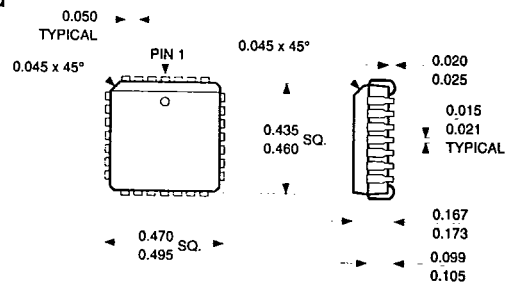


PLASTIC J-LEAD CHIP CARRIER — TYPE J

**J1 — 44-pin Plastic J-Lead
(0.690" x 0.690")**



**J4 — 28-pin Plastic J-Lead
(0.490" x 0.490")**





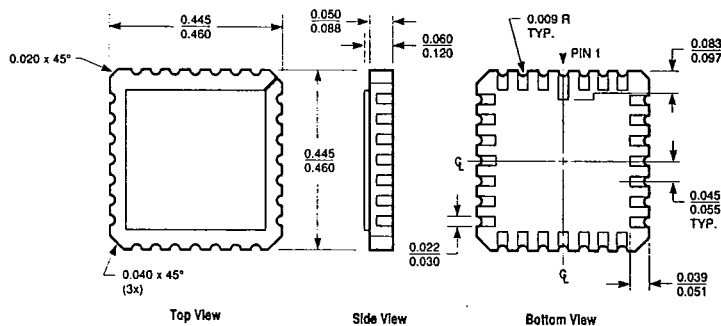
Mechanical Drawings

DEVICES INCORPORATED

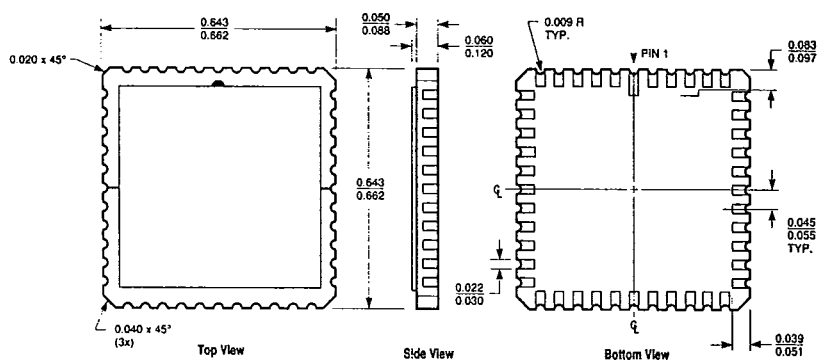
T-90-20

CERAMIC LEADLESS CHIP CARRIER — TYPE K

K1 — 28-pin Ceramic LCC (0.450" x 0.450")

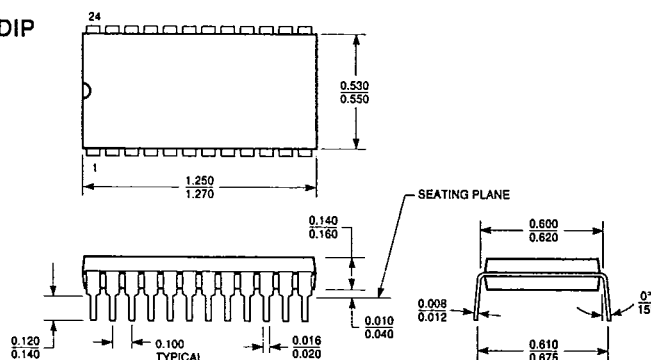


K2 — 44-pin Ceramic LCC (0.650" x 0.650")



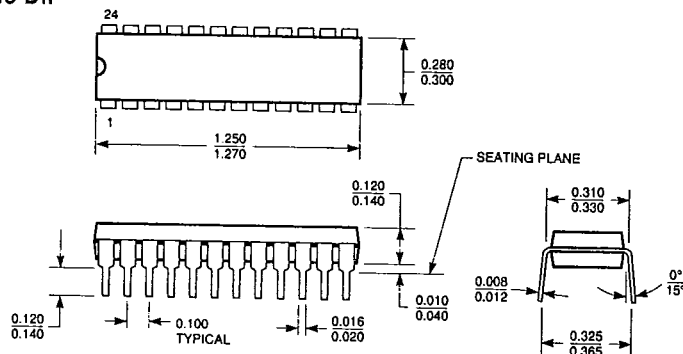
PLASTIC DIP — TYPE P

P1 — 24-pin Plastic DIP (0.6" Wide)

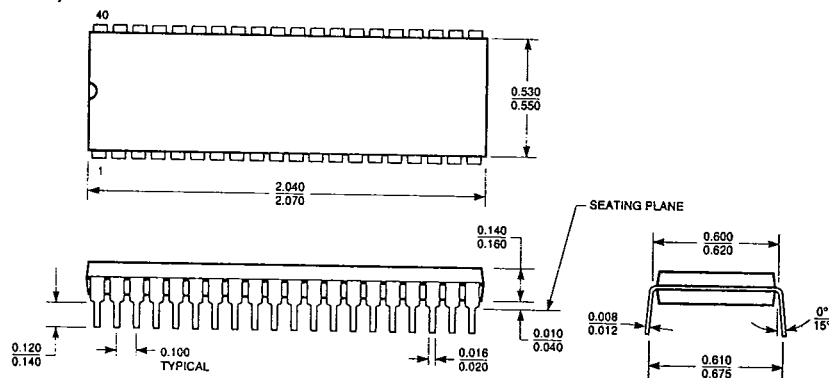


PLASTIC DIP — TYPE P

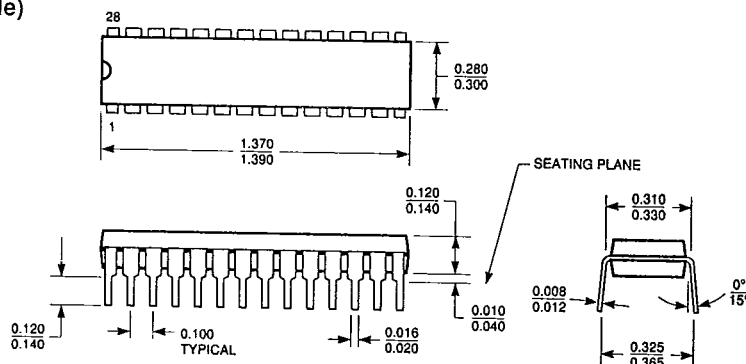
**P2 — 24-pin Plastic DIP
(0.3" Wide)**



**P3 — 40-pin Plastic DIP
(0.6" Wide)**



**P10 — 28-pin Plastic DIP
(0.3" Wide)**



LOGIC**Mechanical Drawings**

DEVICES INCORPORATED

T-90-20

PLASTIC DIP — TYPE P**P11 — 28-pin Plastic DIP**
(0.4" wide)