LR3740/LR3740N Synchronous Signal Generator for 2/3" CCD

■ Description

The LR3740/LR3740N is a CMOS synchronous signal generator LSI which generates TV synchronous pulse and other pulses for NTSC video cameras.

The LR3740 can be synchronized with external signals (generator locking) by using H reset, V reset, FH/2 reset and clock IN inputs.

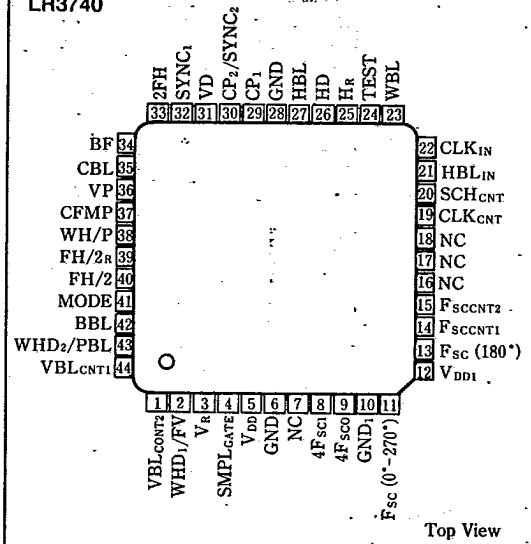
The LR3740 is designed for industry-use packaged in 44-pin QFP, and the LR3740N is for consumer-use packaged in 24-pin SOP.

■ Features

1. Low power consumption
2. +5V single power supply
3. SC-H phase control
4. Synchronized with external signals (generator locking)
5. 44-pin quad flat package : LR3740
   24-pin small outline package : LR3740N

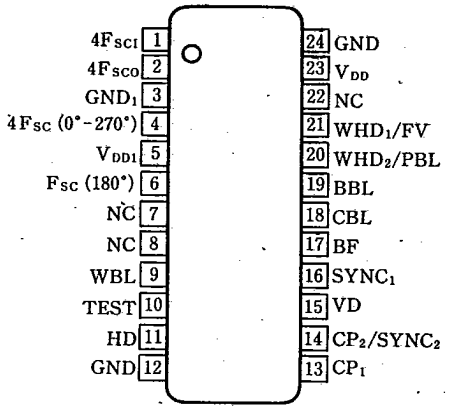
■ Pin Connections

LR3740



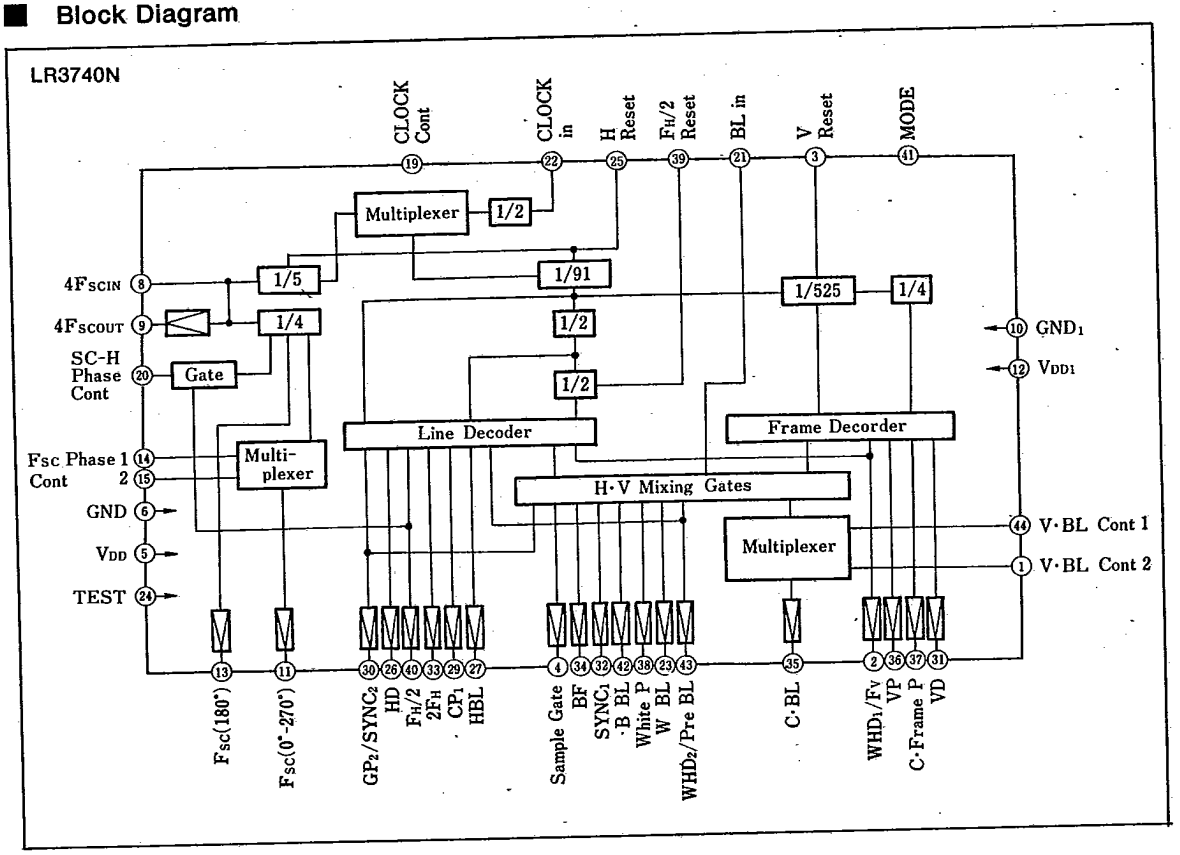
Top View

LR3740N



Top View

Block Diagram



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■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{DD}, V_{DD1}	GND−0.3 to +6.0	V	1, 2
Input voltage	V_I	GND−0.3 to (V_{DD}·V_{DD1})+0.3	V	2
Output voltage	V_O	GND−0.3 to (V_{DD}·V_{DD1})+0.3	V	2
Power dissipation	P_D	400	mW	3
Operating temperature	T_{opr}	−20 to +70	℃	
Storage temperature	T_{stg}	−55 to +150	℃	

Note 1 : $V_{DD}=V_{DD1}$
Note 2 : Referenced to GND
Note 3 : Ta=70℃

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}, V_{DD1}	4.5	5.0	5.5	V	1
Input voltage	V_I	GND		V_{DD}	V	1
Operating temperature	t_{opr}	−20		+70	℃	
Oscillation frequency	f_{CK}		14.31818		MHz	

Note 1 : Referenced to GND

■ Electrical Characteristics

(V_{DD}, V_{DD1}=5.0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IL}		0		1.0	V	
	V_{IH}		4.0		5.0	V	
Output voltage	I_{OL}	V_{OL}=0.4V	−0.25			mA	1
	I_{OH}	V_{OH}=4.6V	0.25			mA	
Input current 1	I_{IL1}	V_{IL}=0V			−1.0	μA	2
	I_{IH1}	V_{IH}=5.0V			1.0	μA	
Input current 2	I_{IL2}	V_{IL}=0V		−100	−250	μA	3
	I_{IH2}	V_{IH}=5.0V			1.0	μA	
Input current 3	I_{IL3}	V_{IL}=0V			−1.0	μA	4
	I_{IH3}	V_{IH}=5.0V		100	250	μA	
Current dissipation	I_{opr}	All I/O pins open		4.5	10	mA	5
Fsc phase error	$\Delta\phi_{SC}$	F_{SC} 0° to 270° pin	−5		+5	dig	6

Note 1 : Applied to all output pins.
Note 2 : Applied to 4 F_{SCIN} pins.
Note 3 : Applied to F_{SC} PHASE Cont 1, 2, SC-H PHASE Cont, $Clock_{IN}$ Cont, $Clock_{IN}$, H·BL_{IN}, H·Reset, V·Reset, and F_H/2 Reset pins.
Note 4 : Applied to output switch V·BL Cont 1, 2 and TEST pins.
Note 5 : Refer to the test circuit example 1.
Note 6 : Referenced to Fsc 180° pin.

■ Switching Characteristics

($V_{DD}=V_{DD1}$=5.0V, C_L=20pF, Ta=−20 to +60℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Rise time	V_r		20	70	ns	
Fall time	V_f		20	70	ns	
Propagation time difference	Δt_{pd}		50	100	ns	1

Refer to the test circuit example 2. The PG has 1/2 duty ratio.
Note 1 : H·BL pin as reference (difference from designed value)

Pin Description

Pin No.		Symbol	Function	Note
LR3740	LR3740N			
1	—	VBL_{CNT2}	Control input of CBL vertical BL time	PD
2	21	WHD_1/FV	*1 WHD=H cycle output *2 FV=V cycle output	
3	—	V_R	Counter reset input	PU
4	—	$SMPL_{GATE}$	Composite output	
5	23	V_{DD}	Power supply	
6	24	GND	Ground	
7	22	NC	Non connection	
8	1	4 F_{SCIN}	14.31818MHz	OG
9	2	4 F_{SCOUT}	14.31818MHz	
10	3	GND_1	Ground 1	
11	4	F_{SC} (0°-270°)	3.579545MHz output, Phase select output (0°-270°)	
12	5	V_{DD1}	Power supply 1	
13	6	F_{SC} 180°	3.579545MHz output (180°)	
14	—	F_{SCCNT1}	Control input of F_{SC} 0°-270° phase	PU
15	—	F_{SCCNT2}	Control input of F_{SC} 0°-270° phase	PU
16	7	NC	Non connection	
17	8	NC	Non connection	
18	—	NC	Non connection	
19	—	CLK_{CNT}	Input selection	PU
20	—	SCH_{CNT}	Control input of fsc 180° and H cycle phase fix and release	PU
21	—	HBL_{IN}	Input of HBL time of CBL	
22	—	CLK_{IN}	5.727272MHz input	PU
23	9	WBL	Composite output	
24	10	TEST	Test input	PD
25	—	H_R	H counter reset input	PU
26	11	HD	H cycle output	
27	—	HBL	H cycle output	
28	12	GND	Ground	
29	13	CP_1	H cycle output	
30	14	CP_2/$SYNC_2$	*1 CP2=H cycle output *2 SYNC2=composite output	
31	15	VD	V frequency output	
32	16	$SYNC_1$	Composite output	
33	—	2FH	H/Z frequency output	
34	17	BF	Composite output	
35	18	CBL	Composite output	
36	—	VP	V frequency output	
37	—	CFMP	4 V frequency output	
38	—	WH/P	Composite output	
39	—	$FH/2_R$	Input of FH/2 output reset	PU
40	—	FH/2	2H frequency output	
41	—	MODE	Consumer use/industrial use switching input	PD
42	19	BBL	Composite output	
43	20	WHD_2/PBL	*1 WHD 2=H frequency output *2 Pre BL=composite output	
44	—	VBL_{CNT1}	Control input of CBL vertical BL time	PD

*1 : LR3740N, *2 : LR3740
Note PD : Pull-down resistor
PU : Pull-up resistor

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■ Input Pin Description

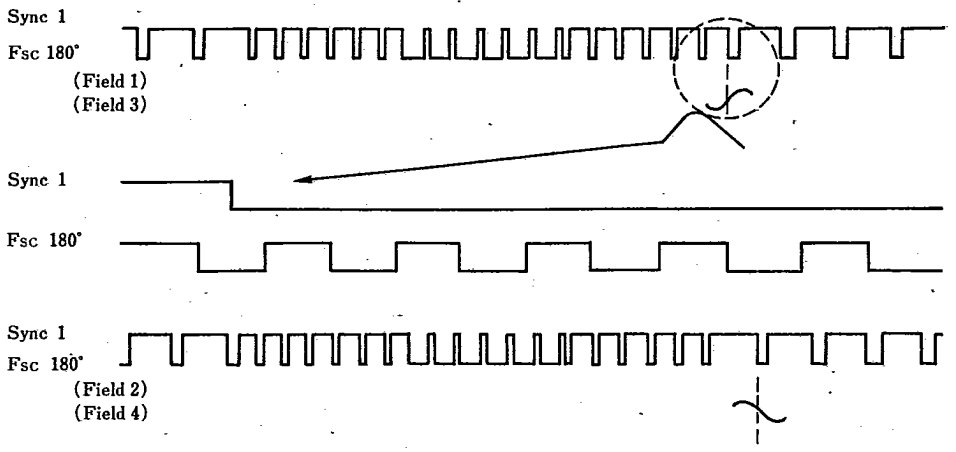
(1) F_{SC} phase cont 1, 2 (Pull-up resistor)

Parameter	Input level			
F_{SC} PHASE Cont 1	L	L	H	H
F_{SC} PHASE Cont 2	L	H	L	H
F_{SC} 0°-270° output	0°	90°	180°	270°

L : Low, H : High

(2) SCH phase cont (Pull-up resistor)

The F_{SC} and SYNC 1 phases are fixed with the SCH PHASE cont. to go High, and released to go Low.



Note : To adjust the SC phase meets the SCH standards (EIA RS-170A)

(3) CLOCK In cont (Pull-up resistor)

The internal clock frequency is selected with the CLOCK In Cont. To go High, and 1/2 dividing clock frequency is selected to go Low.

(4) Output switch (Pull-down resistor)

Each output for the LR3740N is selected with the output switch to go High, and each output for the LR3740 is selected to go Low.

(5) VBL cont 1, 2 (Pull-down resistor)

Parameter	Input level			
VBL Cont 1	L	L	H	H
VBL Cont 2	L	H	L	H
VBL width of C·BL	20H	19H	18H	17H

L : Low, H : High

(6) HBL In (Pull-up resistor)

As for the LR3740, going the HBL in Low during HBL period of CBL outputs Low.

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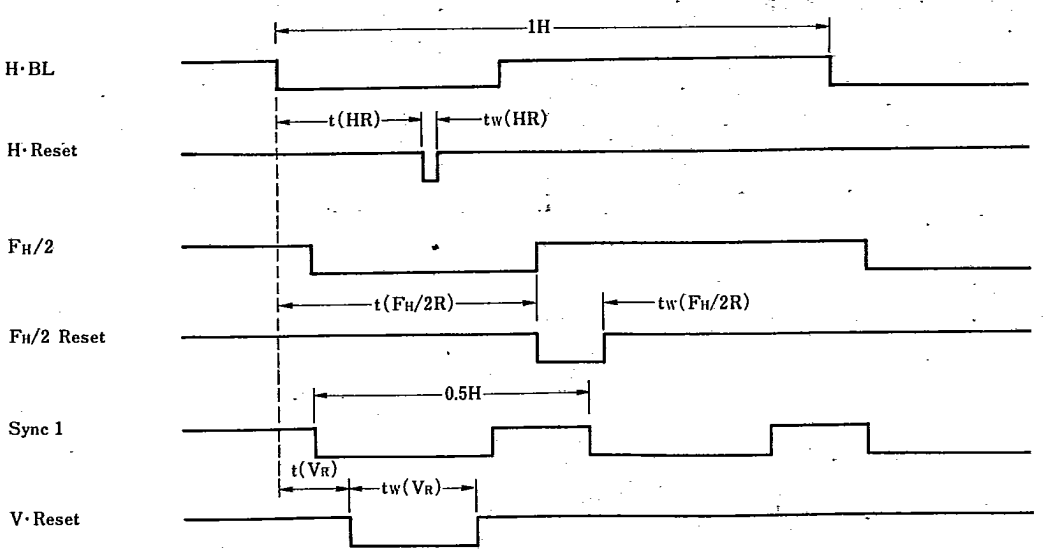
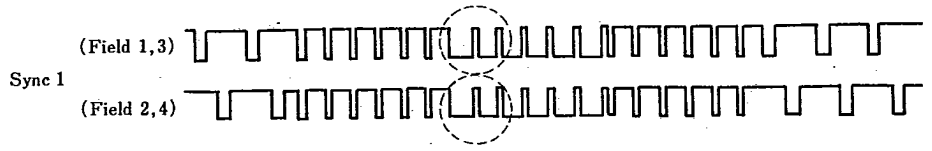
(7) H·Reset, V·Reset, FH/2 Reset (Pull-up resistor)





Parameter		Symbol	Time
H·Reset (1H cycle)	Reset Pulse falling phase	t (HR)	23.5T to 24.5T (Note 1)
	Reset Pulse width	t_W (HR)	1T or more
$F_{H/2}$ Reset (2H cycle or once)	Reset Pulse rising phase	t (F_H/2R)	20.5T to 185.5T (Note 2)
	Reset Pulse width	t_W (F_H/2R)	1T or more
V·Reset (1V cycle)	Reset Pulse falling phase	t (VR)	5.5T to 95T
	Reset Pulse width	t_W (VR)	4T or more

Note 1 : The reset position of H Reset is determined according to the point of single element.
Note 2 : t (F_H/2R)+t_W (F_H/2R)=21.5T−184.5T

(8) TEST (Pull-down resistor)

The output waveforms shown in the Timing Diagram are output with the TEST input to go Low, and tested to go High.

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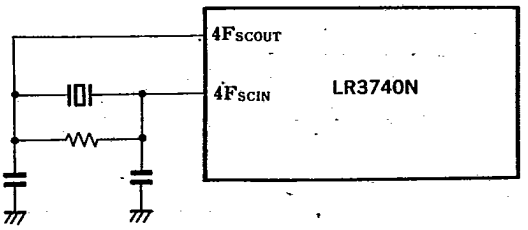
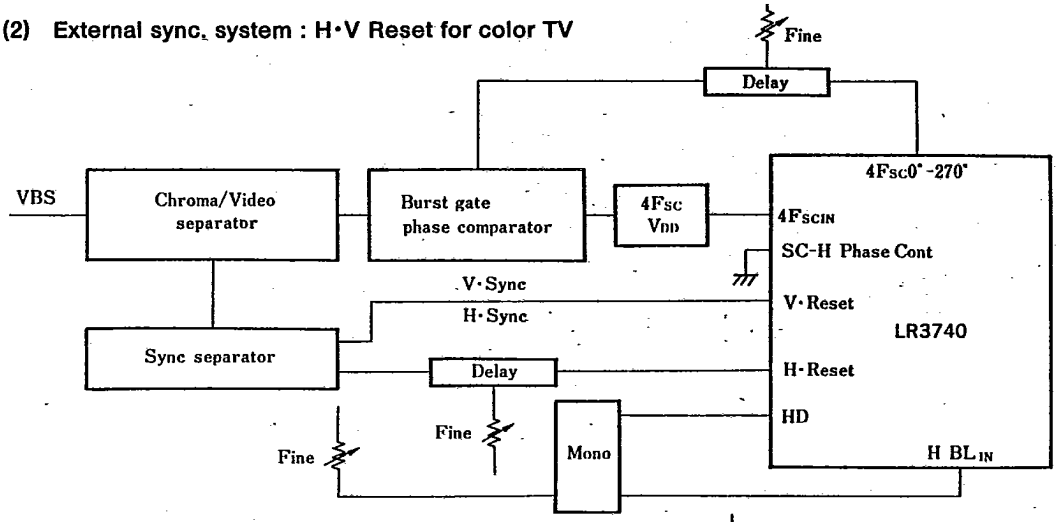
■ Application Circuit Example

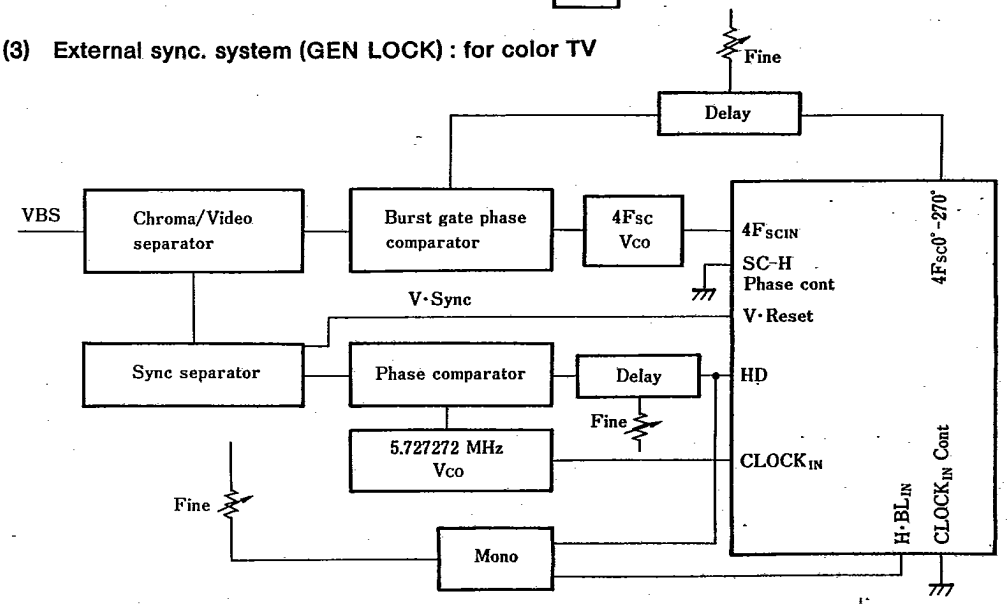
(1) Internal sync. system : for color TV



(2) External sync. system : H·V Reset for color TV



(3) External sync. system (GEN LOCK) : for color TV



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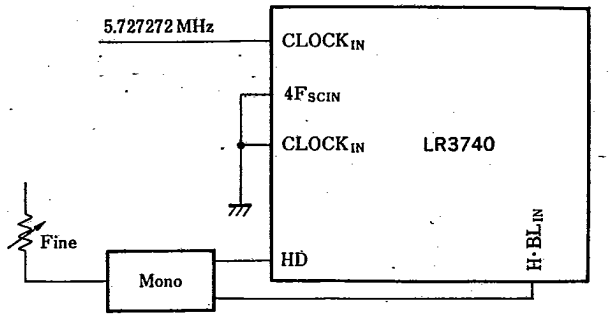
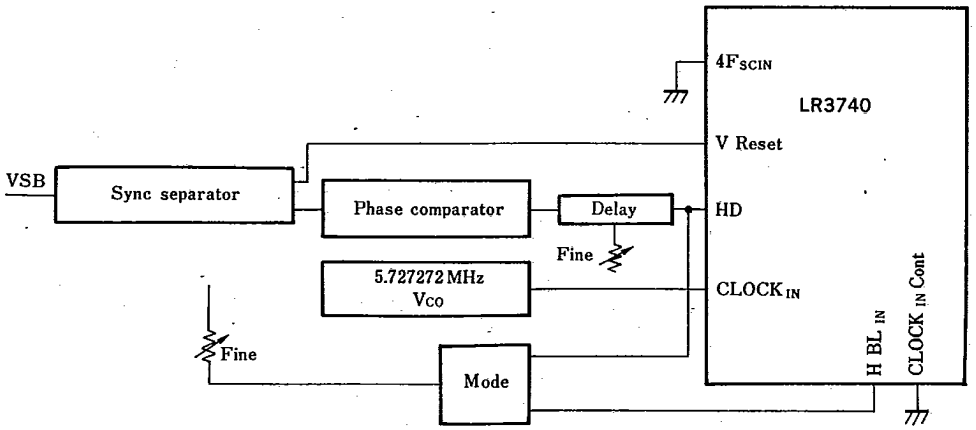
(4) Internal sync. system : for B/W TV



(5) External sync. system (GEN LOCK) : for B/W TV (industrial-use)



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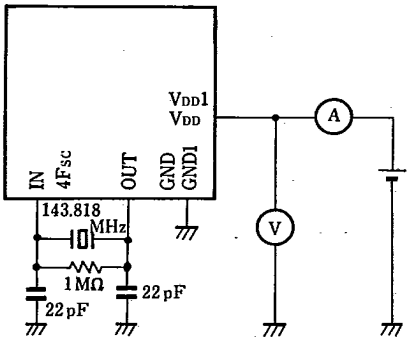
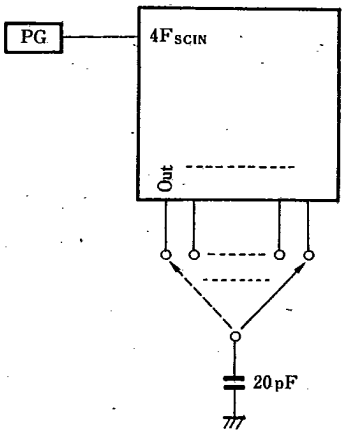
■ Test Circuits

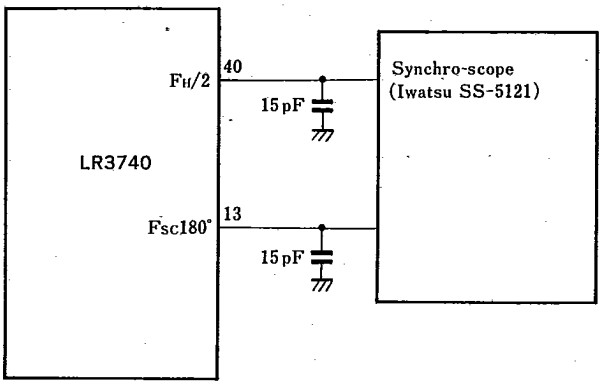
(1) Current consumption



(2) Switching characteristics



(3) F_{SC}-H phase difference test circuit



Test method : Triggered in FH/2, and read the phase difference on each temperature at FSC 180°.

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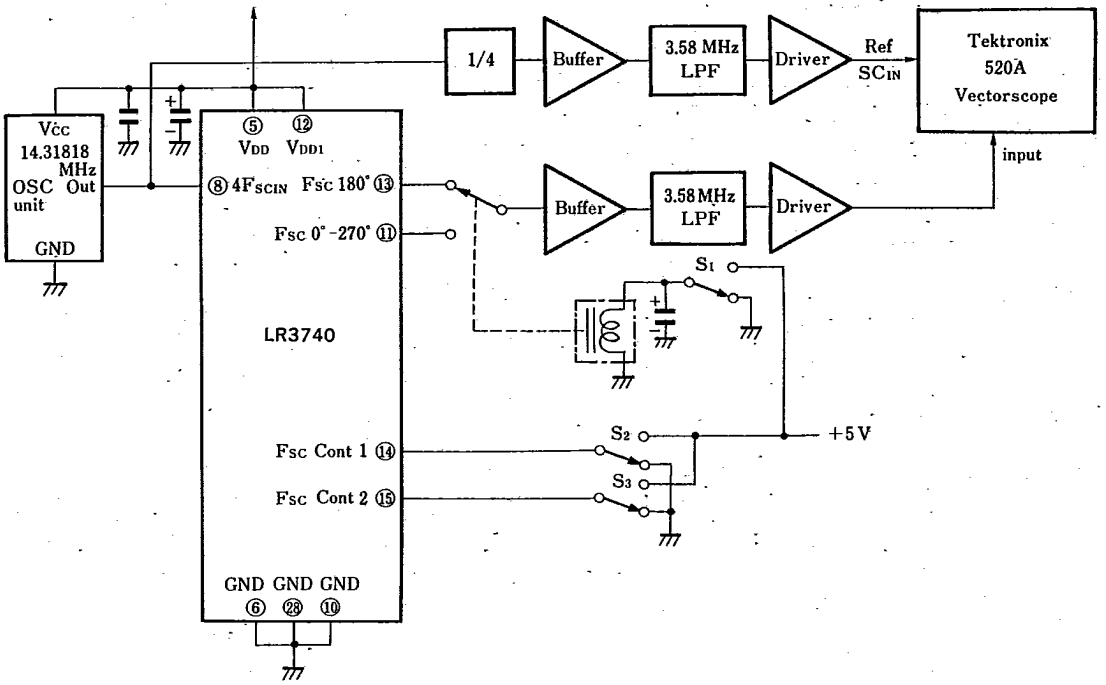
(4) Phase difference test circuit sat F_{SC} 0°-270°



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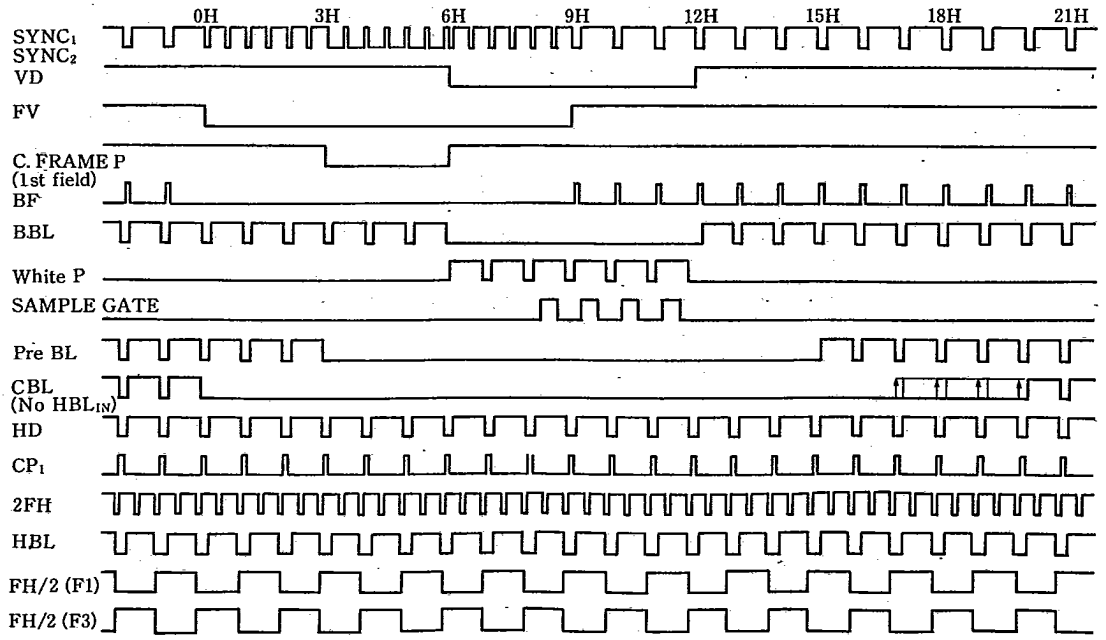
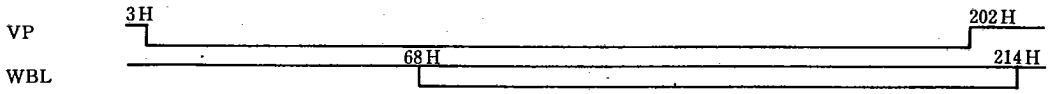
■ Timing Diagram

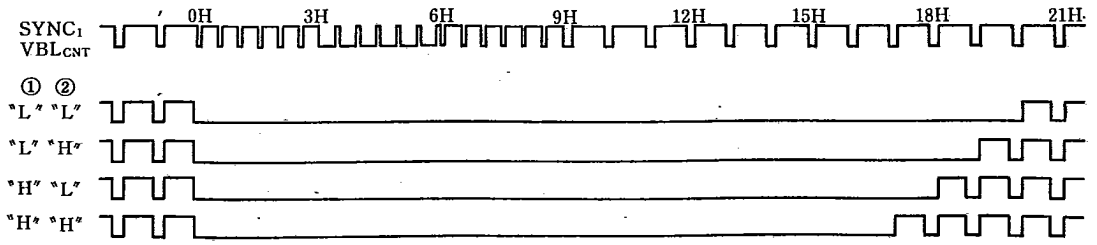
Output switch "H" waveform (1st, 3rd field)



Output switch "H" waveform (1st, 3rd field)



CBL output on HBL_{IN} (VBL_{CNT} ①, ②)



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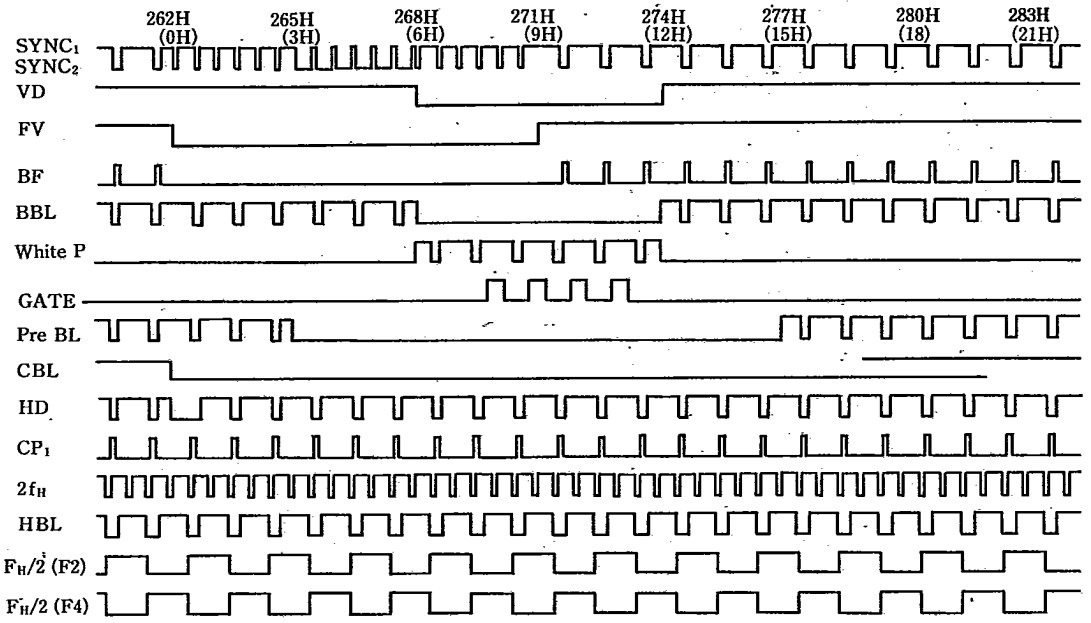
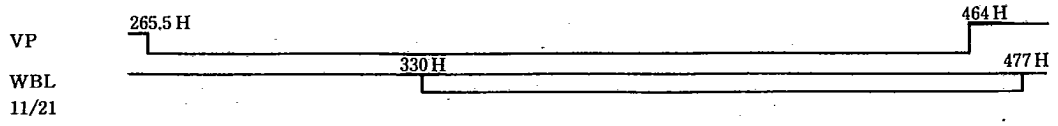
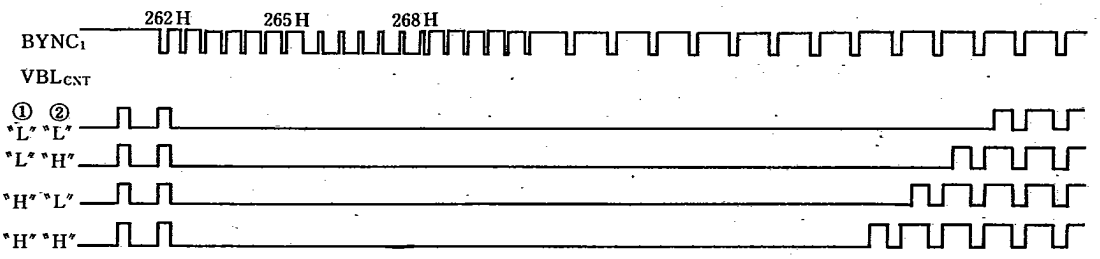
Output switch "H" waveform (2nd, 4th field)



Output switch "H" waveform (2nd, 4th field)



CBL output on HBL_{IN} (VBL_{CNT} ①, ②)



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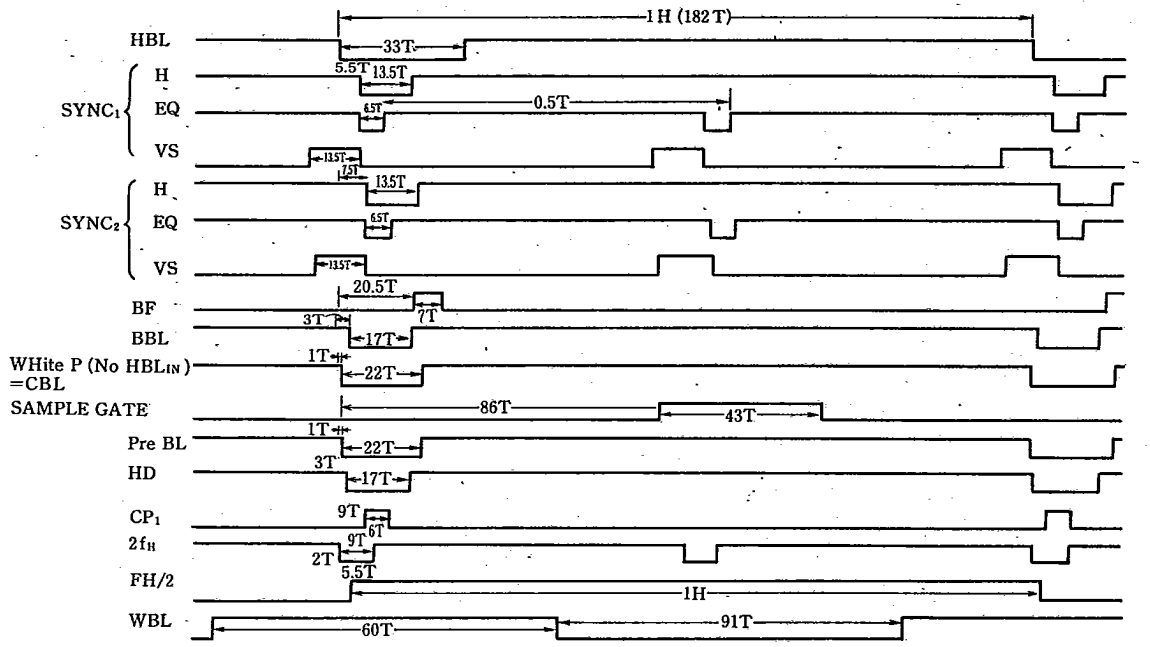
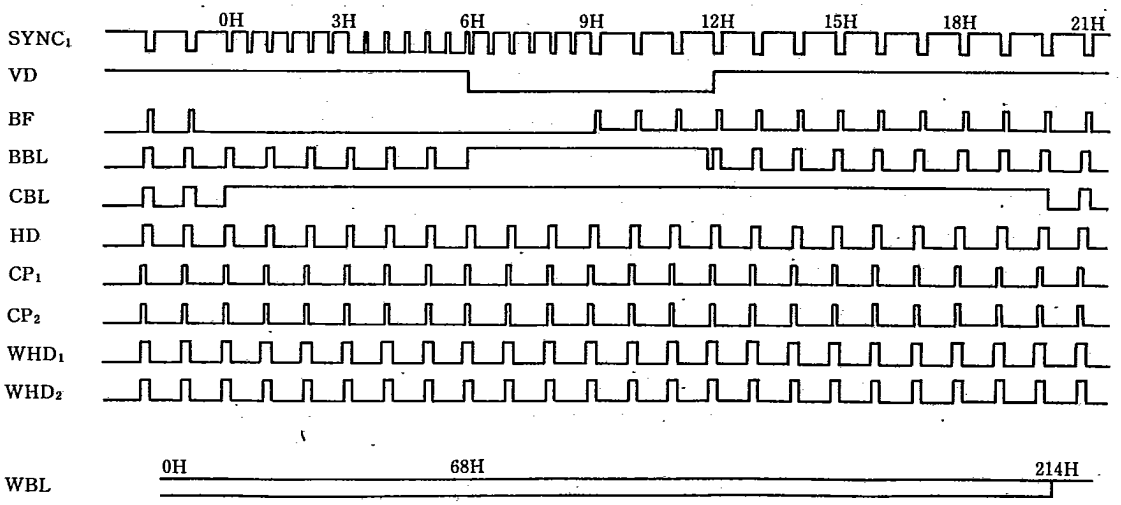
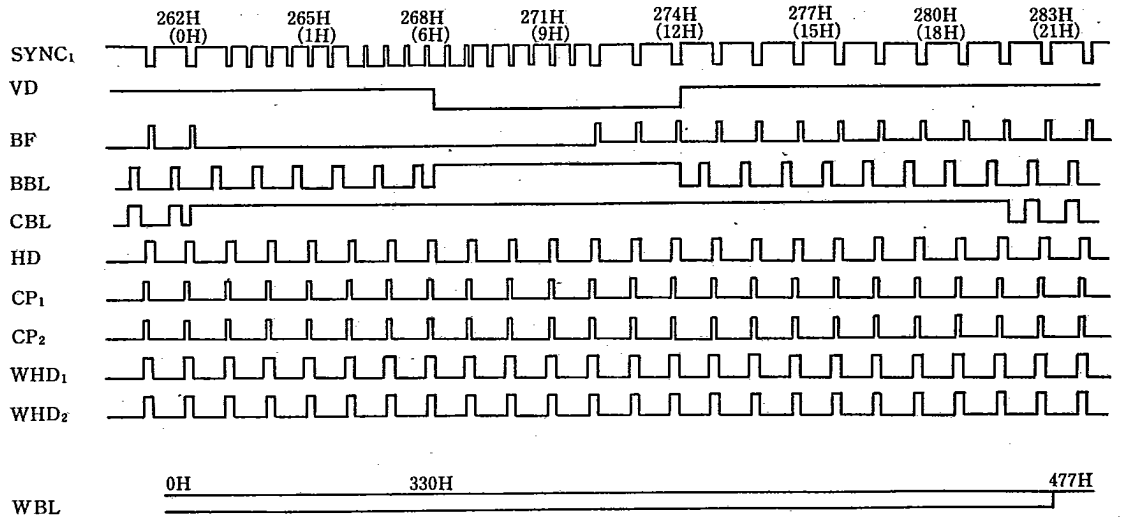
Output switch "H" waveform (H cycle)



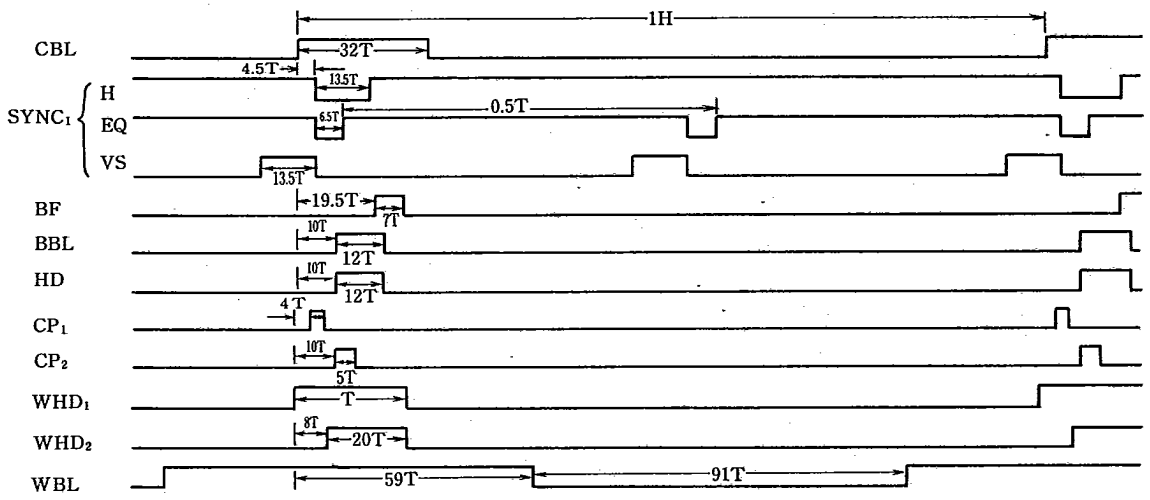
Output switch "H" waveform (1st, 3rd field)



Output switch "L" waveform (2nd, 4th field)



Output switch "L" waveform (H cycle)



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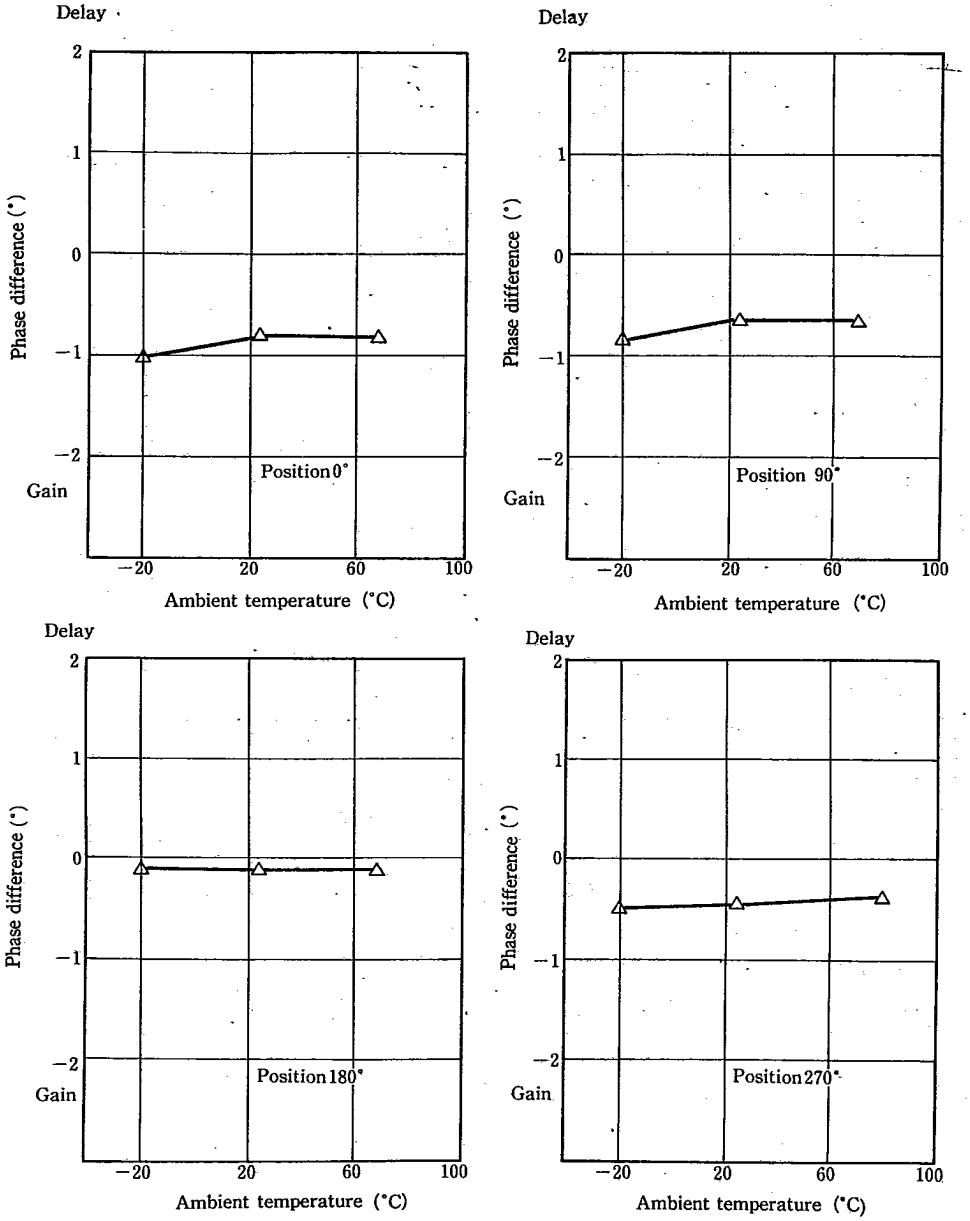
Electrical Characteristic Curves

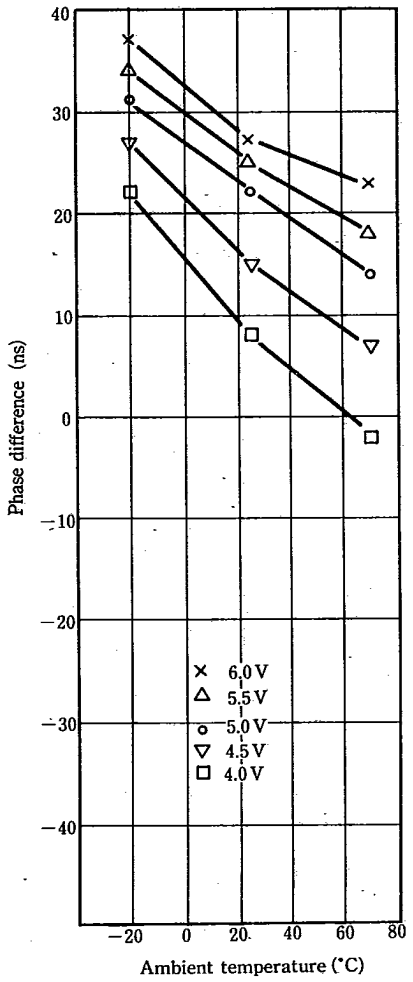
Phase difference vs. Ambient temperature at F_{SC} 0°-270°

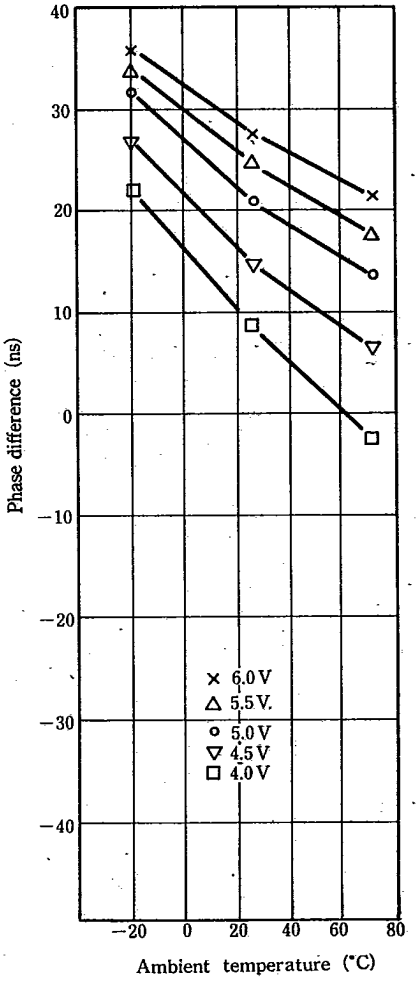
(V_{DD}=5V, Referenced to F_{SC} 180°)



F_{SCH} phase difference vs. Ambient temperature

$F_H/2$ Posi.
F_{SC} 180° Nega.





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F_{SCH} phase difference vs. Ambient temperature

$F_H/2$ Posi.
Fsc 180° Nega.