LR48106

Pulse/Tone Dialer LSI with LCD Driver

DESCRIPTION

The LR48106 is a CMOS pulse/tone dialer LSI which has a 12-digit LCD driver and a clock function. Used in combination with an external RAM, it provides a 32-digit × 34-channel auto-dialing and a 32-digit redialing.

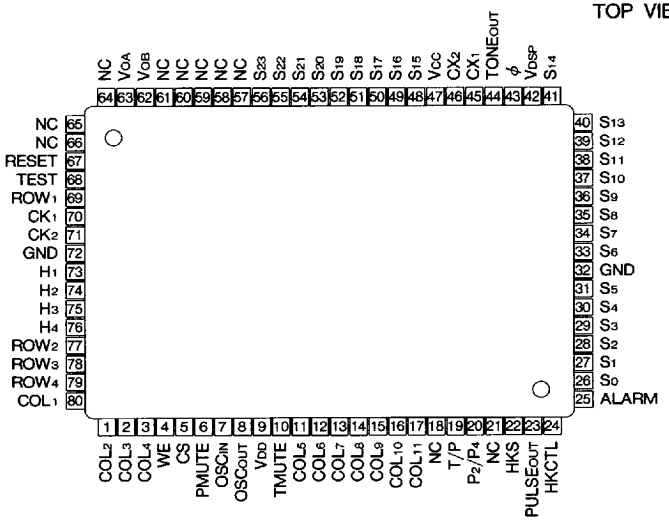
FEATURES

- 12-digit display (1/3 bias, 1/4 duty)
- External RAM for auto-dialing memory
  LH5114 (4k-bit SRAM)
  : 32-digit × 20 one touch memory
  32-digit × 10 two touch memory
  32-digit redial memory
  LH5116 (16k-bit SRAM)
  : 32-digit × 24 one touch memory
  32-digit × 10 two touch memory
  32-digit redial memory
- Make ratio : 33/40% pin-selectable
- Pulse rate : 10/20 pps pin-selectable
- Key or switch input allows switching from pulse to tone mode to provide mixed dialing capability
- Clock function
- Timer function
- ARD (Automatically Repeated Dialing) function
- Alarm function
- Battery check function
- Internal crystal oscillator circuit (32.768 kHz)
- Internal CR oscillator circuit for system clock
- Internal DTMF circuit and crystal oscillator circuit (3.579 545 MHz)
- CMOS process
- Package : 80-pin QFP(QFP080-P-1420)

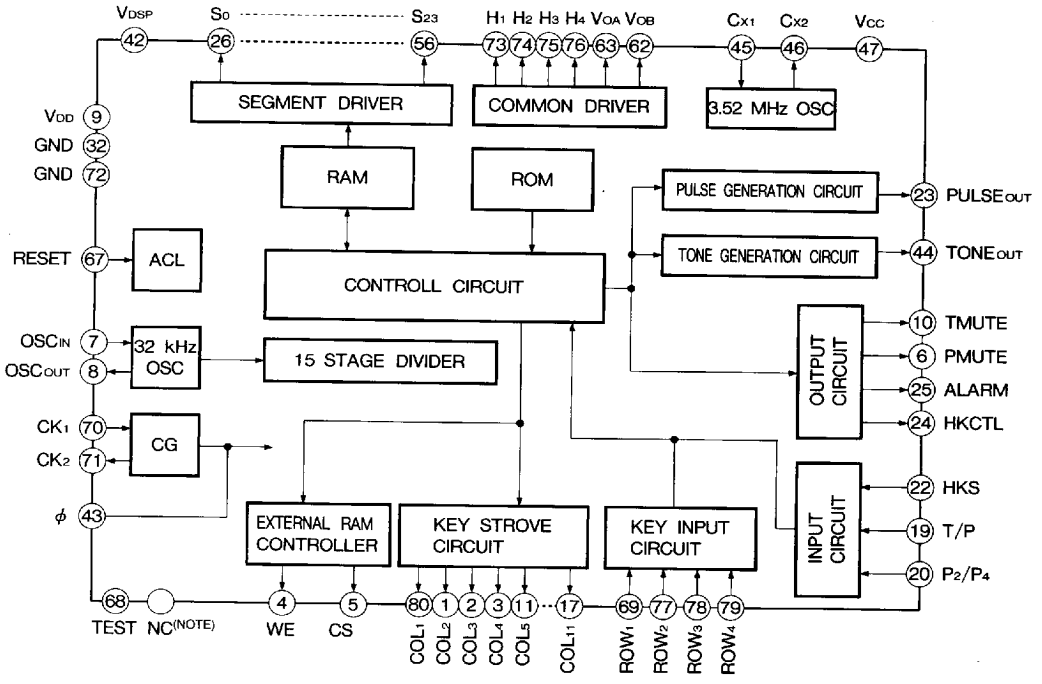
PIN CONNECTIONS

80-PIN QFP

TOP VIEW



BLOCK DIAGRAM



NOTES :

- Pins 18, 21, 57-61, 64-66 are non-connection.
- These are input/output pins or output pins, and must be open.

PIN FUNCTION

SYMBOL	I/O	FUNCTION
GND	I	Power supply
V_{DD}	I	CPU power supply
V_{CC}	I	DTMF power supply
V_{DSP}	I	LCD drive power supply
COL_1-COL_{11}	O	Key strobe output
ROW_1-ROW_4	I	Key input
$PULSE_{OUT}$	O	Pulse output
$TONE_{OUT}$	O	DTMF output
PMUTE	O	PMUTE output
TMUTE	O	TMUTE output
HKCTL	O	Hook control
ALARM	O	Alarm signal output
WE	O	External RAM control
CS	O	External RAM control
T/P	I	Tone/pulse mode switch
P_2/P_4	I	Pause time set
HKS	I	Hook switch input
OSC_{IN}	I	Crystal oscillator connection (32.768 kHz) for clock
OSC_{OUT}	O	Crystal oscillator connection (32.768 kHz) for clock
CX_1	I	Crystal oscillator connection (32.768 kHz) for clock
CX_2	O	Crystal oscillator connection (32.768 kHz) for clock
CK_1	I	CR oscillation for system clock
CK_2	O	CR oscillation for system clock
ϕ	O	Clock output
RESET	I	Reset input
TEST	I	Test
S_0-S_{23}	O	LCD segment drive output
H_1-H_4	O	LCD backplate drive output
V_{OA}	O	LCD bias drive
V_{OB}	O	LCD bias drive
NC	I/O	Input/Output (unused) to be opened in a system
	O	Output (unused) to be opened in a system

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Power supply voltage	V_{DD}	−0.3 to +6.5	V	1
	V_{DSP}	−0.3 to +6.5	V	
	V_{CC}	−0.3 to +6.5	V	
Input voltage	V_I	−0.3 to V_{DD}+0.3	V	
Output voltage	V_O	−0.3 to V_{DD}+0.3	V	
Output current	I_O	20	mA	2
Operating temperature	Topr	−20 to +70	°C	
Storage temperature	Tstg	−55 to +150	°C	

NOTES :

1. The maximum applicable voltage on any pin with respect to GND.
2. The total of the current flowing from (or flowing into) output pins.

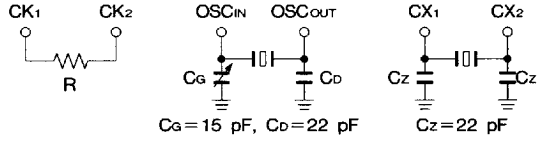
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{DD}	2.7 to 5.5	V	1
	V_{DSP}	$2.7 \leq V_{DSP} \leq V_{CC}$		
	V_{CC}	2.5 to 5.5		
Master clock frequency	f	250 to 600	kHz	2, 3
Instruction cycle	f_{CYC}	6.6 to 16	μs	3
Oscillation frequency	f_{OSC1}	32.768 (TYP.)	kHz	
	f_{OSC2}	3.579 545	MHz	

NOTES :

1. The LSI should be used within the range : V_{DD}-$V_{DSP} \leq 1$ V
2. Frequency variation span : ±30%
3. V_{DD} = 2.7 to 5.5 V

OSCILLATOR CIRCUIT

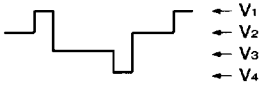


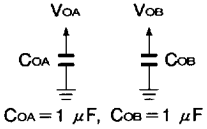
DC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH1}			0.7V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.3V_{DD}		
	V_{IH2}			$V_{DD}-0.5$		V_{DD}	V	2
	V_{IL2}			0		0.5		
Input current	I_{IH}	$V_{IN}=0$ V	$V_{DD}=4.5$ to 5.5 V	20		200	μA	1
			$V_{DD}=2.7$ to 5.5 V	2		200		
Output current	I_{OH1}	$V_{OH}=V_{DD}-0.5$ V		50			μA	3
	I_{OL1}	$V_{OL}=0.5$ V		250			μA	
	I_{OH2}	$V_{OH}=V_{DD}-0.5$ V	$V_{DD}=4.5$ to 5.5 V	400			μA	4
			$V_{DD}=2.7$ to 5.5 V	100				
	I_{OL}	$V_{OL}=0.5$ V	$V_{DD}=4.5$ to 5.5 V	1.6			mA	
			$V_{DD}=2.7$ to 5.5 V	0.5				
	I_{OH}	$V_{OH}=V_{DD}-0.5$ V		1.0	2		mA	5
	I_{OL}	$V_{OL}=0.5$ V		1.0	2		mA	6
Output impedance	R_C				5	20	kΩ	7
	R_S				10	40	kΩ	8
Output voltage	V_1	$V_{DSP}=3.0$ V, No-load		2.7		3.0	V	9
	V_2			1.7	2	2.3		
	V_3			0.7	1	1.3		
	V_4			0		0.3		
Operating current	I_{OP}	f=600 kHz, $V_{DD}=3.0$ V			0.4	1.0	mA	10
Standby current	I_{STVDD}	$V_{DD}=3.0$ V, $V_{DSP}=3.0$ V			15	30	μA	11
	I_{STVCC}	$V_{CC}=3.0$ V			20	40	μA	12
Tone output voltage	V_{OR}	$R_L=10$ kΩ, $V_{DD}=4.0$ V		140	210	260	mVrms	
	V_{OC}	$R_L=10$ kΩ, $V_{DD}=4.0$ V		190	260	310		
Output distortion factor	dis	$R_L=10$ kΩ, $V_{DD}\geq 2.5$ V				−20	dB	13
Pre-emphasis	P_{EHB}	$R_L=10$ kΩ, $V_{DD}\geq 2.5$ V		1.0	2.0	3.0	dB	

NOTES :

1. Applied to pins CK_1, TEST, OSC_{IN}, CX_1.
2. Applied to pins ROW_1-ROW_4, RESET, T/P, P_2/P_4, HKS.
3. Applied to pins CK_2.
4. Applied to pins COL_1-COL_{11}, PMUTE, TMUTE, ϕ.
5. Applied to pins $PULSE_{OUT}$, HKCTL, ALARM.
6. Applied to pins $PULSE_{OUT}$, HKCTL, ALARM.
7. Applied to pins H_1-H_4.
8. Applied to pins S_0-S_{23}.
9. Applied to pins H_1-H_4, S_0-S_{23}.





10. No-load condition.
11. Supply current on V_{DD} under no-load conditions when breeder resistor is ON and f_{OSC1} is oscillating.
12. Supply current V_{CC} under no-load condition.
13. Unnecessary frequency components in the 20 Hz to 80 kHz range with respect to the fundamental tone signals of ROW and COLUMN.

AC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pulse rate	t_{DP}	10/20 open		10		pps
		10/20 connected		20		
Make/brake ratio	t_{MB}	M/B open		40/60		%
		M/B connected		33/67		
Inter-digital pause time	t_{IDPP}	10 pps	800	850	900	ms
		20 pps	450	500	550	
	t_{IDPT}	Normal dialing	110			
		Memory dialing	100	120	140	
Mute overlap time	t_{MO}	Pulse mode	2	5	10	ms
		Tone mode	2	5	10	
Tone output time	t_{DT}	Normal dialing	100			ms
		Memory dialing	100	110	120	

PIN DESCRIPTION

GND, V_{DD}, V_{CC}, V_{DSP} (Pins 32 and 72, 9, 47 and 42)

Both GND pins should be grounded.

The V_{DD} pin is the CPU power supply input which should be positive (2.7 to 5.5 V) with respect to GND.

The V_{CC} pin is the DTMF circuit supply input, which should also be positive (V_{DD} to 5.5 V) with respect to GND.

The V_{DSP} pin is the power supply input for the LCD driver, which should also be positive (2.7 V to V_{DD}) with respect to GND.

TEST (Pin 68)

The TEST input with a pull-down resistor must be grounded and should not be used.

RESET (Pin 67)

The RESET input with a pull-up resistor accepts an active-Low system reset which initializes the internal logic of the device. Normally a capacitor of about 1.0 μF is connected between this pin and GND to provide a power-on reset function.

OSC_{IN}, OSC_{OUT} (Pins 7 and 8)

A crystal oscillator (32.768 kHz) connected between OSC_{IN} and OSC_{OUT}, and a capacitor between GND and them provides an oscillator circuit.

CK_1, CK_2 (Pins 70 and 71)

A resistor connected between CK_1 and CK_2 for system clock CR provides an oscillator circuit.

CX_1, CX_2 (Pins 45 and 46)

A crystal oscillator connected between CX_1 and CX_2, and a capcitor between GND and them provides an oscillator circuit. The oscillation output should be supplied to the DTMF circuit.

TONE (Pin 44)

The $TONE_{OUT}$ pin outputs a DTMF signal.

H_1-H_4 (Pins 73-76)

The H_1-H_4 pins are used to driver the back plate of an LCD.

S_0-S_{23} (Pins 26-31, 33-41, 48-56)

The S_0-S_{23} pins drive LCD segments. Pins S_0 through S_3 may also be used as data I/O, pins S_4 through S_{14} used as address outputs and pins 57-61 and 64-66 may not be used (left open).

COL_1-COL_{11} (Pins 2-4, 11-17, 80)

The COL_1-COL_{11} are the key strobe output pins.

ROW_1-ROW_4 (Pins 69, 77-79)

The ROW_1-ROW_4 are the key input pins with pull-up resistors.

PULSE$_{OUT}$ (Pin 23)
The PULSE$_{OUT}$ is a pulse output pin.

PMUTE (Pin 6)
The PMUTE pin goes "Low" during the pulse output.

TMUTE (Pin 10)
The TMUTE pin goes "Low" during the pulse/tone output or the ARD and the alarm operation. It can be switched from Low to High or High to Low by the MUTE key (Mute function).

HKCTL (Pin 24)
The HKCTL pin is switched by the ON/OFF key, which is used for hook control.

CONDITION		INPUT	HKCTL
HKS	HKCTL		
–	H	ON/OFF key	L
–	L	ON/OFF key	H
H	–	HKS→L	H
L	H	HKS→H	H
L	L	HKS→H	L

ALARM (Pin 25)
The ALARM goes "LOW" during alarm operation.

WE (Pin 4)
The WE pin is connected to the WE in an external RAM to be accessed.

CS (Pin 5)
The CS pin is connected to the CS in an external RAM to be accessed.

T/P (Pin 19)
The T/P pin is used to switch the tone/pulse modes.

T/P PIN	INITIAL MODE
GND	Tone mode
V_{DD}	Pulse mode

P$_2$/P$_4$ (Pin 20)
The P$_2$/P$_4$ pin is used to set the pause time.

P$_2$/P$_4$ PIN	PULSE
GND	2 s
V_{DD}	4 s

HKS (Pin 22)
The HKS is hook input pin.

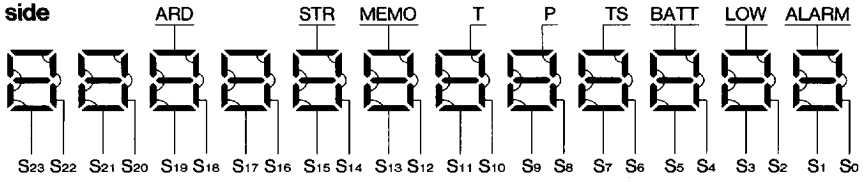
HKS PIN	HOOK CONDITION
GND	Off-Hook
V_{DD}	On-Hook

ϕ (Pin 43)
ϕ, the system clock otuput pin, provides a clock frequency which is one fourth the master clock frequency (CK$_1$ and CK$_2$).

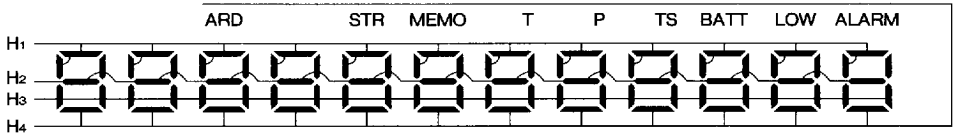
V$_{OA}$ and V$_{OB}$ (Pins 63 and 62)
The V$_{OA}$ and V$_{OB}$ pins supply a bias potential to the LCD. Normally they should be left open. When driving an LCD with a large display area, capacitors may be connected across pins V$_{OA}$ and V$_{DSP}$ (or GND) and across pins V$_{OB}$ and V$_{DSP}$ (or GND) to improve the rising edge of the LCD driving signal.

LIQUID CRYSTAL DISPLAY FORMAT

Segment side



Backplate side



FUNCTIONAL DESCRIPTION

Pulse/Tone Mode Selection

Mode selection with keys

If the T key or the * key is depressed in Off-Hook mode, the dialing is switched from Pulse to Tone mode.

Mode selection with a switch

The T/P switch is used to switch from Pulse to Tone mode. Once the mode is switched from Pulse to Tone, it may not be changed from Tone to Pulse mode unless the T/P switch is reset in Pulse mode following a transition to On-Hook. Immediately after switching from Pulse to Tone mode, a pause of about 2 s or 4 s is inserted automatically. The pause, as well as the dial number, is stored in memory.

Pulse dialing

The pulse rate and the make/break ratio can be set with the key matrix.

Tone dialing

When an effective key input occurs in tone mode, the DTMF signal of 100 ms minimum and the inter-digital pause time of 110 ms minimum may be output. If keys are depressed for more than 100 ms continuously, the DTMF signal is output for the period in succession.

During memory dialing and redialing, the DTMF signal of 100 ms and inter-digital pause time of 110 ms may be output.

Table 1 DTMF Output Frequencies

		STANDARD DTMF (Hz)	LR48106 * (Hz)	DEVIATION (%)
Lower-group frequency	ROW_1	697	701.3	+0.62
	ROW_2	770	771.3	+0.19
	ROW_3	852	857.2	+0.61
	ROW_4	941	935.1	−0.63
Higher-group frequency	COL_1	1209	1215.9	+0.57
	COL_2	1336	1331.7	−0.32
	COL_3	1477	1471.9	−0.35

NOTE :

* These values are obtained with an oscillator frequency of 3.579 545 MHz. Any deviations of oscillation frequency will affect the tone output frequency.

Key Specification

Key input

The LR48106 uses a single contact key board.

PARAMETER	SPECIFICATION
Key-on time	20 ms (MIN.) required
Key-off time	30 ms (MIN.) required

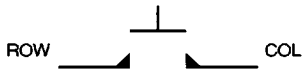


Fig. 1 Single Contact Key

Key Function

KEY	FUNCTION	DISPLAY
0 - 9	Number key	0 1 2 3 4 5 6 7 8 9
*	Pulse mode : Mode switching key	⌐
	Tone mode : Data key	□
#	Pulse mode : Neglected	–
	Tone mode : Data key	□
M_1/M_{13} - M_{12}/M_{24}	One-touch memory key	–
CL	Clear key	–
ARD	ARD key	ARD
STORE	Memory store key	STR
MEMO	Indirect dialing key	MEMO
T	Pulse to tone switching key	⌐
FLASH	Flash key	F
PAUSE	Pause key	P
RD	Redialing key	–
T. S	Clock set key	TS
ALARM	Alarm set key	ALARM
MUTE	Mute key	–
ON/OFF	Hook control on/off key	–
LOWER	M_{13}-M_{24} selection key	LOW
CLOCK	Clock display switching key	–
CALL	Last timer value display key	–
TIMER	Timer key	⌐

NOTE :
The memory keys when used with the LH5116 (16 k CMOS SRAM) for external RAM.

Key matrix

	COL_1	COL_2	COL_3	COL_4	COL_5	COL_6	COL_7	COL_8	COL_9	COL_{10}	COL_{11}
ROW_1	1	2	3	M_1/M_{13}	M_2/M_{14}	M_3/M_{15}	CL	T	T.S	LOWER	10/20
ROW_2	4	5	6	M_4/M_{16}	M_5/M_{17}	M_6/M_{18}	ARD	FLASH	ALARM	CLOCK	M/B
ROW_3	7	8	9	M_7/M_{19}	M_8/M_{20}	M_9/M_{21}	STORE	PAUSE	MUTE	CALL	12/24
ROW_4	*	0	#	M_{10}/M_{22}	M_{11}/M_{23}*	M_{12}/M_{24}*	MEMO	RD	ON/OFF	TIMER	

V_{DD}

LH5116 (16 k-bit CMOS SRAM) for external memory

※ The operation examples described later are based upon the key matrix in the case where the LH5116 (16 k CMOS SRAM) is used for external RAM.

Normal Dialing

Following a transition to Off-Hook, normal dialing is accomplished by data key input.

Memory Dialing

External RAM (LH5116 : 16 k CMOS SRAM)

Redialing = 32 digits [RD]
One-touch dialing = 32 digits × 24 [M_1/M_{13}]
- [M_{12}/M_{24}]

Indirect dialing = 32 digits × 10 [MEMO] [0]
- [MEMO] [9]

External RAM (LH5114 : 4 k CMOS SRAM)

Redialing = 32 digits [RD]
One-touch dialing = 32 digits × 20 [M_1/M_{11}]
- [M_{10}/M_{20}]

Indirect dialing = 32 digits × 10 [MEMO] [0]
- [MEMO] [9]

	OPERATION	MEMORY
Off-hook	STORE N_1 N_2 ⋯ N_n M_1/M_{13}	$M_1 = N_1$ N_2 ⋯ N_n
	STORE N_1 N_2 ⋯ N_n LOWER M_1/M_{13}	$M_{13} = N_1$ N_2 ⋯ N_n
	N_1 N_2 ⋯ N_n after dialing STORE M_1/M_{13}	$M_1 = N_1$ N_2 ⋯ N_n
	N_1 N_2 ⋯ N_n after dialing STORE LOWER M_1/M_{13}	$M_{13} = N_1$ N_2 ⋯ N_n
	STORE N_1 N_2 ⋯ N_n MEMO 1	$MEMO_1 = N_1$ $N_2 \cdots N_n$
On-hook	STORE N_1 N_2 ⋯ N_n M_1/M_{13}	$M_1 = N_1$ N_2 ⋯ N_n
	STORE N_1 N_2 ⋯ N_n LOWER M_1/M_{13}	$M_{13} = N_1$ N_2 ⋯ N_n
	STORE N_1 N_2 ⋯ N_n MEMO 1	$MEMO_1 = N_1$ $N_2 \cdots N_n$

Redialing

Up to 32 digits of normally dialed data may be stored in buffer memory. Immediately after going Off-Hook, the RD key input causes the contents of buffer memory to be dialed. A dial key input following a transition to Off-Hook causes the RD key to be invalid.

One-touch memory dialing

Any one of key input of M_1/M_{13} to M_{12}/M_{24} in Off-Hook mode causes one of the memories M_1 to M_{12} to be dialed.

A couple of key input of LOWER M_1/M_{13} to LOWER M_{12}/M_{24} in Off-Hook mode causes one of the memories M_{13} to M_{24} to be dialed. These operations can be made by using an external memory
(LH5116 : 16 k-bit CMOS static RAM).

Indirect memory dialing

A couple of key input of MEMO plus one of number keys of 0 to 9 in Off-Hook mode causes one of ten memories to be dialed.

Memory storage

Memory is stored either in On-Hook or Off-Hook mode.

When $n > 32$, the data from n-31 digit to the nth digit is stored in memory.

The key inputs of PAUSE, FLASH, T, * and # may also be stored. However, * and # keys are stored only in tone mode.

Memory clear

Memory is cleared by the operation as below.

	OPERATION	MEMORY
On-Hook or Off-Hook	CL	Redialing memory clear
	CL STORE M_1/M_{13}	M_1 clear
	CL STORE LOWER M_1/M_{13}	M_{13} clear
	CL STORE MEMO 1	$MEMO_1$ clear

Flash Function

The FLASH key input causes the Low level signal of 0.6 s to be generated from the PULSEOUT and PMUTE pins.

FLASH key input may be stored in memory in the same way as data key input.

Pause Function

The PAUSE key is used to suspend dial output for intervals of 2 s or 4 s which can be selected by the P_1/P_4 pin. PAUSE key input may be stored in memory in the same way as data key input.

Mute Function

Every time the MUTE key is input in Off-Hook, the TMUTE output may be switched to Low/High by turns. The TMUTE output becomes High level with the transition from Off-Hook to On-Hook.

Clock Function

In standby mode, the real time of Hours, Minutes and Seconds may be indicated on the LCD. The 12/24 input pin is used to select 12-hour

or 24-hour mode of real time display.
(A and P font display in 12-hour format)

12/24 PIN	DISPLAY	MODE
GND	24-hour	display
V_{DD}	12-hour	display

Timer Function

The time from 0-hour, 0-minute, 0-second to 11-hour, 59-minute, 59-second can counted up.

i) The mode may be automatically switched to the timer display in 15 seconds upon completion of dial out.
ii) The timer key input causes the timer to be started.

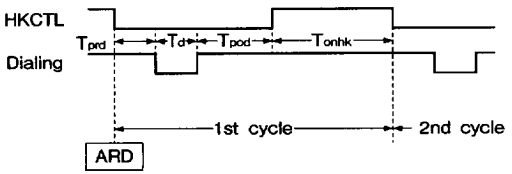
Timer key input : Timer count start
Timer key input : Timer count stop
Timer key input : Timer count start upon completion of timer reset

NOTE :
When the timer starts count, there may have one second (MAX.) tolerance until the first one second count.

ARD Function

In On-Hook mode, the ARD key input causes the contents of redial memory to be automatically dialed in succession. (However when the redial memory is empty, no ARD operation is performed.) If the ARD key is input during ARD operation, the T_{pod} and T_{onhk} time may be one second from the next cycle.

	M/B PIN=GND	M/B PIN=V_{DD}
T_{prd}	3 seconds	3 seconds
T_d	Dialing	Dialing
T_{pod}	25 seconds	25 seconds
T_{onhk}	60 seconds	30 seconds
Repeat times of cycle	Twice	10 times



ARD release

The ARD is released by depressing the ON/OFF key, or the CL key, or Off-Hook. The HKCTL after the ARD is released should be as follows according to the timing to be released.

	ON/OFF KEY INPUT	CL KEY INPUT	OFF-HOOK
T_{prd}	HKCTL=H	HKCTL=L	HKCTL=H
T_d	HKCTL=H Dialing stops	HKCTL=L Dialing stops	HKCTL=H Dialing is continued
T_{pod}	HKCTL=L	HKCTL=L	HKCTL=H
T_{onhk}	HKCTL=H	HKCTL=H	HKCTL=H

Alarm Function

Once the alarm is set, whenever the real time coincides with the alarm time, the ALARM pin goes Low and the buffer memory M_1 is dialed by an ARD operation. If the buffer memory M_1 is cleared, no alarm operation is performed.

Battery Check Function

The external circuit checks the voltage drop of a battery. If the voltage of a battery drops down to the certain level, the BATT mark is blinked on the LCD at 1 Hz rate.

Clock Check Function

After dialing, the CLOCK key input changes the mode to the clock. The next CLOCK key input returns to the dial number display mode. The CLOCK key input immediately after Off-Hook is invalid.

OPERATION AND DISPLAY EXAMPLE

⇧ : Hook switch or Off-Hook mode by ON/OFF key input
⇩ : On-Hook
<> : T/P input pin (Tone or Pulse)
[] : DTMF output
() : Pause

NOTE :
The example is described under conditions of 12-hour format of clock display and 4 s of pause time.

(1) Mode set

KEY INPUT	DIALING OUT	DISPLAY
⇩ <P>		A 3-05-59
⇧		A 3-05-59 P
1 2 3	123	P 123
⇩⇧ <T>		A 3-06-07 T
4 5 6	[456]	T 456

(2) Mode switch

KEY INPUT	DIALING OUT	DISPLAY
⇩⇧ <P> 1 2 3	123	P 123
T 4 5 6	(4 s) [456]	T 123r456
⇩⇧ <P> 1 2 3	123	P 123
<T> 4 5 6 #	(4 s) [456#]	T 123r456o
<P> 7 8 9 *	[789*]	T 123r456o789°

(3) Flash

KEY INPUT	DIALING OUT	DISPLAY
⇩⇧ <P> 1 2 3 FLASH 4 5 6	123 FLASH 456	P 123F456
⇩⇧ <P> 1 2 3 T FLASH 4 5 6	123 FLASH (4 s) [456]	T 123Fr456

(4) Pause

KEY INPUT	DIALING OUT	DISPLAY
⇩⇧ <T> 0 [PAUSE] 4 5 6	[0] (4 s) [456]	T 0P456

(5) Last number redialing

KEY INPUT	DIALING OUT	DISPLAY
⇩⇧ <P> 1 2 3	123	P 123
⇩⇧ <P> [RD] 4 5 6	123456	P 123456
⇩⇧ <P> 1 2 3···5 6 36 digits	123···56 36 digits	567890 P 123456
⇩⇧ <P> [RD] *	567···56 32 digits	567890 P 123456

NOTE :

*In this case, the last 32 digits are redialed.

(6) Memory dialing (Memory content : M_1=123, M_{13}=455, $MEMO_1$=789)

KEY INPUT	DIALING OUT	DISPLAY
⇩⇧ <P> [M_1/M_{13}]	123	P 123
⇩⇧ <T> [LOWER]		A T 5- 11- LOW 12
M_1/M_{13}		T 456
⇩⇧ <P> [MEMO]		A MEMO 5- P 12- 12
1	789	789
⇩⇧ <P> [M_1/M_{13}] [LOWER] [M_1/M_{13}]	123456	P 123456
⇩⇧ <P> [M_1/M_{13}] MEMO 1	123789	P 123789
⇩⇧ <P> 1 2 3 [M_1/M_{13}] [MEMO] 1	123123789	123 P 123789

(7) Memory storage

KEY INPUT	DIALING OUT	DISPLAY
⇩ (or ⇧) <P>		A 3-05-59
STORE		STR P
1 2 3		STR P 123
M1/M13		STR P 123 ↓ *1 A 3-06-15
⇩ (or ⇧) <P>		A 3-05-59
STORE		STR P
1 2 3		STR P 123
LOWER		STR P LOW 123
M1/M13		STR P LOW 123 ↓ A 3-06-15
⇩ (or ⇧) <P>		A 3-05-59
STORE		STR P
1 2 3		STR P 123
MEMO		STR MEMO P 123
		STR MEMO P 123 ↓ A 3-06-15
⇩ (or ⇧) <P>		A 3-05-59
STORE		STR P
1 2 3···4 5 6 (36 digits)		STR P 567890 123456
M1/M13 *2		STR P 567890 123456 ↓ A 3-06-15

NOTES :

* 1 After the display blinks twice within 1 second, the display shifts to clock display.
* 2 In this case, 32 digits, from 567 to 456, are stored in M1.

(8) Memory check

KEY INPUT	DIALING OUT	DISPLAY
⇩ M1/M13		A 10-05-30 123 ↓ After 3 seconds A 10-05-35
LOWER M1/M13		456 ↓ After 3 seconds A 10-06-40
MEMO 1		789 ↓ After 3 seconds A 10-07-45

(9) Clock set

KEY INPUT	DISPLAY	
⇩ (or ⇧)	A 8-25-30	
T.S	A __-__-TS 00	
1	A __-_1-TS 00	
2	A __-12-TS 00	
0	A _1-20-TS 00	
3	A 12-03-TS 00	
4	A 20-34-TS 00	
5	A 03-45-TS 00	
#	P 03-45-TS 00	
*	A 03-45-TS 00	
T.S	A 3-45-00	Count start

(In case setting error)

KEY INPUT	DISPLAY
⇩ (or ⇧)	A 8-25-30
T.S	A TS --:--:-00
3	A TS --:-3-00
4	A TS --:34-00
5	A TS -3:45-00
6	A TS 34:56-00
T.S	A 34:56-00 Setting error ↓ Blinks twice within a half second
	A 8-25-57 Initial clock display

(10) Timer

① **Automatic timer**

KEY INPUT	DISPLAY
⇩⇧ ⟨P⟩ 1 2 3 4	P 1234 P ↓ 15 seconds upon completion of dialing C 00-00-01 Timer start P C 00-02-31
⇩	A P 6-12-30 Clock display (Timer stop)

② **Manual Timer**

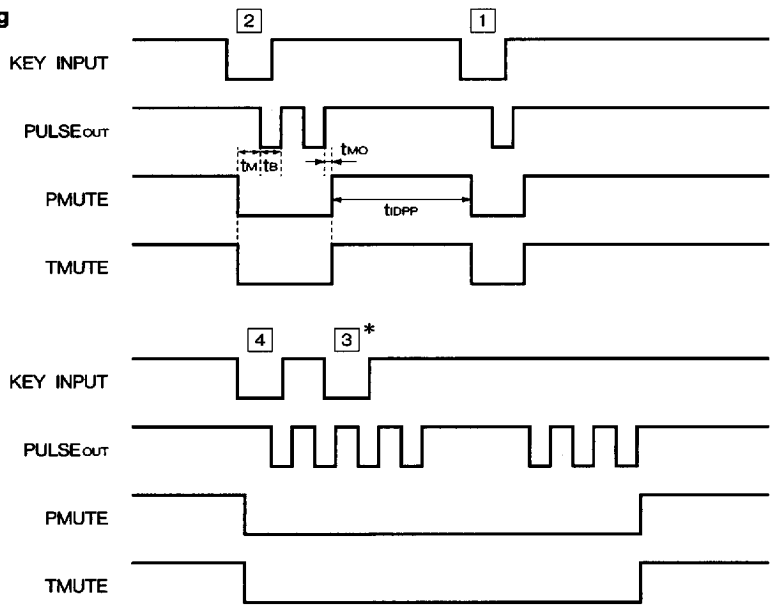
KEY INPUT	DISPLAY
⇩ (or ⇧)	A 6-12-34
TIMER	C 00-00-01 Timer start
TIMER	C 00-01-23 Timer stop
TIMER	C 00-00-01 Timer start

(11) Alarm set

KEY INPUT	DISPLAY
⇩ (or ⇧)	A 11-20-30
ALARM	ALARM blinks A 12-00-00
#	ALARM blinks P 12-00-00
1	ALARM blinks P 20-01-00
2	ALARM blinks P 00-12-00
3	ALARM blinks P 01-23-00
4	P 12-34-00
ALARM	P 12-34-00 ALARM ↓ After 3 seconds A 11-21-07 ALARM Initial clock display
ALARM	A 11-21-09 Alarm-set release

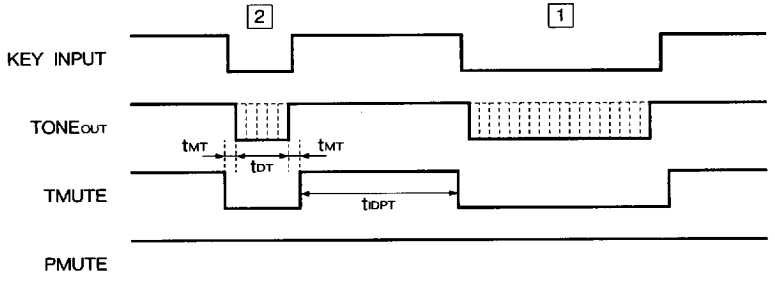
TIMING DIAGRAM

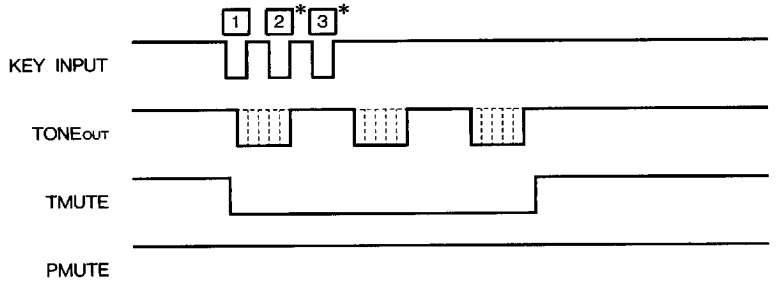
(1) Normal dialing
(Pulse mode)



* If the following data are input during the dialing operation, the PMUTE and TMUTE go "Low" for the period of t_{IDPP}.

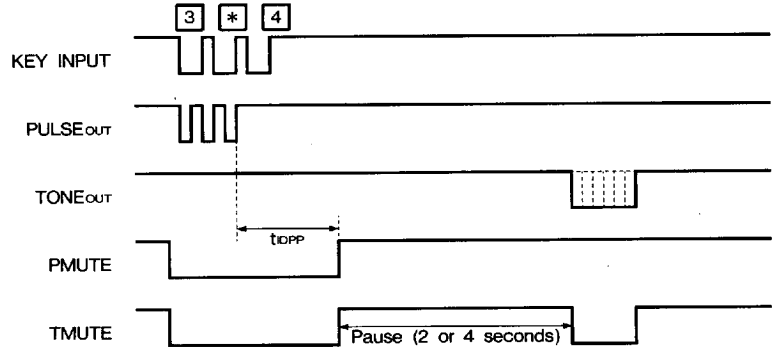
(Tone mode)



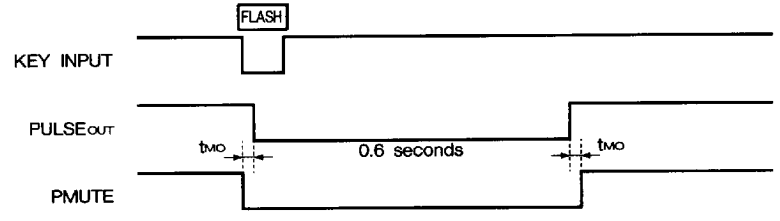


* If the following data are input during the dialing operation, the TMUTE goes "Low" for the period of t_{IDPT}.

(Mode switching)

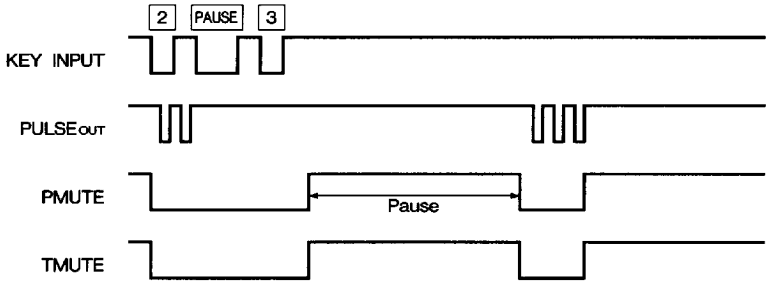


(2) Flash

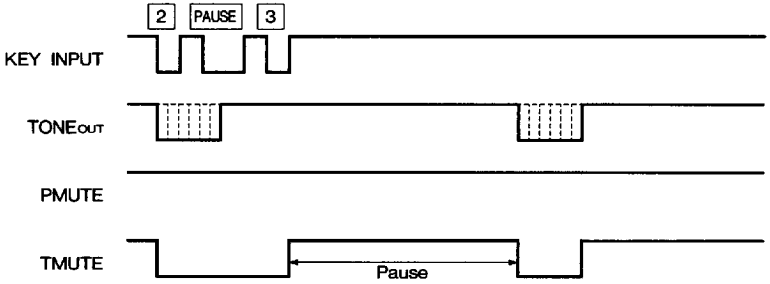


(3) Pause

(Pulse mode)

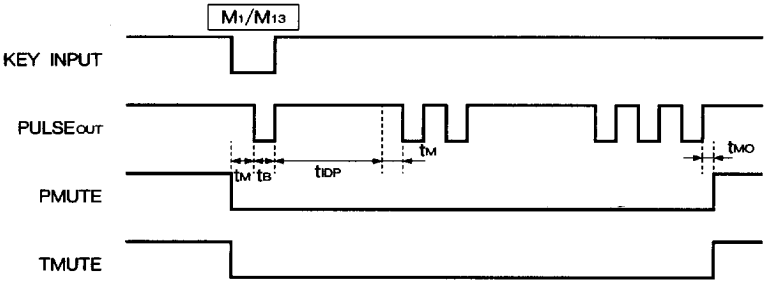


(Tone mode)

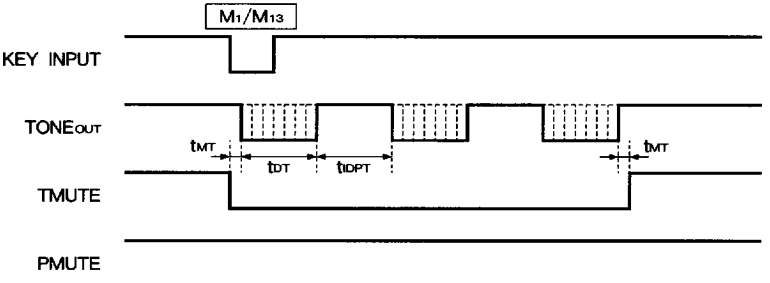


(4) Memory dialing (In case of M1 = 123)

(Pulse mode)

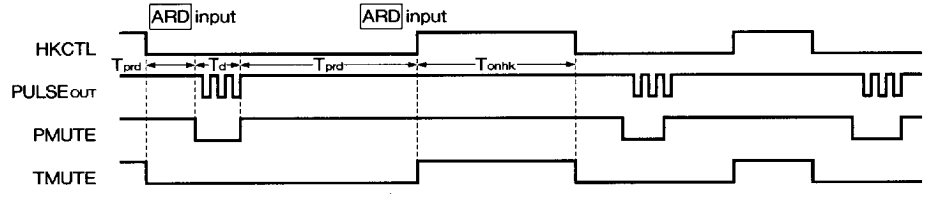


(Tone mode)

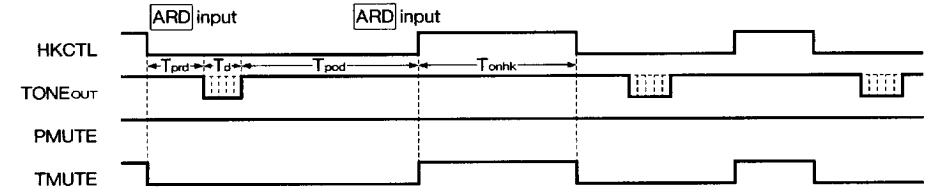


(5) ARD

(Pulse mode)



(Tone mode)



If the ARD key is input during ARD operation, the T_{pod} and T_{onhk} time may be one second from the next cycle. However, once they are shortened, the ARD key input does not affect T_{pod} and T_{onhk} anymore.

SYSTEM CONFIGURATION EXAMPLE