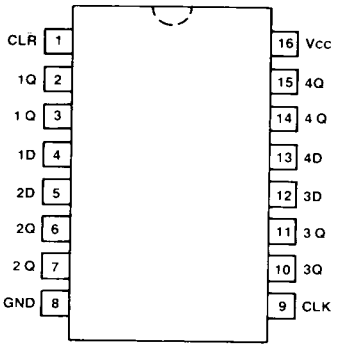
Quad D-Type Flip-Flop with Complementary Outputs/Common Direct Clear

The LS175 is a bipolar, NPN, sealed-junction, silicon integrated circuit. It is manufactured in low-power Schottky technology and is available in a wire-bonded, 16-pin plastic DIP or surface mount package.

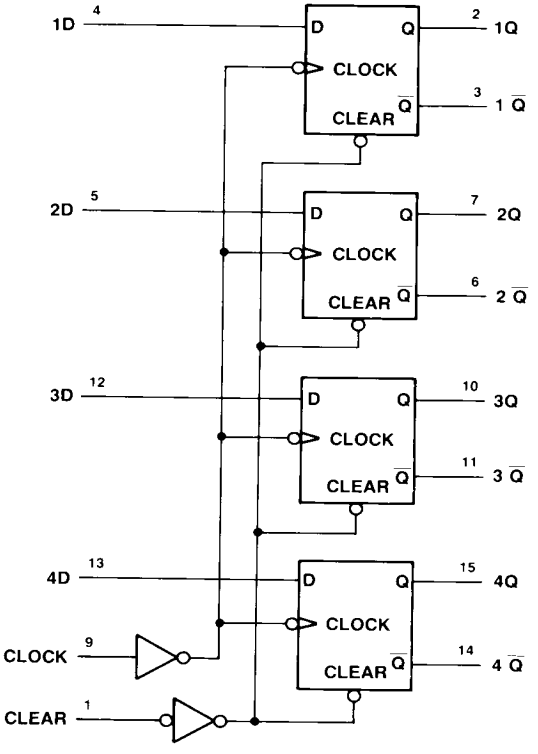


Truth Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High level (steady state)
L = Low level (steady state)
X = Irrelevant
↑ = Transition from low to high level
Q_0= The level of Q before the indicated steady state input conditions were established
$\overline{Q}_0$ = Complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established

Logic Diagram



Electrical Characteristics

V_{CC} = 5.0 ±0.5 V, T_A = −55 to +125°C (WA-LS)
V_{CC} = 5.0 ±0.25 V, T_A = 0 to 70°C (WP90350L1)
V_{CC} = 5.0 ±0.5 V, T_A = −40 to +85°C (WA-LSD, WP91399L2)

		WA-LS		WP, WA-LSD		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
Output Voltage, V_{CC} = 4.5 V (WA-LS), 4.75 V (WP, WA-LSD)						
Low, I_{OL} = 4.0 mA	V_{OL}	—	0.4	—	0.4	V
I_{OL} = 8.0 mA	V_{OL}	—	0.5	—	0.5	V
High, I_{OH} = −0.4 mA	V_{OH}	2.5	—	2.7	—	V
Input Voltage, V_{CC} = 4.5 V (WA-LS), 4.75 V (WP, WA-LSD)						
Low	V_{IL}	—	0.7	—	0.8*	V
High	V_{IH}	2.0	7.5	2.0	5.5	V
Clamp, I_{IN} = −18.0 mA	V_{IK}	—	−1.5	—	−1.5	V
Input Current, V_{CC} = 5.5 V (WA-LS), 5.25 V (WP, WA-LSD)						
Low, V_{IL} = 0.4 V	I_{IL}	—	−0.4	—	−0.4	mA
High, V_{IH} = 2.7 V	I_{IH}	—	20.0	—	20.0	μA
@ V_I max, V_I = 7.0 V (WA-LS), 5.5 V (WP, WA-LSD)	I_I	—	0.1	—	0.1	mA
Output Current, V_{CC} = 5.5 V (WA-LS), 5.25 V (WP, WA-LSD)						
Short-Circuit	I_{OS}	−20.0	−100.0	−20.0	−100.0	mA
Supply Current, V_{CC} = 5.5 V (Outputs Open, Data and Clear High, Clock Momentary Ground; then High)	I_{CC}	—	18.0	—	18.0	mA

* WA-LSD, WP91399L2: V_{IL} = 0.7 V

Timing Characteristics

V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

		WA-LS		WP, WA-LSD		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delay						
Clear-to-Output						
Low-to-High	t_{PLH}	—	25.0	—	30.0	ns
High-to-Low	t_{PHL}	—	28.0	—	30.0	ns
Clock-to-Output						
Low-to-High	t_{PLH}	—	20.0	—	25.0	ns
High-to-Low	t_{PHL}	—	22.0	—	25.0	ns
Operating Conditions						
Width of Clock Pulse	t_W	20.0	—	20.0	—	ns
Setup Time						
Data, Low	t_{DSL}	5.0	—	20.0	—	ns
High	t_{DSH}	0	—	20.0	—	ns
Clear Inactive State, Low	t_{DSL}	25.0	—	25.0	—	ns
High	t_{DSH}	25.0	—	25.0	—	ns
Data Hold Time, Low	t_{DHL}	10.0	—	5.0	—	ns
High	t_{DHH}	10.0	—	5.0	—	ns
Maximum Clock Frequency	f_{max}	30.0	—	30.0	—	MHz

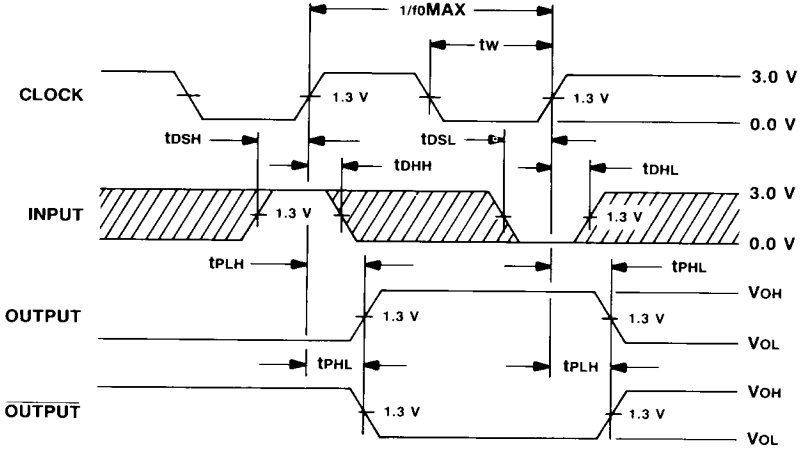
Maximum Ratings

Power supply voltage (V_{CC}) . . . . . 7.0 V
Operating temperature (T_A) . . . . . WA-LS: −55 to +125°C
WP90350L1: 0 to 70°C
WA-LSD, WP91399L2: −40 to +85°C
Storage temperature (T_{stg}) . . . . . −65 to +150°C

Maximum ratings are defined as the limiting conditions that the user can apply to the device under all variations of circuit and environmental conditions. If any rating is exceeded, permanent damage to the device may result.

Bonding or soldering of the external leads of this device can be performed safely at temperatures up to 300°C.

Timing Diagrams



THE SHADED AREAS INDICATE WHEN THE INPUT IS PERMITTED TO CHANGE FOR PREDICTABLE OUTPUT PERFORMANCE

Figure 1. $\overline{\text{Clear}}$ to Output Delay, $\overline{\text{Clear}}$ Pulse Width, and Clearing Time

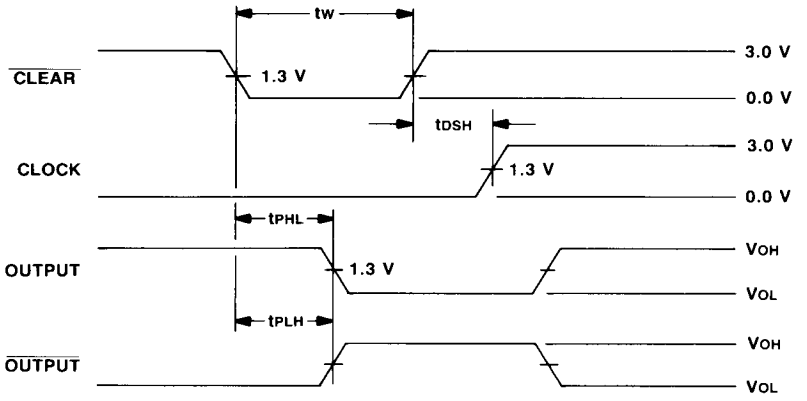


Figure 2. $\overline{\text{Clock}}$ to Output Delays, $\overline{\text{Clock}}$ Pulse Width, Frequency, Set-Up and Hold Times Data to $\overline{\text{Clock}}$