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LSA1500 1.5-Micron HCMOS Structured Array™ Series

Description

The LSA1500 Structured Array series is a high speed HCMOS semicustom family which offers high logic gate counts plus large high speed metal configurable memories. The LSA1500 series is fabricated using a proprietary 1.5-micron drawn gate length, 2-layer metal HCMOS process for speeds rivalling 10K ECL.

The four members of the LSA1500 family provide different combinations of high speed static RAM along with LCA10000 Series Compacted Arrays™. The memories are specially designed for use as ASIC blocks. They are metal configurable for design flexibility and contain scan testing circuitry for ease of testing.

Surrounding the memories is LCA10000 series Compacted Array which features a channeless architecture where all areas of the die are filled with potentially active transistors. With high density memory and high speed logic on the same ASIC circuit, the LSA1500 Structured Array series provides the design flexibility of a cell-based custom approach along with the cost advantages of fast turn-around time inherent with array based technologies.

Features

- Combines high density LCA10000 series Compacted Arrays with dedicated high speed, high performance memory structures
- 1.5-micron drawn (0.9-effective) gate length, 2-layer metal HCMOS
- Four unique masterslices, optimized for typical high end systems architectures
- All memories fully static
- ESD protection over 2001 V, latch up immunity over 200 mA
- Specified to operate over commercial, industrial and military temperature ranges
- Up to 234 total pads
- Gate speeds equivalent to 10K ECL –0.65 ns through two input NAND gate (typ)
- Configurable output drive up to 12 mA with slew rate control capability
- LCA10000 series Compacted Arrays provide efficient implementation of large logic blocks such as megafunctions, metal megacells and RAM and ROM blocks
- Flexible memory architectures—multiple memory blocks, each individually configurable as 9, 18 or 36 bits wide, with bytewrite capability

Product Benefits

- On-chip memory allows higher system performance due to greater integration and fewer I/O boundary crossings
- Masterslice based product—faster prototype delivery and lower engineering costs than cell-based custom
- Full range of popular library elements—ranging from SSI through VLSI building blocks—allows efficient and rapid design of large system architectures
- High density memories can be configured into sizes which are otherwise unavailable as standard products

Product Outline

Device	Compacted Array Gate Count		RAM Size and Type	Total Pads[2,3]	Max I/O Pads	Memory Architecture
	Total Available	Est. Usable[1]				
LSA1501	37,000	13,000	18K-bits	234	214	Two 9K Blocks
LSA1502	30,000	10,000	36K-bits	234	214	Two 18K Blocks
LSA1503	41,000	14,000	4K-bits 3-Port RAM	234	214	Two 2K Blocks 2 Read, 1 Write
LSA1504	37,000	13,000	4K-bits 5-Port RAM	234	214	Two 2K Blocks 3 Read, 2 Write

Notes:
1. Usable gates will vary, depending upon design.
2. I/O pads may be configured on input, output, bidirect VDD or VSS, subject to number and drive strength of output buffers.
3. Total device pads include eight dedicated VDD pads.
4. The difference between total pads and MAX I/O pads represents minimum power and ground pin requirements.

Structured Array Testing

The memory portion of the LSA1500 Structured Arrays may often be buried within some of the customer logic. Gaining access to the internal memory for testing purposes is often difficult. Applying test vectors to an imbedded memory may not be practical or possible.

LSI Logic has developed a scan test methodology which allows access to an imbedded RAM. The overhead required to invoke the test mode is a single dedicated test input pin at the package level.

Scanning is a technique where any register element such as latch, flip-flop, etc., is switchable from a normal operating mode into shift or scan mode. Data from one register in the scan chain is shifted to the next register. This allows serial access into large parallel internal data points. Using this scan circuitry, LSI Logic tests each and every bit location within any memory. This test is written and performed by LSI Logic independent of any customer generated test vectors.

This scan circuitry is available to designers for use within any chip, board or system level test scheme. This technique is the same as that used for all LSI Logic memories, megacells and L64000 Series standard products.

Memory Types and Configurations

The LSA1501 and LSA1502 each contain two separate high speed, high density metal configurable static RAMs. Each of these RAMs are constructed using a six transistor cell. This provides high performance, low speed variation over temperature and low susceptibility to soft errors. The two memory blocks are totally independent of each other. Each has separate addresses, enables, and scan test circuitry. Each can also be independently configured through the personalized two layers of metal. Configurations can be established as 9, 18, or 36 bits wide with bytewrite capability.

The LSA1503 and LSA1504 each contain two separate high speed metal configurable multiport RAMs. The LSA1503 provides two 2304-bit 3-port RAMs. Each memory block features two read addresses (ports) and one write address, all simultaneously available. The LSA1504 provides two 2304-bit 5-port RAMs. Each memory block features three separate read ports and two separate write ports. Both the LSA1503 and LSA1504 RAM blocks are metal configurable as 9, 18, or 36 bits wide with bytewrite capability.

LSA1500 Series Memory

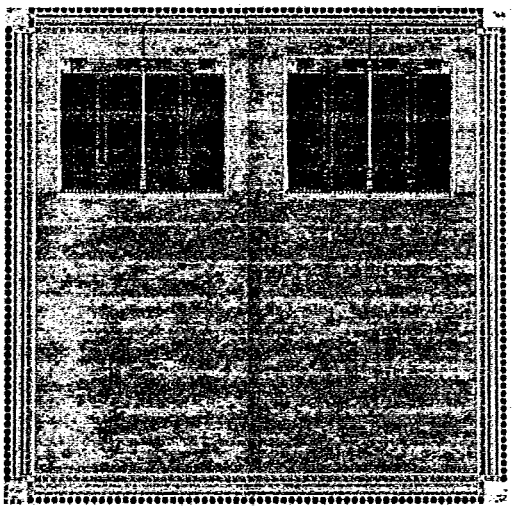
Array Type	Memory Building Blocks	Possible Configurations per Block
LSA1501	Two × 9K-bits	1K × 9 512 × 18 256 × 36
LSA1502	Two × 18K-bits	2K × 9 1K × 18 512 × 36
LSA1503	Two × 2304 bits 3-Port RAM	256 × 9 128 × 18 64 × 36
LSA1504	Two × 2304 bits 5-Port RAM	256 × 9 128 × 18 64 × 36

RAM AC Summary Table

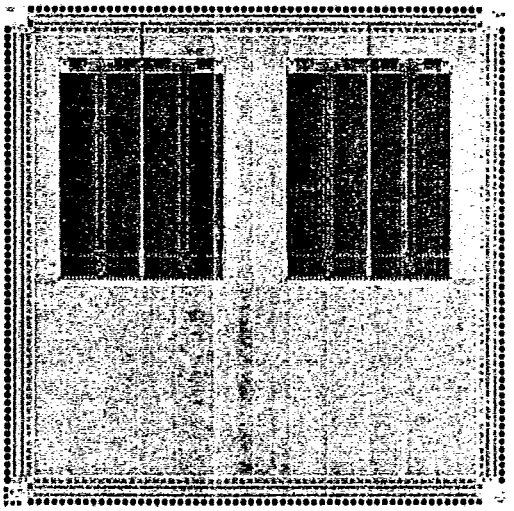
Array Type	LSA1501	LSA1502	LSA1503	LSA1504
RAM Building Block Size	9K-bits	18K-bits	2K-bits 3-Port	2K-bits 5-Port
Total RAM Size	18K-bits	36K-bits	4K-bits	4K-bits
Read Cycle (typ) tRC	16 ns	16 ns	16 ns	19 ns
Write Cycle (typ) tWC	16 ns	16 ns	12 ns	15 ns

Data shown is worst-case configuration. Other configurations will be somewhat faster.
Typical cycle times refer to operation at 25°C, 5.0 V and nominal processing.

LSA1500 Die Photos



LSA1501



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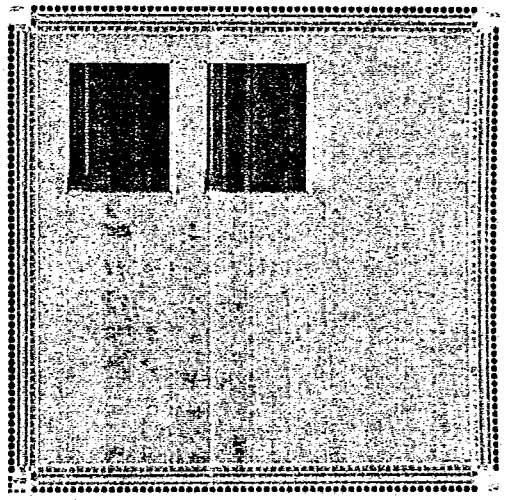
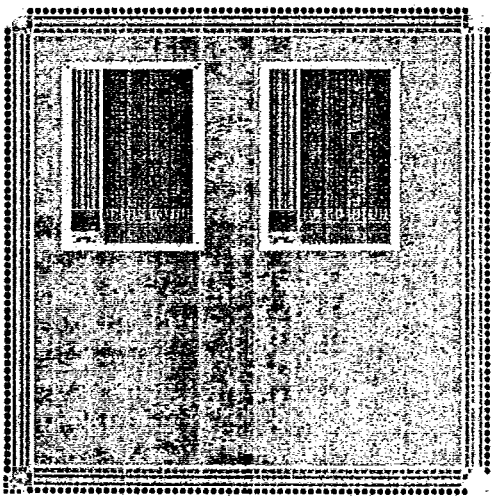


LSA1503



LSA1504