FEATURES

- 32-bit Input, 32-bit Output Multiplexed to 16 Lines
- Full 0-31 Position Barrel Shift Capability
- Integral Priority Encoder for 32-bit Floating Point Normalization
- Sign-Magnitude or Two's Complement Mantissa Representation
- 32-bit Linear Shifts with Sign or Zero Fill
- Independent Priority Encoder Outputs for Block Floating Point
- DECC SMD No. 5962-89717
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC
  - 68-pin Ceramic PGA

DESCRIPTION

The **LSH32** is a 32-bit high speed shifter designed for use in floating point normalization, word pack/unpack, field extraction, and similar applications. It has 32 data inputs, and 16 output lines. Any shift configuration of the 32 inputs, including circular (barrel) shifting, left shifts with zero fill, and right shift with sign extend are possible. In addition, a built-in priority encoder is provided to aid floating point normalization.

SHIFT ARRAY

The 32 inputs to the LSH32 are applied to a 32-bit shift array. The 32 outputs of this array are multiplexed down to 16 lines for presentation at the device outputs. The array may be configured such that any contiguous 16-bit field (including wraparound of the 32 inputs) may be presented to the output pins under control of the shift code field (wrap mode). Alternatively, the wrap feature may be disabled, resulting in zero or sign bit fill, as appropriate (fill mode). The shift code control assignments and the resulting input to output mapping for the wrap mode are shown in Table 1.

Essentially the LSH32 is configured as a left shift device. That is, a shift code of 00000_2 results in no shift of the input field. A code of 000001_2 provides an effective left shift of 1 position, etc. When viewed as a right shift, the shift code corresponds to the two's complement of the shift distance, i.e., a shift code of 111111_2 (-1_{10}) results in a right shift of one position, etc.

When not in the wrap mode, the LSH32 fills bit positions for which there is no corresponding input bit. The fill value and the positions filled depend on the RIGHT/$\overline{\text{LEFT}}$ (R/$\overline{\text{L}}$) direction pin. This pin is a don't care input when in wrap mode. For left shifts in fill mode, lower bits are filled with zero as shown in Table 2. For right shifts, however, the SIGN input is used as the fill value. Table 3 depicts the bits to be filled as a function of shift code for the right shift case. Note that the R/$\overline{\text{L}}$ input changes only the fill convention, and does not affect the definition of the shift code.

In fill mode, as in wrap mode, the shift code input represents the number of shift positions directly for left shifts, but the two's complement of the shift code results in the equivalent right shift. However, for fill mode the R/$\overline{\text{L}}$ input can be viewed as the most

LSH32 BLOCK DIAGRAM
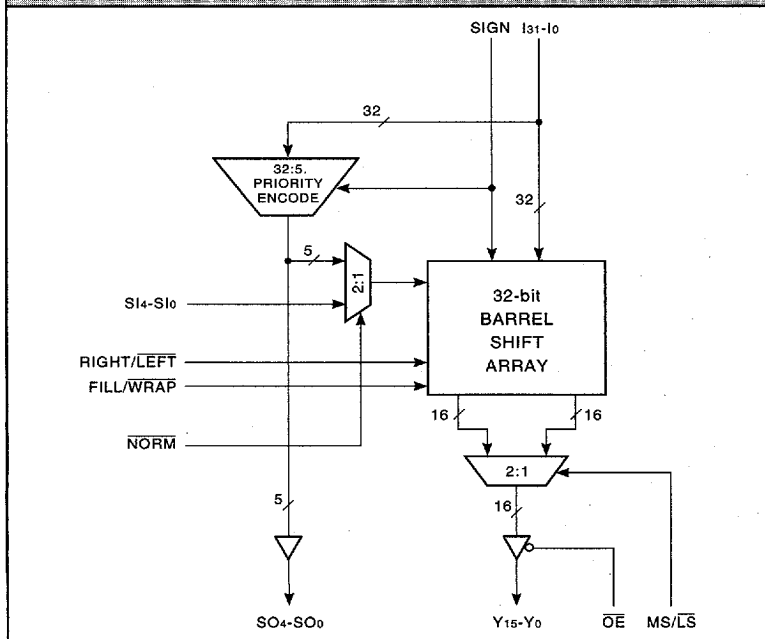
TABLE 1. WRAP MODE SHIFT CODE DEFINITIONS

Shift Code	Y31	Y30	Y29	•••	Y16	Y15	•••	Y2	Y1	Y0
00000	I31	I30	I29	•••	I16	I15	•••	I2	I1	I0
00001	I30	I29	I28	•••	I15	I14	•••	I1	I0	I31
00010	I29	I28	I27	•••	I14	I13	•••	I0	I31	I30
00011	I28	I27	I26	•••	I13	I12	•••	I31	I30	I29
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	I16	I15	I14	•••	I1	I0	•••	I19	I18	I17
10000	I15	I14	I13	•••	I0	I31	•••	I18	I17	I16
10001	I14	I13	I12	•••	I31	I30	•••	I17	I16	I15
10010	I13	I12	I11	•••	I30	I29	•••	I16	I15	I14
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	I3	I2	I1	•••	I20	I19	•••	I6	I5	I4
11101	I2	I1	I0	•••	I19	I18	•••	I5	I4	I3
11110	I1	I0	I31	•••	I18	I17	•••	I4	I3	I2
11111	I0	I31	I30	•••	I17	I16	•••	I3	I2	I1

TABLE 2. FILL MODE SHIFT CODE DEFINITIONS — LEFT SHIFT

Shift Code	Y31	Y30	Y29	•••	Y16	Y15	•••	Y2	Y1	Y0
00000	I31	I30	I29	•••	I16	I15	•••	I2	I1	I0
00001	I30	I29	I28	•••	I15	I14	•••	I1	I0	0
00010	I29	I28	I27	•••	I14	I13	•••	I0	0	0
00011	I28	I27	I26	•••	I13	I12	•••	0	0	0
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	I16	I15	I14	•••	I1	I0	•••	0	0	0
10000	I15	I14	I13	•••	I0	0	•••	0	0	0
10001	I14	I13	I12	•••	0	0	•••	0	0	0
10010	I13	I12	I11	•••	0	0	•••	0	0	0
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	I3	I2	I1	•••	0	0	•••	0	0	0
11101	I2	I1	I0	•••	0	0	•••	0	0	0
11110	I1	I0	0	•••	0	0	•••	0	0	0
11111	I0	0	0	•••	0	0	•••	0	0	0

significant bit of a 6-bit two's complement shift code, comprised of $R/\overline{L}$ concatenated with the SI4–SI0 lines. Thus a positive shift code ($R/\overline{L} = 0$) results in a left shift of 0–31 positions, and a negative code ($R/\overline{L} = 1$) a right shift of up to 32 positions. The LSH32 can thus effectively select any contiguous 32-bit field out of a (sign extended and zero filled) 96-bit "input."

OUTPUT MULTIPLEXER

The shift array outputs are applied to a 2:1 multiplexer controlled by the $MS/\overline{LS}$ select line. This multiplexer makes available at the output pins either the most significant or least significant 16 outputs of the shift array.

PRIORITY ENCODER

The 32-bit input bus drives a priority encoder which is used to determine the first significant position for purposes of normalization. The priority encoder produces a five-bit code representing the location of the first non-zero bit in the input word. Code assignment is such that the priority encoder output represents the number of shift positions required to left align the first non-zero bit of the input word. Prior to the priority encoder, the input bits are individually exclusive OR'ed with the SIGN input. This allows normalization in floating point systems using two's complement mantissa representation. A negative value in two's complement representation will cause the exclusive OR gates to invert the input data to the encoder. As a result the leading significant digit will always be "1." This affects only the encoder inputs; the shift array always operates on the raw input data. The priority encoder function table is shown in Table 4.

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TABLE 3. FILL MODE SHIFT CODE DEFINITIONS — RIGHT SHIFT

Shift Code	Y_{31}	Y_{30}	Y_{29}	···	Y_{16}	Y_{15}	···	Y_2	Y_1	Y_0
00000	S	S	S	···	S	S	···	S	S	S
00001	S	S	S	···	S	S	···	S	S	I_{31}
00010	S	S	S	···	S	S	···	S	I_{31}	I_{30}
00011	S	S	S	···	S	S	···	I_{31}	I_{30}	I_{29}
•	•	•	•	···	•	•	···	•	•	•
•	•	•	•	···	•	•	···	•	•	•
•	•	•	•	···	•	•	···	•	•	•
01111	S	S	S	···	S	S	···	I_{19}	I_{18}	I_{17}
10000	S	S	S	···	S	I_{31}	···	I_{18}	I_{17}	I_{16}
10001	S	S	S	···	I_{31}	I_{30}	···	I_{17}	I_{16}	I_{15}
10010	S	S	S	···	I_{30}	I_{29}	···	I_{16}	I_{15}	I_{14}
•	•	•	•	···	•	•	···	•	•	•
•	•	•	•	···	•	•	···	•	•	•
•	•	•	•	···	•	•	···	•	•	•
11100	S	S	S	···	I_{20}	I_{19}	···	I_6	I_5	I_4
11101	S	S	S	···	I_{19}	I_{18}	···	I_5	I_4	I_3
11110	S	S	I_{31}	···	I_{18}	I_{17}	···	I_4	I_3	I_2
11111	S	I_{31}	I_{30}	···	I_{17}	I_{16}	···	I_3	I_2	I_1

TABLE 4. PRIORITY ENCODER FUNCTION TABLE

I_{31}	I_{30}	I_{29}	···	I_{16}	I_{15}	···	I_2	I_1	I_0	Shift Code
1	X	X	···	X	X	···	X	X	X	00000
0	1	X	···	X	X	···	X	X	X	00001
0	0	1	···	X	X	···	X	X	X	00010
•	•	•	···	•	•	···	•	•	•	•
•	•	•	···	•	•	···	•	•	•	•
0	0	0	···	1	X	···	X	X	X	01111
0	0	0	···	0	1	···	X	X	X	10000
0	0	0	···	0	0	···	X	X	X	10001
•	•	•	···	•	•	···	•	•	•	•
•	•	•	···	•	•	···	•	•	•	•
0	0	0	···	0	0	···	0	1	X	11110
0	0	0	···	0	0	···	0	0	1	11111
0	0	0	···	0	0	···	0	0	0	11111

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NORMALIZE MULTIPLXER

The $\overline{NORM}$ input, when asserted results in the priority encoder output driving the internal shift code inputs directly. It is exactly equivalent to routing the SO4–SO0 outputs back to the SI4–SI0 inputs. The $\overline{NORM}$ input provides faster normalization of 32-bit data by avoiding the delay associated with routing the shift code off chip. When using the $\overline{NORM}$ function, the LSH32 should be placed in fill mode, with the R/$\overline{L}$ input low.

APPLICATIONS EXAMPLES

Normalization of mantissas up to 32 bits can be accomplished directly by a single LSH32. The $\overline{NORM}$ input is asserted, and fill mode and left shift are selected. The normalized mantissa is then available at the device output in two 16-bit segments, under the control of the output data multiplexer select, the MS/$\overline{LS}$.

If it is desirable to avoid the necessity of multiplexing output data in 16-bit segments, two LSH32 devices can be used in parallel. Both devices receive the same input word, with the MS/$\overline{LS}$ select line of one wired high, and the other low. Each device will then independently determine the shift distance required for normalization, and the full 32 bits of output data will be available simultaneously.

LONG-WORD NORMALIZATION (MULTIPLE CYCLES)

Normalization of floating point mantissas longer than 32 bits can be accomplished by cascading LSH32 units. When cascading for normalization, the device inputs are overlapped such that each device lower in priority than the first shares 16 inputs with its more significant neighbor. Fill mode and left shift are selected, however, internal normalization ($\overline{\text{NORM}}$) is not used. The most significant result half of each device is enabled to the output. The shift out (SO4–SO0) lines of the most significant slice are connected to the shift in lines of all

slices, including the first. The exception is that all SI4 lines are grounded, limiting the shift distance to 16 positions. The shift distance required for normalization is produced by the priority encoder in the most significant slice. The priority encoder will produce the shift code necessary to normalize the input word if the leading non-zero digit is found in the upper 16 bits. If this is the case, the number of shift positions necessary to accomplish normalization is placed on the SO4–SO0 outputs for use by all slices, and the appropriate 0–15 bit shift is accomplished. If the upper 16 bits are all zero, then the maximum shift of 15 places is executed. Single

clock normalization requiring shifts longer than 16 bits can be accomplished by a bank-select technique described below.

SINGLE CYCLE LONG-WORD NORMALIZATION

An extension of the above concept is a single clock normalization of long words (potentially requiring shifts of more than 15 places). The arrangement of LSH32s required is shown in Figure 1. Cascading of LSH32 units is accomplished by connecting the SI3–SI0 input lines of each unit to the SO3–SO0 outputs of the most significant device in the row as before. Essen-

FIGURE 1. SINGLE CYCLE LONG-WORD NORMALIZATION USING LSH32s
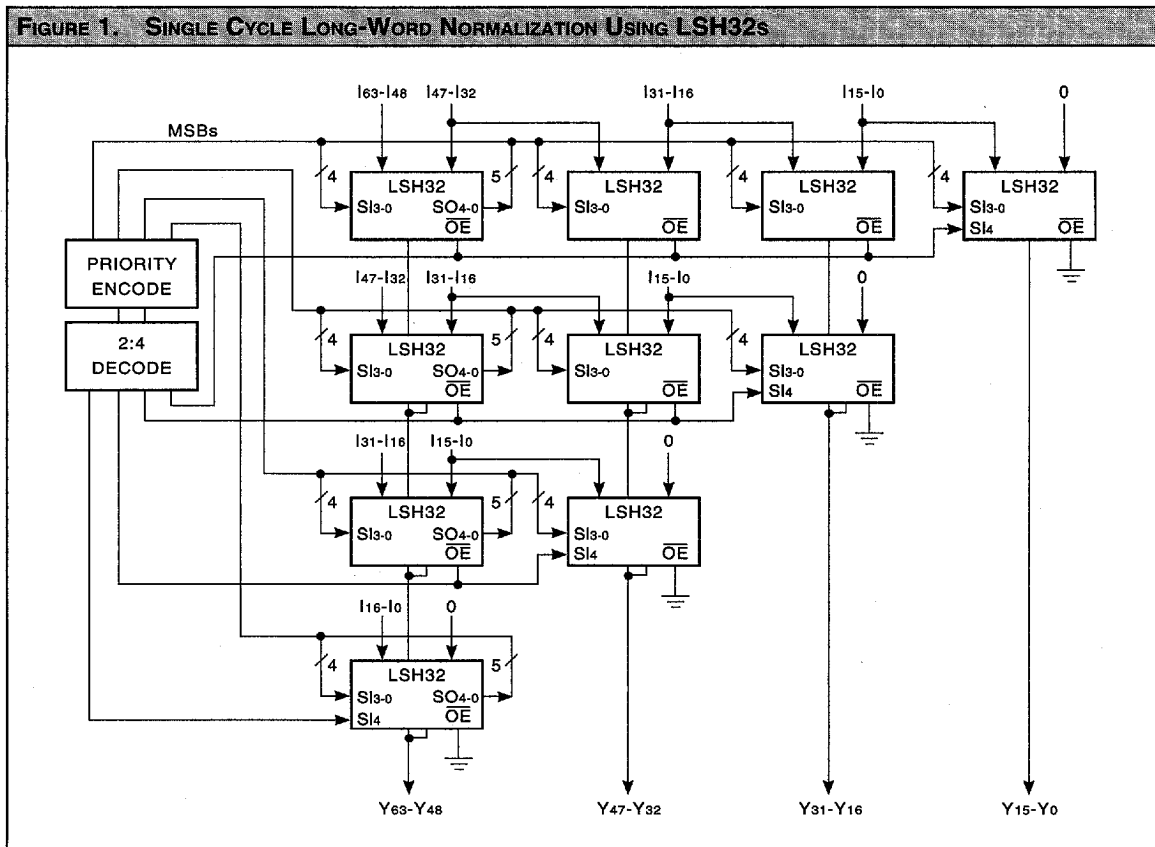
tially the LSH32s are arranged in multiple rows or banks such that the inputs to successive rows are left-shifted by 16 positions. The outputs of each row are multiplexed onto a three-state bus. The normalization problem then reduces to selecting from among the several banks that one which has the first non-zero bit of the input value among its 16 most significant positions. If the most significant one in the input file was within the upper 16 locations of a given bank, the SO4 output of the most significant slice in that bank will be low. Single clock normalization can thus be accomplished simply by enabling onto the three-state output bus the highest priority bank in which this condition is met. In this way the input word will be normalized regardless of the number of shift positions required to accomplish this.

The number of shift positions can be determined simply by concatenation of the SO3–SO0 outputs of the most significant slice in the selected row with the encoded Output Enable-bits determining the row number. Note that lower rows need not be fully populated. This is because they represent left shifts in multiples of 16 positions, and the lower bits of the output word will be zero filled. In order to accomplish this zero fill, the least significant device in each row is always enabled, and the row select is instead connected to the SI4 input. This will force the shift length of the least significant device to a value greater than 15 whenever the row containing that device is not selected. This results in zero fill being accomplished by the equivalently positioned slice in a higher bank, as shown in the diagram.

BLOCK FLOATING POINT

With a small amount of external logic, block floating point operations are easily accomplished by the LSH32. Data resulting from a vector operation are applied to the LSH32 with the $\overline{\text{NORM}}$-input deasserted. The SO4–SO0 outputs fill then represent the normalization shift distance for each vector element in turn. By use of an external latch and comparator, the maximum shift distance encountered across all elements in the vector is saved for use in the next block operation (or block normalization). During this subsequent pass through the data, the shift code saved from the previous pass is applied uniformly across all elements of the vector. Since the LSH32 is not used in the internal normalize mode, this operation can be pipelined, thereby obtaining the desired shift distance for the next pass while simultaneously applying the normalization required from the previous pass.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature .... −65°C to +150°C

Operating ambient temperature .... −55°C to +125°C

Vcc supply voltage with respect to ground .... −0.5 V to +7.0 V

Input signal with respect to ground .... −3.0 V to +7.0 V

Signal applied to high impedance output .... −3.0 V to +7.0 V

Output current into low outputs .... 25 mA

Latchup current .... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

| Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.5	mA

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SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)

Symbol	Parameter	LSH32–					
		42		32		20	
		Min	Max	Min	Max	Min	Max
tIY	I, SIGN Inputs to Y Outputs		42		32		20
tIYN	I, SIGN Inputs to Y Outputs, Normalize Mode		75		60		20
tISO	I, SIGN Inputs to SO Outputs		55		42		20
tSIY	SI, RIGHT/$\overline{\text{LEFT}}$ to Y Outputs		52		40		20
tMSY	MS/$\overline{\text{LS}}$ Select to Y Outputs		28		24		15
tDIS	Three-State Output Disable Delay (Note 11)		20		20		15
tENA	Three-State Output Enable Delay (Note 11)		20		20		15

MILITARY OPERATING RANGE (–55°C to +125°C) Notes 9, 10 (ns)

Symbol	Parameter	LSH32–					
		50		40		30	
		Min	Max	Min	Max	Min	Max
tIY	I, SIGN Inputs to Y Outputs		50		40		30
tIYN	I, SIGN Inputs to Y Outputs, Normalize Mode		85		75		58
tISO	I, SIGN Inputs to SO Outputs		65		52		42
tSIY	SI, RIGHT/$\overline{\text{LEFT}}$ to Y Outputs		62		52		40
tMSY	MS/$\overline{\text{LS}}$ Select to Y Outputs		32		26		24
tDIS	Three-State Output Disable Delay (Note 11)		22		20		17
tENA	Three-State Output Enable Delay (Note 11)		22		20		17

SWITCHING WAVEFORMS
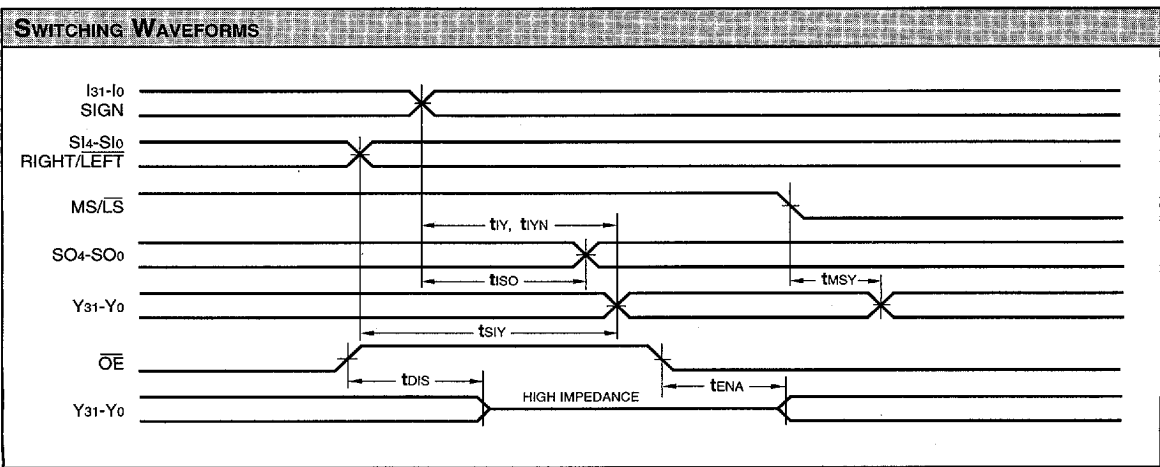
Special Arithmetic Functions

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at –0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except tDIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified IOH and IOL at an output voltage of VOH min and VOL max respectively. Alternatively, a diode bridge with upper and lower current sources of IOH and IOL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.
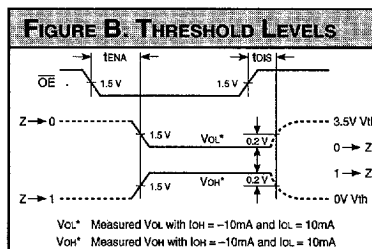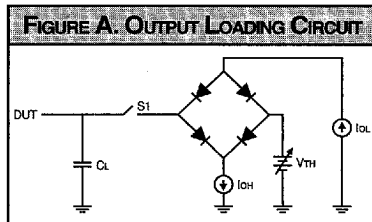
b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the tENA test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the tDIS test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, VTH, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

FIGURE B. THRESHOLD LEVELS

VOL* Measured VOL with IOH = –10mA and IOL = 10mA
VOH* Measured VOH with IOH = –10mA and IOL = 10mA

ORDERING INFORMATION

68-pin

Top View

Left/Top row pins:
I29 I28 I27 I26 I25 I24 I23 I22 I21 I20 I19 I18 I17 I16 I15 I14 GND
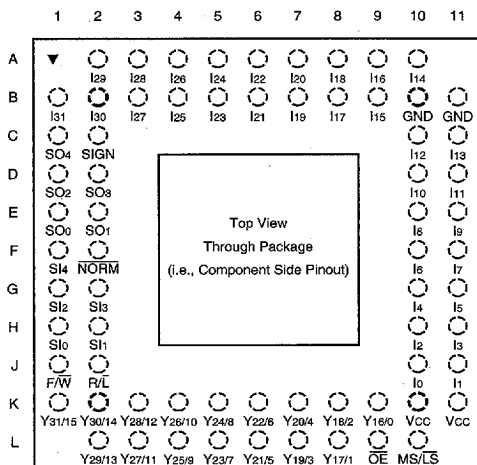(9 8 7 6 5 4 3 2 1 68 67 66 65 64 63 62 61)

Left side:
- I30]10
- I31]11
- SIGN]12
- SO4]13
- SO3]14
- SO2]15
- SO1]16
- SO0]17
- NORM]18
- SI4]19
- SI3]20
- SI2]21
- SI1]22
- SI0]23
- R/L]24
- F/W]25
- Y31/15]26

Right side:
- 60[GND
- 59[I13
- 58[I12
- 57[I11
- 56[I10
- 55[I9
- 54[I8
- 53[I7
- 52[I6
- 51[I5
- 50[I4
- 49[I3
- 48[I2
- 47[I1
- 46[I0
- 45[VCC
- 44[VCC

Bottom row pins (27–43):
Y30/14 Y29/13 Y28/12 Y27/11 Y26/10 Y25/9 Y24/8 Y23/7 Y22/6 Y21/5 Y20/4 Y19/3 Y18/2 Y17/1 Y16/0 OE MS/LS

68-pin

Top View
Through Package
(i.e., Component Side Pinout)

Columns 1–11

- A: ▼ I29 I28 I26 I24 I22 I20 I18 I16 I14
- B: I31 I30 I27 I25 I23 I21 I19 I17 I15 GND GND
- C: SO4 SIGN I12 I13
- D: SO2 SO3 I10 I11
- E: SO0 SO1 I8 I9
- F: SI4 NORM I6 I7
- G: SI2 SI3 I4 I5
- H: SI0 SI1 I2 I3
- J: F/W R/L I0 I1
- K: Y31/15 Y30/14 Y28/12 Y26/10 Y24/8 Y22/6 Y20/4 Y18/2 Y16/0 VCC VCC
- L: Y29/13 Y27/11 Y25/9 Y23/7 Y21/5 Y19/3 Y17/1 OE MS/LS

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Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Ceramic Pin Grid Array (G1)
0°C to +70°C — COMMERCIAL SCREENING			
42 ns	LSH32JC42		LSH32GC42
32 ns	LSH32JC32		LSH32GC32
20 ns	LSH32JC20		LSH32GC20
–55°C to +125°C — COMMERCIAL SCREENING			
50 ns			LSH32GM50
40 ns			LSH32GM40
30 ns			LSH32GM30
–55°C to +125°C — MIL-STD-883 COMPLIANT			
50 ns		LSH32KMB50	LSH32GMB50
40 ns		LSH32KMB40	LSH32GMB40
30 ns		LSH32KMB30	LSH32GMB30

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Special Arithmetic Functions