TECHNICAL MANUAL

LSI53C1510 I_2O-Ready PCI RAID Ultra2 SCSI Controller

Version 2.2

April 2001

LSI LOGIC®

S14024.B

Document DB14-000101-02, Fourth Edition (April 2001)
This document describes the LSI Logic LSI53C1510 I_2O-Ready PCI RAID Ultra2 SCSI Controller and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

To receive product literature, visit us at http://www.lsilogic.com.

Ultra SCSI is the term used by the SCSI Trade Association (STA) to describe Fast-20 SCSI, as documented in the SCSI-3 Fast-20 Parallel Interface standard, X3.277-199X.

Ultra2 SCSI is the term used by the SCSI Trade Association (STA) to describe Fast-40 SCSI, as documented in the SCSI Parallel Interface–2 standard, (SPI–2) X3T10/1142D.

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Preface

This book is the primary reference and technical manual for the LSI Logic Corporation LSI53C1510 I_2O-Ready PCI RAID Ultra2 SCSI Controller. It contains a complete functional description for the product and includes complete physical and electrical specifications.

This technical manual assumes the user is familiar with the current and proposed standards for SCSI and PCI. For additional background information on these topics, please refer to the list of reference materials provided in the Related Publications list.

Audience

This document was prepared for system designers and programmers who are using this device to design an Ultra2 SCSI port for PCI-based personal computers, workstations, servers or embedded applications.

Organization

This document has the following chapters and appendix:

- Chapter 1, **Introduction**, provides a general overview about the LSI53C1510.
- Chapter 2, **Functional Description**, describes the main functional areas of the chip in more detail, including the interfaces to the SCSI bus and external memory.
- Chapter 3, **Software Description**, describes the software features, firmware features, and hardware requirements.
- Chapter 4, **Signal Descriptions**, contains the pin configuration signal definitions.

- Chapter 5, **Registers (Nonintelligent Mode)**, describes the PCI and host interface registers that are visible to the host in nonintelligent mode.
- Chapter 6, **Registers (Intelligent Mode)**, describes the PCI and host interface registers that are visible to the host in intelligent mode.
- Chapter 7, **Specifications**, contains the electrical characteristics and AC timing diagrams.
- Appendix A, **Register Summary**, is a register summary.

Related Publications

For background please contact:

ANSI
11 West 42nd Street
New York, NY 10036
(212) 642-4900
Ask for document number X3.131-199X (SCSI-2)

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
(800) 854-7179 or (303) 397-7956 (outside U.S.) FAX (303) 397-2740
Ask for document number X3.131-1994 (SCSI-2) or X3.253
(SCSI-3 Parallel Interface)

ENDL Publications
14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642
Document names: *SCSI Bench Reference, SCSI Encyclopedia, SCSI Tutor*

Prentice Hall
113 Sylvan Avenue
Englewood Cliffs, NJ 07632
(800) 947-7700
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

LSI Logic World Wide Web Home Page
www.lsil.com

PCI Special Interest Group
2575 N. E. Katherine
Hillsboro, OR 97214
(800) 433-5177; (503) 693-6232 (International); FAX (503) 693-8344

I_2O (Intelligent Input/Output) SIG Web Site
http:\\www.i2osig.org

LSI53C1510 I_2O-Ready PCI RAID Ultra2 SCSI Controller Programming Guide

SCSI SCRIPTS Processors Programming Guide, Order Number S14044.A

LSI53C896 PCI to Dual Channel Ultra2 SCSI Multifunction Controller Technical Manual, Order Number S14015.B

Conventions Used in This Manual

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

Hexadecimal numbers are indicated by the prefix “0x” —for example, 0x32CF. Binary numbers are indicated by the prefix “0b” —for example, 0b0011.0010.1100.1111.

Revision Record

Revision	Date	Remarks
0.1	3/98	First Draft.
0.2	4/98	Second Draft.
1.0	5/98	Preliminary.
1.1	5/98	Preliminary. Change bars mark all changes. In Chapter 7, all GPIO0_FETCH/ and GPIO1_MASTER/ items were deleted.
2.0	1/00	Final Version.
2.1	11/00	Updated Table 7.2 Operating Conditions. All product names changed from SYM to LSI.
2.2	4/01	Updated DC electrical specifications and test conditions.

Contents

Figures

Tables

Chapter 1
Introduction

This chapter provides a general overview of the LSI53C1510 I_2O-Ready PCI RAID Ultra2 SCSI Controller. The chapter contains the following sections:

1.1 General Description

The LSI53C1510 is a single chip I_2O-Ready PCI RAID Ultra2 SCSI Controller. The LSI53C1510 contains a 32-bit RISC ARM7TDMI Processor and a RAID Parity Assist Engine (PAE). The RISC processor frees the host CPU from the burden of processing I/O requests and reduces the number of I/O interrupts, thus improving system performance. The RISC processor and associated firmware contain the ability to manage an I/O from start to finish without host intervention. The RISC processor manages the Intelligent Input/Output (I_2O) message passing interface.

The LSI53C1510 has two modes of operation: intelligent or nonintelligent mode. In intelligent mode, the LSI53C1510 functions as an embedded RAID controller on a motherboard or as an add-in RAID host adapter board. In nonintelligent mode the LSI53C1510 functions as a PCI to SCSI dual channel wide Ultra2 controller.

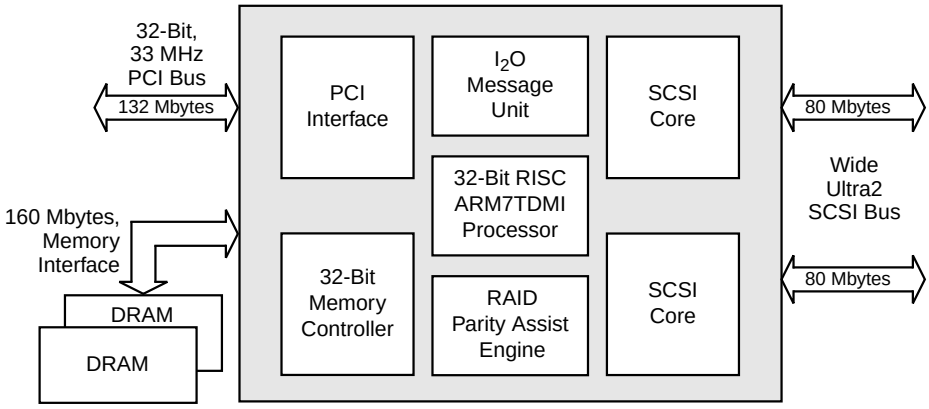
The LSI53C1510 is sold as a package with LSI Logic I_2O RAID software to provide a RAID solution. Therefore, this manual describes the hardware and software only in enough detail for system intergrators to design the LSI53C1510 onto a motherboard or a host adapter board. The I_2O RAID software consists of the LSI Logic I_2O RAID Device Driver Module (DDM), SYMplicity™ Storage Manager, and Wind River Systems' IxWorks RTOS.

The LSI53C1510 is a combination of many tried and proven modules. These modules have been proven in single and multimodule configurations. The following block diagram illustrates the major modules of the LSI53C1510.

1.1.1 Block Diagram

The LSI53C1510 is a multifunction device composed of many modules. Figure 1.1 is a block diagram of the LSI53C1510.

Figure 1.1 LSI53C1510 Block Diagram



1.2 Module Overviews

This section provides an overview of the six major LSI53C1510 modules, which consist of the PCI Interface, Memory Controller, I_2O Messaging Unit, ARM7TDMI RISC Processor, RAID PAE and SCSI Cores. Chapter 2, "Functional Description," provides a detailed description of the functions of each module.

1.2.1 PCI Interface

The PCI interface is a 32-bit, 33 MHz host PCI bus. The PCI interface supports Dual Address Cycle (DAC), PCI Power Management, and Subsystem Vendor ID. The PCI interface also contains a PCI Master and Slave control block, PCI configuration registers, and DMA channel arbitration. This chip supports 64-bit addressing as a PCI master and supports 32-bit addressing as a PCI slave.

1.2.2 Memory Controller

The memory controller provides access to Flash ROM, SRAM, and 32-bit EDO DRAM with parity (50 ns access time). It supports two 64 Mbytes (maximum configuration of 128 Mbytes) banks of DRAM. To support the ROM and SRAM, there is a general purpose 8-bit expansion memory bus that supports up to 4 Mbytes Flash ROM. It also supports up to 2 Mbytes of SRAM and is designed to interface efficiently to an external 8 K x 8 battery backed up SRAM.

1.2.3 I_2O Message Unit

The messaging interface efficiently passes messages between the LSI53C1510 and other I/O agents in an I_2O enabled system. The I_2O Message Unit consists of the following four hardware FIFOs for the message queuing lists: Request Free, Request Post, Reply Free, and Reply Post. The LSI53C1510 provides control logic for the I_2O Message Unit and external local memory provides storage for the messages.

1.2.4 ARM7TDMI RISC Processor

The LSI53C1510 uses an optimized 32-bit ARM7 RISC Processor core to control all RAID functionality. This frees the host CPU for other processing activity and improves I/O performance. The RISC processor and associated firmware contain the ability to manage an I/O from start to finish without host intervention. The RISC processor also manages the I_2O message passing I/O interface.

1.2.5 RAID Parity Assist Engine (PAE)

The Hardware PAE offloads the parity generation and checking from the host. It allows multiple parity operations to be queued for maximum efficiency.

1.2.6 SCSI Cores

The integrated SCSI cores are high-performance dual wide Ultra2 SCSI channels supporting either Single-Ended (SE) or Low Voltage Differential (LVD) SCSI. The cores are based on the popular LSI53C8XX controllers and are capable of up to Ultra2 transfer rates for each channel.

1.3 LSI53C1510 Features

The LSI53C1510 integrates a PCI bus master DMA core, two high-performance SCSI cores, and two LSI Logic SCSI SCRIPTS™ processors to meet the broad requirements of Wide Ultra2 SCSI standards. It is designed to implement multithreaded I/O algorithms with a minimum of processor intervention, solving the protocol overhead problems of previous intelligent and nonintelligent controller designs.

In nonintelligent mode, the LSI53C1510 is fully supported by the Storage Device Management System (SDMS™), a software package that supports the Advanced SCSI Protocol Interface (ASPI). SDMS software provides BIOS and driver support for hard disk, tape, removable media products, and CD-ROM under the major PC operating systems.

In intelligent mode, the LSI53C1510 is a complete, single chip RAID solution for the motherboard—just add memory. The RAID product solution consists of a RAID SYMplicity Storage Manager, SYMplicity I_2O RAID firmware with Wind River System IxWorks, and hardware.

1.3.1 Features List

- Highly integrated single chip RAID Controller
- I_2O Messaging Unit
- RAID PAE
- 32-bit/33 MHz host PCI Bus
  - DAC
  - PCI Power Management
  - PCI cache commands (MRL, MRM, MWI)
- Two wide Ultra2 SCSI Channels
  - SE or LVD SCSI
  - Based upon the popular LSI53C8XX controller
- 32-bit RISC ARM7TDMI Processor
- 32-bit Memory Controller
  - Up to two banks of 64 Mbytes EDO (50 ns access time) DRAM
- General purpose 8-bit expansion bus
  - Supports up to 4 Mbytes ROM
  - Chip enable to support an external 8 K x 8 battery backed SRAM

1.4 LSI53C1510 Benefits

This section provides a description of the major LSI53C1510 benefits.

1.4.1 Ultra2 SCSI Benefits

Ultra2 SCSI is an extension of the SPI-2 draft standard that allows faster synchronous SCSI transfer rates and defines a new physical layer, LVD SCSI, that provides an incremental evolution from SCSI-2 and Ultra SCSI. When enabled, Ultra2 SCSI (8-bit) performs transfers of

40 Mbytes/s, which results in approximately double the synchronous transfer rate of Ultra SCSI. The LSI53C1510 can perform 16-bit (wide), Ultra2 SCSI synchronous transfers as fast as 80 Mbytes/s. This advantage is most noticeable in heavily loaded systems, or large block size applications such as video on-demand and image processing.

An advantage of Ultra2 SCSI is that it significantly improves SCSI bandwidth while preserving existing hardware and software investments.

1.4.2 LVDlink™ Benefits

The LSI53C1510 supports LVD SCSI, a signaling technology that increases the reliability of SCSI data transfers over longer distances than supported by SE SCSI. The low current output of LVD allows the I/O transceivers to be integrated directly onto the chip. LVD provides the reliability of High Voltage Differential (HVD) SCSI without the added cost of external differential transceivers. Ultra2 SCSI with LVD allows a longer SCSI cable and more devices on the bus, with the same cables defined in the SCSI-3 parallel interface standard for Fast-20 (Ultra SCSI). LVD provides a long-term migration path to even faster SCSI transfer rates without compromising signal integrity, cable length, or connectivity.

For backward compatibility to existing SE devices, the LSI53C1510 features universal LVDlink transceivers that can switch between LVD SCSI and SE modes. The LVDlink technology also supports high power differential signaling in legacy systems, when external transceivers are connected to the LSI53C1510. This allows the LSI53C1510 to be used in both legacy and Ultra2 SCSI applications.

1.4.3 TolerANT® Technology Benefits

The LSI53C1510 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Through active negation, the SCSI Request, Acknowledge, Data, and Parity signals are actively driven high rather than passively pulled up by terminators. Active negation is enabled by setting bit 7 in the STEST3 register.

TolerANT receiver technology improves data integrity in unreliable cabling environments, where other devices are subject to data corruption. TolerANT receivers filter the SCSI bus signals to eliminate unwanted transitions, without the long signal delay associated with RC-type input

filters. This improved driver and receiver technology helps eliminate double clocking of data, the single biggest reliability issue with SCSI operations. TolerANT input signal filtering is a built-in feature of the LSI53C1510 and all LSI Logic fast SCSI, Ultra SCSI, and Ultra2 SCSI devices.

The benefits of TolerANT technology include increased immunity to noise on the deasserting signal edge, better performance due to balanced duty cycles, and improved Ultra2 SCSI transfer rates. In addition, TolerANT SCSI devices do not cause glitches on the SCSI bus at power-up or power-down, so other devices on the bus are also protected from data corruption. TolerANT technology is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

1.4.4 I_2O Benefits

The I_2O-ready design of the LSI53C1510 improves system performance by reducing interrupts to the host CPU and minimizing PCI bandwidth through the packetized mailbox interface. These features are particularly important in high-performance symmetric multiprocessing servers and clustered computing systems. The benefits of the I_2O architecture fully compliment those of SCSI and include reduced host CPU I/O overhead for better system performance, improved scalability, reduced time to market for new I/O technology, reduced cost of integration and support for I/O.

1.4.5 PAE Benefits

When the LSI53C1510 is in intelligent mode, the embedded PAE works with RAID applications to perform parity generation or checking as requested. The PAE writes any generated parity data block back into local memory. The hardware PAE offloads the parity generation and checking from the host and it generates parity faster than software applications. The PAE allows multiple parity operations to be queued for maximum efficiency. This frees the host CPU for other processing activity and improves I/O performance.

1.4.6 ARM7TDMI RISC Processor Benefits

The ARM processor manages the I_2O message passing I/O interface. The embedded RISC processor (ARM7TDMI) improves system performance by reducing interrupts to the host CPU and minimizing PCI bandwidth. The ARM processor and associated software contain the ability to manage an I/O from start to finish without host intervention. This frees the host CPU for other processing activity and improves I/O performance.

1.5 LSI53C1510 Benefits Summary

This section provides a summary of the PCI, SCSI, and RAID performance benefits. It also provides a summary of the Testability, Integration, and Reliability benefits.

1.5.1 PCI Performance

- Fully PCI 2.1 Specification compliant
- True multifunction device as defined in PCI 2.1 Specification in nonintelligent mode and it presents only one load to the PCI bus
- Supports 32-bit word data bursts with variable burst lengths of 2, 4, 8, 16, 32, 64 or 128 Dwords across the PCI bus
- Prefetches up to 8 Dwords of SCSI SCRIPTS
- Performs zero wait-state bus master data bursts at 132 Mbytes/s (@ 33 MHz)
- Supports PCI Cache Line Size register
- Supports PCI Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple commands

1.5.2 SCSI Performance

- Includes 4 Kbytes internal RAM on each SCSI channel for SCRIPTS instruction storage, thus reducing PCI bus utilization
- Wide Ultra SCSI SE Interface
- Performs Wide Ultra2 SCSI synchronous transfers as fast as 80 Mbytes/s with LVD

- 816-byte DMA FIFO for more effective PCI and SCSI bus utilization
- SCSI synchronous offset of 31 levels for maximum performance in long cable situations
- Supports variable block size and scatter/gather data transfers
- Minimizes SCSI I/O start latency
- Performs complex bus sequences without interrupts, including restore data pointers
- Reduces ISR overhead through a unique interrupt status reporting method
- Load/Store SCRIPTS instruction increases performance of data transfers to and from chip registers
- Supports target disconnect and later reconnect with no interrupt to the system processor
- Supports multithreaded I/O algorithms in SCSI SCRIPTS with fast I/O context switching
- Expanded register Move instruction support
- Software (drivers and SCRIPTS) compatible with LSI53C8XX
- Integrated clock quadrupler enables Ultra2 SCSI with 40 MHz SCSI clock input

1.5.3 RAID Performance

- Maximum transfer rate: 80 Mbytes/s with Wide Ultra2 SCSI
- Number of drives: 30 maximum (10 to 15 drives in typical application)
- Supports RAID levels 0, 1, 3, 5, 10 and JBOD

1.5.4 Testability

- Access to all SCSI signals through programmed I/O
- SCSI loopback diagnostics
- SCSI bus signal continuity checking
- Single-step mode operation

1.5.5 Integration

- Dual Channel SCSI Multifunction Controller
- 3.3 V/5 V PCI interface
- Full 32-bit PCI DMA bus master
- High-performance SCSI cores
- Integrated SCSI SCRIPTS processors
- ARM7TDMI 32-bit RISC processor
- RAID PAE
- I_2O Message Unit

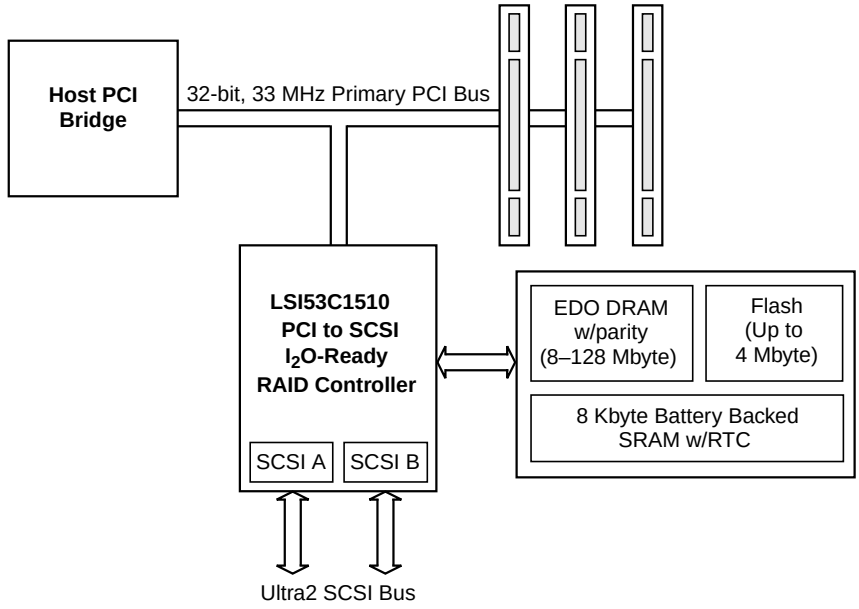
1.5.6 Reliability

- 2 kV ESD protection on SCSI signals
- Typical 300 mV SCSI bus hysteresis
- Protection against bus reflections due to impedance mismatches
- Controlled bus assertion times (reduces RFI, improves reliability, and eases FCC certification)
- Latch-up protection greater than 150 mA
- Voltage feed-through protection (minimum leakage current through SCSI pads)
- Power and ground isolation of I/O pads and internal chip logic
- TolerANT technology provides:
  - Active negation of SCSI Data, Parity, Request, and Acknowledge signals for improved fast SCSI transfer rates
  - Input signal filtering on SCSI receivers improves data integrity, even in noisy cabling environments

1.6 Applications

There are many different applications and configurations for the LSI53C1510 I_2O-Ready PCI RAID Ultra2 SCSI Controller. Figure 1.2 illustrates a typical LSI53C1510 embedded motherboard application. Figure 1.3 illustrates a typical LSI53C1510 host adapter board application.

Figure 1.2 Typical LSI53C1510 Mainboard Applications



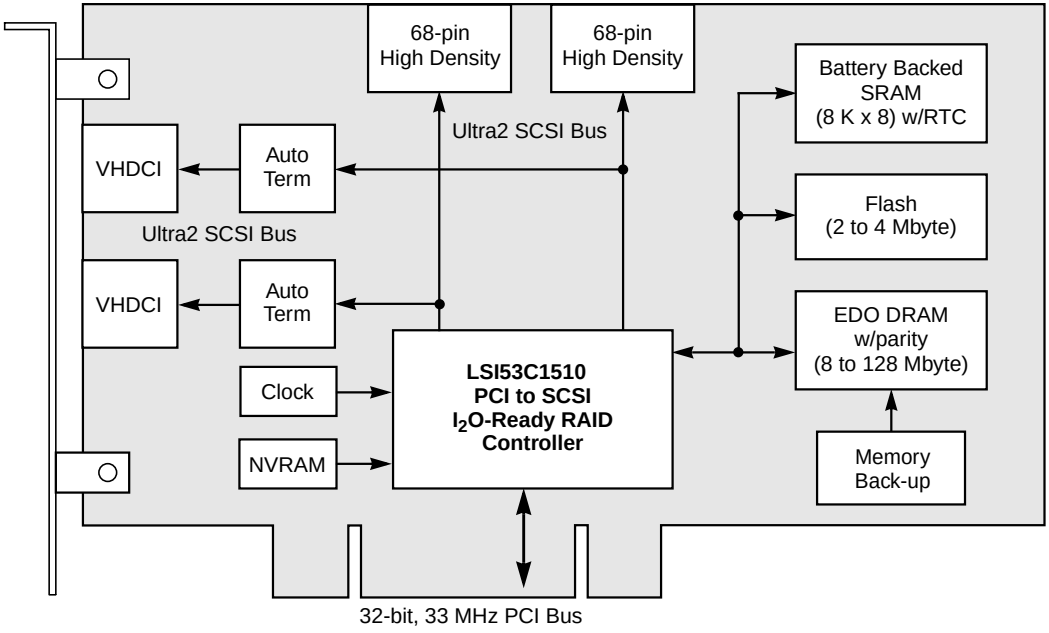
1.6.1 Embedded Motherboard Application

The LSI53C1510 is ideally suited for embedded motherboard RAID applications. The amount of motherboard space required to implement such an application is critical. The limited space available on the motherboard dictates a highly integrated solution like the LSI53C1510. All of the major functional blocks of RAID controller including processor, memory controller, XOR engine, and SCSI controllers are integrated into the LSI53C1510. This greatly reduces the amount of board space

required to implement a RAID controller. Not only does this make RAID on the motherboard a viable solution, it also greatly reduces the cost of implementing it.

Because the LSI53C1510 supports both RAID and non-RAID operational modes, it gives the motherboard designer the option of building a base motherboard that uses the LSI53C1510 as a dual channel Ultra2 SCSI controller. The additional memory and real time clock required for RAID operation can then be provided on an optional RAID upgrade card that plugs into a connector mounted on the motherboard.

Figure 1.3 Typical LSI53C1510 Host Adapter Board Application



1.6.2 Host Adapter Board Application

The LSI53C1510 single chip RAID solution can be designed on an add-in host adapter card. This provides a highly scalable solution where additional storage and/or performance can be obtained by adding additional host adapter cards.

Chapter 2
Functional Description

The chapter contains the following sections:

The LSI53C1510 contains an ARM7 32-bit RISC Processor, a RAID PAE, and a DMA engine. The RISC processor frees the host CPU for other processing activity and improves performance. The RISC processor and associated software contain the ability to manage an I/O from start to finish without host intervention. The RISC processor also manages the I_2O message passing I/O interface. The DMA engine moves blocks of data between system memory and the LSI53C1510 local memory.

The LSI53C1510 uses a 32-bit PCI interface for communication with the host CPUs and system memory. The host interface to the LSI53C1510 is designed to minimize the amount of PCI bandwidth required to support I/O requests. A packetized message passing I/O interface is used to reduce the number of single cycle PCI bus cycles. All data traffic across the PCI bus occurs with zero wait-state bursts.

The intelligent LSI53C1510 architecture allows the host to specify I/Os at a very high level. Complete SCSI functionality is provided in the LSI53C1510, relieving the host CPU(s) from managing I/Os.

2.1 Modes of Operation

The LSI53C1510 has two modes of operation: intelligent or nonintelligent mode. In intelligent mode, the LSI53C1510 functions as an embedded RAID controller on a motherboard or as an add-in RAID host adapter board. In nonintelligent mode the LSI53C1510 functions as a PCI to SCSI dual channel wide Ultra2 controller. These modes are entered during the initialization of the LSI53C1510 on power-up. The presence or absence of external memory determines which mode is entered. In intelligent mode, the LSI53C1510 uses its built-in ARM processor. In nonintelligent mode, the ARM processor is disabled. Table 2.1 shows the LSI53C1510 modes of operation.

Table 2.1 LSI53C1510 Modes

Modes	External Memory	Configurations
Intelligent I_2O RAID Controller	Yes	RAID
Nonintelligent Dual Channel Controller	No	Dual Channel Wide Ultra2 SCSI Controller

2.1.1 LSI53C1510 Overview

Figure 2.1 LSI53C1510 Block Diagram

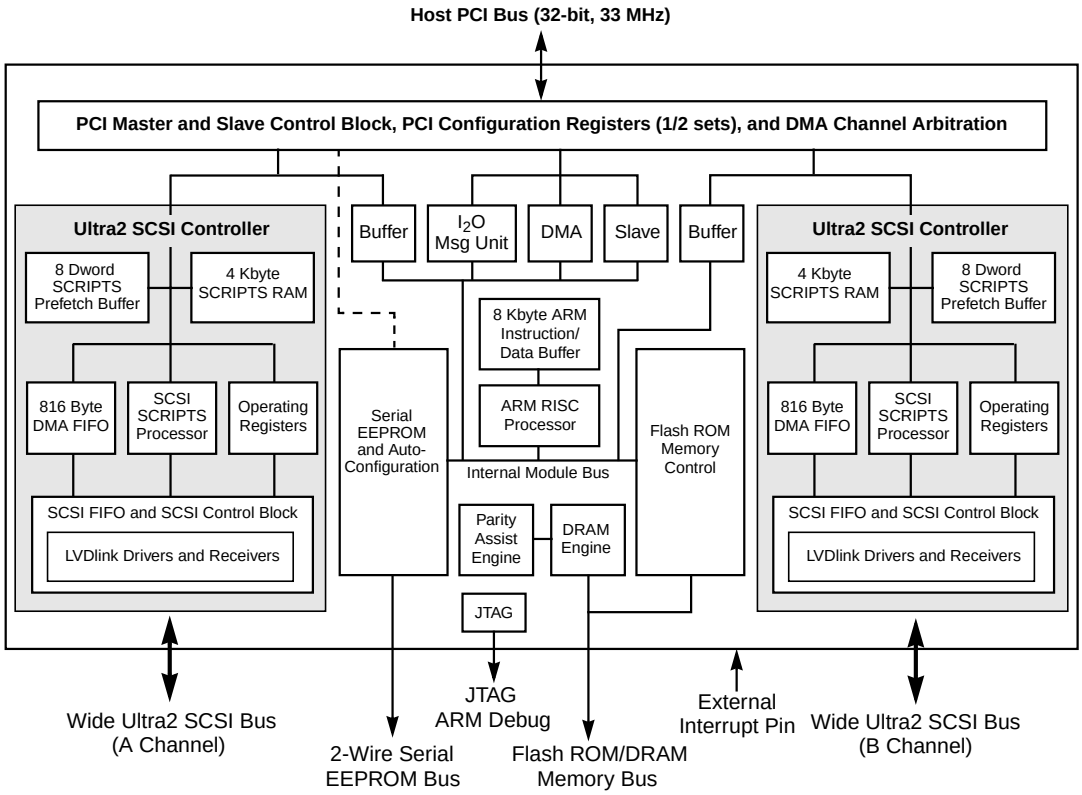


Figure 2.1 illustrates the major components of the LSI53C1510 controller. A dual channel PCI interface function block provides slave access steering between the two SCSI cores when operating in nonintelligent mode.

The Slave Access and Messaging Unit utilizes a FIFO for fast host system service and for speed matching between the 33 MHz domain of the PCI bus and the 40 MHz clock domain of the memory controller. The DMA unit contains a single data FIFO for both read and write operations. The SCSI cores each contain control registers and 4 Kbytes SCRIPTS RAM. When operating in nonintelligent mode, these are mapped

according to the Memory 0 and Memory 1 Base Address registers. When in intelligent mode, the control registers are mapped into Memory 0 Base Address registers.

The PAE accesses data and parity in the LSI53C1510 local memory and performs XOR operations to generate parity and data blocks. Multiple sources can be specified for each operation and multiple operations can be queued within the unit.

The memory controller includes a 32-bit with parity EDO DRAM interface, plus an 8-bit utility interface supporting SRAM, Flash ROM, plus user-defined external components.

2.1.2 Configuration and Initialization

The LSI53C1510 initializes as a nonintelligent dual channel SCSI controller, or as an intelligent I/O Processor (IOP). External pins are sensed at power-on and either nonintelligent mode or intelligent mode is selected. The power-on mode also determines which set of PCI configuration register values will be used. When in nonintelligent mode, the LSI53C1510 is a dual function PCI device with two sets of configuration registers. When in intelligent mode, the LSI53C1510 is a single function device with a single set of PCI configuration registers.

The MEM_ADDR bus is used to determine power-on configuration. During power-on, internal 25 µA pull-downs are activated. If desired, these pull-downs can be overridden using 10 kΩ external pull-up resistors. This will change the default power-up conditions of the part. Table 2.2 shows the ROM size configurations the eight MEM_ADDR lines generate. The eight MEM_ADDR lines control the following configuration options. Options shown in Table 2.3 are enabled using pull-up resistors.

Table 2.2 ROM Size Configurations

MEM_ADDR [3:0]	Options
0000	16 Kbytes ROM Size (No external pull-ups)
0001	32 Kbytes ROM Size
0010	64 Kbytes ROM Size
0011	128 Kbytes ROM Size
0100	256 Kbytes ROM Size
0101	512 Kbytes ROM Size
0110	1024 Kbytes ROM Size
0111	2048 Kbytes ROM Size
1000	4096 Kbytes ROM Size
1001–1110	Reserved
1111	No ROM present

Table 2.3 Configuration Options

MEM_ADDR [4:9]	Options
Bit 4	Disable boot
Bit 5	RAID_MODE, based on SIMM/memory population
Bit 6	Disables SCSI SCRIPTS RAM
Bit 7	Disables EEPROM downloads
Bit 8	Reserved
Bit 9	Channel B uses INTA instead of INTB

2.1.3 I_2O Overview

When the LSI53C1510 is in intelligent mode, the RISC processor manages the I_2O message passing I/O interface. I_2O defines a standard architecture for intelligent I/O, where low level interrupts are offloaded from the host CPU to the ARM IOP designed specifically to handle I/O. With support for message passing between multiple independent processors, the I_2O architecture relieves the host of interrupt intensive I/O tasks, greatly improving I/O performance in high bandwidth applications such as RAID. I_2O imposes no restrictions on where layered modules execute, providing support for single processor, multiprocessor and clustered systems.

The I_2O specification also defines a “split driver” model for creating drivers that are portable across multiple OSs and host platforms. Through the split driver model, I_2O significantly decreases the number of drivers required. OS vendors write a single I_2O-ready driver for each class of device, such as SCSI Peripheral Class or Random Block Storage Class. Device manufacturers, like LSI Logic, write a single I_2O software program for each device, such as the LSI53C1510, which works for any OS that supports I_2O.

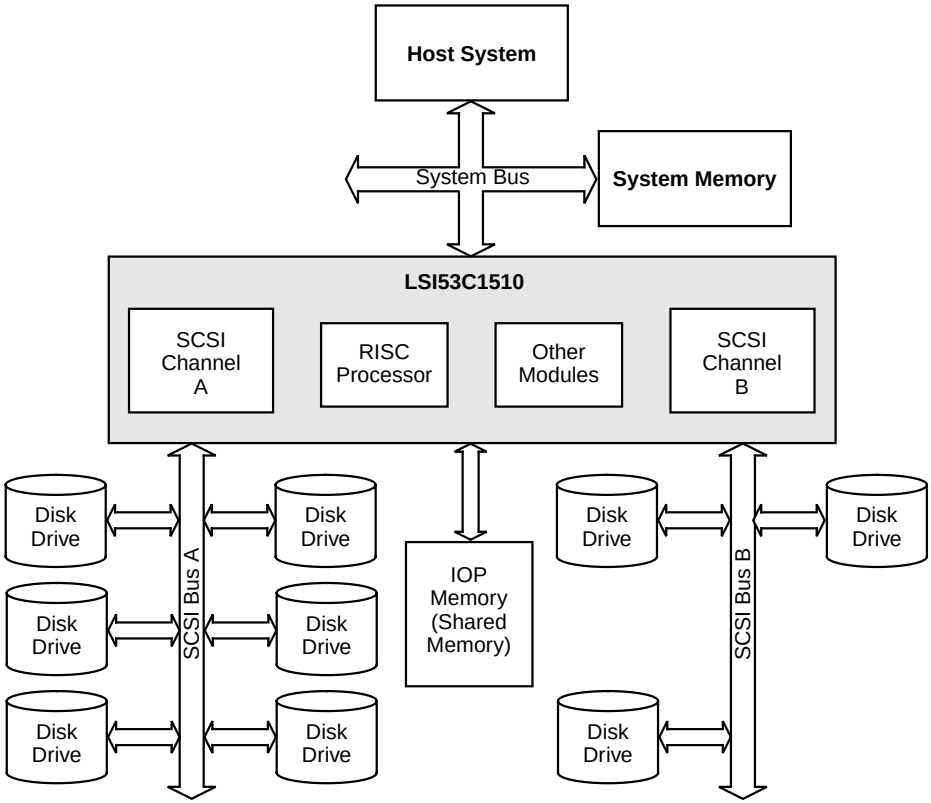
2.1.4 I_2O Conceptual Overview

The split I_2O drivers are composed of two parts: the Operating System Services Module (OSM), that resides on and interfaces to the host OS; and the Hardware Device Module (HDM), that resides on and interfaces with the LSI53C1510 adapter to be managed by the driver. The HDM and the Intermediate Service Module (ISM) are often referred to collectively as DDMs. The ISM is a driver an independent software vendor can supply to add value or a specialized function to the LSI53C1510. These modules interface with each other through a communication system comprised of two layers: a Message Layer that sets up a communication session, and a Transport Layer that defines how information will be shared. Much like a standard communications protocol, the Message Layer resides on top of the Transport Layer.

2.1.5 I_2O Benefits

The I_2O operating environment of the LSI53C1510 provides two main advantages. First, it enables the system vendor, LSI Logic, to create an I/O platform that can support a number of intelligent configurations. The second advantage is the capability of stacked drivers, that enable a third party software vendor to provide value added expansion capability, independent of both the OS and the hardware. Figure 2.2 illustrates various ways the LSI53C1510 can be configured.

Figure 2.2 Example of LSI53C1510 Physical Configurations



2.1.6 The I_2O Communications Model

The communications model for the I_2O architecture is a message passing system. The communication model defines how two entities exchange messages by using the Message Layer to set up a connection and exchange data and control.

When the OSM is presented with a request from the host OS, it translates the request into an I_2O message and dispatches it to the LSI53C1510 for processing. Upon completion of the request, the LSI53C1510 dispatches the result back to the OSM by sending a message through the I_2O Message Layer. To the host OS, the OSM appears just like any other device driver. See Section 2.2.1, "Messages," later in this chapter for more detail.

2.1.7 Operational Overview

After power-on, the LSI53C1510 is configured as either a nonintelligent or intelligent controller. In intelligent mode, the LSI53C1510 initializes from local ROM and then issues and responds to I_2O messages exchanged with the host system. Messages are decoded into local actions, usually involving the transfer of data. Data may be moved between the host system and the LSI53C1510 local memory through the LSI53C1510's DMA controller, or by the host system. The two SCSI cores transfer data between disk and local memory or between disk and host system memory.

2.1.8 System Interface

The LSI53C1510 architecture features a generic, message passing I/O interface. The LSI53C1510 Protocol Engine provides a set of four hardware FIFOs for Message Queuing between the LSI53C1510 and the primary host (or other hosts and peers). The four FIFOs are:

- Request Free List
- Request Post List
- Reply Free List
- Reply Post List

These FIFOs are used to manage how/where messages are sent and received.

Control logic for the four hardware FIFOs is provided within the Protocol Engine. Storage for the FIFO entries is provided in external local memory. Each element within each of these FIFOs contains a Message Frame Address (MFA). The MFA is the offset from the first memory base address register (Memory 0 Base Address) where a Message Frame is located (Push model). The number of FIFO elements is configurable. Supported FIFO depths are powers of two between 256 and 4096.

In addition to the hardware FIFOs, a region of shared memory is provided (the LSI53C1510 local memory mapped to System Addresses) for the host to write Request Message Frames into. This is the default method (Push model) for Request Message Frame transport, where the host itself copies the Request Message Frame into the LSI53C1510 local memory.

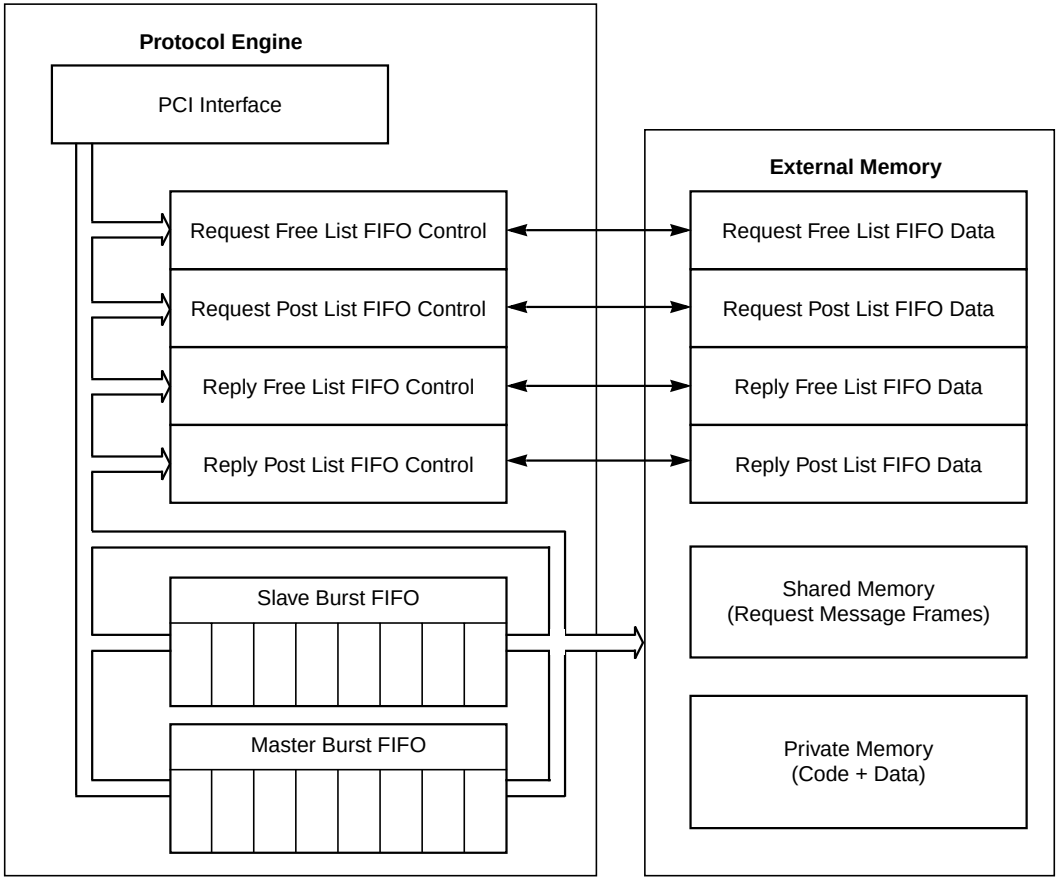
To support shared memory access (read/write), the LSI53C1510 Protocol Engine includes a slave burst FIFO (depth of 128 bytes), slave burst logic including address capture and increment, and address translation between System and Local memory addresses.

Reply Message Frames are always pushed from the LSI53C1510 Protocol Engine to System memory; the Protocol Engine includes a DMA channel for transferring Reply Message Frames. This DMA channel may also be used for other purposes such as downloading software or uploading trace information. Also present within the Protocol Engine is a System Read/Write interface which provides the ARM processor the ability to read/write a single arbitrary Dword from system memory. See Figure 2.3 for an illustration of the FIFOs and memory in the Protocol Engine and External Memory.

2.1.8.1 LSI53C1510 Protocol Engine Overview

The LSI53C1510 Protocol Engine contains an ARM processor core, a local bus and controller, an 8 Kbytes Instruction Cache, an 8 Kbyte Instruction/Data Buffer, an External Memory Controller, an Instruction Prefetch Unit, a write Buffer, an interface to the host system, and a Timer/Control block. The LSI53C1510 Protocol Engine functions as an intelligent IOP. It receives Request Messages from the host CPU, processes them, and sends Reply Messages back to the host. Processing of Request Messages typically involves an I/O transaction; the Protocol Engine and associated software together contain the ability to manage an I/O from start to finish without host intervention.

Figure 2.3 Hardware Messaging Unit



2.2 The Host Interface

The LSI53C1510 host interface is compliant with the I_2O Specification, Revision 1.5. This host interface is a high-performance, packetized, mailbox architecture which leverages intelligence in the LSI53C1510 to minimize traffic on PCI. See http:\\www.i2osig.org on the I_2O Special Interest Group (SIG) web site for more information.

SYMplicity is the LSI Logic implementation of I_2O architecture. There are two basic constructs in I_2O. The first construct, the Message, is used to communicate between the host and the LSI53C1510. Messages are moved between the host(s) and the LSI53C1510 using the second construct, a Transport mechanism.

2.2.1 Messages

The LSI53C1510 uses Request and Reply Messages to communicate with the host. Request messages are created by the host to “request” an action by the LSI53C1510. Reply messages are used by the LSI53C1510 to send status information back to the host.

Request message data structures are 128 bytes in length. The message includes a message header and a payload. The header includes information to uniquely identify the message. The message header information is sophisticated enough to support multiple hosts and targets. The payload may be any one of three different mechanisms to communicate scatter/gather information to the LSI53C1510.

2.2.2 Message Transport

Request and Reply Messages reside in preallocated message frames. Message frames may reside in PCI shared memory local to the LSI53C1510 or in host memory.

The host selects where the Request and Reply messages are located during the LSI53C1510 initialization. The default, power-up configuration, places Request messages in PCI shared memory local to the LSI53C1510. As an option, the Request messages can reside in host memory. The Reply messages, however, always reside in host memory.

Pointers that point to the Request and Reply Messages are called MFAs. The LSI53C1510 is responsible for the initialization and management of the MFAs in the default model. The LSI53C1510 includes a set of four FIFOs which are used to track the Request and Reply MFAs. The four FIFOs are:

- Request Free List
- Request Post List
- Reply Free List
- Reply Post List

Each element within the FIFOs contains the 32-bit MFAs. The Free List FIFO contains MFAs to memory locations which are “free” to be used for new messages. The LSI53C1510 first enters these MFAs into the Request Free List FIFO at initialization. The Host initializes the Reply Free List by writing the MFAs for the Reply messages into the Reply Register. The act of writing to this register pushes the MFA into the FIFO. The Post List FIFOs contain pointers to memory locations which contain new messages. The presence of a MFA in the Post FIFO indicates to the host or to the LSI53C1510 that a message is pending. The depth of the FIFOs determines the number of outstanding Request Messages which may be pending. The total number of outstanding or open I/Os is limited by the number of Request Messages. Therefore, the maximum number of open I/Os is determined by the size or depth of the FIFOs. The depth of the FIFOs in the LSI53C1510 is software configurable, from 256 to 4096, in powers of two. The storage elements for the FIFO are in the local DRAM external to the chip. Therefore, the size of the FIFOs will have an impact on the total amount of DRAM required. See Section 2.4.1, “DRAM Memory,” later in the chapter for more information regarding local DRAM requirements.

2.2.3 Request Message

The LSI53C1510 maintains a list of pointers to memory structures. The pool of pointers (MFAs) are stored in the LSI53C1510 Free FIFO. The top FIFO entry is provided to the host driver by reading the LSI53C1510 Request Register. In the default operation, the LSI53C1510 provides MFAs to the LSI53C1510 local memory, mapped as shared memory. The

process of the host writing to shared memory local to the LSI53C1510 is analogous to “pushing” messages down the PCI hierarchy to the LSI53C1510. This process may be referred to as the Push model.

Alternatively, the LSI53C1510 may be configured to provide MFAs to memory located on the host. Once configured as such, the LSI53C1510 will “pull” the messages to memory local to the LSI53C1510 using PCI bus master cycles. This process may be referred to as the Pull model. The LSI Logic I_2O RAID software uses the Push model.

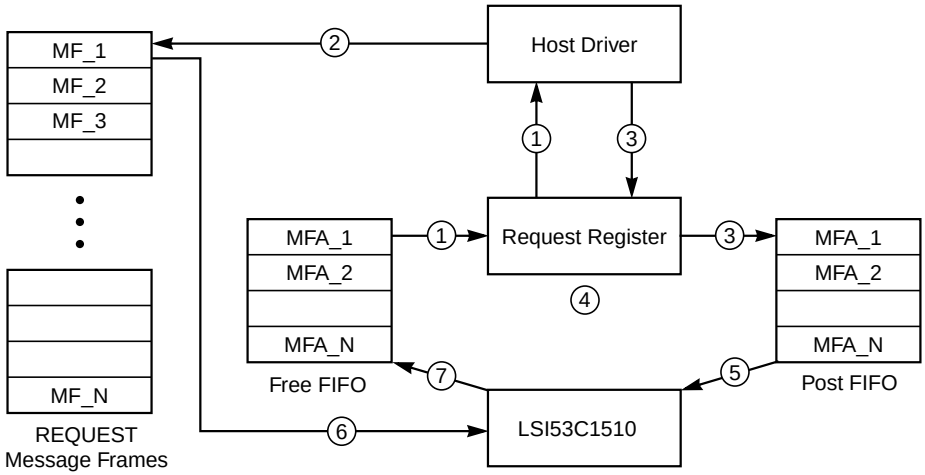
2.2.3.1 To Send a Request Message

Figure 2.4 illustrates the LSI53C1510 Request Message Transport.

1. The host driver reads the LSI53C1510 Request Register to retrieve a pointer to the next available message structure. If the Message structure resides in PCI shared memory local to the LSI53C1510 (the default), the host reads the offset of the Message structure with shared memory. Device drivers may be written to request several pointers through a series of fast back-to-back PCI slave read cycles. If there are no available message structures, Request Register reads return the value of FFFF–0xFFFF.
2. The host driver then builds the Request Message(s) and writes the contents to the available message structure(s).
3. When the Request Message is built, the host driver writes the MFA(s) back to the LSI53C1510 Request Register. This action creates a queued entry in the LSI53C1510 Post FIFO. Host drivers may post several MFAs during fast back-to-back PCI write cycles.
4. The LSI53C1510 Protocol Engine is interrupted on the first post creating a “Request Post FIFO Not Empty” condition.
5. The LSI53C1510 removes all of the MFAs from the Post FIFO.
6. If the LSI53C1510 is operating under the Pull model, then the LSI53C1510 arbitrates for the PCI bus with the intent to copy the Request Message(s) in host memory using burst read cycles to memory local to the LSI53C1510. The LSI53C1510 will immediately start operating on request message(s) already written to local PCI shared memory, if it is operating in the Push model.

7. Finally, the LSI53C1510 frees the memory associated with the message request by placing the MFA back in the Request Free FIFO. If the operation requested by the Request Message requires a Reply Message from the LSI53C1510 to the host, then a similar message transfer process is initiated (see Section 2.2.4, “Reply Message”). The host driver may choose to poll the Reply Messages or have the LSI53C1510 interrupt on exception conditions.

Figure 2.4 LSI53C1510 Request Message Transport



2.2.4 Reply Message

The Reply Queue provided by the LSI53C1510 is managed similarly, except the LSI53C1510 generates the Reply Messages. The host has the responsibility to allocate the Reply Message Pool, and post the MFA of each message frame to the Reply Register.

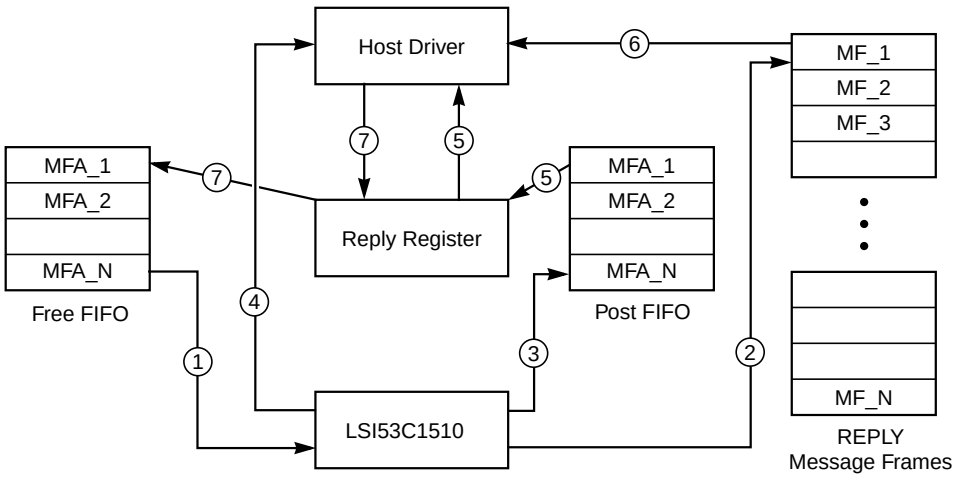
2.2.4.1 To Send a Reply Message

Figure 2.5 illustrates the LSI53C1510 Reply Message Transport.

1. The LSI53C1510 retrieves a MFA to the next free message frame from the Reply Message Free FIFO.
2. The LSI53C1510 then writes the message to the Reply Message frame queue.

3. When the Reply Message is written into the queue, the LSI53C1510 writes the pointer into the LSI53C1510 Post FIFO.
4. The LSI53C1510 Protocol Engine causes an interrupt to the host when the Reply Message is posted.
5. The host driver reads the Reply Register to retrieve the Reply Message pointer from the Post FIFO. If there are no posted messages when the host reads the Reply Register, the host receives the value FFFF–0xFFFF.
6. The host driver then retrieves the Reply Message.
7. Finally, the host driver writes the MFA (now a free message frame) to the Reply Register.

Figure 2.5 LSI53C1510 Reply Message Transport



2.2.4.2 The “Push” Model

The “Push” model for the data transfer defines the host’s “push” of request messages down to the PCI shared memory local to the LSI53C1510. The location to which the host writes is provided by the Request Free List.

2.3 LSI53C1510 Protocol Engine

The LSI53C1510 provides a Protocol Engine to manage the execution of various I_2O protocols. The Protocol Engine offloads the host processor from management of the I_2O protocol by providing a higher level of abstraction for the SCSI protocols. This abstraction allows multiple SCSI protocols to operate simultaneously, with no coordination required between the host-based drivers.

Each of the abstracted classes of service has well defined Request and Reply Message protocols. The SYMplicity I_2O RAID software supports the Random Block Storage Class. This class provides a high level abstraction for random access block-oriented storage devices.

2.3.1 Random Block Storage Class

The Random Block Storage Class provides a high level abstraction for random access block-oriented storage media. The class definition abstracts normal I/O operation using a message that consists of the starting logical block address, the number of bytes, the data buffer, the operation code, and the device handle on which to operate. The LSI53C1510 optimizes the request processing by attempting to sort and concatenate different requests, thereby reducing seek and latency time on the drives, and overall command overhead per request. Each request is managed as a single exchange and appropriate error recovery and reporting is provided. Table 2.4 lists the base messages that comprise the Random Block Storage Class message protocol.

Table 2.4 Supported Random Block Storage Messages

Function	Description
BsaBlockRead	Read from device to memory
BsaBlockReassign	Reassign block addresses
BsaBlockWrite	Write to device from memory
BsaBlockWriteVerify	Write to device from memory then verify
BsaCacheFlush	Write dirty cache to media
BsaDeviceReset	Reset the device
BsaMediaFormat	Not defined at this time
BsaMediaVerify	Verify accessibility of data
BsaPowerMgt	Power Management
BsaStatusCheck	Check device status

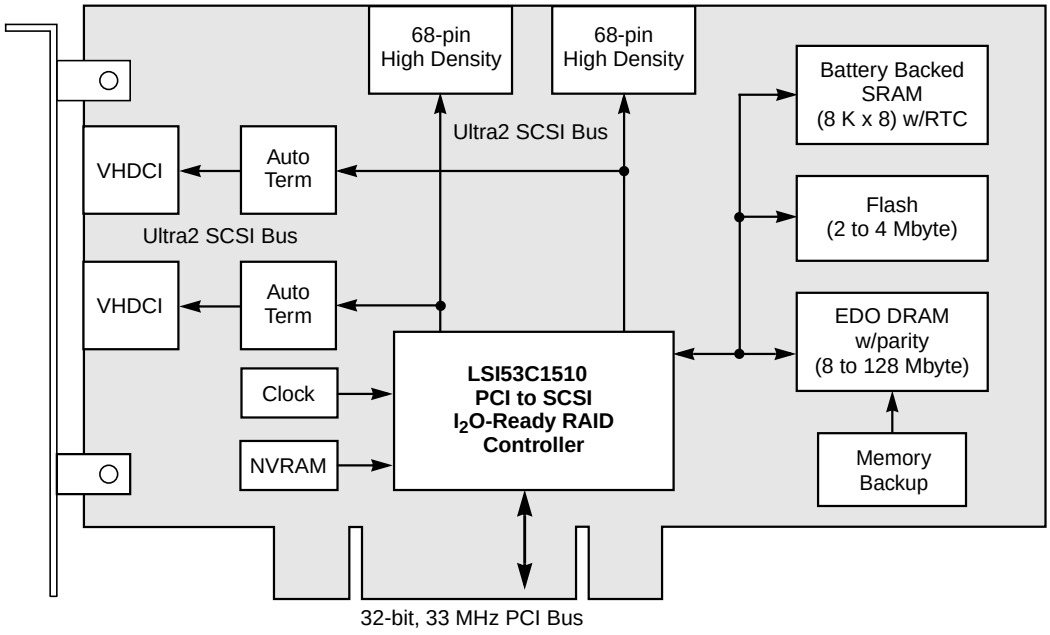
In addition to the base messages for each class, the class definitions also provide utility messages to allow for management and configuration of devices. A generic user interface scripting language is used to allow for building generic configuration and management applications.

2.4 Support Components

The memory controller block within the LSI53C1510 provides access to external local memory resources. External memory devices supported include Flash ROM, DRAM, and SRAM.

The sections below provide guidance in choosing the support components necessary for a fully functional implementation using the LSI53C1510. A LSI53C1510 typical implementation diagram is shown below in Figure 2.6 for reference.

Figure 2.6 Typical Implementations



2.4.1 DRAM Memory

The DRAM memory stores a run time image of the LSI53C1510 software. This memory also provides a data cache for RAID operations.

The LSI53C1510 uses a 32-bit demultiplexed memory bus to access the DRAM. This memory bus has the capability to address up to 128 Mbytes of EDO DRAM. The memory controller managing this bus has the flexibility to support variable DRAM access speeds. The speed of the DRAMs will have a dramatic impact on the performance of the LSI53C1510 and 50 ns EDO DRAM is required. The LSI53C1510 memory controller also supports optional byte-wide parity error detection.

2.4.2 Flash ROM

The memory controller in the LSI53C1510 manages an optional Flash ROM. If present, the Flash ROM is used to store the software for the LSI53C1510 Protocol Engine and INT 0x13 boot software.

If the Flash ROM is not used, then the host platform is responsible for downloading the Protocol Engine software to the LSI53C1510 through the PCI interface. The LSI53C1510 supports a diagnostic interface that is enabled through a sequence of commands issued to the WRSEQ register in the host interface register set. Software may be directly written to the LSI53C1510 internal memory and external DRAM through the diagnostic interface. Details of this implementation are not currently defined; therefore, LSI Logic recommends using Flash ROM for software storage.

The Flash ROM is accessed using the lower 8 bits of the DRAM Memory Interface.

2.4.3 Serial EEPROM

The serial EEPROM is primarily used during nonintelligent mode operations. It can be programmed using the host interface of the LSI53C1510.

Chapter 3
Software Description

This chapter describes the software features, firmware features, and memory requirements for the LSI53C1510 in the following sections:

3.1 PCI RAID Software Solutions

The LSI53C1510 is the first in high-integration RAID processor. LSI Logic offers a full PCI RAID software solution consisting of the LSI Logic RAID DDM, SYMplicity Storage Manager utility, and Wind River Systems’ IxWorks RTOS. These applications run in the LSI53C1510 intelligent mode.

3.1.1 PCI RAID

Operating in intelligent mode, the LSI53C1510 can use the LSI Logic PCI RAID software package.

Leveraging third generation software from the LSI Logic established and successful bridge controllers and subsystems, the LSI Logic RAID software for the LSI53C1510 provides an extremely stable, feature rich, high availability platform.

3.1.2 SYMplicity Storage Manager

SYMplicity Storage Manager provides host-based, transparent management of disk array controllers and the following features.

- Common Features
  - Obtaining a RAID Module Profile
  - Naming a RAID Module (user-defined)
  - Locating a RAID Module
- Configuration
  - LUN creation, deletion using GUI or command line
  - Easy default configurations or detailed parameter options available
  - Manages multiple RAID modules
  - Hot Spare Creation/Deletion
  - Dynamic Reconfiguration features
- Status
  - Event logging in system log or Storage Manager (specific log)
  - Scriptable error notification_SNMP, email, etc.
  - LUN Reconstruction progress and in-progress tuning
  - Performance Monitor
    - ◊ GUI displays key statistics for a card and its logical units
    - ◊ Command line interface captures full set of detailed data
- Recovery
  - Health Check for immediate report of component failures
  - Lead-through Recovery Steps from Single or Multiple Failures
- Maintenance/Tuning
  - Cache Management
  - Parity Check and Repair
  - Set LUN Reconstruction Rates

3.1.3 Wind River Systems' IxWorks RTOS

Wind River Systems has ported IxWorks to the LSI53C1510. This version of IxWorks has been tuned for optimal performance.

3.2 Management Software Features

Management software has the following features:

- Supported by SYMplicity Storage Manager
- Client/Server Model (Windows NT/Win95 Client with Windows NT, Netware, or UNIXWare Server)
- Compatible with Microsoft Cluster Server (Wolfpack)
- Online maintenance and event notification
- BBU Support with Utility level software
- Remote Diagnostic Capability
- Configurable Drive Rebuild rate
- Recovery Guru

3.3 RAID Firmware Features

RAID firmware has the following features:

- RAID Levels 0, 1, 3, 5, and 10
- Caching
  - Caching (Read-ahead, write through, or write back)
  - Cache memory options of 8 Mbyte to 128 Mbyte
- Runs in optimal and degraded mode
- Hardware Assisted Parity Calculation
- Variable Stripe Size
- Tagged Command Queuing
- Global hot spare drives
- Drive hot swap with automatic, transparent reconstruction

- Online Dynamic Capacity Expansion
- Online RAID Level Migration/Reconfiguration
- Battery Backup Support and Cache Recovery
- Supports SCSI Accessed Fault-Tolerant Enclosure (SAF-TE)

3.3.1 RAID Levels 0, 1, 3, 5, and 10

This section describes RAID and the different RAID levels.

3.3.1.1 RAID (Redundant Array of Independent Disks)

A disk array in which part of the storage capacity is used to store redundant information about user data stored on the remainder of the storage capacity. The redundant information enables regeneration of user data if one of the disk drives in the drive group fails.

3.3.1.2 RAID Level

Indicates the way the controller reads and writes data and array parity on the drives. The LSI53C1510 controller can create RAID Level 0, 1, 3, and 5 logical units. These levels DO NOT indicate any certain hierarchy or preference.

3.3.1.3 RAID Level 0

RAID Level 0 is a nonredundant RAID Level where data, without parity, is striped across a drive group/LUN. All drives are available for storing user data. Any single drive failure causes data loss and a logical unit status of Dead.

3.3.1.4 RAID Level 1

RAID Level 1 or disk mirroring, protects data against disk failure by replicating all data stored on the virtual disk at least once. For some I/O intensive applications, a RAID Level 1 can improve performance significantly over a single disk. As implemented by LSI Logic, RAID 1 combines both striping and mirroring. The striping and mirroring combination is also referred to as RAID 0+1 or RAID 10.

3.3.1.5 RAID Level 3

RAID Level 3 adds parity to a striped array, permitting user data to be regenerated in the event of a failure. RAID Level 3 arrays use normal disk mechanisms for failure detection and the parity for data regeneration in the event of a failure. RAID Level 3 relies on close coordination of member disk activities.

3.3.1.6 RAID Level 5

RAID Level 5 is another independent access RAID Level. It is functionally equivalent to RAID Level 4, using a single parity strip to protect data stored on several data strips in the same stripe. It differs from RAID Level 4 in that its parity strips are distributed across multiple array members rather than being concentrated on a dedicated parity disk. This provides some relief from the write bottleneck that characterizes RAID Level 4, and is the reason that RAID 5 is most often implemented in independent access RAID array products rather than RAID Level 4.

3.3.2 Caching

Cache memory is an area on the controller used for intermediate storage of read and write data. By using cache, you can increase system performance because the data for a read or write operation from the host may already be in the cache from a previous operation (thus the need to access the drive itself is eliminated), or the write operation is considered complete once it is written to the cache. The following caching options are supported.

- Caching (Read-ahead, write through, or write back)
- Cache memory options of 8 Mbyte to 128 Mbyte

3.3.3 Runs in Optimal and Degraded Mode

The software permits your RAID system to produce optimal performance. If a failure occurs, the system can run in a degraded mode until replacement of the failed unit occurs.

3.3.4 Hardware Assisted Parity Calculation

RAID firmware uses the Hardware PAE in the LSI53C1510 to offload parity generation and checking from the host. The PAE calculates the parity for write operations much faster than what can be done in software/firmware. It also allows multiple parity operations to be queued for maximum efficiency.

3.3.5 Tagged Command Queuing

Tagged command queuing provides the capability for the host to issue multiple commands to a logical unit. This capability is essential for an array logical unit that is made up of multiple devices. Without tagged queuing, the controller can only execute one operation on the logical unit at a time, even though there are multiple drives available for overlapped operations. The maximum number of commands which can be queued in the controller (the sum of all logical units) is 256. This is the number of available structures the controller has for operations received from the host. If the host attempts to issue more commands to the controller than it has structures available for, a Queue Full status will be returned.

The controller maintains a queue for each logical unit and a queue for each drive in the logical unit. How a command moves from queue to queue is dependent on the type of queue tag received with the command.

3.3.6 Global Hot Spare Drives

This drive contains no valid data but if a failure occurs, the controller can automatically reconstruct and use the global hot spare drive to replace a failed drive. Hot spare drive allows full performance and data redundancy to be restored without user intervention. The user simply replaces the failed drive at a later time. This is an important feature because it can significantly reduce mean time to data loss. A global hot spare drive can replace a failed drive of the same or smaller capacity anywhere on the disk array.

3.3.7 Hot Swap Drive with Automatic, Transparent Reconstruction

This disk drive replaces a failed drive. Hot Swap technology makes it possible to remove and replace an array component while power is applied and data activity to and from the system continues. The controller automatically reconstructs data on the new drive, or initiates copying back the data from the global hot spare drive that is standing in for the failed drive. This data reconstruction is transparent to the user and allows full performance and data redundancy to be restored.

3.3.8 Variable Stripe Size

The Dynamic Segment Sizing (DSS) feature provides the ability to change the segment size for a LUN. Changing the segment size causes the LUN to be reconfigured such that the data is mapped according to the new segment size. This feature is provided while allowing full user data availability and accessibility. The RAID firmware allows variable stripe size. A striped array is also known as a RAID Level 0 array.

3.3.9 Online Dynamic Capacity Expansion

The Dynamic Capacity Expansion feature provides the ability to add drives to a drive group. Adding drives to a drive group causes the LUNs on that drive group to be reconfigured such that the data is spread onto the additional drives. After reconfiguration, the additional capacity may be used to create additional LUNs on the drive group. This feature is provided while allowing full user data availability and accessibility.

3.3.10 Online RAID Level Migration/Reconfiguration

The Dynamic RAID Migration (DRM) feature provides the ability to change the RAID Level for a drive group. Changing the RAID Level causes the LUNs in the drive group to be reconfigured such that the data is mapped according to the definition of the new RAID Level. This feature is provided while allowing full user data availability and accessibility. Valid RAID Level Migrations are: 0>1, 0>3, 0>5, 1>0, 1>3, 1>5, 3>0, 3>1, 3>5, 5>0, 5>1, and 5>3.

3.3.11 Battery Backup Support and Cache Recovery

The Battery Backup feature allows data in cache memory to be saved and then recovered following a power failure.

3.3.12 Supports SAF-TE

SAF-TE support has been added to the destination (drive) side of the controller. This allows attachment of drive enclosures that support SAF-TE.

3.4 SDMS Software

Operating in nonintelligent mode, the LSI53C1510 can use the SDMS software package.

SDMS software is a complete software package that solves the increasingly complex problem of managing system I/O. It seamlessly addresses hardware and software interfaces by supporting the LSI Logic family of SCSI processors and controllers, and a wide range of SCSI peripheral devices, while offering interoperability across application programs, operating systems, and host platforms. SDMS software consists of a resident SCSI BIOS that manages all SCSI controller or processor specific functions, and a series of SCSI device drivers that provide operating system and peripheral specific support.

SDMS software provides a standard method to interface SCSI I/O subsystems with devices, operating systems, and application software. It also enhances system capabilities already provided by SCSI controllers and processors by facilitating multithreaded I/O support, system wide SCSI device access, and the creation of new applications.

3.5 Memory Requirements

To run the LSI53C1510 in intelligent mode, with the PCI RAID software solutions (LSI Logic RAID DDM, SYMplicity Storage Manager utility, and Wind River Systems' IxWorks RTOS), your memory should meet the following requirements.

- EDO DRAM (with parity) - 8 Mbytes to 128 Mbytes
- Flash ROM - minimum of 2 Mbytes
- NVRAM (with real time clock) - 8 Kbytes
  (equivalent to SGS-Thomson MK48T18)

To run the LSI53C1510 in nonintelligent mode, with LSI Logic the SDMS software package, your memory should meet the following requirements.

- Two Serial EEPROM - 2 Kbytes
- Flash ROM - 128 Kbytes

Chapter 4
Signal Descriptions

This chapter presents the LSI53C1510 pin configuration and signal definitions using tables and illustrations. Figure 4.1 is the functional signal grouping. The signal descriptions are organized into functional groups:

- Section 4.1, “Signal Groupings,” page 4-2
- Section 4.2, “PCI Interface Signals,” page 4-4
- Section 4.3, “SCSI Interface Signals,” page 4-10
- Section 4.4, “Memory Interface Signals,” page 4-15
- Section 4.5, “Miscellaneous Interface Signals,” page 4-18

A slash (/) at the end of a signal name indicates that the active state occurs when the signal is at a LOW voltage. When the slash is absent, the signal is active at a HIGH voltage.

All signals/pins described in this chapter are identified by a pin type described in Table 4.1.

Table 4.1 Pin Type Description

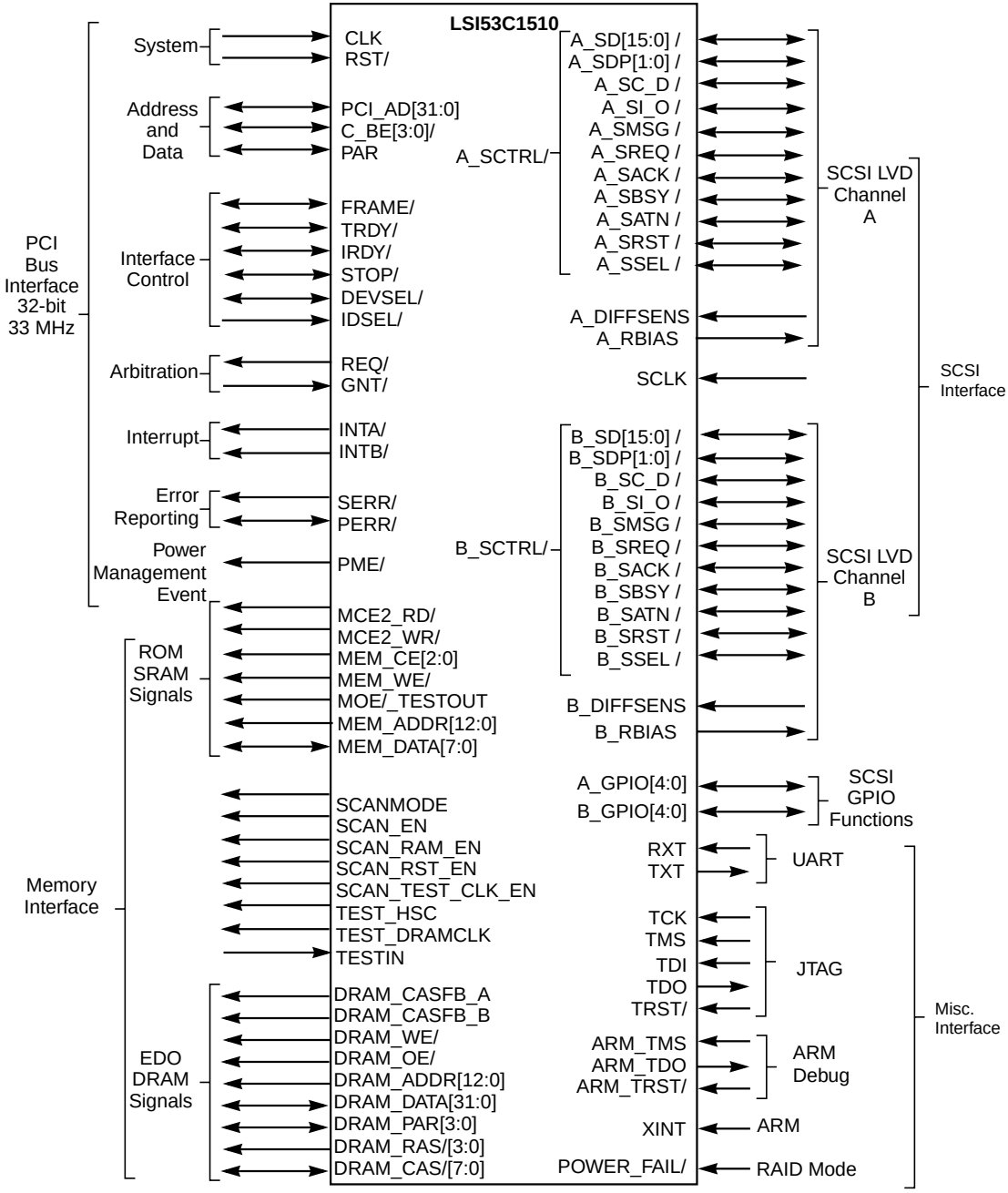
Type	Description
I	Input, a standard input only signal
O	Totem Pole Output, a standard output driver
I/O	Input and Output (bidirectional)
T/S	3-state, a bidirectional, 3-state input/output signal
S/T/S	Sustained 3-state, an active LOW 3-state signal owned and driven by one and only one agent at a time

4.1 Signal Groupings

The LSI53C1510 signals fall into the following groups. These groups are illustrated in Figure 4.1.

- PCI Interface Signals
  - System Signals
  - Address and Data Signals
  - Interface Control Signals
  - Arbitration Signals
  - Interrupt Signals
  - Error Reporting Signals
  - Power Management Event Signals
- SCSI Interface Signals
  - A-Channel
  - B-Channel
- Memory Interface Signals
  - ROM/SRAM Signals
  - EDO DRAM Signals
- Miscellaneous Interface Signals
  - SCSI GPIO Function Signals
  - UART Signals
  - JTAG Signals
  - ARM Debug Signals
  - ARM
  - RAID Mode
- Power and Ground Signals

Figure 4.1 LSI53C1510 Functional Signal Groupings



4.2 PCI Interface Signals

The PCI Bus Interface Signals section contains tables describing the signals for the following signal groups: System Signals, Address and Data Signals, Interface Control Signals, Arbitration Signals, Interrupt Signals, the ARM Signal, Error Recording Signals, the Power Management Signal, and GPIO Interface Signals.

4.2.1 System Signals

Table 4.2 describes the System signals.

Table 4.2 System Signals

Name	Bump	Type	Strength	Description
CLK	F25	I	N/A	**Clock** provides timing for all transactions on the PCI bus and is an input to every PCI device. All other PCI signals are sampled on the rising edge of CLK, and other timing parameters are defined with respect to this edge. Clock can optionally serve as the SCSI core clock, but this may effect fast SCSI transfer rates.
RST/	N24	I	N/A	**Reset** forces the PCI sequencer of each device to a known state. All T/S and S/T/S signals are forced to a high impedance state, and all internal logic is reset. The RST/ input is synchronized internally to the rising edge of CLK. The CLK input must be active while RST/ is active to properly reset the device.

4.2.2 Address and Data Signals

Table 4.3 describes the Address and Data signals.

Table 4.3 Address and Data Signals

Name	Bump	Type	Strength	Description
PCI_AD[31:0]	M25, M24, M26, L25, L24, L26, K23, K25, J25, H25, J24, H26, H23, G25, G26, H24, C25, D24, A25, C23, B24, A24, D22, B23, B22, A22, D20, B21, A21, C21, B20, A20	T/S	16 mA PCI	Physical dword **PCI Address and Data** are multiplexed on the same PCI pins. During the first clock of a transaction, AD[31:0] contain a physical byte address. During subsequent clocks, AD[31:0] contain data. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. AD[7:0] define the least significant byte, and AD[31:24] define the most significant byte.
C_BE[3:0]/	K26, G23, E24, A23	T/S	16 mA PCI	**Bus Command and Byte Enables** are multiplexed on the same PCI pins. During the address phase of a transaction, C_BE[3:0]/ define the bus command. During the data phase, C_BE[3:0]/ are used as byte enables. The byte enables determine which byte lanes carry meaningful data. C_BE[0]/ applies to byte 0, and C_BE[3]/ to byte 3.
PAR	C26	T/S	16 mA PCI	**Parity** is even parity across the AD[31:0] and C_BE[3:0]/ lines. During the address phase, both the address and command bits are covered. During data phase, both data and byte enables are covered.

4.2.3 Interface Control Signals

Table 4.4 describes the Interface Control signals.

Table 4.4 Interface Control Signals

Name	Bump	Type	Strength	Description
FRAME/	G24	S/T/S	16 mA PCI	**Cycle Frame** is driven by the current master to indicate the beginning and duration of an access. FRAME/ is asserted to indicate that a bus transaction is beginning. While FRAME/ is deasserted, either the transaction is in the final data phase or the bus is idle.
IRDY/	E26	S/T/S	16 mA PCI	**Initiator Ready** indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY/ is used with TRDY/. A data phase is completed on any clock when both IRDY/ and TRDY/ are sampled asserted. During a write, IRDY/ indicates that valid data is present on AD[31:0]. During a read, it indicates that the master is prepared to accept data. Wait cycles can be inserted until both IRDY/ and TRDY/ are asserted together**.**
TRDY/	E25	S/T/S	16 mA PCI	**Target Ready** indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY/ is used with IRDY/. A data phase is completed on any clock when both TRDY/ and IRDY/ are sampled asserted. During a read, TRDY/ indicates that valid data is present on AD[31:0]. During a write, it indicates that the target is prepared to accept data. Wait cycles can be inserted until both IRDY/ and TRDY/ are asserted together.
STOP/	D26	S/T/S	16 mA PCI	**Stop** indicates that the selected target is requesting the master to stop the current transaction.
DEVSEL/	F24	S/T/S	16 mA PCI	**Device Select** indicates that the driving device has decoded its address as the target of the current access. As an input, it indicates to a master whether any device on the bus has been selected.
IDSEL	K24	I	N/A	**Initialization Device Select** is used as a chip select in place of the upper 24 address lines during configuration read and write transactions.

4.2.4 Arbitration Signals

Table 4.5 describes the Arbitration signals.

Table 4.5 Arbitration Signals

Name	Bump	Type	Strength	Description
REQ/	N26	O	16 mA PCI	**Request** indicates to the arbiter that this agent desires use of the PCI bus. Both SCSI functions share the REQ/ signal.
GNT/	M23	I	N/A	**Grant** indicates to the agent that access to the PCI bus has been granted. Both SCSI functions share the GNT/ signal in nonintelligent mode. In intelligent mode, the GNT/ signal is shared by the Internal Module Bus (IMB) bus agents.

4.2.5 Interrupt Signals

Table 4.6 describes the Interrupt signals.

Table 4.6 Interrupt Signals

Name	Bump	Type	Strength	Description
INTA/	P24	O	16 mA PCI	**Interrupt Function A.** This signal, when asserted LOW, indicates an interrupting condition in SCSI Function A and that service is required from the host CPU. The output drive of this pin is open drain. If the SCSI Function B interrupt is rerouted at power-up using the INTA/ enable sense resistor (pull-down on MEM_ADDR9), this signal indicates that an interrupting condition has occurred in either the SCSI Function A or SCSI Function B.
INTB/	N23	O	16 mA PCI	**Interrupt Function B.** This signal, when asserted LOW, indicates an interrupting condition in SCSI Function B and that service is required from the host CPU. The output drive of this pin is open drain. This interrupt can be rerouted to INTA/ at power-up using the INTA/ enable sense resistor (pull-down on MEM_ADDR9). This causes the LSI53C1510 to program the SCSI Function B PCI register Interrupt Pin (3D) to 0x01. In intelligent mode, this signal is not used.

4.2.6 ARM Signal

Table 4.7 describes the ARM signal.

Table 4.7 ARM Signal

Name	Bump	Type	Strength	Description
XINT	N25	I	–	**External Interrupt.** This pin, when asserted, indicates that an interrupting condition is pending.

4.2.7 Error Recording Signals

Table 4.8 describes the Error Recording signals.

Table 4.8 Error Recording Signals

Name	Bump	Type	Strength	Description
PERR/	D25	S/T/S	16 mA PCI	**Parity Error.** This may be pulsed active by an agent that detects a data parity error. PERR/ can be used by any agent to signal data corruption. However, on detection of a PERR/ pulse, the central resource may generate a nonmaskable interrupt to the host CPU, which often implies the system is unable to continue operation once error processing is complete.
SERR/	E23	O	16 mA PCI	**System Error.** This output is used to report address and data parity errors.

4.2.8 Power Management Signal

Table 4.9 describes the Power Management signal.

Table 4.9 Power Management Signal

Name	Bump	Type	Strength	Description
PME/	TI	O	16 mA PCI	**Power Management Event.** This signal, when asserted LOW, indicates a power management event has occurred.

4.2.9 GPIO Interface Signals

Table 4.10 describes the GPIO Interface signals.

Table 4.10 GPIO Interface Signals

Name	Bump	Type	Strength	Description
A_GPIO [4:0]	W24, V26, V25, V24, U26	I/O	24 mA	**A General Purpose I/O.** Signals GPIO0–GPIO3 default to input mode on reset. Signal GPIO4 defaults to output mode on reset. These signals are controlled or observed by firmware and may be configured as inputs or outputs.
B_GPIO [4:0]	W2, V1, U3, U1, U2	I/O	24 mA	**B General Purpose I/O.** Signals GPIO0–GPIO3 default to input mode on reset. Signal GPIO4 defaults to output mode on reset. These signals are controlled or observed by firmware and may be configured as inputs or outputs.

4.3 SCSI Interface Signals

The SCSI Bus Interface Signals section contains tables describing the signals for the following signal groups: the SCSI Clock Signal, SCSI A-Channel Interface Signals, and SCSI B-Channel Interface Signals.

4.3.1 SCSI Clock Signal

Table 4.11 describes the SCSI Clock signal.

Table 4.11 SCSI Clock Signal

Name	Bump	Type	Strength	Description
SCLK	AD13	I	N/A	**SCSI Clock** is used to derive all SCSI related timings. The speed of this clock is determined by the application's requirements. The clock supplied to SCLK must be at 40 MHz. This frequency is doubled to create the 80 MHz clock required by both SCSI functions. For Ultra2, this frequency is quadrupled to create 160 MHz.

4.3.2 SCSI A-Channel Interface Signals

Table 4.12 describes the SCSI A-Channel Interface signals.

Table 4.12 SCSI A-Channel Interface Signals[1]

Name	Bump	Type	Strength	Description
A_SD[15:0]–/	AA26, Y25, Y24, W26, AF14, AD15, AE16, AF16, AE23, AF24, AE24, AE26, AD25, AB23, AC26, AB25	I/O	48 mA SCSI	**SCSI Function A Data.** LVD Mode: A_SD[15:0]–/ signals are the negative half of the LVDlink 16-bit pair of SCSI data lines. SE Mode: The SE interface uses only the plus signals, therefore, these signals are not used.

Table 4.12 SCSI A-Channel Interface Signals[1] (Cont.)

Name	Bump	Type	Strength	Description
A_SD[15:0]+/	AA24, Y26, W25, W23, AE15, AF15, AD16, AC17, AC22, AD22, AD23, AC24, AD26, AC25, AB24, AB26	I/O	48 mA SCSI	**SCSI Function A Data.** LVD Mode: A_SD[15:0]+/ signals are the positive half of the LVDlink 16-bit pair of SCSI data lines. SE Mode: The SE interface uses only the plus signals as the 16-bit SCSI data and parity bus.
A_SDP[1:0]–/	Y23, AD21	I/O	48 mA SCSI	**SCSI Function A Data Parity.** LVD Mode: A_SDP[1:0]–/ are the negative half of the LVDlink pair for SCSI data parity lines. SE Mode: The SE interface uses only the plus signals, therefore, these signals are not used.
A_SDP[1:0]+/	AA25, AF23	I/O	48 mA SCSI	**SCSI Function A Data Parity.** LVD Mode: A_SDP[1:0]+/ are the positive half of the LVDlink pair for SCSI data parity lines. SE Mode: The SE interface uses only the plus signals as the 16-bit SCSI data and parity bus.
A_DIFFFSENS	AD14	I	N/A	**SCSI Function A Differential Sense.** This pin detects the presence of a SE device on a differential system. When external differential transceivers are used, and a zero is detected on this pin, all SCSI Function A chip outputs are 3-stated to avoid damage to the transceivers. Tie this pin HIGH during SE operation.
A_SC_D /	AE19, AF18	I/O	48 mA SCSI	**Control/Data.** The target asserts this signal with the MSG/ and C_D signals to determine the information transfer phase.
A_SI_O /	AF17, AE17	I/O	48 mA SCSI	**Input/Output.** The target asserts this signal with the MSG/ and C_D signals to determine the information transfer phase.
A_SMSG /	AE20, AC19	I/O	48 mA SCSI	**Message.** The target asserts this signal with the I_O and C_D signals to determine the information transfer phase.

Table 4.12 SCSI A-Channel Interface Signals[1] (Cont.)

Name	Bump	Type	Strength	Description
A_SREQ /	AE18, AE17	I/O	48 mA SCSI	**Request.** This signal is a data handshake line from a target device. The target asserts this signal when requesting a data transfer.
A_SACK /	AF21, AC20	I/O	48 mA SCSI	**Acknowledge.** This signal is a data handshake signal from initiator device. The initiator asserts this signal in response to the REQ/ signal to acknowledge a data transfer.
A_SBSY /	AD20, AE21	I/O	48 mA SCSI	**Busy.** This signal is asserted when the SCSI bus is busy. When a device wants to arbitrate to use the SCSI bus, BSY/ is driven active. Once the arbitration and selection phases are complete, the target drives this signal active.
A_SATN /	AE22, AF22	I/O	48 mA SCSI	**Attention.** The initiator asserts this signal when requesting a message out phase.
A_SRST /	AD19, AF20	I/O	48 mA SCSI	**Reset.** This signal performs a SCSI bus reset when asserted.
A_SSEL /	AF, AD18	I/O	48 mA SCSI	**Select.** This signal selects or reselects another SCSI device when asserted.

1. The SE interface uses only the – signals. LVD interface uses both the + and – signals.

4.3.3 SCSI B-Channel Interface Signals

Table 4.13 describes the SCSI B-Channel Interface signals.

Table 4.13 SCSI B-Channel Interface Signals[1]

Name	Bump	Type	Strength	Description
B_SD[15:0]–/	AE11, AD11, AF13, AD12, W1, Y2, W3, AA1, AE6, AD6, AF7, AE8, AC8, AF9, AD9, AE10	I/O	48 mA SCSI	**SCSI Function B Data.** LVD Mode: B_SD[15:0]–/ signals are the negative half of the LVDlink 16-bit pair of SCSI data lines. SE Mode: The SE interface uses only the plus signals, therefore, these signals are not used.
B_SD[15:0]+/	AC10, AF12, AE12, AE13, V3, W4, Y1, Y4, AC7, AF6, AE7, AD7, AF8, AD8, AE9, AF10	I/O	48 mA SCSI	**SCSI Function B Data.** LVD Mode: B_SD[15:0]+/ signals are the positive half of the LVDlink 16-bit pair of SCSI data lines. SE Mode: The SE interface uses only the plus signals as the 16-bit SCSI data and parity bus.
B_SDP[1:0]–/	AF11, AF5	I/O	48 mA SCSI	**SCSI Function B Data Parity.** LVD Mode: B_SDP[1:0]–/ are the negative half of the LVDlink pair for SCSI data parity lines. SE Mode: The SE interface uses only the plus signals, therefore, these signals are not used.
B_SDP[1:0]+/	AD10, AE5	I/O	48 mA SCSI	**SCSI Function B Data Parity.** LVD Mode: B_SDP[1:0]+/ are the positive half of the LVDlink pair for SCSI data parity lines. SE Mode: The SE interface uses only the plus signals as the 16-bit SCSI data and parity bus.
B_DIFFFSENS	AC12	I	N/A	**SCSI Function B Differential Sense.** This pin detects the presence of a SE device on a differential system. When external differential transceivers are used, and a zero is detected on this pin, all SCSI Function B chip outputs are 3-stated to avoid damage to the transceivers. Tie this pin HIGH during SE operation.

Table 4.13 SCSI B-Channel Interface Signals[1] (Cont.)

Name	Bump	Type	Strength	Description
B_SC_D /	AA3, AC1	I/O	48 mA SCSI	**Control/Data.** The target asserts this signal with the MSG/ and C_D signals to determine the information transfer phase.
B_SI_O /	AA2, Y3	I/O	48 mA SCSI	**Input/Output.** The target asserts this signal with the MSG/ and C_D signals to determine the information transfer phase.
B_SMSG /	AD1, AB3	I/O	48 mA SCSI	**Message.** The target asserts this signal with the I_O and C_D signals to determine the information transfer phase.
B_SREQ /	AB1, AB2	I/O	48 mA SCSI	**Request.** This signal is a data handshake line from a target device. The target asserts this signal when requesting a data transfer.
B_SACK /	AF2, AD4	I/O	48 mA SCSI	**Acknowledge.** This signal is a data handshake signal from initiator device. The initiator asserts this signal in response to the REQ/ signal to acknowledge a data transfer.
B_SBSY /	AE3, AF3	I/O	48 mA SCSI	**Busy.** This signal is asserted when the SCSI bus is busy. When a device wants to arbitrate to use the SCSI bus, BSY/ is driven active. Once the arbitration and selection phases are complete, the target drives this signal active.
B_SATN /	AC5, AE4	I/O	48 mA SCSI	**Attention.** The initiator asserts this signal when requesting a message out phase.
B_SRST /	AD2, AC3	I/O	48 mA SCSI	**Reset.** This signal performs a SCSI bus reset when asserted.
B_SSEL /	AC2, AB4	I/O	48 mA SCSI	**Select.** This signal selects or reselects another SCSI device when asserted.

1. The SE interface uses only the – signals. LVD interface uses both the + and – signals.

4.4 Memory Interface Signals

The Memory Interface Signals section contains tables describing the signals for the following groups: ROM/SRAM Interface Signals, SCAN Signals, and DRAM Interface Signals.

4.4.1 ROM/SRAM Interface Signals

Table 4.14 describes the ROM/SRAM Interface signals.

Table 4.14 ROM/SRAM Interface Signals

Name	Bump	Type	Strength	Description
MCE2_RD/	K4	O	8 mA	**Memory Signal for MEM_CE(2).**
MCE2_WR/	L2	O	8 mA	**Memory Signal for MEM_CE(2).**
MEM_CE/[2:0]	K3, K2, K1	O	8 mA	**Memory Chip Enable.** These pins are used as chip enable signals to external memory devices.
MEM_WE/	M1	O	8 mA	**Memory Write Enable**. This pin is used as a write enable signal to external memories selected by MEM_CE[2:0].
MOE/_TESTOUT	J3	O	8 mA	**Memory.** This pin is used as an output enable signal to external memories during read operations.
MEM_ADDR [12:0]	J2, J1, H3, H1, H2, G3, G1, G2, F3, F1, F2, G4, E1	O	24 mA	**Memory Address.** The memory address bus provides a total of 8 K addressing of general purpose memory addressing. The memory address bus is also used for power-on configuration with pull-up/pull-down resistors. The resistors determine the ROM size. Is concatenated with DRAM_ADDR for MEM_CE cycles. Mirrors DRAM_ADDR signals for DRAM cycles.
MEM_DATA [7:0]	N3, M4, P2, M3, N2, N1, M2, L3	I/O	8 mA	**Memory Data** lines**.**

4.4.2 SCAN Signals

Table 4.15 describes the SCAN signals.

Table 4.15 SCAN Signals

Name	Bump	Type	Strength	Description
SCANMODE	R1	I	N/A	**Scan Mode Enable.** Used for manufacturing test.
SCAN_EN	R3	I	N/A	**Scan Enable.** Used for manufacturing test.
SCAN_RAM_EN	P3	I	N/A	**Scan RAM Enable.** Used for manufacturing test.
SCAN_RST_EN	R2	I	N/A	**Scan Reset Enable.** Used for manufacturing test.
SCAN_TEST_CLK_EN	R4	I	N/A	**Scan Test Clock Enable.** Used for manufacturing test.
SCAN_TRI_EN	P1	I	N/A	**Scan 3-State Enable**. Used for manufacturing test.

4.4.3 DRAM Interface Signals

Table 4.16 describes the DRAM Interface signals.

Table 4.16 DRAM Interface Signals

Name	Bump	Type	Strength	Description
DRAM_CASFB_A	A5	I	N/A	**DRAM Column Address Strobe Feedback**.
DRAM_CASFB_B	C7	I	N/A	**DRAM Column Address Strobe Feedback**.
DRAM_WE/	B4	O	24 mA	**DRAM Write Enable**. Indicates the direction data is to be transferred to/from DRAM.
DRAM_OE/	A4	O	16 mA	**DRAM Output Enable**.
DRAM_ADDR [12:0]	E3, D1, D2, E4, C1, C2, D3, B1, C4, B3, C5, A3, D5	O	24 mA	**DRAM Memory Address** lines.
DRAM_DATA [31:0]	B19, D19, A18, C18, B17, A16, B16, C16, A14, C15, D15, D13, D12, B12, A12, C11, A19, C19, B18, A17, C17, D17, A15, B15, B14, B13, C14, C13, A13, C12, B11, ALL	I/O	8 mA	**DRAM Data** lines.
DRAM_PAR[3:0]	D10, A10, B10, C10	I/O	8 mA	**DRAM Data Parity**. These bits provide one parity bit for each byte of data.
DRAM_RAS[3:0]/	C6, B5, A9, B8	O	24 mA	**DRAM Row Address Strobe.** Indicates the presence of a valid row address.
DRAM_CAS[7:0]/	C9, D8, A7, D7, A8, B7, C8, B6	O	26 mA	**DRAM Column Address Strobe.** Indicates the presence of a valid column address.

4.5 Miscellaneous Interface Signals

The Miscellaneous Interface Signals section contains tables describing the signals for the following signal groups: UART Interface Signals, JTAG Interface Signals, ARM Debug Interface Signals, the RAID Interface Signal and Power and Ground Signals.

4.5.1 UART Interface Signals

Table 4.17 describes the UART Interface signals.

Table 4.17 UART Interface Signals

Name	Bump	Type	Strength	Description
RXT	P25	I	N/A	**Receive Data.**
TXT	R24	O	4 mA	**Transmit Data.**

4.5.2 JTAG Interface Signals

Table 4.18 describes the JTAG Interface signals.

Table 4.18 JTAG Interface Signals

Name	Bump	Type	Strength	Description
TCK	T25	I	N/A	**Test Clock.** This signal provides the clock for the JTAG test logic.
TMS	T24	I	4 mA	**Test Mode Select.** This signal is decoded to select the JTAG test operation.
TDI	R26	I	N/A	**Test Data Input.** This signal is the serial input signal for JTAG. It receives the JTAG test logic instructions.
TDO	P26	O	4 mA	**Test Data Output.** This signal is the serial output signal for test instructions and data from the JTAG test logic.
TRST/	R25	I	N/A	**Test Reset.** This signal resets the JTAG logic.
TESTIN	P4	I	N/A	**Test In.** For test purposes only. This signal, when driven HIGH, is used for manufacturing test. It should be pulled LOW or left unconnected for normal operation.

Table 4.18 JTAG Interface Signals (Cont.)

Name	Bump	Type	Strength	Description
TEST_HSC	AC14	I	N/A	**Test HSC.** For test purposes only.
TEST_DRAMCLK	E2	I	N/A	**Test DRAM Clock.** For test purposes only.

4.5.3 ARM Debug Interface Signals

Table 4.19 describes the ARM Debug Interface signals.

Table 4.19 ARM Debug Interface Signals

Name	Bump	Type	Strength	Description
ARM_TMS	U23	I	N/A	**ARM Test Mode Select.** This signal is decoded to select the test operation.
ARM_TDO	U24	O	N/A	**ARM Test Data Output.** This signal is the serial output for test instructions and data from the ARM test logic.
ARM_TRST/	T26	I	N/A	**ARM Test Reset.** This signal resets the ARM test logic.

4.5.4 RAID Interface Signal

Table 4.20 describes the signal for the RAID Interface signal.

Table 4.20 RAID Interface Signal

Name	Bump	Type	Strength	Description
POWER_FAIL/	T3	I	N/A	**Power Fail.**

4.5.5 Power and Ground Signals

Table 4.21 describes the signals for the Power and Ground signals.

Table 4.21 Power and Ground Signals

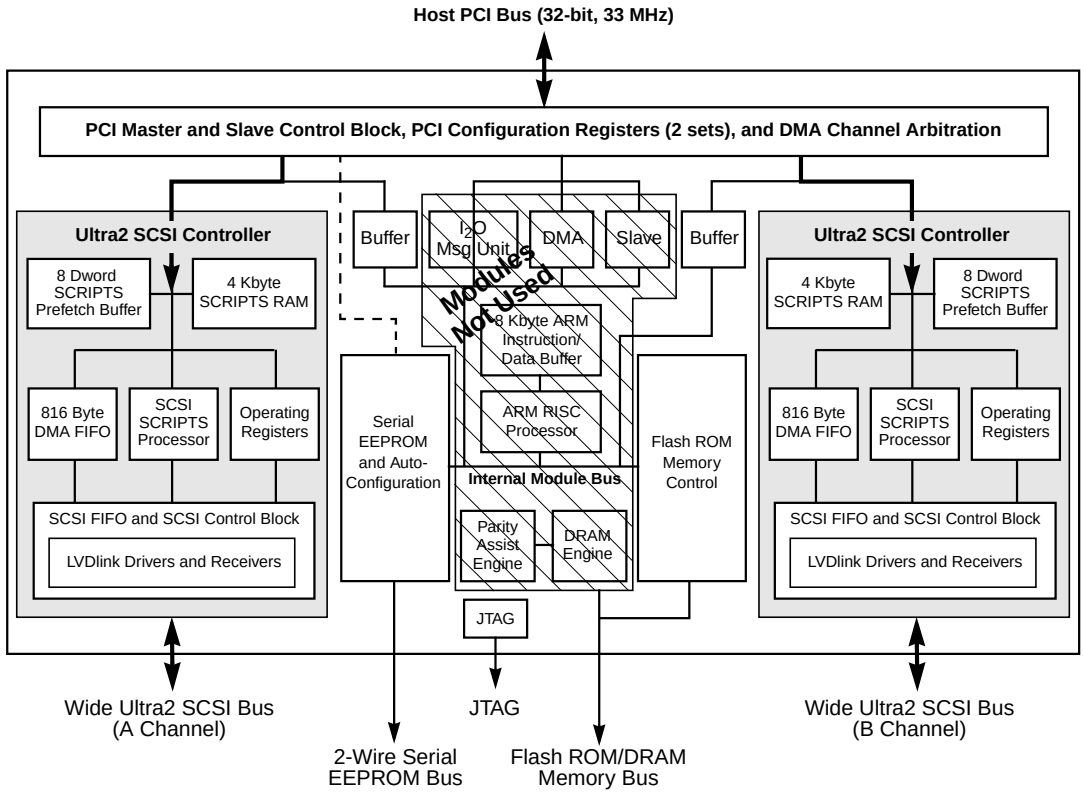
Name	Bump	Type	Strength	Description
V_{dd}	D6, D11, D16, D21, F4, F23, L4, L23, T4, T23, AA4, AA23, AC6, AC11, AC16, AC21	P	N/A	Power for PCI bus drivers/receivers, SCSI bus drivers/receivers, local memory interface drivers/receivers, and other I/O pins.
V_{dd}-A	AC15	P	N/A	Power for analog cells (clock quadrupler and DIFFSENS logic).
V_{dd}CORE [5:0]	V2, H4, A6, C20, J26, U25	P	N/A	Power for core logic.
V_{SS}	A1, A2, A26, B2, B25, B26, C3, C24, D4, D9, D14, D18, D23, J4, J23, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N4, N11, N12, N13, N14, N15, N16, P11, P12, P13, P14, P15, P16, P23, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, V4, V23, AC4, AC9, AC13, AC18, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26	G	N/A	Ground for PCI bus drivers/receivers, SCSI bus drivers/receivers, local memory interface drivers, and other I/O pins.
V_{SS}-A	AE14	G	N/A	Ground for analog cells (clock quadrupler and DIFFSENS logic).
V_{SS}CORE [5:0]	U4, L1, B9, C22, F26, R23	G	N/A	Ground for core logic.

Chapter 5
Registers
(Nonintelligent Mode)

This chapter contains the following sections:

After power-on, the LSI53C1510 is configured as either a nonintelligent or intelligent controller. This chapter describes the PCI and host interface registers that are visible to the host in nonintelligent mode. In nonintelligent mode the LSI53C1510 operates similar to the LSI53C896 product. Therefore, for detailed information, see the *LSI53C896 PCI to Dual Channel Ultra2 SCSI Multifunction Controller Technical Manual*. In nonintelligent mode, two Base Address regions (one for control and one for SCRIPTS RAM registers) are defined for each SCSI core. Figure 5.1 illustrates which modules are used in the nonintelligent mode.

Figure 5.1 LSI53C1510 Block Diagram in Nonintelligent Mode



This section contains descriptions of the LSI53C1510 PCI and host interface commands and registers. In the descriptions the term “set” is used to refer to bits that are programmed to a binary one. Similarly, the terms “clear” and “reset” are used to refer to bits that are programmed to a binary zero. **Do not set reserved bits.** Reserved bit functions may change at any time. Unless otherwise indicated, all bits in registers are active high, that is, the feature is enabled by setting the bit. The bottom row of every register diagram shows the default register values, which are enabled after the chip is powered on or reset.

5.1 PCI Functional Description (Nonintelligent Mode)

In nonintelligent mode, the LSI53C1510 implements two PCI to Wide Ultra2 SCSI controllers in a single package. This configuration presents only one load to the PCI bus and uses one REQ/ - GNT/ pair to arbitrate for PCI bus mastership. However, separate interrupt signals are generated for SCSI Function A and SCSI Function B.

5.1.1 PCI Addressing

There are three physical PCI defined address spaces:

- Configuration Space
- I/O Space
- Memory Space

5.1.1.1 Configuration Space

The host processor uses this configuration space to initialize the LSI53C1510. Two independent sets of PCI configuration space registers are defined, one set for each SCSI function. The PCI configuration space registers are accessible only by system BIOS during PCI configuration cycles. Each configuration space is a contiguous 256 x 8-bit set of addresses. Decoding C_BE/[3:0] determines if a PCI cycle is intended to access the configuration register space. The IDSEL bus signal is a “chip select” that allows access to the configuration register space only. A configuration read/write cycle without IDSEL is ignored. The eight lower order addresses AD[7:0] are used to select a specific 8-bit register. Since the LSI53C1510 is a PCI multifunction device, AD[10:8] decodes either SCSI Function A configuration register (AD[10:8] = 000 binary) or SCSI Function B configuration register (AD[10:8] = 001 binary).

At initialization time, each PCI device is assigned a base address for memory accesses and I/O accesses. This is accomplished using registers in the configuration space. On every nonconfiguration space access, the LSI53C1510 compares its assigned base addresses with the value on the Address/Data bus during the PCI address phase. If there is a match of the upper 24 bits, the access is for the LSI53C1510 and the low order eight bits to define the register to be accessed. A decode of C_BE/[3:0] determines which registers and what type of access is to be performed.

5.1.1.2 I/O Space

The PCI specification defines I/O space as a contiguous 32-bit I/O address that is shared by all system resources, including the LSI53C1510. Base Address Register Zero (I/O) register determines which 256 byte I/O area this device occupies.

5.1.1.3 Memory Space

The PCI specification defines memory space as a contiguous 32-bit memory address that is shared by all system resources, including the LSI53C1510. Base Address Register One (MEMORY) register determines which 1 Kbyte memory area this device occupies. Each SCSI function uses a 4 K SCRIPTS RAM memory space. Base Address Register Two (SCRIPTS RAM) register determines the 4 Kbyte memory area that the SCRIPTS RAM occupies.

5.1.2 PCI Bus Commands and Functions Supported

Bus commands indicate to the target the type of transaction the master is requesting. Bus commands are encoded on the C_BE/[3:0] lines during the address phase. PCI bus command encoding and types appear in Table 5.1. Reserved commands are shaded.

Table 5.1 PCI Bus Commands Encoding

C_BE[3:0]/	Command Type	Supported as Master	Supported as Slave
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	N/A	N/A
0101	Reserved	N/A	N/A
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	N/A	N/A
1001	Reserved	N/A	N/A
1010	Configuration Read	No	Yes
1011	Configuration Write	No	Yes
1100	Memory Read Multiple	Yes	Yes (defaults to 0110)
1101	DAC	Yes	Yes
1110	Memory Read Line	Yes	Yes (defaults to 0110)
1111	Memory Write and Invalidate	Yes	Yes (defaults to 0111)

5.1.2.1 Interrupt Acknowledge Command

The LSI53C1510 does not respond to this command as a slave and it never generates this command as a master.

5.1.2.2 Special Cycle Command

The LSI53C1510 does not respond to this command as a slave and it never generates this command as a master.

5.1.2.3 I/O Read Command

The LSI53C1510 uses the I/O Read command to read data from an agent mapped in I/O address space.

5.1.2.4 I/O Write Command

The LSI53C1510 uses the I/O Write command to write data to an agent mapped in I/O address space.

5.1.2.5 Reserved Command

The LSI53C1510 does not respond to this command as a slave and it never generates this command as a master.

5.1.2.6 Memory Read Command

The LSI53C1510 uses the Memory Read command to read data from an agent mapped in the Memory Address Space. The target is free to do an anticipatory read for this command only if it can guarantee that such a read has no side effects.

5.1.2.7 Memory Write Command

The LSI53C1510 uses the Memory Write command to write data to an agent mapped in the Memory Address Space. When the target returns “ready”, it assumes responsibility for the coherency (which includes ordering) of the subject data.

5.1.2.8 Configuration Read Command

The LSI53C1510 uses the Configuration Read command to read the configuration space of each agent. An agent is selected during a configuration access when its IDSEL signal is asserted and AD[1:0] are 00. During the address phase of a configuration cycle AD[7:2] addresses one of the 64 Dword registers (where byte enables address the bytes

within each Dword) in the configuration space of each device. AD[31:11] are logical don't cares to the selected agent. AD[10:8] indicate which device of a multifunction agent is being addressed.

5.1.2.9 Configuration Write Command

The LSI53C1510 uses the Configuration Write command to transfer data to the configuration space of each agent. An agent is selected when its IDSEL signal is asserted and AD[1:0] are 00. During the address phase of a configuration cycle, the AD[7:2] lines address the 64 Dword registers (where byte enables address the bytes within each Dword) in the configuration space of each device. AD[31:11] are logical don't cares to the selected agent. AD[10:8] indicate which device of a multifunction agent is addressed.

5.1.2.10 Memory Read Multiple Command

This command is identical to the Memory Read command except it indicates that the master may intend to fetch more than one cache line before disconnecting. The LSI53C1510 supports PCI Memory Read Multiple functionality and issues Memory Read Multiple commands on the PCI bus when the Memory Read Multiple Mode is enabled.

5.1.2.11 DAC Command

The LSI53C1510 performs DACs when 64-bit addressing is required. See PCI 2.1 Specification.

5.1.2.12 Memory Read Line Command

This command is identical to the Memory Read command, except that it additionally indicates that the master intends to fetch a complete cache line. This command is intended for use with bulk sequential data transfers where the memory system and the requesting master might gain some performance advantage by reading to a cache line boundary rather than a single memory cycle.

Read Multiple with Read Line Enabled – When both the Read Multiple and Read Line modes are enabled, a Memory Read Multiple command is issued, even though conditions for Memory Read Line are met.

If the Read Multiple mode is enabled and the Read Line mode is disabled, Memory Read Multiple commands are issued if the Memory Read Multiple conditions are met.

5.1.2.13 Memory Write and Invalidate Command

The Memory Write and Invalidate command is identical to the Memory Write command, except that it additionally guarantees a minimum transfer of one complete cache line; that is to say, the master intends to write all bytes within the addressed cache line in a single PCI transaction unless interrupted by the target. This command requires implementation of the PCI Cache Line Size register at address 0x0C in PCI configuration space.

Multiple Cache Line Transfers – The Memory Write and Invalidate command can write multiple cache lines of data in a single bus ownership. The chip issues a burst transfer as soon as it reaches a cache line boundary. The size of the transfer is not automatically the cache line size, but rather a multiple of the cache line size specified in PCI 2.1 Specification.

After each data transfer, the chip re-evaluates the burst size based on the amount of remaining data to transfer and again selects the highest possible multiple of the cache line size, and no larger than the burst size. The most likely scenario of this scheme is that the chip selects the burst size after alignment, and issues bursts of this size. The burst size is, in effect, throttled down toward the end of a long Memory Move or Block Move transfer until only the cache line size burst size is left. The chip finishes the transfer with this burst size.

Latency – In accordance with the PCI specification, the latency timer is ignored when issuing a Memory Write and Invalidate command such that when a latency time-out occurs, the LSI53C1510 continues to transfer up to a cache line boundary. At that point, the chip relinquishes the bus, and finishes the transfer at a later time using another bus ownership. If the chip is transferring multiple cache lines it continues to transfer until the next cache boundary is reached.

PCI Target Retry – During a Memory Write and Invalidate transfer, if the target device issues a retry (STOP with no TRDY, indicating that no data was transferred), the chip relinquishes the bus and immediately tries to

finish the transfer on another bus ownership. The chip issues the appropriate command on the next ownership, in accordance with the PCI specification.

PCI Target Disconnect – During a Memory Write and Invalidate transfer, if the target device issues a disconnect the LSI53C1510 relinquishes the bus and immediately tries to finish the transfer on another bus ownership. The chip issues the appropriate command on the next ownership, in accordance with the PCI specification.

5.1.3 Internal Arbiter

The PCI SCSI controller uses a single REQ/ - GNT/ signal pair to arbitrate for access to the PCI bus. An internal arbiter circuit allows the different bus mastering functions resident in the chip to arbitrate among themselves for the privilege of arbitrating for PCI bus access. There are two independent bus mastering functions inside the LSI53C1510, one for each of the SCSI functions.

The internal arbiter uses a round robin arbitration scheme to decide which internal bus mastering function may arbitrate for access to the PCI bus. This ensures that no function is starved for access to the PCI bus.

5.1.4 PCI Cache Mode

The LSI53C1510 supports the PCI specification for an 8-bit Cache Line Size register located in the PCI configuration space. The Cache Line Size register provides the ability to sense and react to nonaligned addresses corresponding to cache line boundaries. In conjunction with the Cache Line Size register, the PCI commands Memory Read Line, Memory Read Multiple, Memory Write and Invalidate are each software enabled or disabled to allow the user full flexibility in using these commands.

5.1.4.1 Memory to Memory Moves

Memory to Memory Moves also support PCI cache commands, as described above, with one limitation. Memory Write and Invalidate on Memory to Memory Move writes are only supported if the source and destination address are quad word aligned. If the source and destination are not quad word aligned (i.e. Source address[2:0] == Destination Address[2:0]), no write aligning will be performed nor will Memory Write and Invalidates be issued. The LSI53C1510 is little endian only.

5.2 PCI Configuration Registers (Nonintelligent Mode)

The PCI Configuration Registers, as shown in Table 5.2, are accessed by performing a configuration read/write to the device with its IDSEL pin asserted and the appropriate value in AD[10:8] during the address phase of the transaction. SCSI Function A is identified by a binary value of 000b, and SCSI Function B by a value of 001b. Each SCSI function contains the same register set with identical default values, except the Interrupt Pin register.

All PCI compliant devices, such as the LSI53C1510, must support the Vendor ID, Device ID, Command, and Status registers. Support of other PCI compliant registers is optional. In the LSI53C1510, registers that are not supported are not writable and return all zeros when read. Only those registers and bits that are currently supported by the LSI53C1510 are described in this chapter. Reserved bits should not be accessed. Reserved registers and bits are shaded.

Table 5.2 PCI Configuration Register Map

31	24	23	16	15	8	7	0	Address	Page
Device ID				Vendor ID				0x00	5-11
Status				Command				0x04	5-11
Class Code						Revision ID (Rev ID)		0x08	5-15
BIST	Header Type			Latency Timer		Cache Line Size		0x0C	5-15
Base Address Register Zero (I/O)								0x10	5-17
Base Address Register One (MEMORY)								0x14	5-18
Base Address Register Two (SCRIPTS RAM)								0x18	5-18
Reserved								0x1C	5-18
Reserved								0x20	5-18
Reserved								0x24	5-18
Reserved								0x28	5-18
Subsystem ID				Subsystem Vendor ID				0x2C	5-19
Expansion ROM Base Address								0x30	5-20
Reserved						Capabilities Pointer		0x34	5-21
Reserved								0x38	5-21
Max_Lat	Min_Gnt			Interrupt Pin		Interrupt Line		0x3C	5-22
Power Management Capabilities				Next Item Pointer		Capability ID		0x40	5-23
Data	Bridge Support Extensions			Power Management Control/Status				0x44	5-25

Registers: 0x00–0x01

Vendor ID

Read Only

15															0
VID															
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

VID **Vendor ID** **[15:0]**

This 16-bit register identifies the manufacturer of the device. The Vendor ID is 0x1000.

Registers: 0x02–0x03

Device ID

Read Only

15															0
DID															
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

DID **Device ID** **[15:0]**

This 16-bit register identifies the particular device. The Device ID in nonintelligent mode is 0x000A.

Registers: 0x04–0x05

Command

Read/Write

15						9	8	7	6	5	4	3	2	1	0
R							SE	R	EPER	R	WIE	R	EBM	EMS	EIS
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SCSI Command register provides coarse control over a device's ability to generate and respond to PCI cycles. When a zero is written to this register, the LSI53C1510 is logically disconnected from the PCI bus for all accesses except configuration accesses.

R **Reserved** **[15:9]**

SE	**SERR/ Enable** This bit enables the SERR/ driver. SERR/ is disabled when this bit is clear. The default value of this bit is zero. This bit and bit 6 must be set to report address parity errors.	**8**
R	**Reserved**	**7**
EPER	**Enable Parity Error Response** This bit allows the LSI53C1510 to detect parity errors on the PCI bus and report these errors to the system. Only data parity checking is enabled and disabled with this bit. The LSI53C1510 always generates parity for the PCI bus.	**6**
R	**Reserved**	**5**
WIE	**Write and Invalidate Enable** This bit allows the LSI53C1510 to generate memory Write and Invalidate commands on the PCI bus.	**4**
R	**Reserved**	**3**
EBM	**Enable Bus Mastering** This bit controls the ability of the LSI53C1510 to act as a master on the PCI bus. A value of zero disables this device from generating PCI bus master accesses. A value of one allows the LSI53C1510 to behave as a bus master. The device must be a bus master in order to fetch SCRIPTS instructions and transfer data.	**2**
EMS	**Enable Memory Space** This bit controls the ability of the LSI53C1510 to respond to Memory space accesses. A value of zero disables the device response. A value of one allows the LSI53C1510 to respond to Memory Space accesses at the address range specified by the Base Address Register One (MEMORY) and Base Address Register Two (SCRIPTS RAM) registers in the PCI configuration space.	**1**
EIS	**Enable I/O Space** This bit controls the LSI53C1510 response to I/O space accesses. A value of zero disables the device response. A value of one allows the LSI53C1510 to respond to I/O Space accesses at the address range specified by the Base Address Register Zero (I/O) register in the PCI configuration space.	**0**

Registers: 0x06–0x07

Status

Read/Write

15	14	13	12	11	10	9	8	7		5	4	3			0
DPE	SSE	RMA	RTA	R	DT		DPR	R			NC	R			
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Reads to this register behave normally. Writes are slightly different in that bits can be cleared, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a one. For instance, to clear bit 15 and not affect any other bits, write the value 0x8000 to the register.

DPE — **Detected Parity Error (from Slave)** — **15**

This bit is set by the LSI53C1510 whenever it detects a data parity error, even if the data parity error handling is disabled.

SSE — **Signaled System Error** — **14**

This bit is set whenever the device asserts the SERR/ signal.

RMA — **Received Master Abort (from Master)** — **13**

A master device should set this bit whenever its transaction (except for Special Cycle) is terminated with Master Abort.

RTA — **Received Target Abort (from Master)** — **12**

A master device should set this bit whenever its transaction is terminated by target abort.

R — **Reserved** — **11**

DT — **DEVSEL/ Timing** — **[10:9]**

These bits encode the timing of DEVSEL/. These are encoded as:

00b	fast
01b	medium
10b	slow
11b	reserved

These bits are read only and should indicate the slowest time that a device asserts DEVSEL/ for any bus command except Configuration Read and Configuration Write. The LSI53C1510 supports a value of 01b.

DPR **Data Parity Error Reported** **8**

This bit is set when the following conditions are met:

- The bus agent asserted PERR/ itself or observed PERR/ asserted and;
- The agent setting this bit acted as the bus master for the operation in which the error occurred and;
- The Parity Error Response bit in the Command register is set.

R **Reserved** **[7:5]**

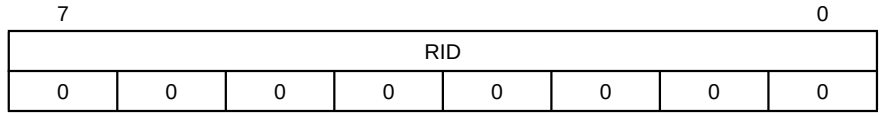
NC **New Capabilities** **4**

A value of one implements a list of extended capabilities.

R **Reserved** **[3:0]**

Register: 0x08

Revision ID (Rev ID)
Read Only

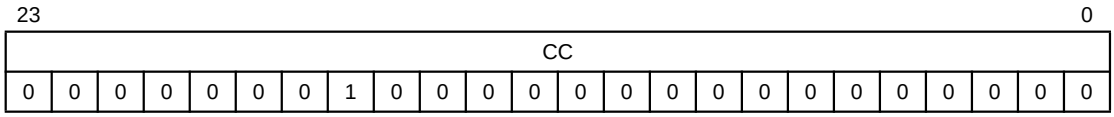


RID **Revision ID** **[7:0]**

This register specifies a device specific revision identifier. This silicon version of the LSI53C1510 is set to 0x00 for Rev A silicon.

Registers: 0x09–0x0B

Class Code
Read Only

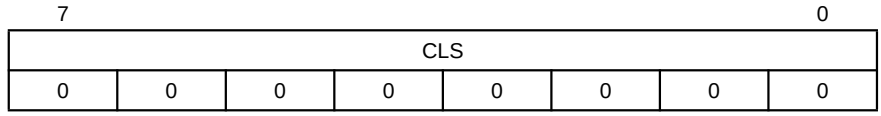


CC **Class Code** **[23:0]**

This 24-bit register is used to identify the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register level programming interface. The value of this register is 0x010000, which identifies a SCSI controller.

Register: 0x0C

Cache Line Size
Read/Write



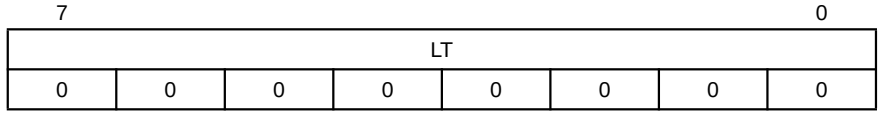
CLS **Cache Line Size** **[7:0]**

This register specifies the system cache line size in units of 32-bit words. The value in this register is used by the device to determine whether to use Memory Write and Invalidate or Write commands for performing write cycles,

and whether to use Memory Read, Memory Read Line, or Memory Read Multiple commands for performing read cycles as a bus master. Devices participating in the caching protocol use this field to know when to retry burst accesses at cache line boundaries. If this register is programmed to a number which is not a power of 2, the device will not use PCI performance commands to perform data transfers.

Register: 0x0D

Latency Timer
Read/Write



LT **Latency Timer** **[7:0]**

The Latency Timer register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. The SCSI functions of the LSI53C1510 support this timer. All eight bits are writable, allowing latency values of 0–255 PCI clocks. Use the following equation to calculate an optimum latency value for the SCSI functions of the LSI53C1510.

Latency = 2 + (Burst Size * (typical wait states + 1))

Values greater than optimum are also acceptable.

Register: 0x0E

Header Type
Read Only

7							0
HT[7:0]							
1	0	0	0	0	0	0	0

HT **Header Type** **[7:0]**
This 8-bit register identifies the layout of bytes 0x10 through 0x3F in configuration space and also whether or not the device contains multiple functions. Since the LSI53C1510 is a multifunction controller the value of this register is 0x80.

Register: 0x0F

Not Supported

Registers: 0x10–0x13

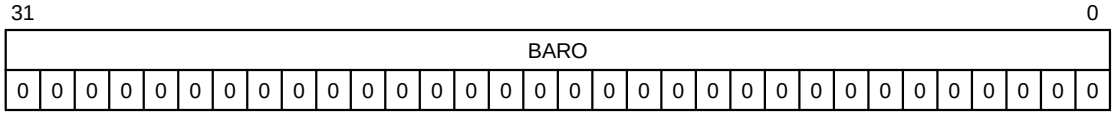
Base Address Register Zero (I/O)
Read/Write

31																													0
BARZ																													
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

BARZ **Base Address Register Zero - I/O** **[31:0]**
This base address register is used to map the operating register set into I/O space. The LSI53C1510 requires 256 bytes of I/O space for this base address register. It has bit zero hardwired to one. Bit 1 is reserved and returns a zero on all reads, and the other bits are used to map the device into I/O space. For detailed information on the operation of this register, refer to the PCI 2.1 Specification.

Registers: 0x14–0x17

Base Address Register One (MEMORY)
Read/Write

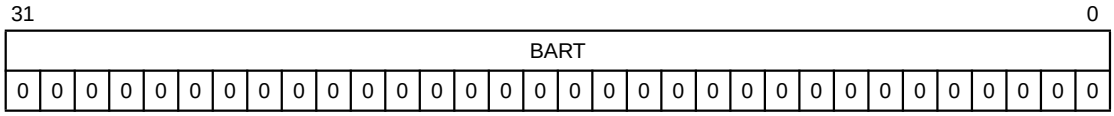


BARO **Base Address Register One** **[31:0]**

This base address register maps SCSI operating registers into memory space. This device requires 1024 bytes of address space for this base register. The default value of this register is 0x00000000. For detailed information on the operation of this register, refer to the PCI 2.1 Specification.

Registers: 0x18–0x1B

Base Address Register Two (SCRIPTS RAM)
Read/Write



BART **Base Address Register Two** **[31:0]**

This base register is used to map the SCRIPTS RAM into memory space.

The LSI53C1510 requires 4 K of address space for this base register. This register has bits [11:0] hardwired to 000000000000.

For detailed information on the operation of this register, refer to the PCI 2.1 Specification.

Registers: 0x1C–0x2B

Reserved

Registers: 0x2C–0x2D
Subsystem Vendor ID
Read Only

15															0
SVID															
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Default: If MEM_ADDR7 is HIGH

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Default: If MEM_ADDR7 is LOW

SVID **Subsystem Vendor ID** **[15:0]**

This 16-bit register is used to uniquely identify the vendor manufacturing the add-in board or subsystem where this PCI device resides. It provides a mechanism for an add-in card vendor to distinguish its cards from another vendor's cards, even if the cards have the same PCI controller installed on them (and therefore the same Vendor ID and Device ID).

If the external serial EEPROM interface is disabled (MEM_ADDR7 pulled HIGH), this register returns a value of 0x1000 (LSI Logic Vendor ID). The 16-bit value that should be stored in the external serial EEPROM for this register is the vendor's PCI Vendor ID and must be obtained from the PCI SIG. Please see Section 2.4.3, "Serial EEPROM," for more information on downloading a value for this register.

If the external serial EEPROM interface is enabled (MEM_ADDR7 pulled LOW), this register is automatically loaded at power-up from the external serial EEPROM and will contain the value downloaded from the serial EEPROM or a value of 0x0 if the download fails.

Registers: 0x2E–0x2F

Subsystem ID

Read Only

15															0
SID															
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Default: If MEM_ADDR7 is HIGH

x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Default: If MEM_ADDR7 is LOW

SID **Subsystem ID** **[15:0]**

This 16-bit register is used to uniquely identify the add-in board or subsystem where this PCI device resides. It provides a mechanism for an add-in card vendor to distinguish its cards from one another even if the cards have the same PCI controller installed on them (and therefore the same Vendor ID and Device ID).

If the external serial EEPROM is disabled (MEM_ADDR7 pulled HIGH), the register returns a value of 0x1000. The 16-bit value that should be stored in the external serial EEPROM is vendor specific.

If the external serial EEPROM interface is enabled (MEM_ADDR7 pulled LOW), this register is automatically loaded at power-up from the external serial EEPROM.

Registers: 0x30–0x33

Expansion ROM Base Address

Read/Write

31																													0
ERBA																													
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

ERBA **Expansion ROM Base Address** **[31:0]**

This four byte register handles the base address and size information for the expansion ROM. It functions exactly like the Base Address Register One (MEMORY) and Base Address Register Two (SCRIPTS RAM) registers,

except that the encoding of the bits is different. The upper 21 bits correspond to the upper 21 bits of the expansion ROM base address.

The expansion ROM Enable bit, bit 0, is the only bit defined in this register. This bit is used to control whether or not the device accepts accesses to its expansion ROM. When the bit is set, address decoding is enabled, and a device is used with or without an expansion ROM depending on the system configuration. To access the external memory interface, also set the Memory Space bit in the Command register.

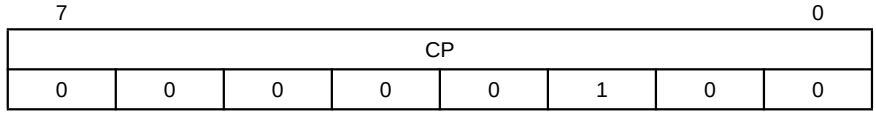
The host system detects the size of the external memory by first writing the Expansion ROM Base Address register with all ones and then reading back the register. The SCSI functions of the LSI53C1510 respond with zeros in all don't care locations. The ones in the remaining bits represent the binary version of the external memory size. For example, to indicate an external memory size of 32 Kbytes, this register, when written with ones and read back, returns ones in the upper 17 bits.

The size of the external memory is set through MEM_ADDR[3:0]. Please see Section 2.1.2, "Configuration and Initialization," for the possible size encodings available.

Register: 0x34

Capabilities Pointer

Read Only



CP **Capabilities Pointer** **[7:0]**

This register indicates that the first extended capability register is located at offset 0x40 in the PCI Configuration.

Registers: 0x35–0x3B

Reserved

Register: 0x3C

Interrupt Line
Read/Write

7							0
IL							
0	0	0	0	0	0	0	0

IL **Interrupt Line** **[7:0]**

This register is used to communicate interrupt line routing information. POST software writes the routing information into this register as it configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. Values in this register are specified by system architecture.

Register: 0x3D

Interrupt Pin
Read Only

7							0
IP							
0	0	0	0	0	0	0	1

Default: SCSI Function A, INTA/ signal

0	0	0	0	0	0	1	0

Default: SCSI Function B, INTB/ signal

IP **Interrupt Pin** **[7:0]**

This register is unique to each SCSI function. It tells which interrupt pin the device uses. Its value is set to 0x01 for the Function A (INTA/) signal, and 0x02 for the Function B (INTB/) signal at power-up.

Register: 0x3E

Min_Gnt
Read Only

7							0
MG							
0	0	0	1	1	1	1	0

MG **Min_Gnt** **[7:0]**
This register is used to specify the desired settings for latency timer values. Min_Gnt is used to specify how long a burst period the device needs. The value specified in these registers is in units of 0.25 microseconds. The LSI53C1510 sets this register to 0x1E.

Register: 0x3F

Max_Lat
Read Only

7							0
ML							
0	0	0	0	1	0	0	0

ML **Max_Lat** **[7:0]**
This register is used to specify the desired settings for latency timer values. Max_Lat is used to specify how often the device needs to gain access to the PCI bus. The value specified in these registers is in units of 0.25 microseconds. The LSI53C1510 SCSI function sets this register to 0x08.

Register: 0x40

Capability ID
Read Only

7							0
CID							
0	0	0	0	0	0	0	1

CID **Cap_ID** **[7:0]**
Bits [7:0] identify this register as a PCI power management register (0x01).

Register: 0x41

Next Item Pointer
Read Only

7							0
NIP							
0	0	0	0	0	0	0	0

NIP **Next_Item_Ptr** **[7:0]**
Bits [7:0] contain the offset location of the next item in the function's capabilities list. The LSI53C1510 has these bits set to zero indicating no further extended capabilities registers exist.

Registers: 0x42–0x43

Power Management Capabilities
Read Only

15				11	10	9	8		6	5	4	3	2		0
PMES[4:0]					D2S	D1S	R			DSI	APS	PMEC	VER[2:0]		
0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1

PMES[4:0] **PME_Support** **[15:11]**
Bits [15:11] define the power management states in which the LSI53C1510 will assert the PME pin. These bits are all set to zero.

D2S **D2_Support** **10**
D2 power management state is not supported.

D1S **D1_Support** **9**
D1 power management state is not supported.

R **Reserved** **[8:6]**

DSI **Device Specific Initialization** **5**
This bit is a device specific initialization bit and is set to zero to indicate that no special initialization is required.

APS **Auxiliary Power Source** **4**
This bit is set to zero and indicates that an auxiliary power source is not needed for the LSI53C1510.

PMEC **PME Clock** **3**
Bit 3 is set to zero and indicates that no PCI clock is required to assert the PME pin.

VER[2:0] **Version** **[2:0]**
These three bits indicate that the LSI53C1510 complies with Version 1.0 of the PCI Power Management Specification.

Registers: 0x44–0x45

Power Management Control/Status
Read/Write

15	14	13	12			9	8	7					2	0
PST	DSCL[1:0]		DSLT				PEN	R						PWS[1:0]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PST **PME_Status** **15**
This bit defines if the LSI53C1510 has generated a Power Management Event.

DSCL[1:0] **Data_Scale** **[14:13]**
These bits are not used in the LSI53C1510.

DSLT **Data_Select** **[12:9]**
These bits are not used in the LSI53C1510.

PEN **PME_Enable** **8**
This bit is not used in the LSI53C1510.

R **Reserved** **[7:2]**

PWS[1:0] **Power State** **[1:0]**
These bits are used to determine the current power state of the LSI53C1510. They are used to place the LSI53C1510 in a new power state. Power states are defined as:

00b	D0
11b	D3 hot

Register: 0x46
Bridge Support Extensions
Read Only

7							0
BSE							
0	0	0	0	0	0	0	0

BSE **Bridge Support Extensions** **[7:0]**
Bits [7:0] are not used and will return to 0x00 if read.

Register: 0x47
Data
Read Only

7							0
DATA							
0	0	0	0	0	0	0	0

DATA **Data** **[7:0]**
Bits [7:0] are not used and will return to 0x00 if read.

5.3 Differences from the LSI53C895 and the LSI53C896

The LSI53C1510 SCSI cores are similar to the LSI53C895 and LSI53C896, but there are differences. The differences are listed below.

- FIFO Depth

  The LSI53C1510 SCSI DMA FIFOs are 816 bytes deep (the same as the LSI53C895). The LSI53C896 FIFOs are 944 bytes deep.

- SCRIPTS RAM

  The LSI53C1510 SCRIPTS RAMs are 4 Kbytes while the LSI53C896 are 8 Kbytes.

- Register Differences

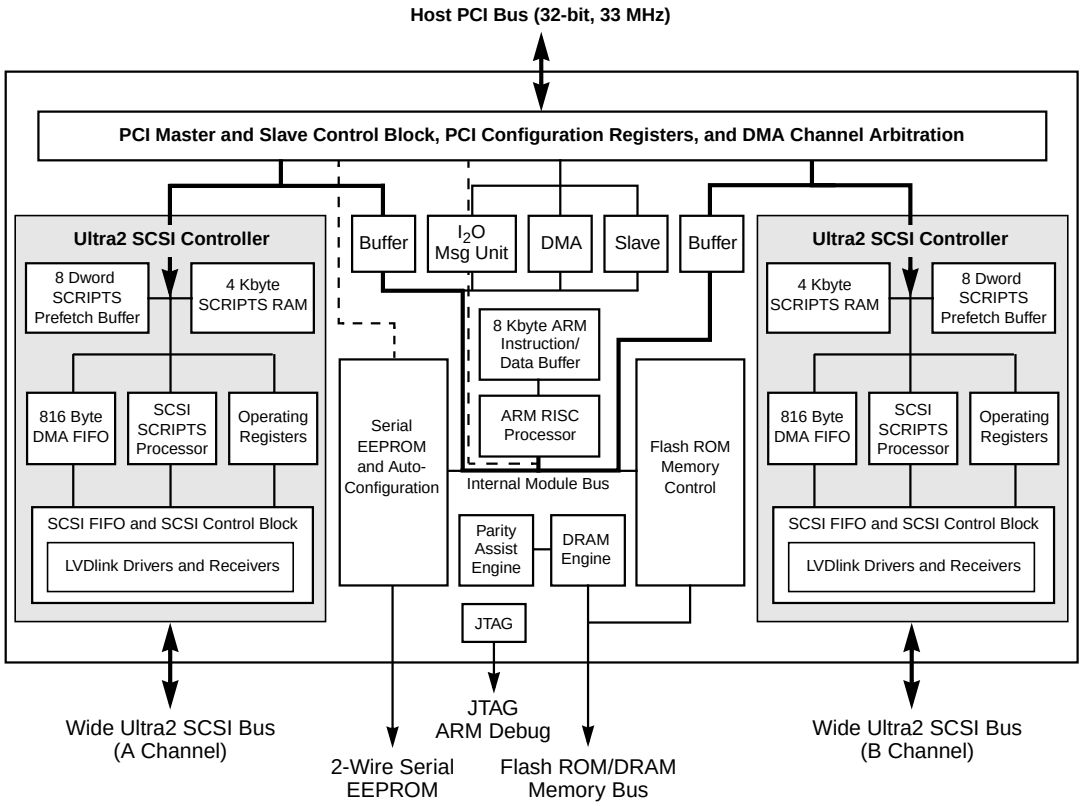
  Differences do exist between the LSI53C1510 and the LSI53C896 register bits. Chapter 12, “SCSI Interface,” in the *LSI53C1510 I_2O-Ready PCI RAID Ultra2 SCSI Controller Programming Guide* describes the differences.

Chapter 6
Registers
(Intelligent Mode)

This chapter contains the following sections:

After power-on, the LSI53C1510 is configured as either a nonintelligent or intelligent controller. This chapter describes the PCI and host interface registers that are visible to the host in intelligent mode. In intelligent mode, the LSI53C1510 is configured as an Intelligent IOP supporting either dual channel SCSI or RAID. In intelligent mode, a single Base Address region is defined that contains the I_2O messaging interface and control. Figure 6.1 illustrates how, in intelligent mode of operation, the I_2O messages are routed to the ARM RISC processor and the processor controls the other modules including the two SCSI modules.

Figure 6.1 LSI53C1510 Block Diagram in Intelligent Mode



This section contains descriptions of the LSI53C1510 PCI and host interface commands and registers. In the descriptions the term “set” is used to refer to bits that are programmed to a binary one. Similarly, the terms “clear” and “reset” are used to refer to bits that are programmed to a binary zero. **Do not set reserved bits.** Reserved bit functions may change at any time. Unless otherwise indicated, all bits in registers are active high, that is, the feature is enabled by setting the bit. The bottom row of every register diagram shows the default register values, which are enabled after the chip is powered on or reset. Reserved registers and bits are shaded.

6.1 Programming Models

The LSI53C1510 in intelligent mode contains two programming models: a System (host) Programming Model and a Local Programming Model. The system model includes all necessary hardware registers, shared memory and associated memory addresses from the host viewpoint using system addresses. The Local Programming Model includes all hardware and memory which are private from the system.

6.1.1 System Programming Model

The System Programming Model consists of PCI Configuration Registers, Host Interface Registers, and a Shared Memory Region.

6.1.2 Local Programming Model

The Local Programming Model consists of ARM Registers, Protocol Engine Registers, and Local Memory Regions.

6.2 PCI Configuration Registers (Intelligent Mode)

The PCI Configuration registers, as shown in Table 6.1, are accessed by performing a configuration read/write to the device with its IDSEL pin asserted and the appropriate value in AD[10:8] during the address phase of the transaction.

All PCI compliant devices, such as the LSI53C1510, must support the Vendor ID, Device ID, Command, and Status registers. Support of other PCI compliant registers is optional. In the LSI53C1510, registers that are not supported are not writable and return all zeros when read. Only those registers and bits that are currently supported by the LSI53C1510 are described in this chapter. Reserved bits should not be accessed. Reserved registers and bits are shaded.

Table 6.1 PCI Configuration Register Map

31 16	15 0	Address	Page
Device ID	Vendor ID	0x00	6-5
Status	Command	0x04	6-5
Class Code	Revision ID (Rev ID)	0x08	6-8
BIST (Built-In Self Test) / Header Type	Latency Timer / Cache Line Size	0x0C	6-9
Base Address Register Zero (I/O)		0x10	6-11
Base Address Register One (Shared MEMORY)		0x14	6-12
Reserved		0x18	6-12
Reserved		0x1C	6-12
Reserved		0x20	6-12
Reserved		0x24	6-12
Reserved		0x28	6-12
Subsystem ID	Subsystem Vendor ID	0x2C	6-12
Expansion ROM Base Address		0x30	6-13
Reserved	Capabilities Pointer	0x34	6-14
Reserved		0x38	6-14
Max_Lat / Min_Gnt	Interrupt Pin / Interrupt Line	0x3C	6-14
Power Management Capabilities (PMC)	Next Item Pointer / Capability ID	0x40	6-16
Data / Bridge Support Extensions (PMCSR_BSE)	Power Management Control/Status (PMCSR)	0x44	6-17

Registers: 0x00–0x01

Vendor ID

Read Only

15															0
VID															
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

VID **Vendor ID** **[15:0]**

This 16-bit register identifies the manufacturer of the device. The Vendor ID is 0x1000.

Registers: 0x02–0x03

Device ID

Read Only

15															0
DID															
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

DID **Device ID** **[15:0]**

This 16-bit register identifies the particular device. The Device ID is 0x10.

Registers: 0x04–0x05

Command

Read/Write

15						9	8	7	6	5	4	3	2	1	0
R							SE	R	EPER	R	WIE	R	EBM	EMS	EIS
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles. When a zero is written to this register, the LSI53C1510 is logically disconnected from the PCI bus for all accesses except configuration accesses.

R	**Reserved**	**[15:9]**
SE	**SERR/ Enable** This bit enables the SERR/ driver. SERR/ is disabled when this bit is zero and enabled when the bit is one. The default value of this bit is zero. This bit and bit 6 must be set to report address parity errors.	**8**
R	**Reserved**	**7**
EPER	**Enable Parity Error Response** This bit allows the LSI53C1510 to detect parity errors on the PCI bus and report these errors to the system. Only data parity checking is enabled and disabled with this bit. The LSI53C1510 always generates parity for the PCI bus.	**6**
R	**Reserved**	**5**
WIE	**Write and Invalidate Enable** This bit allows the LSI53C1510 to generate write and invalidate commands on the PCI bus.	**4**
R	**Reserved**	**3**
EBM	**Enable Bus Mastering** This bit controls the ability of the LSI53C1510 to act as a master on the PCI bus. A value of zero disables this device from generating PCI bus master accesses. A value of one allows the LSI53C1510 to behave as a bus master. The device must be a bus master in order to fetch SCRIPTS instructions and transfer data.	**2**
EMS	**Enable Memory Space** This bit controls the ability of the LSI53C1510 to respond to Memory space accesses. A value of zero disables the device response. A value of one allows the LSI53C1510 to respond to Memory Space accesses.	**1**
EIS	**Enable I/O Space** This bit controls the LSI53C1510 response to I/O space accesses. A value of zero disables the device response. A value of one allows the LSI53C1510 to respond to I/O space accesses.	**0**

Registers: 0x06–0x07

Status

Read/Write

15	14	13	12	11	10	9	8	7		5	4	3			0
DPE	SSE	RMA	RTA	R	DT		DPR	R			NC	R			
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

The Status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be cleared, but not set. A bit is cleared whenever the register is written, and the data in the corresponding bit location is a one. For instance, to clear bit 15 and not affect any other bits, write the value 0x8000 to the register.

DPE — **Detected Parity Error (from Slave)** **15**

This bit is set by the LSI53C1510 whenever it detects a data parity error, even if data parity error handling is disabled.

SSE — **Signaled System Error** **14**

The LSI53C1510 sets this bit whenever it asserts the SERR/ signal.

RMA — **Received Master Abort (from Master)** **13**

A master device should set this bit whenever its transaction (except for Special Cycle) is terminated with Master Abort.

RTA — **Received Target Abort (from Master)** **12**

A master device should set this bit whenever its transaction is terminated by target abort.

R **Reserved** **11**

DT **DEVSEL/Timing** **[10:9]**
These bits encode the timing of DEVSEL/. These bits are read only and should indicate the slowest time that a device asserts DEVSEL/ for any bus command except Configuration Read and Configuration Write. The LSI53C1510 supports a value of 01b.

0, 0	fast
0, 1	medium
1, 0	slow
1, 1	reserved

DPR **Data Parity Error Reported** **8**
This bit is set when the following conditions are met:

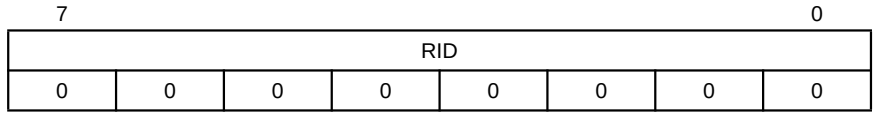
- The bus agent asserted PERR/ itself or observed PERR/ asserted and;
- The agent setting this bit acted as the bus master for the operation in which the error occurred and;
- The Parity Error Response bit in the Command register is set.

R **Reserved** **[7:5]**

NC **New Capabilities** **4**
A value of one implements a list of extended capabilities.

R **Reserved** **[3:0]**

Register: 0x08
Revision ID (Rev ID)
Read Only



RID **Revision ID** **[7:0]**
This register specifies a device specific revision identifier. This silicon version of the LSI53C1510 is set to 0x00 for Rev A silicon.

Registers: 0x09–0x0B

Class Code
Read Only

23																						0
CC																						
0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0

CC **Class Code** **[23:0]**

This 24-bit register is used to identify the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register level programming interface. The value of this register is 0x0E0000, which identifies an I_2O IOP (LSI53C1510 in intelligent mode).

Register: 0x0C

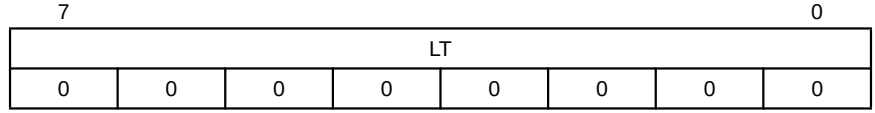
Cache Line Size
Read/Write

7							0
CLS							
0	0	0	0	0	0	0	0

CLS **Cache Line Size** **[7:0]**

This register specifies the system cache line size in units of 32-bit words. The value in this register is used by the device to determine whether to use Write and Invalidate or Write commands for performing write cycles, and whether to use Memory Read, Memory Read Line, or Memory Read Multiple commands for performing read cycles as a bus master. Devices participating in the caching protocol use this field to know when to retry burst accesses at cache line boundaries. These devices can ignore the PCI cache support lines (SDONE and SB0/) when this register is set to 0. If this register is programmed to a number which is not a power of 2, the device will not use PCI performance commands to perform data transfers.

Register: 0x0D
Latency Timer
Read/Write



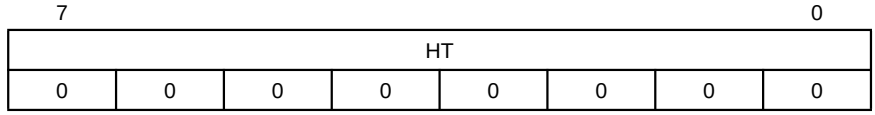
LT **Latency Timer** **[7:0]**

The Latency Timer register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. The SCSI functions of the LSI53C1510 support this timer. All eight bits are writable, allowing latency values of 0–255 PCI clocks. Use the following equation to calculate an optimum latency value for the SCSI functions of the LSI53C1510.

Latency = 2 + (Burst Size * (typical wait states + 1))

Values greater than optimum are also acceptable.

Register: 0x0E
Header Type
Read Only



HT **Header Type** **[7:0]**

This 8-bit register identifies the layout of bytes 0x10 through 0x3F in configuration space and also whether or not the device contains multiple functions. In intelligent mode, the LSI53C1510 is a single function controller, therefore, the value of this register is 0x00.

Register: 0x0F

BIST (Built-In Self Test)
Read/Write

7	6	5	4	3			0
BC	SB	R		CC			
0	0	0	0	0	0	0	0

BC **BIST Capable** **7**
Should return a one if the device implements a BIST, a zero if it does not.

SB **Start BIST** **6**
Writing a one into this bit starts the device's BIST. The device resets this bit automatically upon completion. Software should fail the device if the BIST does not complete within two seconds.

R **Reserved** **[5:4]**

CC **Completion Code** **[3:0]**
A value of zero indicates successful completion, while a nonzero result indicates a device specific error.

Registers: 0x10–0x13

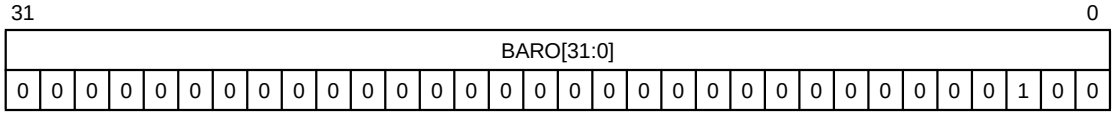
Base Address Register Zero (I/O)
Read/Write

31																													0
BARZ																													
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BARZ **Base Address Register Zero - I/O** **[31:0]**
This base address register is used to map the operating register set into I/O space. The LSI53C1510 requires 256 bytes of I/O space for this base address register. This register has bit zero hardwired to one. Bit 1 is reserved and returns a zero on all reads, and the other bits are used to map the device into I/O space. For detailed information on the operation of this register, refer to the PCI 2.1 Specification.

Registers: 0x14–0x17

Base Address Register One (Shared MEMORY)
Read/Write



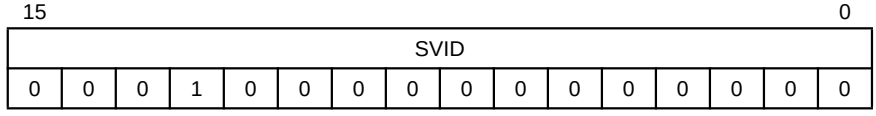
BARO **MEMORY Base Address Register One [31:0]**
This base address register map indicates width (32-bit) and location of memory required by the device and its size is programmable from 1 K (2^{10}) through 128 M (2^{27}) bytes in steps of powers of 2. This memory is specified as nonprefetchable due to the messaging FIFOs. The default size is 128 K.

Registers: 0x18–0x2B

Reserved

Registers: 0x2C–0x2D

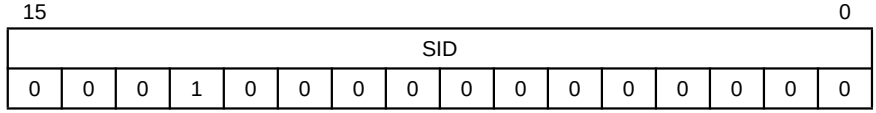
Subsystem Vendor ID
Read Only



SVID **Subsystem Vendor ID [15:0]**
This 16-bit register is used to uniquely identify the vendor manufacturing the add-in board or subsystem where this PCI device resides. It provides a mechanism for an add-in card vendor to distinguish its cards from another vendor's cards, even if the cards have the same PCI controller installed on them (and therefore the same Vendor ID and Device ID). The ARM programs this 16-bit value at startup or reset time.

Registers: 0x2E–0x2F

Subsystem ID
Read Only

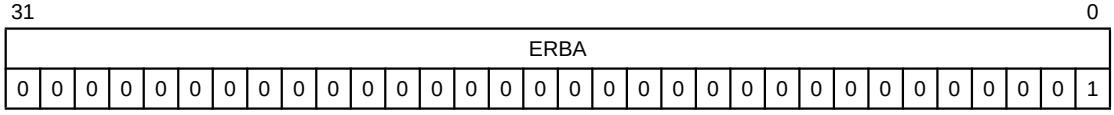


SID **Subsystem ID** **[15:0]**

This 16-bit register is used to uniquely identify the add-in board or subsystem where this PCI device resides. It provides a mechanism for an add-in card vendor to distinguish its cards from one another even if the cards have the same PCI controller installed on them (and therefore the same Vendor ID and Device ID). The ARM programs this 16-bit value at startup or reset time.

Registers: 0x30–0x33

Expansion ROM Base Address
Read/Write



ERBA **Expansion ROM Base Address** **[31:0]**

This register indicates the location of expansion ROM device and is programmable from 16 K (2^{14}) through 4 (2^{22}) Mbytes in steps of powers of 2 (using external pin pull-up options on the external memory address (MEM_ADDR) bits [3:0]).

Register: 0x34

Capabilities Pointer
Read Only

7							0
CP							
0	0	0	0	0	1	0	0

CP **Capabilities Pointer** **[7:0]**
This register indicates that the first extended capability register is located at offset 0x40 in the PCI Configuration.

Registers: 0x35–0x3B

Reserved

Register: 0x3C

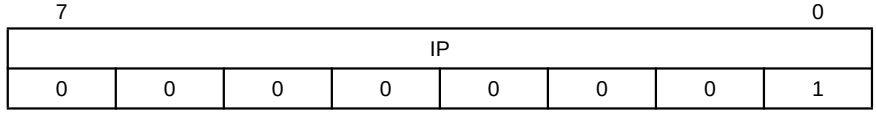
Interrupt Line
Read/Write

7							0
IL							
0	0	0	0	0	0	0	0

IL **Interrupt Line** **[7:0]**
This register is used to communicate interrupt line routing information. POST software writes the routing information into this register as it configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. Values in this register are specified by system architecture.

Register: 0x3D

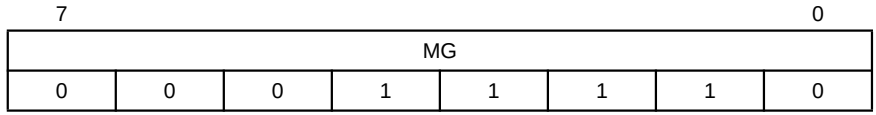
Interrupt Pin
Read Only



IP **Interrupt Pin** **[7:0]**
This register tells which interrupt pin the device uses. Its value is set to 0x01.

Register: 0x3E

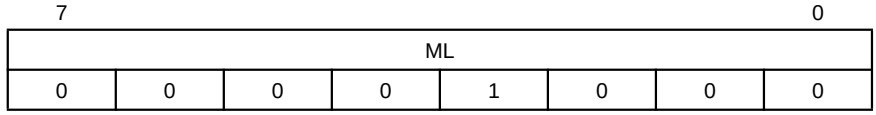
Min_Gnt
Read Only



MG **Min_Gnt** **[7:0]**
This register is used to specify the desired settings for latency timer values. Min_Gnt is used to specify how long a burst period the device needs. The value specified in these registers is in units of 0.25 microseconds. The LSI53C1510 sets this register to 0x1E.

Register: 0x3F

Max_Lat
Read Only



ML **Max_Lat** **[7:0]**
This register is used to specify the desired settings for latency timer values. Max_Lat is used to specify how often the device needs to gain access to the PCI bus.

The value specified in these registers is in units of 0.25 microseconds. The LSI53C1510 SCSI function sets this register to 0x08.

Register: 0x40

Capability ID
Read Only

7							0
CID							
0	0	0	0	0	0	0	1

CID **Cap_ID** **[7:0]**
Bits [7:0] identify this register as a PCI power management register (0x01).

Register: 0x41

Next Item Pointer
Read Only

7							0
NIP							
0	0	0	0	0	0	0	0

NIP **Next_Item_Ptr** **[7:0]**
The LSI53C1510 has these bits set to zero indicating PCI does not have any further PCI extended capabilities registers.

Registers: 0x42–0x43

Power Management Capabilities (PMC)
Read Only

15				11	10	9	8		6	5	4	3	2		0
PMES[4:0]					D2S	D1S	R			DSI	APS	PMEC	VER[2:0]		
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1

PMES[4:0] **PME_Support** **[15:11]**
Bits [15:11] define the power management states in which the LSI53C1510 will assert the PME pin. These bits are all set to zero.

D2S **D2_Support** **10**
D2 power management state is not supported.

D1S **D1_Support** **9**
D1 power management state is not supported.

R **Reserved** **[8:6]**

DSI **Device Specific Initialization** **5**
This bit is a device specific initialization bit and is set to zero to indicate that no special initialization is required.

APS **Auxiliary Power Source** **4**
This bit is set to zero and indicates that an auxiliary power source is not needed for the LSI53C1510.

PMEC **PME Clock** **3**
Bit 3 is set to zero and indicates that no PCI clock is required to assert the PME pin.

VER[2:0] **Version** **[2:0]**
These bits indicate the version of the PCI Power Management Specification the LSI53C1510 complies to version 1.0.

Registers: 0x44–0x45

Power Management Control/Status (PMCSR)
Read/Write

15	14	13	12			9	8	7					2	0
PST	DSCL[1:0]		DSLT				PEN	R						PWS[1:0]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PST **PME_Status** **15**
Bit 15 defines if the LSI53C1510 has generated a Power Management Event.

DSCL[1:0] **Data_Scale** **[14:13]**
Bits [14:13] are not supported in the LSI53C1510.

DSLT **Data_Select** **[12:9]**
Bits [12:9] are not supported in the LSI53C1510.

PEN **PME_Enable** **8**
Bit 8 is not supported in the LSI53C1510.

R **Reserved** **[7:2]**

PWS[1:0] **Power State** **[1:0]**

Bits [1:0] are used to determine the current power state of the LSI53C1510. They are also used to set the LSI53C1510 to a new power state. Power states are defined as:

00b00	D0
0b11	D3 hot

Register: 0x46

Bridge Support Extensions (PMCSR_BSE)
Read Only

7							0
BSE							
0	0	0	0	0	0	0	0

BSE **Bridge Support Extensions** **[7:0]**

Bits [7:0] are not supported and will return 0x00 when read.

Register: 0x47

Data
Read Only

7							0
DATA							
0	0	0	0	0	0	0	0

DATA **Data** **[7:0]**

Bits [7:0] are not supported and will return 0x00 when read.

6.3 Host Interface Registers (Intelligent Mode)

The host interface contains the following registers as shown in Table 6.2. Reserved registers and bits are shaded.

Table 6.2 LSI53C1510 Host Interface Register Map

31 16 15	0 Address	Page
DiagINT[1]	0x00	6-20
WRSEQ[1]	0x04	6-21
DIAG[1]	0x08	6-22
Test Base Address[1]	0x0C	6-23
Reserved	0x10	6-23
Reserved	0x14	6-23
Reserved	0x18	6-23
Reserved	0x1C	6-23
Host Doorbell	0x20	6-24
Reserved	0x24	6-24
Reserved	0x28	6-24
Reserved	0x2C	6-24
Reply Interrupt Status	0x30	6-25
Reply Interrupt Mask	0x34	6-25
Reserved	0x38	6-26
Reserved	0x3C	6-26
Request Free List FIFO (read only), Request Post List FIFO (write only)[2]	0x40	6-26
Reply Post List FIFO (read only), Reply Free List FIFO (write only)[2]	0x44	6-26

1. These registers are for diagnostic or test use only.
2. Write access to the Request Post List and Reply Free List FIFOs that are less than 32 bits are ignored.

Register: 0x00
DiagINT
Read/Write

31																										2	1	0
R																											IEN	DiagINT/CLRINT
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: This register is intended for diagnostic/test use only.

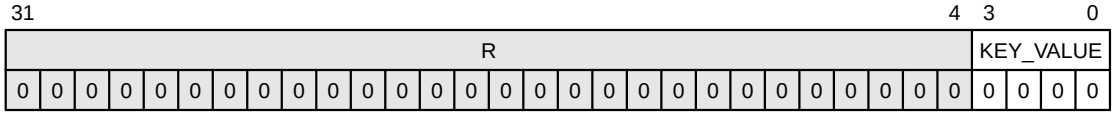
The DiagINT register contains interrupt status and control as described below. The LSI53C1510 Protocol Engine can be configured to generate interrupts using direct F/W control. This register is used to report and enable/mask interrupts to PCI. The normal PCI interrupt reporting mechanism occurs in the Reply Interrupt Status register. This register is provided for diagnostic purposes only.

R **Reserved** **[31:2]**

IEN **Interrupt Enable** **1**
The IEN control bit provides an enable function for the PCI interrupt pin when F/W generated interrupts are selected. In order for the external PCI INT/ interrupt pin to be asserted when F/W generated interrupts are selected, the IEN bit must be set to one.

DiagINT/CLRINT
Diagnostic Interrupt (read)/ Clear Interrupt (write) **0**
The DiagINT status bit indicates that the Protocol Engine is alerting the host of an interrupt condition. When the F/W generated interrupt source is selected, writing a one to bit 0 of this register will clear the F/W generated interrupt. This interrupt status bit is not normally used except for diagnostic purposes.

Register: 0x04
WRSEQ
Write Only



Note: This register is intended for diagnostic/test use only.

The WRSEQ register is used to enable write accesses to the DIAG register. In order to prevent inadvertent access, the DIAG register cannot be written to unless a specific sequence of data is written to the WRSEQ register. The WRSEQ register is write only.

R **Reserved** **[31:4]**

KEY_VALUE **KEY_VALUE** **[3:0]**
A sequence of five data writes must be written into the KEY_VALUE field of the WRSEQ register in order to enable writes to the DIAG register. Any data value written out that does not match the expected sequence value will cause the WRSEQ register to restart by looking for the first sequence value. The required data sequence is:

0x4, 0xB, 0x2, 0x7, 0xD

After the last value (0xD) is written, the DIAG register may be written to until another write to the WRSEQ register occurs of any value. A bit is provided within the DIAG register which may be read at any time to determine if write access is enabled for the DIAG register (e.g. to verify that the WRSEQ data sequence was correct or to verify that writes to the DIAG register are disabled).

Register: 0x08
DIAG
Read/Write

31	8	7	6	4	3	2	1	0
R		DWE	R		TTL_INT	RSTA	DISARM	DMMAP
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		0	0	0 0	0	0	0	0

Note: This register is intended for diagnostic/test use only.

The register contains low level diagnostic control and status.

R **Reserved** **[31:8]**

DWE **DIAG Register Write Enabled (read only)** **7**
This read only bit when set indicates that write access to the DIAG register may occur. The DWE bit is set when the correct key sequence has been written to the WRSEQ register.

R **Reserved** **[6:4]**

TTL_INT **Select TTL Output for PCI-INTA/** **3**
This bit determines whether the LSI53C1510 PCI-INTA/ interrupt pin is configured as a TTL or open drain output. This bit defaults to zero (open drain) on reset. This bit should only be set to one (TTL) during chip testing.

RSTA **Reset Adapter (write only)** **2**
This write only bit will cause the Protocol Engine reset controller to generate a soft reset to all LSI53C1510 logic. This bit will be automatically cleared when the soft reset condition is generated. The ARM core will start executing from its Reset Vector when the soft reset condition subsides.

DISARM **Disable ARM Core** **1**
The DISARM control bit causes the ARM core, the Instruction Prefetch Unit, the Read Path Control Unit, and the Write Buffer to be held reset. This bit will remain set until cleared by the host. This bit is included to allow low level testing and programming of FLASH memory using a host resident utility.

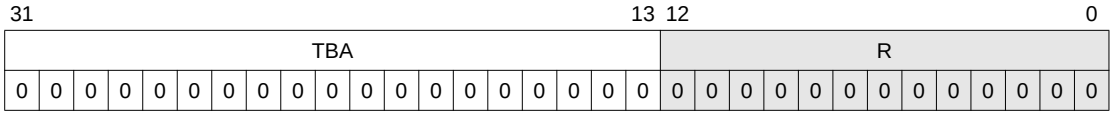
DMMAP **Diagnostic Memory Map** **0**

This bit when set causes all PCI accesses to Memory Base 0 address space (except for offsets 0x00–0x7F) to be mapped to internal local bus accesses. This allows Host utilities the capability to read or write any arbitrary internal local address. This is useful for low level testing and for programming FLASH memory using host resident utilities. To form an internal local address, the lower 13 bits of the PCI address are combined with the contents of the Test Base Address register. This gives an 8 Kbyte window of addressability into local address space at any one time.

Register: 0x0C

Test Base Address

Read/Write



Note: This register is intended for diagnostic/test use only.

TBA **Test Base Address** **[31:13]**

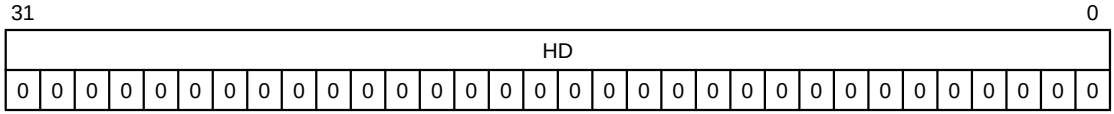
The TBA Register is used to provide address bits [31:13] of the local address during diagnostic host<->local accesses (the lower 13 address bits come directly from the host address).

R **Reserved** **[12:0]**

Registers: 0x10–0x1F

Reserved

Register: 0x20
Host Doorbell
Read/Write



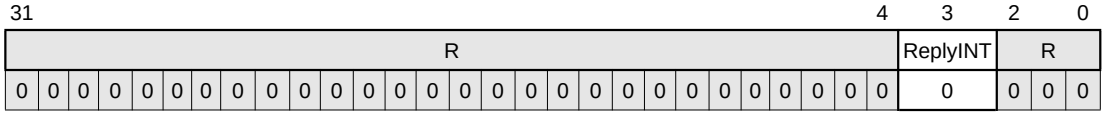
HD **Host Doorbell** **[31:0]**

This is a 32-bit inbound doorbell register accessible by the host. All 32 bits of the register are read/write by a PCI master, although the PCI master can only set a bit to one. The PCI master cannot clear a bit to zero. The ARM can read and write all 32 doorbell bits using a locally mapped ARM Doorbell register, although the ARM can only clear a bit to zero. The ARM cannot set a bit to one. Should a PCI master setting operation occur simultaneously with an ARM clearing operation, the clearing operation takes precedence. The default reset state of the doorbell register is all zeros. A read only interrupt status bit is available to the ARM to indicate that any of the 32 doorbell bits are set. A read/write interrupt enable bit is available to the ARM to allow the interrupt status bit to generate an interrupt to the ARM when both the interrupt status bit and the interrupt enable bit are set to one.

Registers: 0x24–0x2F
Reserved

Register: 0x30

Reply Interrupt Status
Read Only



The Reply Interrupt Status register reports interrupt status to PCI.

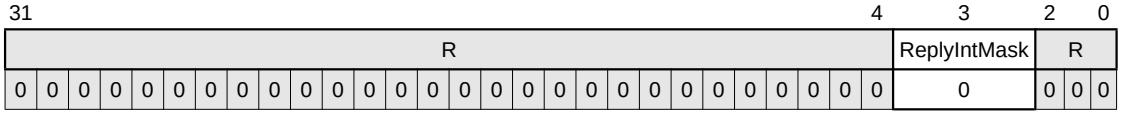
R **Reserved** **[31:4]**

ReplyINT **Reply Message Interrupt** **3**
This read only bit is set whenever a Posted Reply Message is available for the host to process (ReplyPostFIFO not empty and prefetch of ReplyPost-MFA complete). This bit will cause a PCI interrupt to be generated when ReplyIntMask = 0. This is the default interrupt reporting mechanism for the LSI53C1510 Protocol Engine.

R **Reserved** **[2:0]**

Register: 0x34

Reply Interrupt Mask
Read/Write



The Reply Interrupt Mask register masks interrupt reporting to PCI.

R **Reserved** **[31:4]**

ReplyIntMask **Reply Message Interrupt Mask** **3**
This bit masks the PCI interrupt generated by the Reply-PostFIFO not empty condition. When this bit is set to one, the PCI interrupt will not be generated. When this bit is reset to zero, the PCI interrupt will be generated. This bit defaults to one on hard or soft reset.

R **Reserved** **[2:0]**

Registers: 0x38–0x3F
Reserved

Register: 0x40
Request Free List FIFO (Read Only)
Request Post List FIFO (Write Only)

31																													0
FIFO																													
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Request messages are created by the host to “request” an action by the LSI53C1510. For a complete explanation of how the Request Free/Post List FIFOs are used in the message passing I/O interface, see Section 2.2, “The Host Interface.”

Register: 0x44
Reply Post List FIFO (Read Only)
Reply Free List FIFO (Write Only)

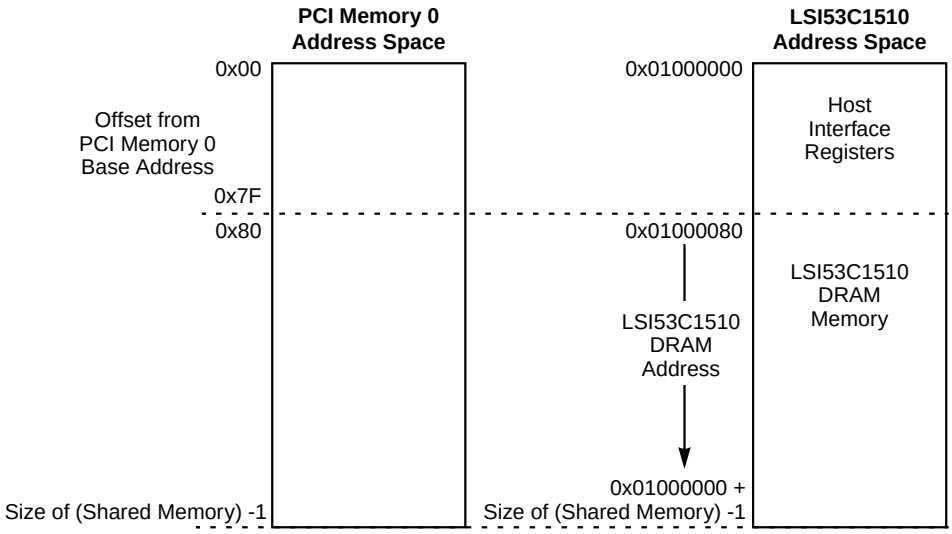
31																													0
FIFO																													
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reply messages are used by the LSI53C1510 to send status information back to the host. For a complete explanation of how the Reply Post/Free List FIFOs are used in the message passing I/O interface, see Section 2.2, “The Host Interface.”

6.4 Shared Memory

A region of Shared Memory (LSI53C1510 local memory mapped to System Addresses) is provided to allow the host to write Request Message Frames into. This is the default method (Push model) for Request Message Frame transport, where the host itself copies the Request Message Frame into the LSI53C1510 local memory. The total size of Shared Memory is configured by the Protocol Engine on reset. Supported values are: 32 Kbytes, 64 Kbytes, 128 Kbytes (default), 256 Kbytes, 512 Kbytes, 1 Mbyte, 2 Mbytes, 4 Mbytes, 8 Mbytes, 16 Mbytes, 32 Mbytes, 64 Mbytes, and 128 Mbytes. Address translation between System and Local addresses is performed as illustrated in Figure 6.2.

Figure 6.2 Shared Memory Address Translation



Chapter 7
Specifications

This chapter specifies the LSI53C1510 electrical and mechanical characteristics. It is divided into the following sections:

7.1 DC Characteristics

This section of the manual describes the LSI53C1510 DC characteristics. Table 7.1 through Table 7.13 give current and voltage specifications. Figure 7.1 and Figure 7.2 are driver schematics.

Table 7.1 Absolute Maximum Stress Ratings

Symbol	Parameter	Min	Max[1]	Unit	Test Conditions
T_{STG}	Storage temperature	–55	150	°C	–
V_{DD}	Supply voltage	–0.5	5.0	V	–
V_{IN}	Input voltage	V_{SS} –0.3	V_{DD} +0.3	V	–
V_{IN5V}	Input voltage (5 V tolerant pins)	V_{SS} –0.3	5.25	V	–
I_{LP}[2]	Latch-up current	150	–	mA	–
ESD[3]	Electrostatic discharge	–	2 K	V	MIL-STD 883C, Method 3015.7

1. Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions section of the manual is not implied.
2. $-2\ V < V_{PIN} < 8\ V$.
3. SCSI pins only.

Table 7.2 Operating Conditions

Symbol	Parameter	Min	Max[1]	Unit	Test Conditions
V_{DD}	Supply voltage	3.13	3.47	V	–
I_{DD}	Supply current (dynamic) Supply current (static)	–	800 1	mA mA	–
$I_{DD\text{-}SCSI}$	LVD pad current supply	–	1.2	A	RBIAS = 9.76 kΩ V_{DD} = 3.3 V
T_A	Operating free air	0	70	°C	–
θ_{JA}	Thermal resistance (junction to ambient air)	–	14.8	°C/W	–
Tj	Temperature of the die	–	110	°C	–
Tc	Temperature of the case	–	100	°C	–

1. Conditions that exceed the operating limits may cause the device to function incorrectly.

Table 7.3 LVD Driver SCSI Signals—SD[15:0]+, SDP[1:0]/, SREQ/, SACK/, SMSG/, SIO/, SCD/, SATN/, SBSY/, SSEL/, SRST/

Symbol	Parameter	Min	Max	Units	Test Conditions
I_O+	Source (+) current	7	11	mA	Asserted state
I_O-	Sink (–) current	–7	–11	mA	Asserted state
I_O+	Source (+) current	–3.5	–5.5	mA	Negated state
I_O-	Sink (–) current	3.5	5.5	mA	Negated state
I_{OZ}	3-state leakage	–20	20	µA	V_{PIN} = 0 V, 3.47 V
I_{OZ} ($_{SRST\ -\ only}$)	3-state leakage	–500	–50	µA	–

Notes: V_{CM} = 0.7–1.8 V.
R_L = 0–110 Ω.
R_{bias} = 9.76 kΩ.

Figure 7.1 LVD Driver

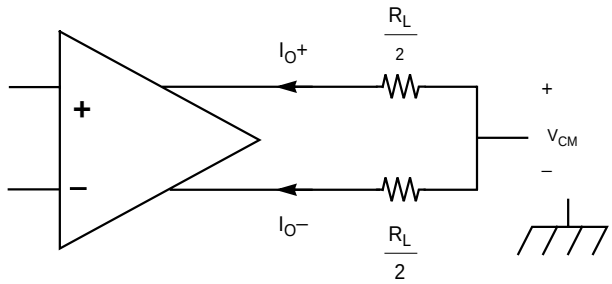


Table 7.4 LVD Receiver SCSI Signals—SD[15:0]/, SDP[1:0]/, SREQ/, SACK/, SMSG/, SIO/, SCD/, SATN/, SBSY/, SSEL/, SRST/

Symbol	Parameter	Min	Max	Units
V_I	LVD receiver voltage asserting	60	–	mV
V_I	LVD receiver voltage negating	–	–60	mV

Note:V_{CM} = 0.7–1.8 V

Figure 7.2 LVD Receiver

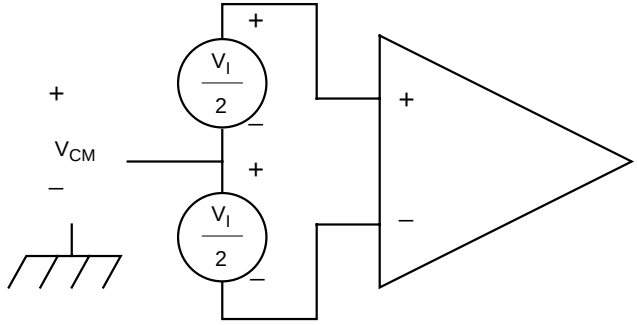


Table 7.5 DIFFSENS SCSI Signal

Symbol	Parameter	Min	Max	Unit	Test Conditions[1]
V_{IH}	HVD sense voltage	2.4	5.0	V	Note 1
V_S	LVD sense voltage	0.7	1.9	V	Note 1
V_{IL}	SE sense voltage	V_{SS} –0.3	0.5	V	Note 1
I_{IN}	Input leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V

1. Functional test specified for each mode (V_{IH}, V_S, V_{IL}).

Table 7.6 RBIAS SCSI Signal

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IN}	Input Voltage	V_{DD} –0.2	–	V	–125 µA

Table 7.7 Input Capacitance

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input capacitance of input pads	–	7	pF	–
C_{IO}	Input capacitance of I/O pads	–	15	pF	–

Table 7.8 Bidirectional Signals—GPIO0, GPIO1, GPIO2, GPIO3, GPIO4

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	5.0	V	–
V_{IL}	Input low voltage	V_{SS} –0.3	0.8	V	–
V_{OH}	Output high voltage	2.4	V_{DD}	V	–8 mA dynamic
V_{OL}	Output low voltage	V_{SS}	0.4	V	8 mA dynamic
I_{OZ}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V
I_{PULL}	Pull-down current	7.5	75	µA	–

Table 7.9 Output Signals—MCE/, MOE/_TESTOUT, MWE/, TDO

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	–4 mA dynamic
V_{OL}	Output low voltage	V_{SS}	0.4	V	4 mA dynamic
I_{OZ}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V

Table 7.10 Bidirectional Signals—AD[31:0], C_BE[7:0]/, FRAME/, IRDY/, TRDY/, DEVSEL/, STOP/, PERR/, PAR

Symbol	Parameters	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	0.5 V_{DD}	5.0	V	–
V_{IL}	Input low voltage	V_{SS} –0.3	0.3 V_{DD}	V	–
V_{OH}	Output high voltage	0.9 V_{DD}	–	V	–500 µA
V_{OL}	Output low voltage	–	0.1 V_{DD}	V	1500 µA
V_{OH}	5 V tolerant output high voltage	2.4	–	V	–16 mA
V_{OL}	5 V tolerant output low voltage	–	0.55	V	16 mA
I_{OZ}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V
I_{PULL}	Pull-down current	7.5	75	µA	–

Table 7.11 Input Signals—CLK, GNT/, IDSEL, RST/, SCLK, TCK, TDI, TEST_HSC[1], TEST_RSTN, TMS

Symbol	Parameters	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	0.5 V_{DD}	5.0	V	–
V_{IL}	Input low voltage	V_{SS} –0.3	0.3 V_{DD}	V	–
I_{IN}	Input leakage[2]	–10	10	µA	V_{PIN} = 0 V, 5.25 V
I_{PULL}[3]	Pull-down current	–75	–7.5	µA	–

1. TEST_HSC has a pull-down
2. The Input leakage test does not apply to the TEST_RST/ pin with V_{PIN} = 0 V.
3. Pull-up spec does not apply to: SCLK, CLK, GNT/, IDSEL, and RST/.

Table 7.12 Output Signals—INTA, INTB

Symbol	Parameters	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	0.9 V_{DD}	–	V	–500 µA
V_{OL}	Output low voltage	–	0.1 V_{DD}	V	1500 µA
V_{OH}	5 V tolerant output high voltage	2.4	–	V	–16 mA
V_{OL}	5 V tolerant output low voltage	–	0.55	V	16 mA
I_{OZ}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V
I_{PULL}	Pull-down current	–75	–7.5	µA	–

Table 7.13 Output Signal—SERR/

Symbol	Parameters	Min	Max	Unit	Test Conditions
V_{OL}	Output low voltage	–	0.1 V_{DD}	V	1.5 mA
I_{OZ}	3-state leakage	–10	10	µA	–

7.2 TolerANT Technology Electrical Characteristics

The LSI53C1510 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation actively drives the SCSI Request, Acknowledge, Data, and Parity signals HIGH rather than allowing them to be passively pulled up by terminators. Table 7.14 provides electrical characteristics for SE SCSI signals. Figure 7.3 through Figure 7.7 provide reference information for testing SCSI signals.

Table 7.14 TolerANT Technology Electrical Characteristics for SE SCSI Signals[1]

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}[2]	Output high voltage	2.0	V_{DD}	V	I_{OH} = –7 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	2.0	V_{DD} +0.3	V	–
V_{IL}	Input low voltage	V_{SS} –0.3	0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	–0.66	–0.77	V	V_{DD} = 4.75; I_I = –20 mA
V_{TH}	Threshold, HIGH to LOW	1.0	1.2	V	–
V_{TL}	Threshold, LOW to HIGH	1.4	1.6	V	–
V_{TH}–V_{TL}	Hysteresis	300	500	mV	–
I_{OH}[2]	Output high current	2.5	24	mA	V_{OH} = 2.5 V
I_{OL}	Output low current	100	200	mA	V_{OL} = 0.5 V
I_{OSH}[2]	Short-circuit output high current	–	625	mA	Output driving low, pin shorted to V_{DD} supply[3]
I_{OSL}	Short-circuit output low current	–	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	–	20	µA	V_{DD} 5%, V_{PIN} = 2.7 V
I_{LL}	Input low leakage	–20	–	µA	V_{DD} 5%, V_{PIN} = 0 V
I_{PD}	Power down leakage	–	20	µA	V_{DD} = 0 V, V_{PIN} = 1.2 V
R_I	Input resistance	20	–	MΩ	SCSI pins[4]
C_P	Capacitance per pin	–	15	pF	388 BGA

Table 7.14 TolerANT Technology Electrical Characteristics for SE SCSI Signals[1]

Symbol	Parameter	Min	Max	Units	Test Conditions
t_R[2]	Rise time, 10% to 90%	4.0	18.5	ns	Figure 7.3
t_F	Fall time, 90% to 10%	4.0	18.5	ns	Figure 7.3
dV_H/dt	Slew rate LOW to HIGH	0.15	0.50	V/ns	Figure 7.3
dV_L/dt	Slew rate, HIGH to LOW	0.15	0.50	V/ns	Figure 7.3
ESD	Electrostatic discharge	2	–	kV	MIL-STD-883C; 3015-7
	Latch-up	100	–	mA	–
	Filter delay	20	30	ns	Figure 7.4
	Ultra filter delay	10	15	ns	Figure 7.4
	Ultra2 filter delay	5	8	ns	Figure 7.4
	Extended filter delay	40	60	ns	Figure 7.4

1. These values are guaranteed by periodic characterization; they are not 100% tested on every device.
2. Active negation outputs only: Data, Parity, SREQ/, SACK/.
3. Single pin only; irreversible damage may occur if sustained for one second.
4. SCSI RESET pin has 10 kΩ pull-up resistor.

Figure 7.3 Rise and Fall Time Test Condition

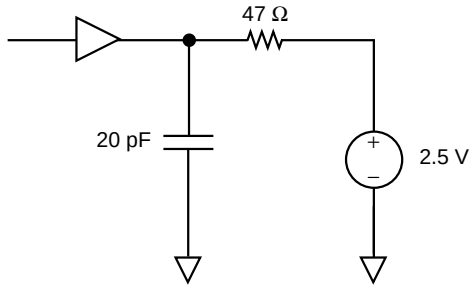
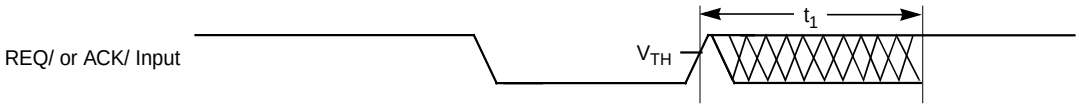


Figure 7.4 SCSI Input Filtering



Note: t_1 is the input filtering period.

Figure 7.5 Hysteresis of SCSI Receivers

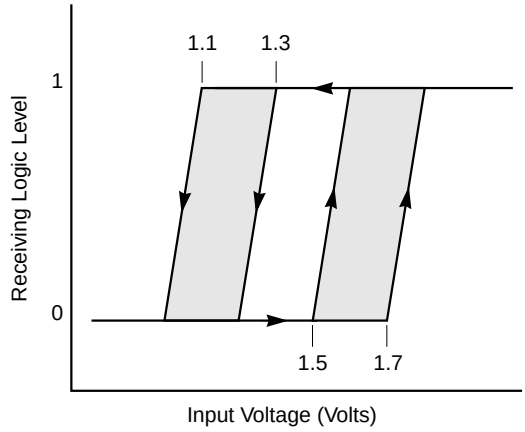


Figure 7.6 Input Current as a Function of Input Voltage

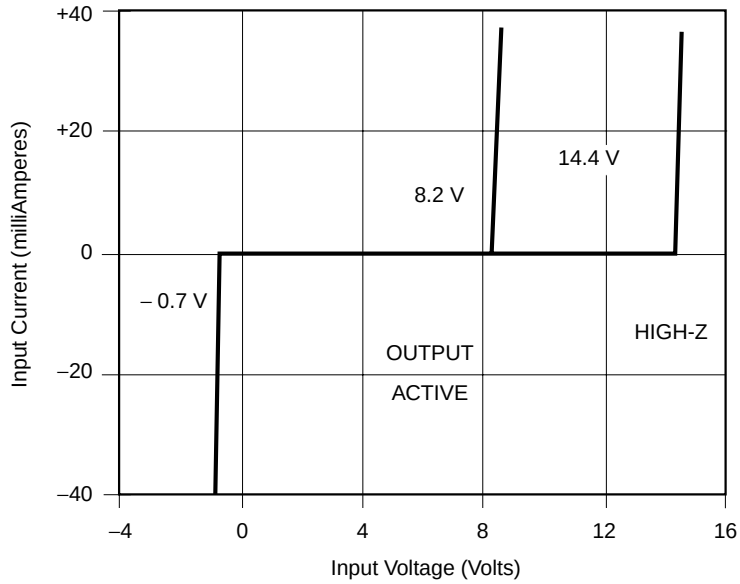
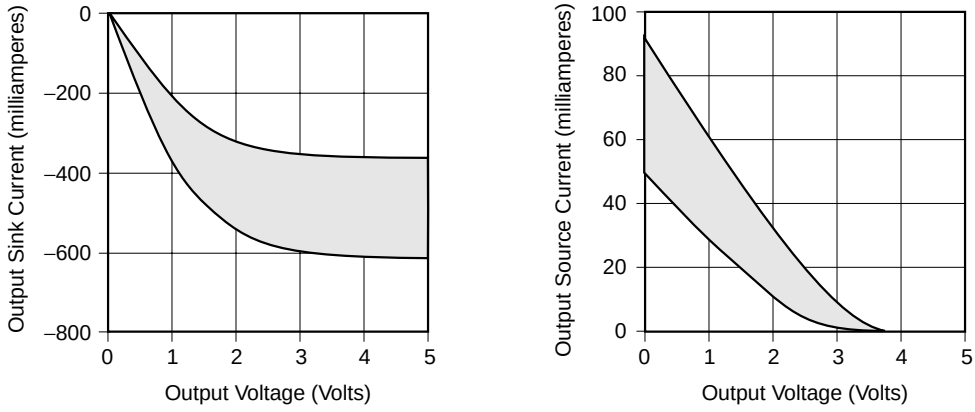


Figure 7.7 Output Current as a Function of Output Voltage



7.3 AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to the Section 7.1, “DC Characteristics”). Chip timing is based on simulation at worst case voltage, temperature, and processing. Timing was developed with a load capacitance of 50 pF Table 7.15 and Figure 7.8 provide External Clock data.

Table 7.15 External Clock[1]

Symbol	Parameter	Min	Max	Units
t_1	PCI bus clock cycle time	30	DC	ns
	SCSI clock cycle time (SCLK)[2]	25	60	ns
t_2	CLK LOW time[3]	12	–	ns
	SCLK LOW time[3]	10	36	ns
t_3	CLK HIGH time[3]	12	–	ns
	SCLK HIGH time[3]	10	36	ns
t_4	CLK slew rate	1	–	V/ns
	SCLK slew rate	1	–	V/ns

1. Timing is for an external 40 MHz clock. A quadrupled 40 MHz clock is required for Ultra2 SCSI operation.
2. This parameter must be met to ensure SCSI timing is within specification.
3. Duty cycle not to exceed 60/40.

Figure 7.8 External Clock

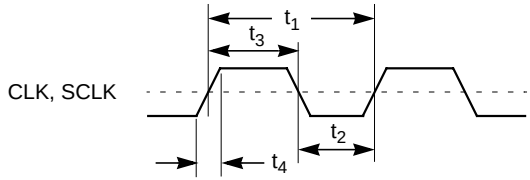


Table 7.16 and Figure 7.9 provide Reset Input data.

Table 7.16 Reset Input

Symbol	Parameter	Min	Max	Units
t_1	Reset pulse width	10	–	t_{CLK}
t_2	Reset deasserted setup to CLK HIGH	0	–	ns
t_3	MEM_ADDR setup time to CLK HIGH (for configuring the MEM_ADDR bus only)	20	–	ns
t_4	MEM_ADDR hold time from CLK HIGH (for configuring the MEM_ADDR bus only)	20	–	ns

Figure 7.9 Reset Input

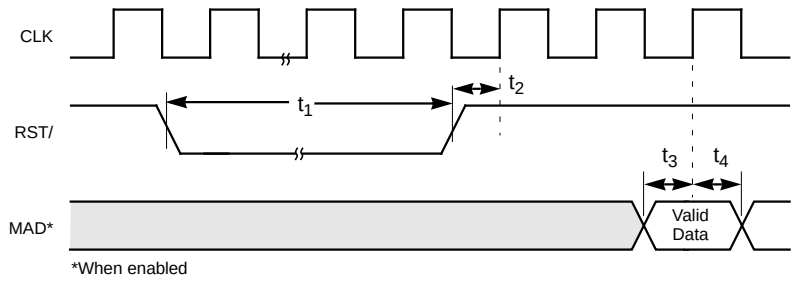
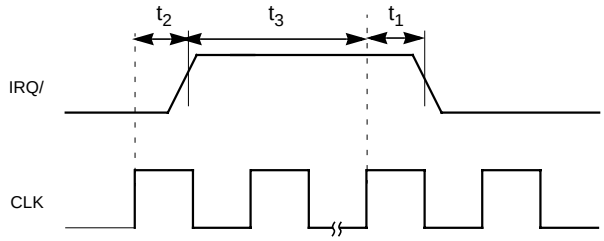


Table 7.17 and Figure 7.10 provide Interrupt Output data.

Table 7.17 Interrupt Output

Symbol	Parameter	Min	Max	Units
t_1	CLK HIGH to IRQ/ LOW	2	11	ns
t_2	CLK HIGH to IRQ/ HIGH	2	11	ns
t_3	IRQ/ deassertion time	3	–	CLK

Figure 7.10 Interrupt Output



7.4 PCI and External Memory Interface Timing Diagrams

Figure 7.11 through Figure 7.14 represent signal activity when the LSI53C1510 accesses the PCI bus. This section includes timing diagrams for access to four groups of memory configurations. The first group applies to Target Timing. The second group applies to Initiator Timing. The third group applies to External Memory Timing.

Note: Multiple byte accesses to the external memory bus increase the read or write cycle by 11 clocks for each additional byte.

Timing diagrams included in this section are:

- Target Timing
  - PCI Configuration Register Read
  - PCI Configuration Register Write
  - Operating Registers/SCRIPTS RAM Read, 32-Bit
  - Operating Registers/SCRIPTS RAM Write, 32-Bit
- Initiator Timing
  - Nonburst Opcode Fetch, 32-Bit Address and Data
  - Burst Opcode Fetch, 32-Bit Address and Data
  - Back-to-Back Read, 32-Bit Address and Data
  - Back-to-Back Write, 32-Bit Address and Data
  - Burst Read, 32-Bit Address and Data
  - Burst Write, 32-Bit Address and Data
- External Memory Timing
  - EDO DRAM Burst Read
  - FLASH ROM Normal Read Only Mode
  - FLASH ROM Program/Verify Mode

7.4.1 Target Timing

Table 7.18 through Table 7.21 and Figure 7.11 through Figure 7.14 describe Target timing.

Table 7.18 PCI Configuration Register Read

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns

Figure 7.11 PCI Configuration Register Read

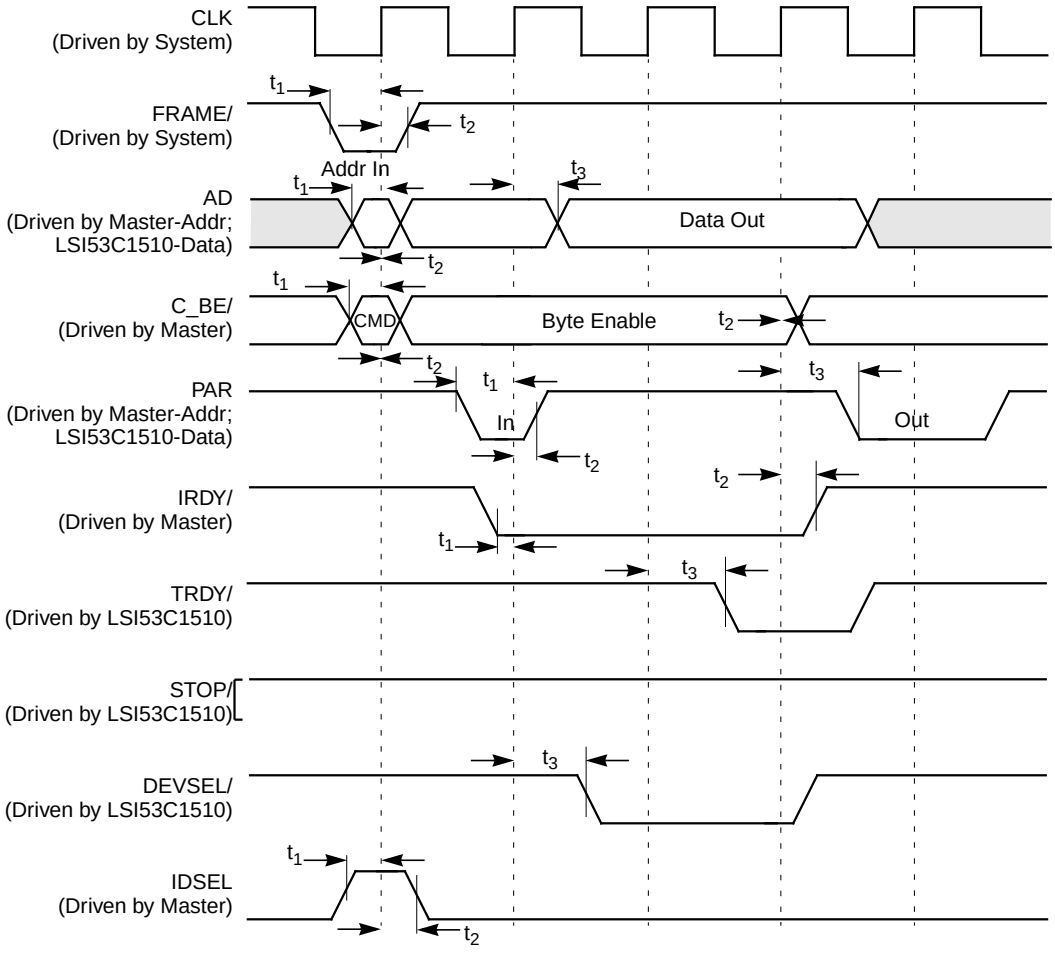


Table 7.19 PCI Configuration Register Write

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns

Figure 7.12 PCI Configuration Register Write

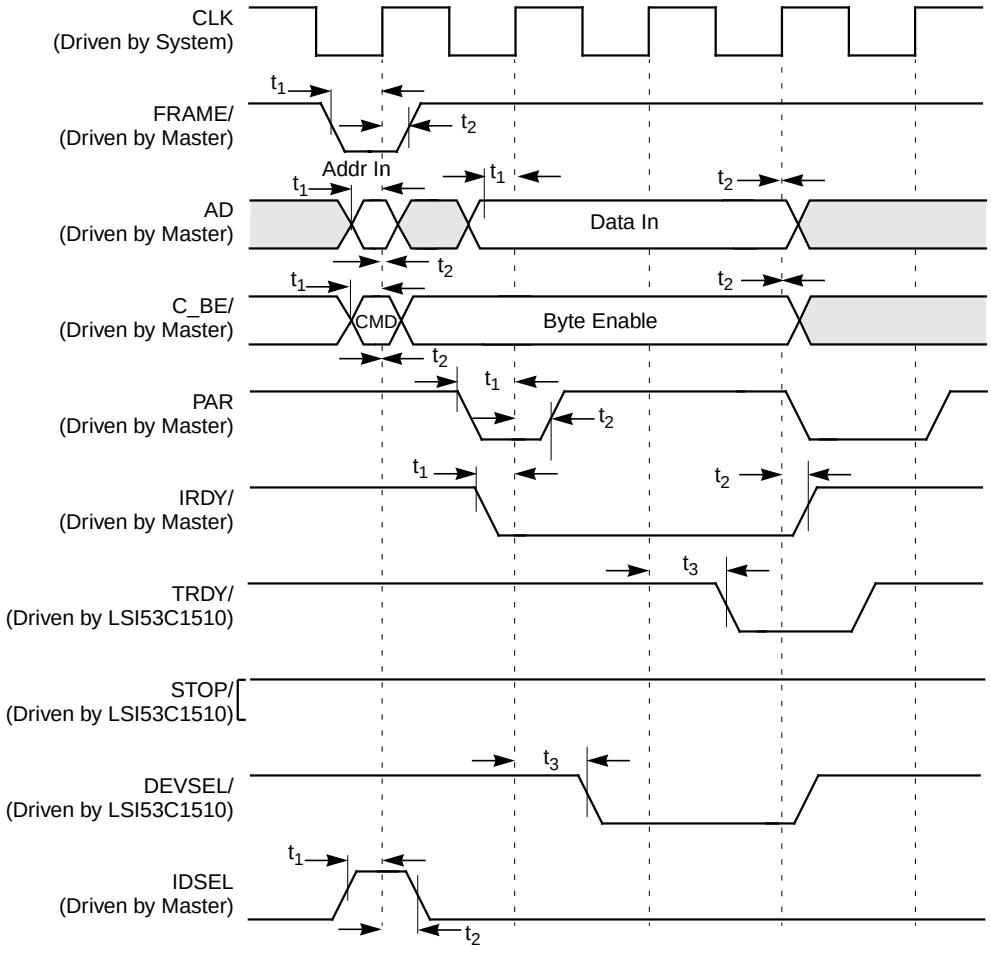


Table 7.20 Operating Registers/SCRIPTS RAM Read, 32-Bit

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns

Figure 7.13 Operating Registers/SCRIPTS RAM Read, 32-Bit

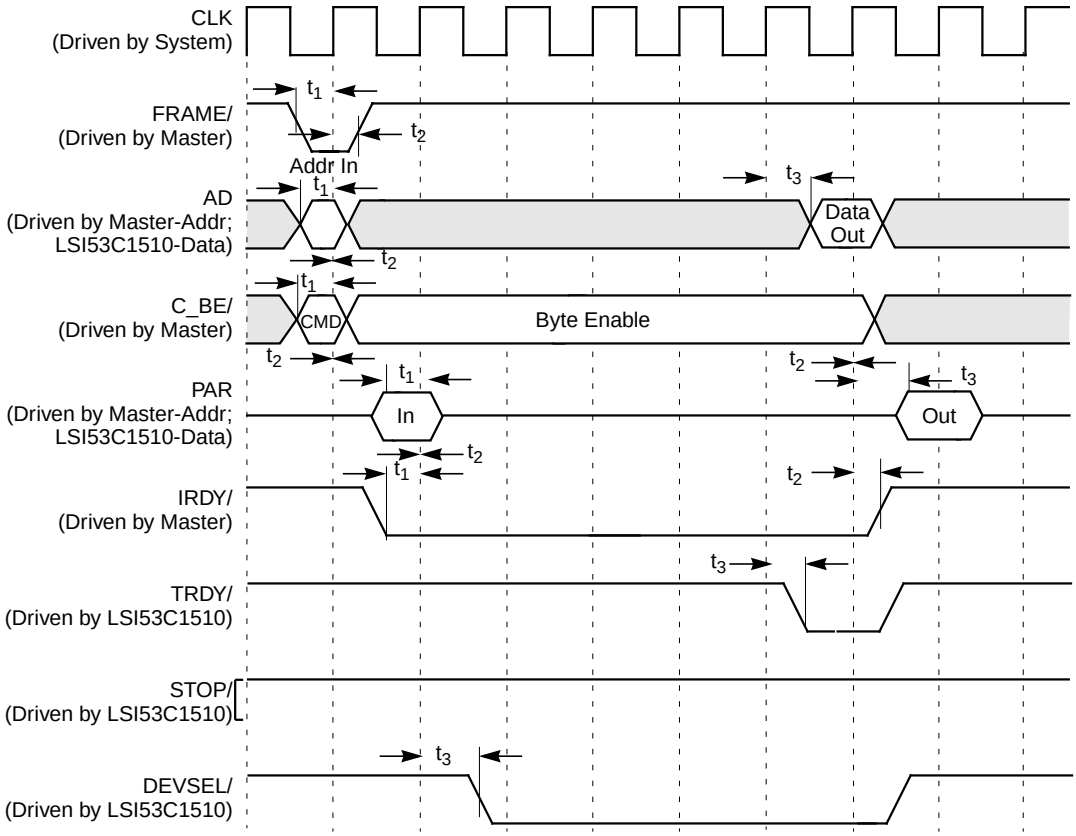
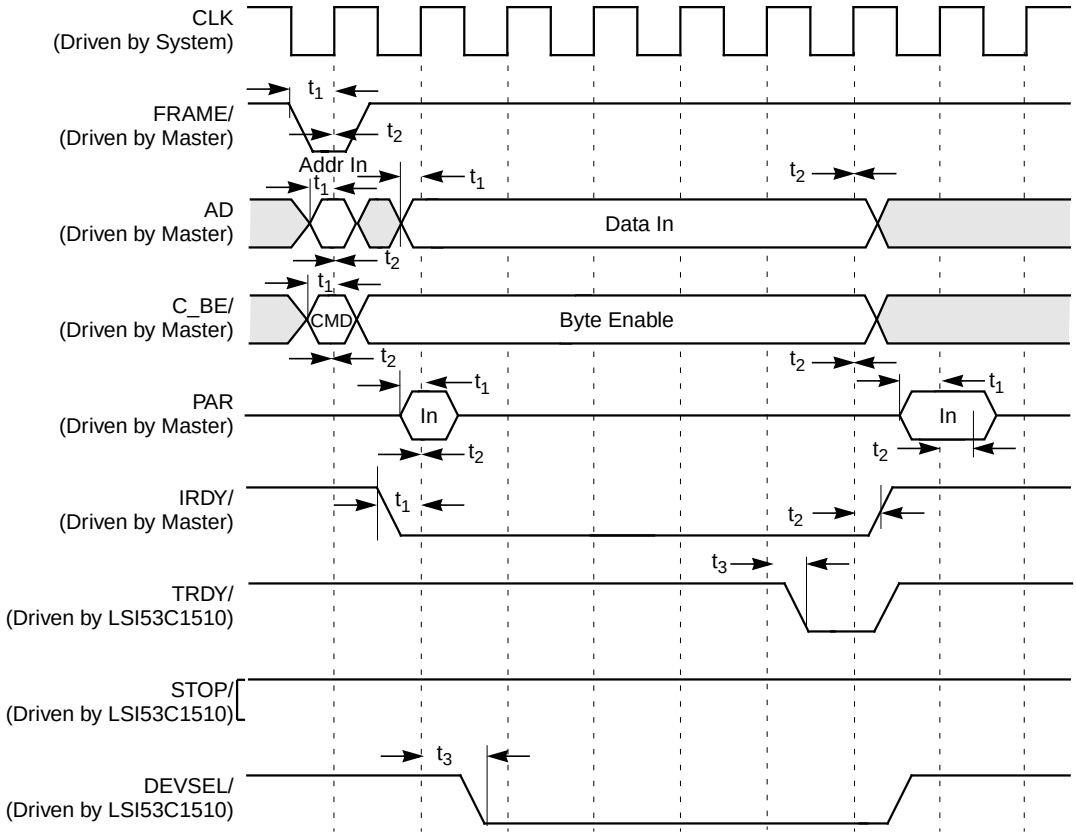


Table 7.21 Operating Registers/SCRIPTS RAM Write, 32-Bit

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns

Figure 7.14 Operating Registers/SCRIPTS RAM Write, 32-Bit



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7.4.2 Initiator Timing

Table 7.22 through Table 7.27 and Figure 7.15 through Figure 7.20 describe Initiator timing.

Table 7.22 Nonburst Opcode Fetch, 32-Bit Address and Data

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	–	ns
t_5	Side signal input hold time	0	–	ns
t_6	CLK to side signal output valid	–	12	ns

Figure 7.15 Nonburst Opcode Fetch, 32-Bit Address and Data

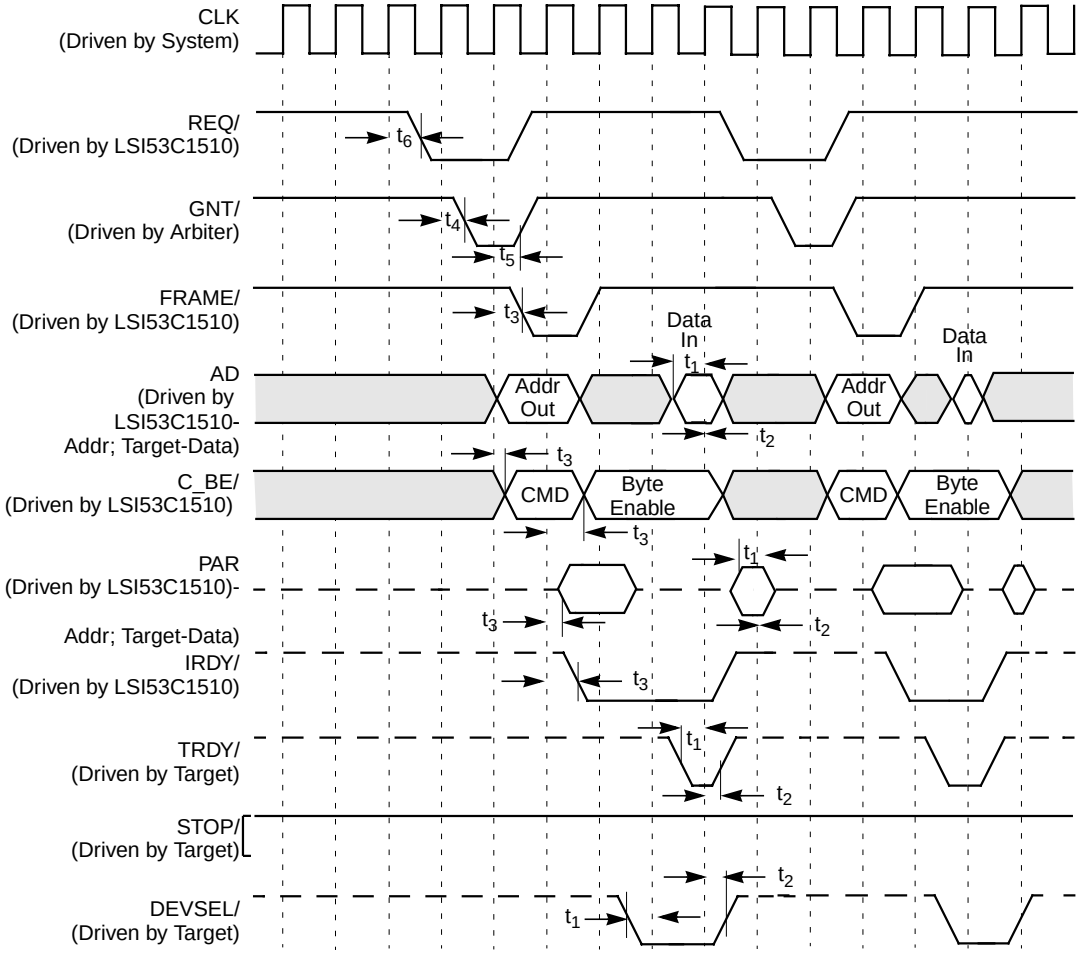


Table 7.23 Burst Opcode Fetch, 32-Bit Address and Data

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	–	ns
t_5	Side signal input hold time	0	–	ns
t_6	CLK to side signal output valid	–	12	ns

Figure 7.16 Burst Opcode Fetch, 32-Bit Address and Data

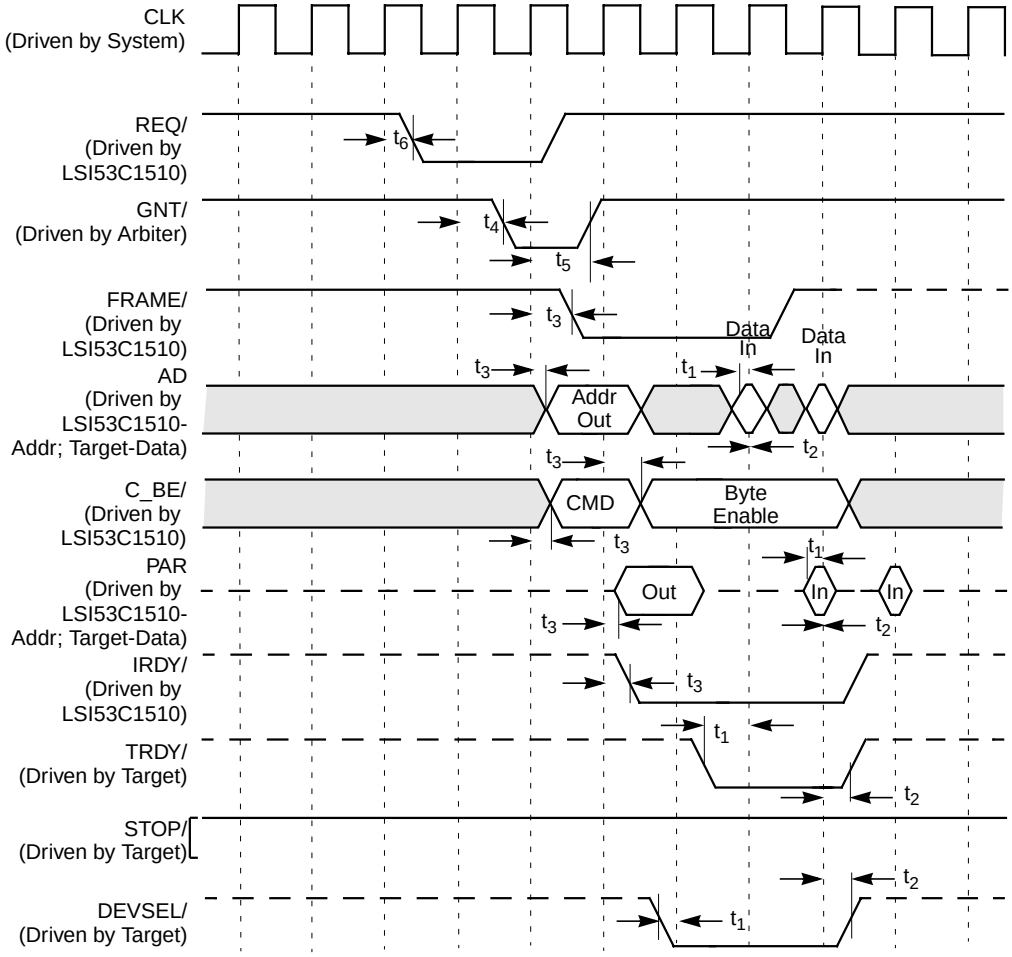


Table 7.24 Back-to-Back Read, 32-Bit Address and Data

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	–	ns
t_5	Side signal input hold time	0	–	ns
t_6	CLK to side signal output valid	–	12	ns

Figure 7.17 Back-to-Back Read, 32-Bit Address and Data

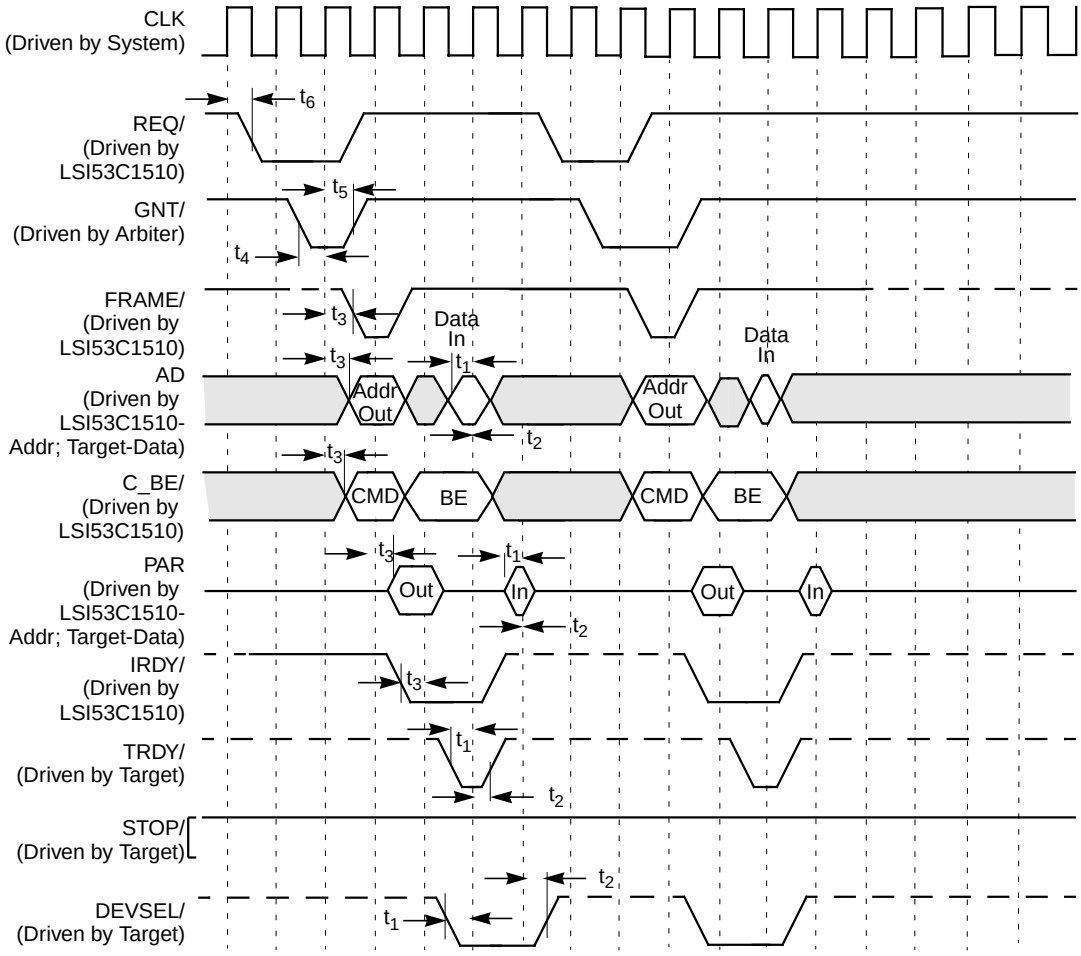


Table 7.25 Back-to-Back Write, 32-Bit Address and Data

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	–	ns
t_5	Side signal input hold time	0	–	ns
t_6	CLK to side signal output valid	–	12	ns

Figure 7.18 Back-to-Back Write, 32-Bit Address and Data

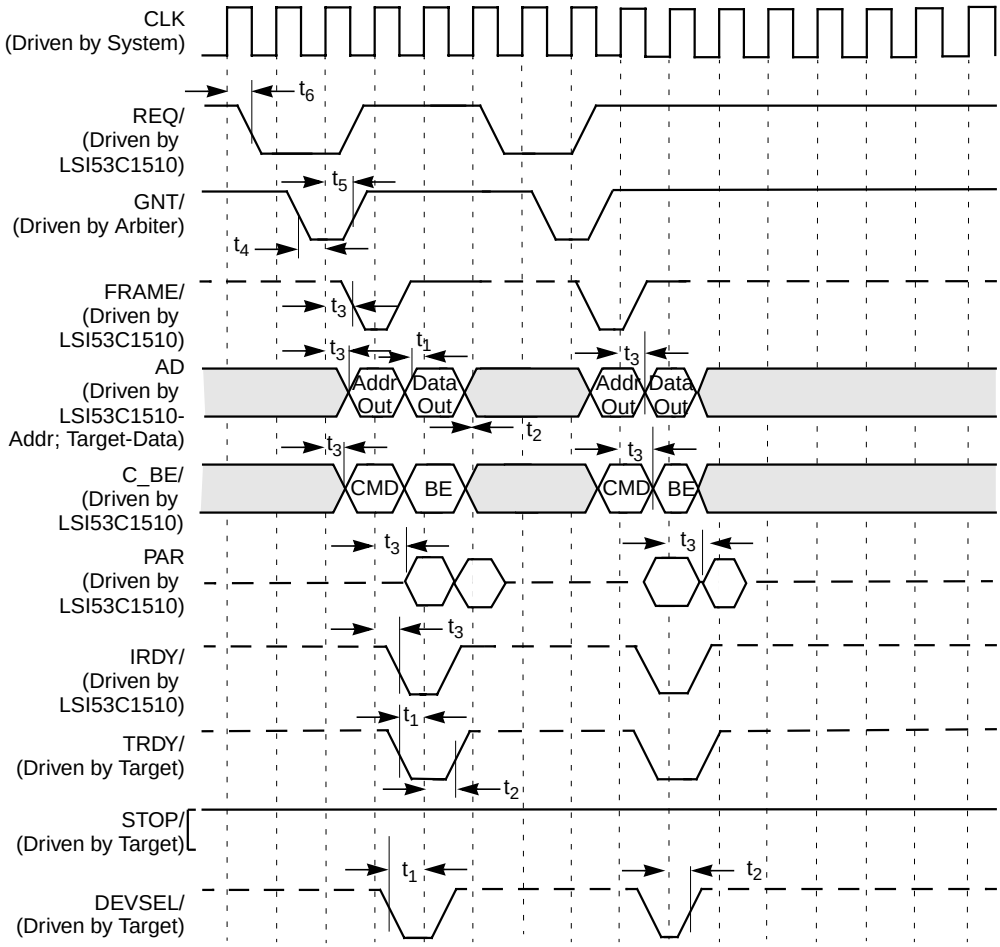


Table 7.26 Burst Read, 32-Bit Address and Data

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns

Figure 7.19 Burst Read, 32-Bit Address and Data

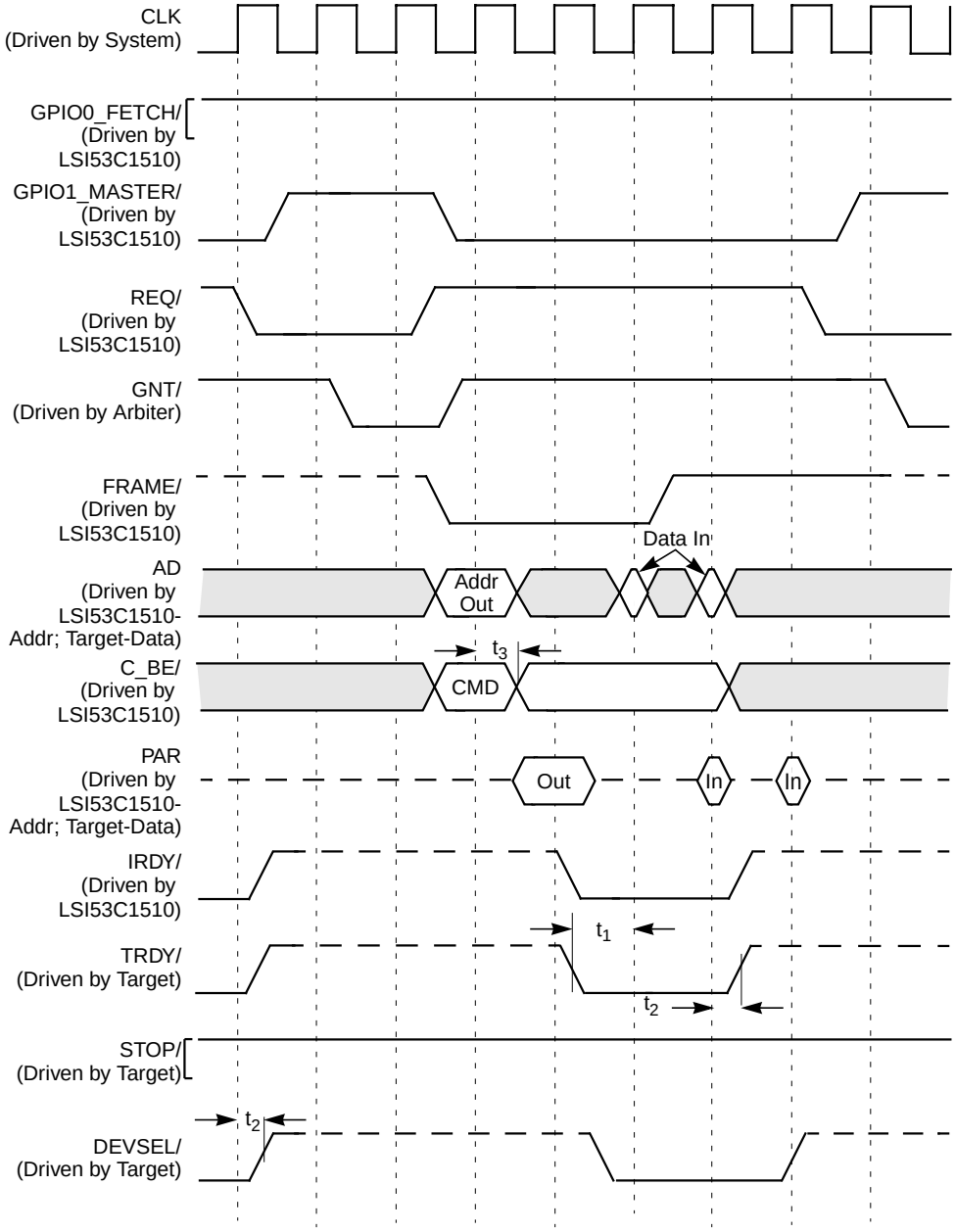
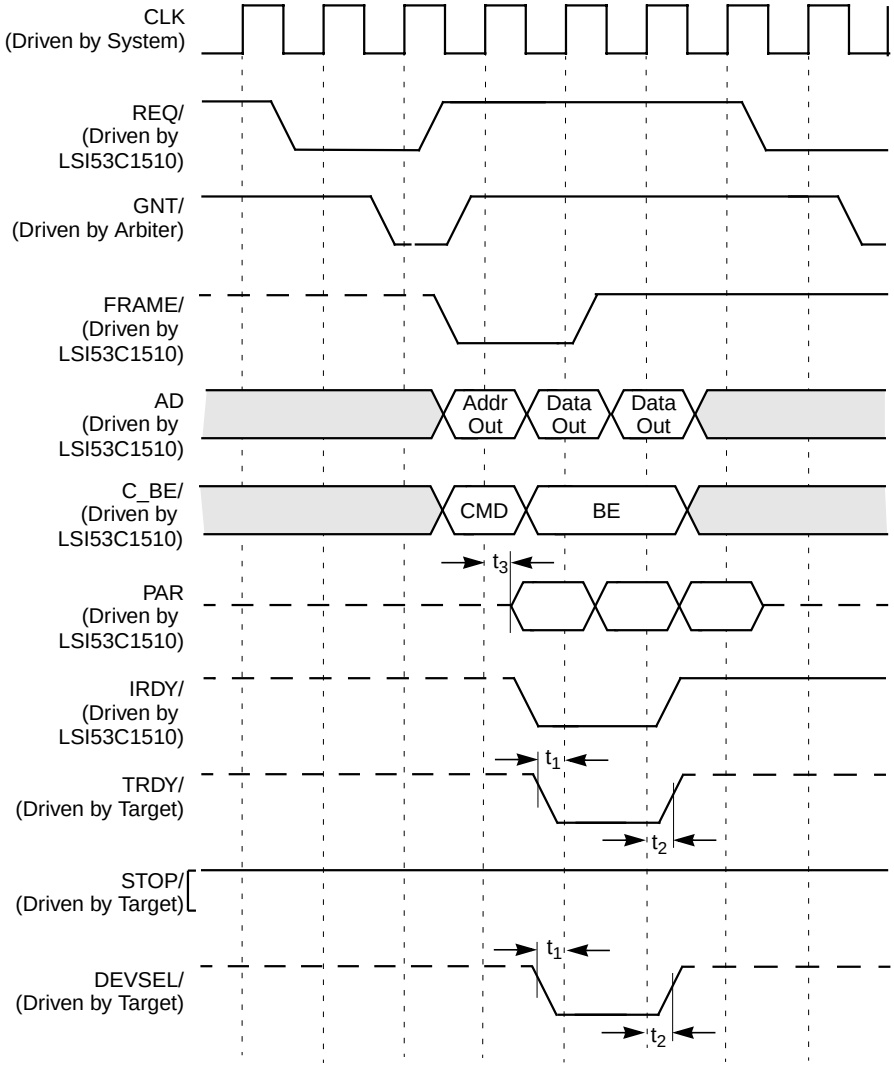


Table 7.27 Burst Write, 32-Bit Address and Data

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	–	ns
t_2	Shared signal input hold time	0	–	ns
t_3	CLK to shared signal output valid	2	11	ns

Figure 7.20 Burst Write, 32-Bit Address and Data



7.4.3 External Memory Timing

Table 7.28 and Figure 7.21 through Figure 7.23 describe DRAM timing parameters.

Table 7.28 DRAM Timing Parameters (Using 50 ns Extended Data Out Mode)

Symbol	Parameter	Min	Max	Unit
Taa	Access from column address	25	–	ns
Tasc	Common address setup	0	–	ns
Tasr	Row address setup	0	–	ns
Tcac	Access time from CAS/	–	15	ns
Tcah	Column address hold	8	–	ns
Tcas	CAS/ LOW	10	10,000	ns
Tcp	CAS/ precharge	8	–	ns
Tcpa	Access time from CAS/ HIGH	30	–	ns
Tcrp	CAS/ to RAS/ precharge	5	–	ns
Tcsh	RAS/ LOW to CAS/ HIGH	40	–	ns
Tdh	DRAM data in hold	8	–	ns
Tds	DRAM data in setup	0	–	ns
Tpc	EDO page cycle time	25	–	ns
Trac	Access time for RAS/	–	50	ns
Trad	RAS/ to column address	9	25	ns
Trah	Row address hold	9	–	ns
Tral	Column address lead time to rising RAS/	25	–	ns
Trasp	RAS/ LOW, EDO fast page mode	50	100,000	ns
Trc	Random access cycle time	90	–	ns
Trcd	RAS/ to CAS/ delay	11	35	ns
Trp	RAS/ precharge	30	–	ns
Trsh	RAS/ hold time (CAS/ LOW to RAS/ HIGH)	13	–	ns

Figure 7.21 EDO DRAM Burst Read

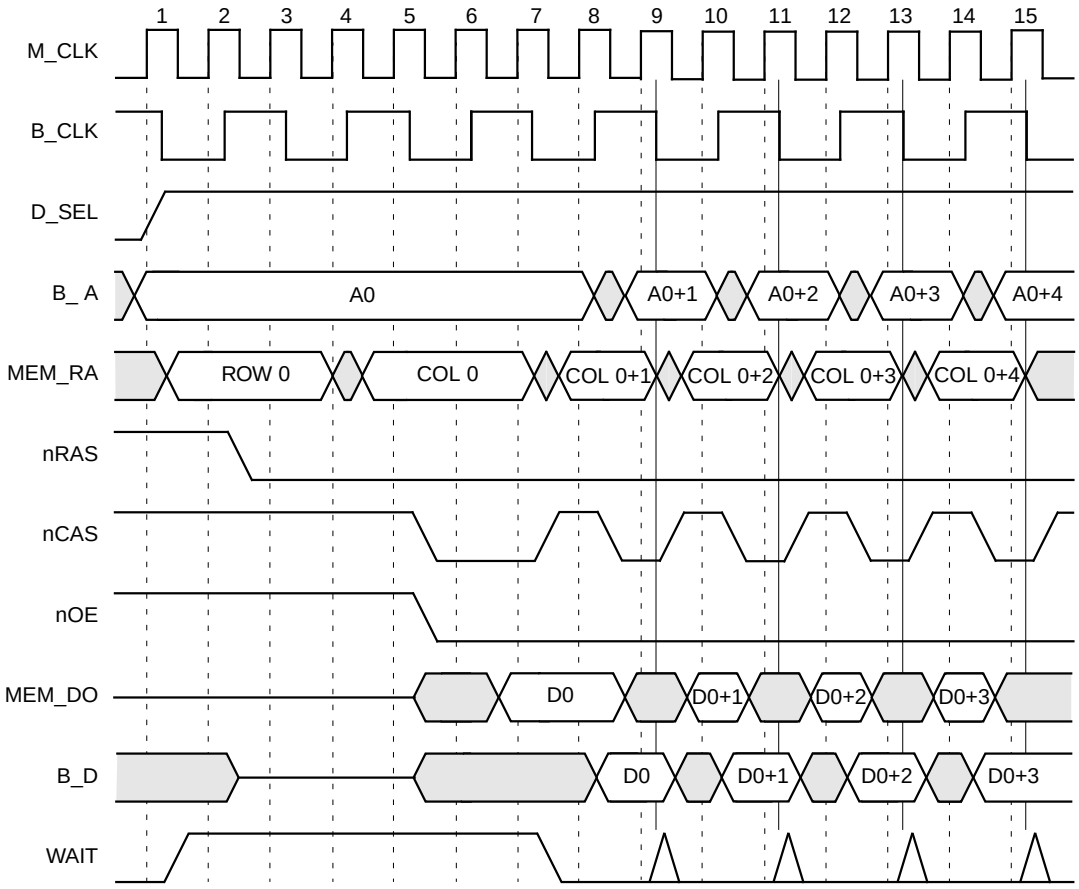


Figure 7.22 FLASH ROM Normal Read Only Mode

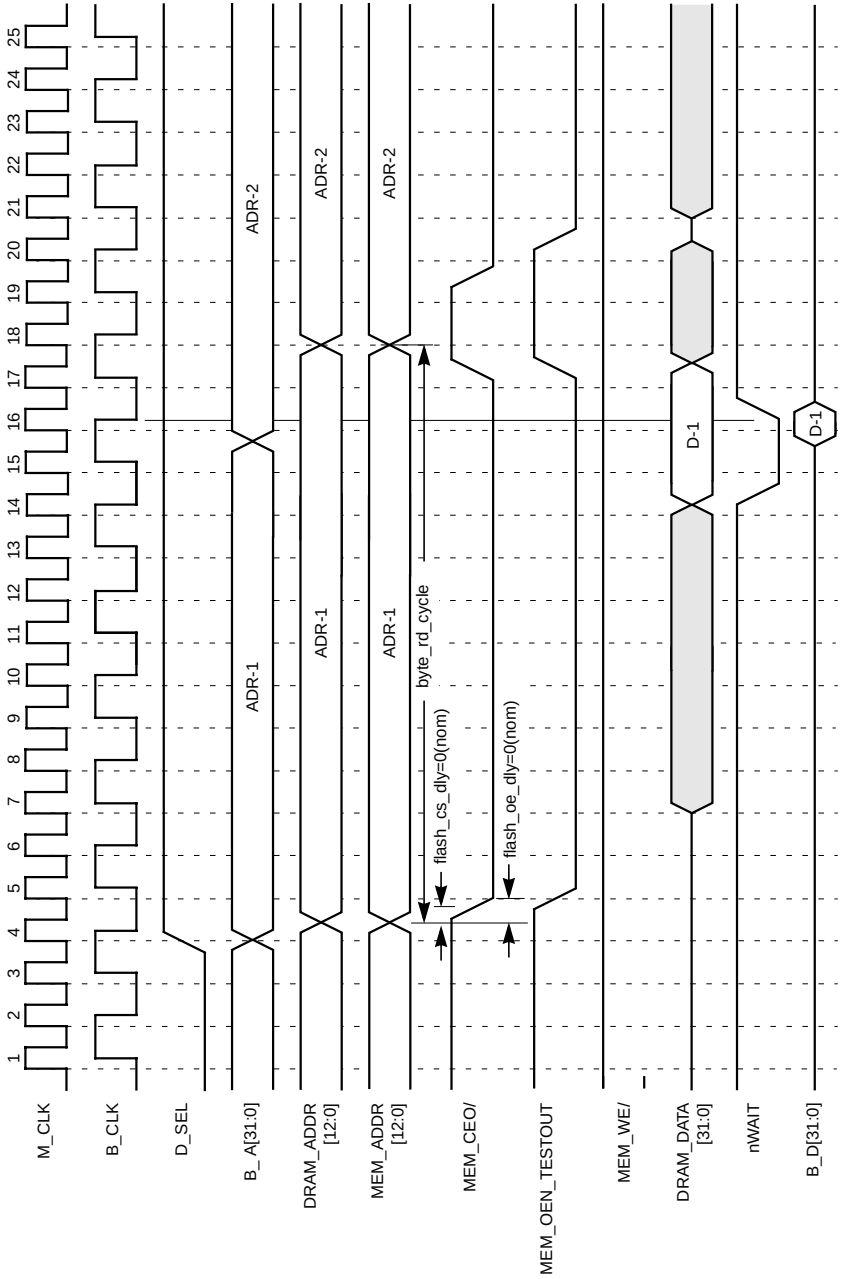
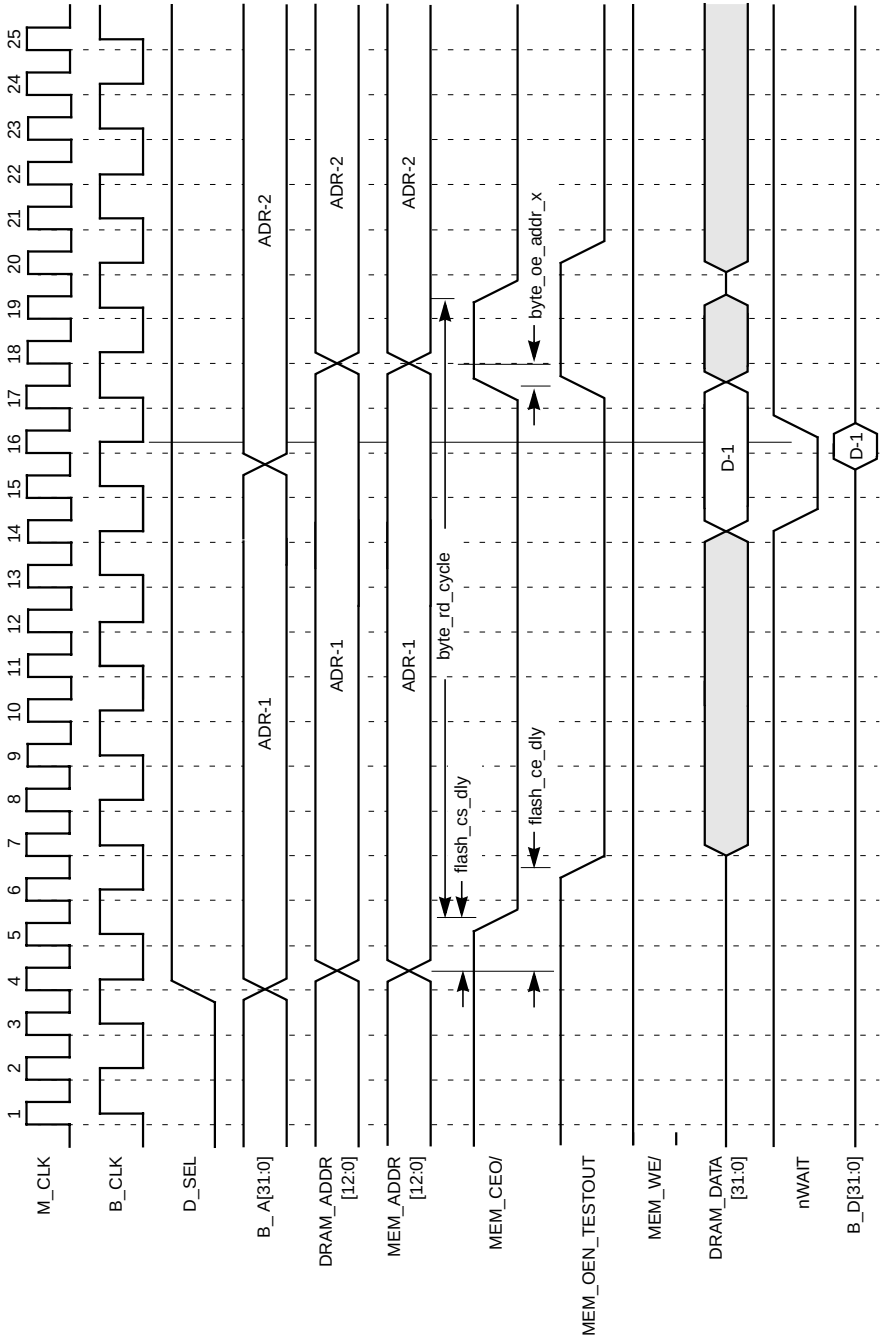


Figure 7.23 FLASH ROM Program/Verify Mode



7.5 SCSI Timing Diagrams

Table 7.29 through Table 7.39 and Figure 7.24 through Figure 7.28 describe SCSI timing data.

Table 7.29 Initiator Asynchronous Send

Symbol	Parameter	Min	Max	Units
t_1	SACK/ asserted from SREQ/ asserted	5	–	ns
t_2	SACK/ deasserted from SREQ/ deasserted	5	–	ns
t_3	Data setup to SACK/ asserted	55	–	ns
t_4	Data hold from SREQ/ deasserted	20	–	ns

Figure 7.24 Initiator Asynchronous Send

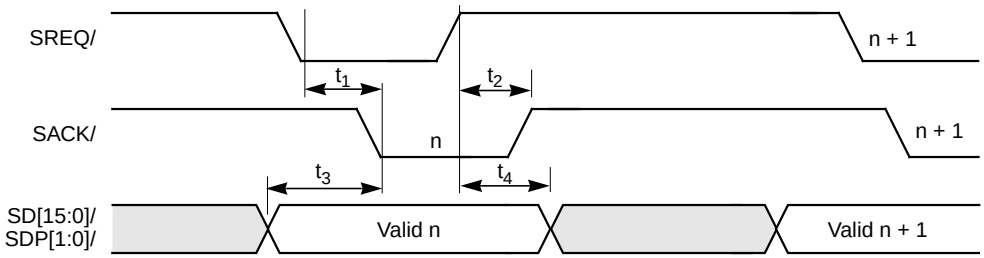


Table 7.30 Initiator Asynchronous Receive

Symbol	Parameter	Min	Max	Units
t_1	SACK/ asserted from SREQ/ asserted	5	–	ns
t_2	SACK/ deasserted from SREQ/ deasserted	5	–	ns
t_3	Data setup to SREQ/ asserted	0	–	ns
t_4	Data hold from SACK/ asserted	0	–	ns

Figure 7.25 Initiator Asynchronous Receive

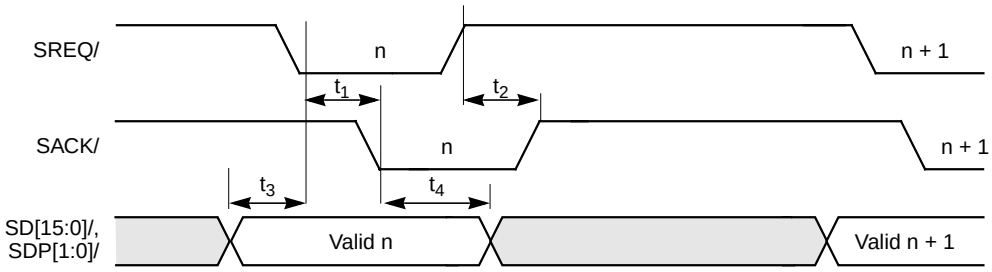


Table 7.31 Target Asynchronous Send

Symbol	Parameter	Min	Max	Units
t_1	SREQ/ deasserted from SACK/ asserted	5	–	ns
t_2	SREQ/ asserted from SACK/ deasserted	5	–	ns
t_3	Data setup to SREQ/ asserted	55	–	ns
t_4	Data hold from SACK/ asserted	20	–	ns

Figure 7.26 Target Asynchronous Send

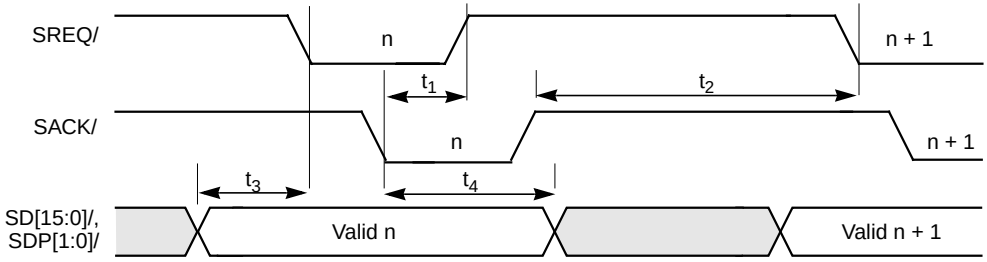


Table 7.32 Target Asynchronous Receive

Symbol	Parameter	Min	Max	Units
t_1	SREQ/ deasserted from SACK/ asserted	5	–	ns
t_2	SREQ/ asserted from SACK/ deasserted	5	–	ns
t_3	Data setup to SACK/ asserted	0	–	ns
t_4	Data hold from SREQ/ deasserted	0	–	ns

Figure 7.27 Target Asynchronous Receive

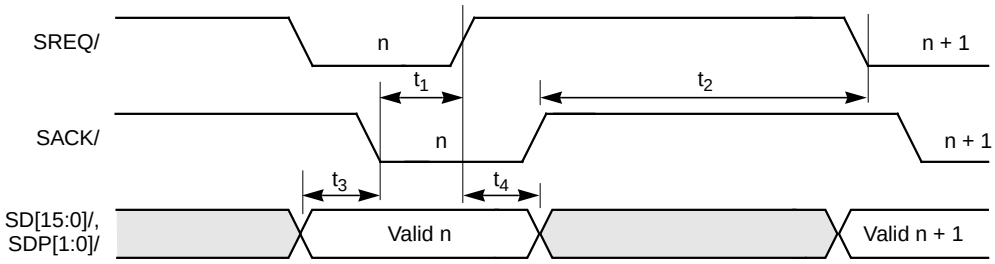


Table 7.33 SCSI-1 Transfers (SE 5.0 Mbytes)

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	90	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	90	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	90	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	90	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	55	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	100	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	45	–	ns

Table 7.34 SCSI-1 Transfers (Differential 4.17 Mbytes)

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	96	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	96	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	84	–	ns
t_2	Receive SREQ/ or SACK/deassertion pulse width	84	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	65	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	110	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	45	–	ns

Table 7.35 SCSI-2 Fast Transfers 10.0 Mbytes (8-Bit transfers) or 20.0 Mbytes (16-Bit transfers) 40 MHz Clock

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	35	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	35	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	20	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	20	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	33	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	45	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	10	–	ns

Table 7.36 SCSI-2 Fast Transfers 10.0 Mbytes (8-Bit Transfers) or 20.0 Mbytes (16-Bit Transfers) 50 MHz Clock[1]

Symbol	Parameter[2]	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	35	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	35	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	20	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	20	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	33	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	40[3]	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	10	–	ns

1. Transfer period bits (bits [6:4] in the SXFER register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCNTL1) is set.
2. Note: for fast SCSI, set the TolerANT Enable bit (bit 7 in STEST3).
3. Analysis of system configuration is recommended due to reduced driver skew margin in differential systems.

Table 7.37 Ultra SCSI SE Transfers 20.0 Mbytes (8-Bit Transfers) or 40.0 Mbytes (16-Bit Transfers) Quadrupled 40 MHz Clock[1]

Symbol	Parameter[2]	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	16	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	16	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	10	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	10	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	12	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	17	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	6	–	ns

1. Transfer period bits (bits [6:4] in the SXFER register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCNTL1) is set.
2. Note: for fast SCSI, set the TolerANT Enable bit (bit 7 in STEST3). During Ultra SCSI transfers, the value of the Extend REQ/ACK Filtering bit (STEST2, bit 1) has no effect.

Table 7.38 Ultra SCSI HVD Transfers 20.0 Mbytes (8-Bit Transfers) or 40.0 Mbytes (16-Bit Transfers) 80 MHz Clock[1]

Symbol	Parameter[2]	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	16	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	16	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	10	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	10	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	16	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	21	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	6	–	ns

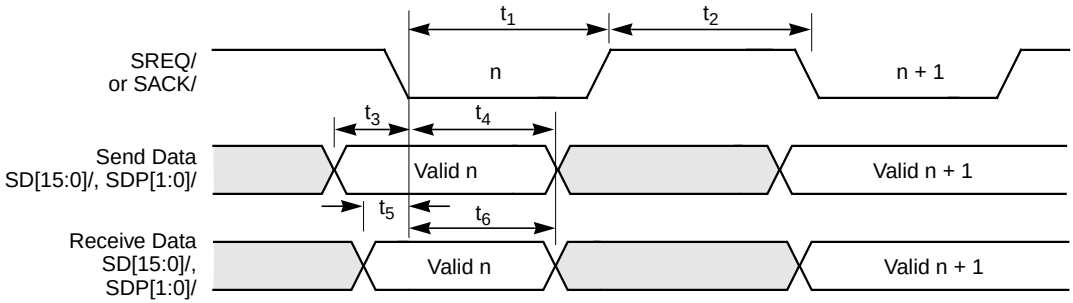
1. Transfer period bits (bits [6:4] in the SXFER register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCNTL1) is set.
2. During Ultra SCSI transfers, the value of the Extend REQ/ACK Filtering bit (STEST2, bit 1) has no effect.

Table 7.39 Ultra2 SCSI Transfers 40.0 Mbytes (8-Bit Transfers) or 80.0 Mbytes (16-Bit Transfers) Quadrupled 40 MHz Clock[1]

Symbol	Parameter[2]	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	8	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	8	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	6.5	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	6.5	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	9.5	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	9.5	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	3.5	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	3.5	–	ns

1. Transfer period bits (bits [7:5] in the SXFER register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCNTL1) is set.
2. During Ultra2 SCSI transfers, the value of the Extend REQ/ACK Filtering bit (STEST2, bit 1) has no effect.

Figure 7.28 Initiator and Target Synchronous Transfer



7.6 Pinouts and Packaging

Figure 7.29 is pinout information for the LSI53C1510 388 BGA chip package. Table 7.40 provides the 388 BGA pin list by location and Table 7.41 provides the same pin list alphabetically. Figure 7.30 illustrates the signal locations on the LSI53C1510 388 BGA. Figure 7.31 is the package drawing for the LSI53C1510.

Figure 7.29 Left Half of the LSI53C1510 388 BGA Chip - Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	V_{SS}	V_{SS}	DRAM_ ADD1	DRAM_OE/	DRAM_ CASFB_A	V_{DD}CORE3	DRAM_ CAS5/	DRAM_ CAS3/	DRAM_ RAS1/	DRAM_ PAR2	DRAM_ DATA0	DRAM_ DATA17	DRAM_ DATA3	A
B	DRAM_ ADD5	V_{SS}	DRAM_ ADD3	DRAM_WE/	DRAM_ RAS2/	DRAM_ CAS0/	DRAM_ CAS2/	DRAM_ RAS0/	V_{SS}CORE3	DRAM_ PAR1	DRAM_ DATA1	DRAM_ DATA18	DRAM_ DATA6	B
C	DRAM_ ADD8	DRAM_ ADD7	V_{SS}	DRAM_ ADD4	DRAM_ ADD2	DRAM_ RAS3/	DRAM_ CASFB_B	DRAM_ CAS1/	DRAM_ CAS7/	DRAM_ PAR0	DRAM_ DATA16	DRAM_ DATA2	DRAM_ DATA4	C
D	DRAM_ ADD11	DRAM_ ADD10	DRAM_ ADD6	V_{SS}	DRAM_ ADD0	V_{DD}	DRAM_ CAS4/	DRAM_ CAS6/	V_{SS}	DRAM_ PAR3	V_{DD}	DRAM_ DATA19	DRAM_ DATA20	D
E	MEM_ ADD0	TEST_ DRAMCLK	DRAM_ ADD12	DRAM_ ADD9										E
F	MEM_ ADD3	MEM_ ADD2	MEM_ ADD4	V_{DD}										F
G	MEM_ ADD6	MEM_ ADD5	MEM_ ADD7	MEM_ ADD1										G
H	MEM_ ADD9	MEM_ ADD8	MEM_ ADD10	V_{DD}CORE4										H
J	MEM_ ADD11	MEM_ ADD12	MO3/ TESTOUT	V_{SS}										J
K	MEM_CE0/	MEM_CE1/	MEM_CE2/	MCE2_RD/										K
L	V_{SS}CORE4	MCE2_WR/	MEM_ DATA0	V_{DD}							V_{SS}	V_{SS}	V_{SS}	L
M	MEM_WE/	MEM_ DATA1	MEM_ DATA4	MEM_ DATA6							V_{SS}	V_{SS}	V_{SS}	M
N	MEM_ DATA2	MEM_ DATA3	MEM_ DATA7	V_{SS}							V_{SS}	V_{SS}	V_{SS}	N
P	SCAN_ TRI_E/	MEM_ DATA5	SCAN_ RAM_E/	TESTIN							V_{SS}	V_{SS}	V_{SS}	P
R	SCANMODE	SCAN_ RST_E/	SCAN_E/	SCAN_TEST _CLK_E/							V_{SS}	V_{SS}	V_{SS}	R
T	PME	NC	POWER_ FAIL	V_{DD}							V_{SS}	V_{SS}	V_{SS}	T
U	B_GPIO1	B_GPIO0	B_GPIO2	V_{SS}CORE5										U
V	B_GPIO3	V_{DD}CORE5	B_SD11+/	V_{SS}										V
W	B_SD11–/	B_GPIO4	B_SD9–/	B_SD10+/										W
Y	B_SD9+/	B_SD10–/	B_SI_O–/	B_SD8+/										Y
AA	B_SD8–/	B_SI_O+/	B_SC_D+/	V_{DD}										AA
AB	B_SREQ+/	B_SREQ–/	B_SMSG–/	B_SSEL–/										AB
AC	B_SC_D–/	B_SSEL+/	B_SRST–/	V_{SS}	B_SATN+/	V_{DD}	B_SD7+/	B_SD3–/	V_{SS}	B_SD15+/	V_{DD}	B_DIFFSENS	V_{SS}	AC
AD	B_SMSG+/	B_SRST+/	V_{SS}	B_SACK–/	B_RBIAS-	B_SD6–/	B_SD4+/	B_SD2+/	B_SD1–/	B_SDP1+/	B_SD14–/	B_SD12–/	SCLK	AD
AE	V_{SS}	V_{SS}	B_SBSY+/	B_SATN–/	B_SDP0+/	B_SD7–/	B_SD5+/	B_SD4–/	B_SD1+/	B_SD0–/	B_SD15–/	B_SD13+/	B_SD12+/	AE
AF	V_{SS}	B_SACK+/	B_SBSY–/	B_RBIAS+	B_SDP0-/	B_SD6+/	B_SD5–/	B_SD3+/	B_SD2–/	B_SD0+/	B_SDP1–/	B_SD14+/	B_SD13–/	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 7.29 Right Half of the LSI53C1510 388 BGA Chip - Top View (Cont.)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	DRAM_DATA23/	DRAM_DATA9/	DRAM_DATA26/	DRAM_DATA12/	DRAM_DATA29/	DRAM_DATA15/	PCI_AD0	PCI_AD3	PCI_AD6	C_BE0	PCI_AD10	PCI_AD13	V_{SS}	A
B	DRAM_DATA7/	DRAM_DATA8/	DRAM_DATA25/	DRAM_DATA27/	DRAM_DATA13/	DRAM_DATA31/	PCI_AD1	PCI_AD4	PCI_AD7	PCI_AD8	PCI_AD11	V_{SS}	V_{SS}	B
C	DRAM_DATA5/	DRAM_DATA22/	DRAM_DATA24/	DRAM_DATA11/	DRAM_DATA28/	DRAM_DATA14/	V_{DD}CORE2	PCI_AD2	V_{SS}CORE2	PCI_AD12	V_{SS}	PCI_AD15	PAR	C
D	V_{SS}	DRAM_DATA21/	V_{DD}	DRAM_DATA10/	V_{SS}	DRAM_DATA30/	PCI_AD5	V_{DD}	PCI_AD9	V_{SS}	PCI_AD14	PEER/	STOP/	D
E										SERR/	C_BE1	TRDY/	IRDY/	E
F										V_{DD}	DEVSEL/	CLK	V_{SS}CORE1	F
G										C_BE2	FRAME/	PCI_AD18	PCI_AD17	G
H										PCI_AD19	PCI_AD16	PCI_AD22	PCI_AD20	H
J										V_{SS}	PCI_AD21	PCI_AD23	V_{DD}CORE1	J
K										PCI_AD25	IDSEL	PCI_AD24	C_BE3	K
L	V_{SS}	V_{SS}	V_{SS}							V_{DD}	PCI_AD27	PCI_AD28	PCI_AD26	L
M	V_{SS}	V_{SS}	V_{SS}							GNT/	PCI_AD30	PCI_AD31	PCI_AD29	M
N	V_{SS}	V_{SS}	V_{SS}							INTB	RST/	XINT	REQ/	N
P	V_{SS}	V_{SS}	V_{SS}							V_{SS}	INTA	RXT	TDO	P
R	V_{SS}	V_{SS}	V_{SS}							V_{SS}CORE0	TXT	TRST	TDI	R
T	V_{SS}	V_{SS}	V_{SS}							V_{DD}	TMS	TCK	ARM_TRST/	T
U										ARM_TMS	ARM_TDO	V_{DD}CORE0	A_GPIO0	U
V										V_{SS}	A_GPIO1	A_GPIO2	A_GPIO3	V
W										A_SD12+/	A_GPIO4	A_SD13+/	A_SD12–/	W
Y										A_SDP1–/	A_SD13–/	A_SD14–/	A_SD14+/	Y
AA										V_{DD}	A_SD15+/	A_SDP1+/	A_SD15–/	AA
AB										A_SD2–/	A_SD1+/	A_SD0–/	A_SD0+/	AB
AC	TEST_HSC	V_{DD}_A	V_{DD}	A_SD8+/	V_{SS}	A_SMSG–/	A_SACK–/	V_{DD}	A_SD7+/	V_{SS}	A_SD4+/	A_SD2+/	A_SD1–/	AC
AD	A_DIFFSENS	A_SD10–/	A_SD9+/	A_SREQ–/	A_SSEL–/	A_SRST+/	A_SBSY+/	A_SDP0–/	A_SD6+/	A_SD5+/	V_{SS}	A_SD3–/	A_SD3+/	AD
AE	V_{SS}_A	A_SD11+/	A_SD9–/	A_SI_O–/	A_SREQ+/	A_SC_D+/	A_SMSG+/	A_SBSY–/	A_SATN+/	A_SD7–/	A_SD5–/	V_{SS}	A_SD4–/	AE
AF	A_SD11–/	A_SD10+/	A_SD8–/	A_SI_O+/	A_SC_D-/	A_SSEL+/	A_SRST–/	A_SACK+/	A_SATN–/	A_SDP0+/	A_SD6–/	V_{SS}	V_{SS}	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Table 7.40 Signal Names and BGA Position

Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos
VSS	A1	DRAM_ADDR11	D1	VSS	L11	TCK	T25	VSS	AD3
VSS	A2	DRAM_ADDR10	D2	VSS	L12	ARM_TRST/	T26	B_SACK–/	AD4
DRAM_ADDR1	A3	DRAM_ADDR6	D3	VSS	L13	B_GPIO1	U1	B_RBIAS–	AD5
DRAM_OE/	A4	VSS	D4	VSS	L14	B_GPIO0	U2	B_SD6–/	AD6
DRAM_CASFB_A	A5	DRAM_ADDR0	D5	VSS	L15	B_GPIO2	U3	B_SD4+/	AD7
VDDCORE3	A6	VDD	D6	VSS	L16	VSSCORE5	U4	B_SD2+/	AD8
DRAM_CAS5/	A7	DRAM_CAS4/	D7	VDD	L23	ARM_TMS	U23	B_SD1–/	AD9
DRAM_CAS3/	A8	DRAM_CAS6/	D8	PCI_AD27	L24	ARM_TDO	U24	B_SDP1+/	AD10
DRAM_RAS1/	A9	VSS	D9	PCI_AD28	L25	VDDCORE0	U25	B_SD14–/	AD11
DRAM_PAR2	A10	DRAM_PAR3	D10	PCI_AD26	L26	A_GPIO0	U26	B_SD12–/	AD12
DRAM_DATA0	A11	VDD	D11	MEM_WE/	M1	B_GPIO3	V1	SCLK	AD13
DRAM_DATA17	A12	DRAM_DATA19	D12	MEM_DATA1	M2	VDDCORE5	V2	A_DIFFSENS	AD14
DRAM_DATA3	A13	DRAM_DATA20	D13	MEM_DATA4	M3	B_SD11+/	V3	A_SD10–/	AD15
DRAM_DATA23	A14	VSS	D14	MEM_DATA6	M4	VSS	V4	A_SD9+/	AD16
DRAM_DATA9	A15	DRAM_DATA21	D15	VSS	M11	VSS	V23	A_SREQ–/	AD17
DRAM_DATA26	A16	VDD	D16	VSS	M12	A_GPIO1	V24	A_SSEL–/	AD18
DRAM_DATA12	A17	DRAM_DATA10	D17	VSS	M13	A_GPIO2	V25	A_SRST+/	AD19
DRAM_DATA29	A18	VSS	D18	VSS	M14	A_GPIO3	V26	A_SBSY+/	AD20
DRAM_DATA15	A19	DRAM_DATA30	D19	VSS	M15	B_SD11–/	W1	A_SDP0–/	AD21
PCI_AD0	A20	PCI_AD5	D20	VSS	M16	B_GPIO4	W2	A_SD6+/	AD22
PCI_AD3	A21	VDD	D21	GNT/	M23	S_SD9–/	W3	A_SD5+/	AD23
PCI_AD6	A22	PCI_AD9	D22	PCI_AD30	M24	B_SD10+/	W4	VSS	AD24
C_BE0	A23	VSS	D23	PCI_AD31	M25	A_SD12+/	W23	A_SD3–/	AD25
PCI_AD10	A24	PCI_AD14	D24	PCI_AD29	M26	A_GPIO4	W24	A_SD3+/	AD26
PCI_AD13	A25	PERR/	D25	MEM_DATA2	N1	A_SD13+/	W25	VSS	AE1
VSS	A26	STOP/	D26	MEM_DATA3	N2	A_SD12–/	W26	VSS	AE2
DRAM_ADDR5	B1	MEM_ADDR0	E1	MEM_DATA7	N3	B_SD9+/	Y1	B_SBSY+/	AE3
VSS	B2	TEST_DRAMCLK	E2	VSS	N4	B_SD10–/	Y2	B_SATN–/	AE4
DRAM_ADDR3	B3	DRAM_ADDR12	E3	VSS	N11	B_SI_O–/	Y3	B_SDP0+/	AE5
DRAM_WE/	B4	DRAM_ADDR9	E4	VSS	N12	B_SD8+/	Y4	B_SD7–/	AE6
DRAM_RAS2/	B5	SERR/	E23	VSS	N13	A_SDP–/	Y23	B_SD5+/	AE7
DRAM_CAS0/	B6	C_BE1	E24	VSS	N14	A_SD13–/	Y24	B_SD4–/	AE8
DRAM_CAS2/	B7	TRDY/	E25	VSS	N15	A_SD14–/	Y25	B_SD1+/	AE9
DRAM_RAS0/	B8	IRDY/	E26	VSS	N16	A_SD14+/	Y26	B_SD0–/	AE10
VSSCORE3	B9	MEM_ADDR3	F1	INTB	N23	B_SD8–/	AA1	B_SD15–/	AE11
DRAM_PAR1	B10	MEM_ADDR2	F2	RST/	N24	B_SI_O+/	AA2	B_SD13+/	AE12
DRAM_DATA1	B11	MEM_ADDR4	F3	XINT	N25	B_SC_D+/	AA3	B_SD12+/	AE13
DRAM_DATA18	B12	VDD	F4	REQ/	N26	VDD	AA4	VSS-A	AE14
DRAM_DATA6	B13	VDD	F23	SCAN_TRI_EN	P1	VDD	AA23	A_SD11+/	AE15
DRAM_DATA7	B14	DEVSEL/	F24	MEM_DATA5	P2	A_SD15+/	AA24	A_SD9–/	AE16
DRAM_DATA8	B15	CLK	F25	SCAN_RAM_EN	P3	A_SDP1+/	AA25	A_SI_O–/	AE17
DRAM_DATA25	B16	VSSCORE1	F26	TESTIN	P4	A_SD15–/	AA26	A_SREQ+/	AE18
DRAM_DATA27	B17	MEM_ADDR6	G1	VSS	P11	B_SREQ+/	AB1	A_SC_D+/	AE19
DRAM_DATA13	B18	MEM_ADDR5	G2	VSS	P12	B_SREQ–/	AB2	A_SMSG+/	AE20
DRAM_DATA31	B19	MEM_ADDR7	G3	VSS	P13	B_SMSG–/	AB3	A_SBSY–/	AE21
PCI_AD1	B20	MEM_ADDR1	G4	VSS	P14	B_SSEL–/	AB4	A_SATN+/	AE22
PCI_AD4	B21	C_BE2	G23	VSS	P15	A_SD2–/	AB23	A_SD7–/	AE23
PCI_AD7	B22	FRAME/	G24	VSS	P16	A_SD1+/	AB24	A_SD5–/	AE24
PCI_AD8	B23	PCI_AD18	G25	VSS	P23	A_SD0–/	AB25	VSS	AE25
PCI_AD11	B24	PCI_AD17	G26	INTA	P24	A_SD0+/	AB26	A_SD4–/	AE26
VSS	B25	MEM_ADDR9	H1	RXT	P25	B_SC_D–/	AC1	VSS	AF1
VSS	B26	MEM_ADDR8	H2	TDO	P26	B_SSEL+/	AC2	B_SACK+/	AF2
DRAM_ADDR8	C1	MEM_ADDR10	H3	SCANMODE	R1	B_SRST–/	AC3	B_SBSY–/	AF3
DRAM_ADDR7	C2	VDDCORE4	H4	SCAN_RST_EN	R2	VSS	AC4	B_RBIAS+	AF4
VSS	C3	PCI_AD19	H23	SCAN_EN	R3	B_SATN+/	AC5	B_SDP0–/	AF5
DRAM_ADDR4	C4	PCI_AD16	H24	SCAN_TST_CLK_EN	R4	VDD	AC6	B_SD6+/	AF6
DRAM_ADDR2	C5	PCI_AD22	H25	VSS	R11	B_SD7+/	AC7	B_SD5–/	AF7
DRAM_RAS3/	C6	PCI_AD20	H26	VSS	R12	B_SD3–/	AC8	B_SD3+/	AF8
DRAM_CASFB_B	C7	MEM_ADDR11	J1	VSS	R13	VSS	AC9	B_SD2–/	AF9
DRAM_CAS1/	C8	MEM_ADDR12	J2	VSS	R14	B_SD15+/	AC10	B_SD0+/	AF10
DRAM_CAS7/	C9	MOE/_TESTOUT	J3	VSS	R15	VDD	AC11	B_SDP1–/	AF11
DRAM_PAR0	C10	VSS	J4	VSS	R16	B_DIFFSENS	AC12	B_SD14+/	AF12
DRAM_DATA16	C11	VSS	J23	VSSCORE0	R23	VSS	AC13	B_SD13–/	AF13
DRAM_DATA2	C12	PCI_AD21	J24	TXT	R24	TEST_HSC	AC14	A_SD11–/	AF14
DRAM_DATA4	C13	PCI_AD23	J25	TRST/	R25	VDD-A	AC15	A_SD10+/	AF15
DRAM_DATA5	C14	VDDCORE1	J26	TDI	R26	VDD	AC16	A_SD8–/	AF16
DRAM_DATA22	C15	MEM_CE0/	K1	PME	T1	A_SD8+/	AC17	A_SI_O+/	AF17
DRAM_DATA24	C16	MEM_CE1/	K2	NC	T2	VSS	AC18	A_SC_D–/	AF18
DRAM_DATA11	C17	MEM_CE2/	K3	POWER_FAIL/	T3	A_SMSG–/	AC19	A_SSEL+/	AF19
DRAM_DATA28	C18	MCE2_RD/	K4	VDD	T4	A_SACK–/	AC20	A_SRST–/	AF20
DRAM_DATA14	C19	PCI_AD25	K23	VSS	T11	VDD	AC21	A_SACK+/	AF21
VDDCORE2	C20	IDSEL	K24	VSS	T12	A_SD7+/	AC22	A_SATN–/	AF22
PCI_AD2	C21	PCI_AD24	K25	VSS	T13	VSS	AC23	A_SDP0+/	AF23
VSSCORE2	C22	C_BE3	K26	VSS	T14	A_SD4+/	AC24	A_SD6–/	AF24
PCI_AD12	C23	VSSCORE4	L1	VSS	T15	A_SD2+/	AC25	VSS	AF25
VSS	C24	MCE2_WR/	L2	VSS	T16	A_SD1–/	AC26	VSS	AF26
PCI_AD15	C25	MEM_DATA0	L3	VDD	T23	B_SMSG+/	AD1		
PAR	C26	VDD	L4	TMS	T24	B_SRST+/	AD2		

Table 7.41 Signal Names By BGA Position

Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos
A_SACK–/	AC20	B_SI_O+/	AA2	DRAM_DATA2	C12	PCI_AD2	C21	VSS	A1
A_SACK+/	AF21	B_SMSG–/	AB3	DRAM_DATA3	A13	PCI_AD3	A21	VSS	A2
A_SATN–/	AF22	B_SMSG+/	AD1	DRAM_DATA4	C13	PCI_AD4	B21	VSS	A26
A_SATN+/	AE22	B_RBIAS–	AD5	DRAM_DATA5	C14	PCI_AD5	D20	VSS	B2
A_SBSY–/	AE21	B_RBIAS+	AF4	DRAM_DATA6	B13	PCI_AD6	A22	VSS	B25
A_SBSY+/	AD20	B_SREQ–/	AB2	DRAM_DATA7	B14	PCI_AD7	B22	VSS	B26
A_SC_D–/	AF18	B_SREQ+/	AB1	DRAM_DATA8	B15	PCI_AD8	B23	VSS	C3
A_SC_D+/	AE19	B_SRST–/	AC3	DRAM_DATA9	A15	PCI_AD9	D22	VSS	C24
A_DIFFSENS	AD14	B_SRST+/	AD2	DRAM_DATA10	D17	PCI_AD10	A24	VSS	D4
A_GPIO0	U26	B_SD0–/	AE10	DRAM_DATA11	C17	PCI_AD11	B24	VSS	D9
A_GPIO1	V24	B_SD1–/	AD9	DRAM_DATA12	A17	PCI_AD12	C23	VSS	D14
A_GPIO2	V25	B_SD2–/	AF9	DRAM_DATA13	B18	PCI_AD13	A25	VSS	D18
A_GPIO3	V26	B_SD3–/	AC8	DRAM_DATA14	C19	PCI_AD14	D24	VSS	D23
A_GPIO4	W24	B_SD4–/	AE8	DRAM_DATA15	A19	PCI_AD15	C25	VSS	J4
A_SI_O–/	AE17	B_SD5–/	AF7	DRAM_DATA16	C11	PCI_AD16	H24	VSS	J23
A_SI_O+/	AF17	B_SD6–/	AD6	DRAM_DATA17	A12	PCI_AD17	G26	VSS	L11
A_SMSG–/	AC19	B_SD7–/	AE6	DRAM_DATA18	B12	PCI_AD18	G25	VSS	L12
A_SMSG+/	AE20	B_SD8–/	AA1	DRAM_DATA19	D12	PCI_AD19	H23	VSS	L13
A_SREQ–/	AD17	B_SD9–/	W3	DRAM_DATA20	D13	PCI_AD20	H26	VSS	L14
A_SREQ+/	AE18	B_SD10–/	Y2	DRAM_DATA21	D15	PCI_AD21	J24	VSS	L15
A_SRST–/	AF20	B_SD11–/	W1	DRAM_DATA22	C15	PCI_AD22	H25	VSS	L16
A_SRST+/	AD19	B_SD12–/	AD12	DRAM_DATA23	A14	PCI_AD23	J25	VSS	M11
A_SD0–/	AB25	B_SD13–/	AF13	DRAM_DATA24	C16	PCI_AD24	K25	VSS	M12
A_SD1–/	AC26	B_SD14–/	AD11	DRAM_DATA25	B16	PCI_AD25	K23	VSS	M13
A_SD2–/	AB23	B_SD15–/	AE11	DRAM_DATA26	A16	PCI_AD26	L26	VSS	M14
A_SD3–/	AD25	B_SD0+/	AF10	DRAM_DATA27	B17	PCI_AD27	L24	VSS	M15
A_SD4–/	AE26	B_SD1+/	AE9	DRAM_DATA28	C18	PCI_AD28	L25	VSS	M16
A_SD5–/	AE24	B_SD2+/	AD8	DRAM_DATA29	A18	PCI_AD29	M26	VSS	N4
A_SD6–/	AF24	B_SD3+/	AF8	DRAM_DATA30	D19	PCI_AD30	M24	VSS	N11
A_SD7–/	AE23	B_SD4+/	AD7	DRAM_DATA31	B19	PCI_AD31	M25	VSS	N12
A_SD8–/	AF16	B_SD5+/	AE7	DRAM_OE/	A4	PERR/	D25	VSS	N13
A_SD9–/	AE16	B_SD6+/	AF6	DRAM_PAR0	C10	PME	T1	VSS	N14
A_SD10–/	AD15	B_SD7+/	AC7	DRAM_PAR1	B10	POWER_FAIL/	T3	VSS	N15
A_SD11–/	AF14	B_SD8+/	Y4	DRAM_PAR2	A10	REQ/	N26	VSS	N16
A_SD12–/	W26	B_SD9+/	Y1	DRAM_PAR3	D10	RST/	N24	VSS	P11
A_SD13–/	Y24	B_SD10+/	W4	DRAM_RAS0/	B8	RXT	P25	VSS	P12
A_SD14–/	Y25	B_SD11+/	V3	DRAM_RAS1/	A9	SCAN_EN	R3	VSS	P13
A_SD15–/	AA26	B_SD12+/	AE13	DRAM_RAS2/	B5	SCAN_RAM_EN	P3	VSS	P14
A_SD0+/	AB26	B_SD13+/	AE12	DRAM_RAS3/	C6	SCAN_RST_EN	R2	VSS	P15
A_SD1+/	AB24	B_SD14+/	AF12	DRAM_WE/	B4	SCAN_TST_CLK_EN	R4	VSS	P16
A_SD2+/	AC25	B_SD15+/	AC10	FRAME/	G24	SCAN_TRI_EN	P1	VSS	P23
A_SD3+/	AD26	B_SDP0–/	AF5	GNT/	M23	SCANMODE	R1	VSS	R11
A_SD4+/	AC24	B_SDP1–/	AF11	IDSEL	K24	SCLK	AD13	VSS	R12
A_SD5+/	AD23	B_SDP0+/	AE5	INTA	P24	SERR/	E23	VSS	R13
A_SD6+/	AD22	B_SDP1+/	AD10	INTB	N23	STOP/	D26	VSS	R14
A_SD7+/	AC22	B_SSEL–/	AB4	IRDY/	E26	TCK	T25	VSS	R15
A_SD8+/	AC17	B_SSEL+/	AC2	MCE2_RD/	K4	TDI	R26	VSS	R16
A_SD9+/	AD16	C_BE0	A23	MCE2_WR/	L2	TDO	P26	VSS	T11
A_SD10+/	AF15	C_BE1	E24	MEM_ADDR0	E1	TEST_DRAMCLK	E2	VSS	T12
A_SD11+/	AE15	C_BE2	G23	MEM_ADDR1	G4	TEST_HSC	AC14	VSS	T13
A_SD12+/	W23	C_BE3	K26	MEM_ADDR2	F2	TESTIN	P4	VSS	T14
A_SD13+/	W25	CLK	F25	MEM_ADDR3	F1	TMS	T24	VSS	T15
A_SD14+/	Y26	DEVSEL/	F24	MEM_ADDR4	F3	TRDY/	E25	VSS	T16
A_SD15+/	AA24	DRAM_ADDR0	D5	MEM_ADDR5	G2	TRST/	R25	VSS	V4
A_SDP0–/	AD21	DRAM_ADDR1	A3	MEM_ADDR6	G1	TXT	R24	VSS	V23
A_SDP1–/	Y23	DRAM_ADDR2	C5	MEM_ADDR7	G3	VDD	D6	VSS	AC4
A_SDP0+/	AF23	DRAM_ADDR3	B3	MEM_ADDR8	H2	VDD	D11	VSS	AC9
A_SDP1+/	AA25	DRAM_ADDR4	C4	MEM_ADDR9	H1	VDD	D16	VSS	AC13
A_SSEL–/	AD18	DRAM_ADDR5	B1	MEM_ADDR10	H3	VDD	D21	VSS	AC18
A_SSEL+/	AF19	DRAM_ADDR6	D3	MEM_ADDR11	J1	VDD	F4	VSS	AC23
ARM_TDO	U24	DRAM_ADDR7	C2	MEM_ADDR12	J2	VDD	F23	VSS	AD3
ARM_TMS	U23	DRAM_ADDR8	C1	MEM_CE0/	K1	VDD	L4	VSS	AD24
ARM_TRST/	T26	DRAM_ADDR9	E4	MEM_CE1/	K2	VDD	L23	VSS	AE1
B_SACK–/	AD4	DRAM_ADDR10	D2	MEM_CE2/	K3	VDD	T4	VSS	AE2
B_SACK+/	AF2	DRAM_ADDR11	D1	MEM_DATA0	L3	VDD	T23	VSS	AE25
B_SATN–/	AE4	DRAM_ADDR12	E3	MEM_DATA1	M2	VDD	AA4	VSS	AF1
B_SATN+/	AC5	DRAM_CASFB_A	A5	MEM_DATA2	N1	VDD	AA23	VSS	AF25
B_SBSY–/	AF3	DRAM_CASFB_B	C7	MEM_DATA3	N2	VDD	AC6	VSS	AF26
B_SBSY+/	AE3	DRAM_CAS0/	B6	MEM_DATA4	M3	VDD	AC11	VSS-A	AE14
B_SC_D–/	AC1	DRAM_CAS1/	C8	MEM_DATA5	P2	VDD	AC16	VSSCORE0	R23
B_SC_D+/	AA3	DRAM_CAS2/	B7	MEM_DATA6	M4	VDD	AC21	VSSCORE1	F26
B_DIFFSENS	AC12	DRAM_CAS3/	A8	MEM_DATA7	N3	VDD-A	AC15	VSSCORE2	C22
B_GPIO0	U2	DRAM_CAS4/	D7	MEM_WE/	M1	VDDCORE0	U25	VSSCORE3	B9
B_GPIO1	U1	DRAM_CAS5/	A7	MOE/_TESTOUT	J3	VDDCORE1	J26	VSSCORE4	L1
B_GPIO2	U3	DRAM_CAS6/	D8	NC	T2	VDDCORE2	C20	VSSCORE5	U4
B_GPIO3	V1	DRAM_CAS7/	C9	PAR	C26	VDDCORE3	A6	XINT	N25
B_GPIO4	W2	DRAM_DATA0	A11	PCI_AD0	A20	VDDCORE4	H4		
B_SI_O–/	Y3	DRAM_DATA1	B11	PCI_AD1	B20	VDDCORE5	V2		

Figure 7.30 LSI53C1510 388 Ball Grid Array

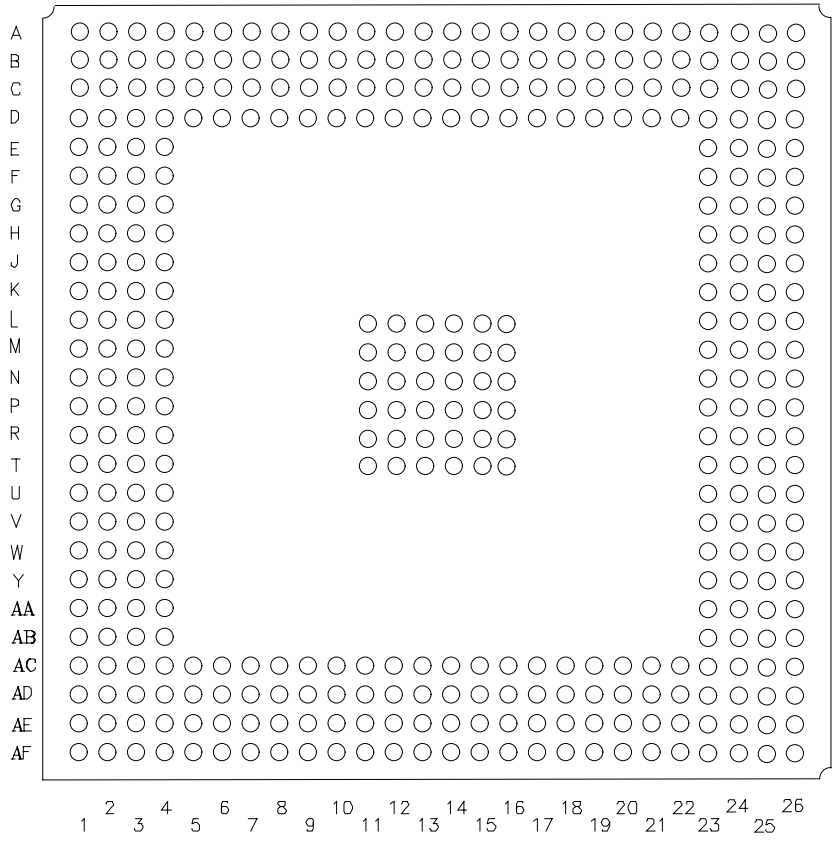
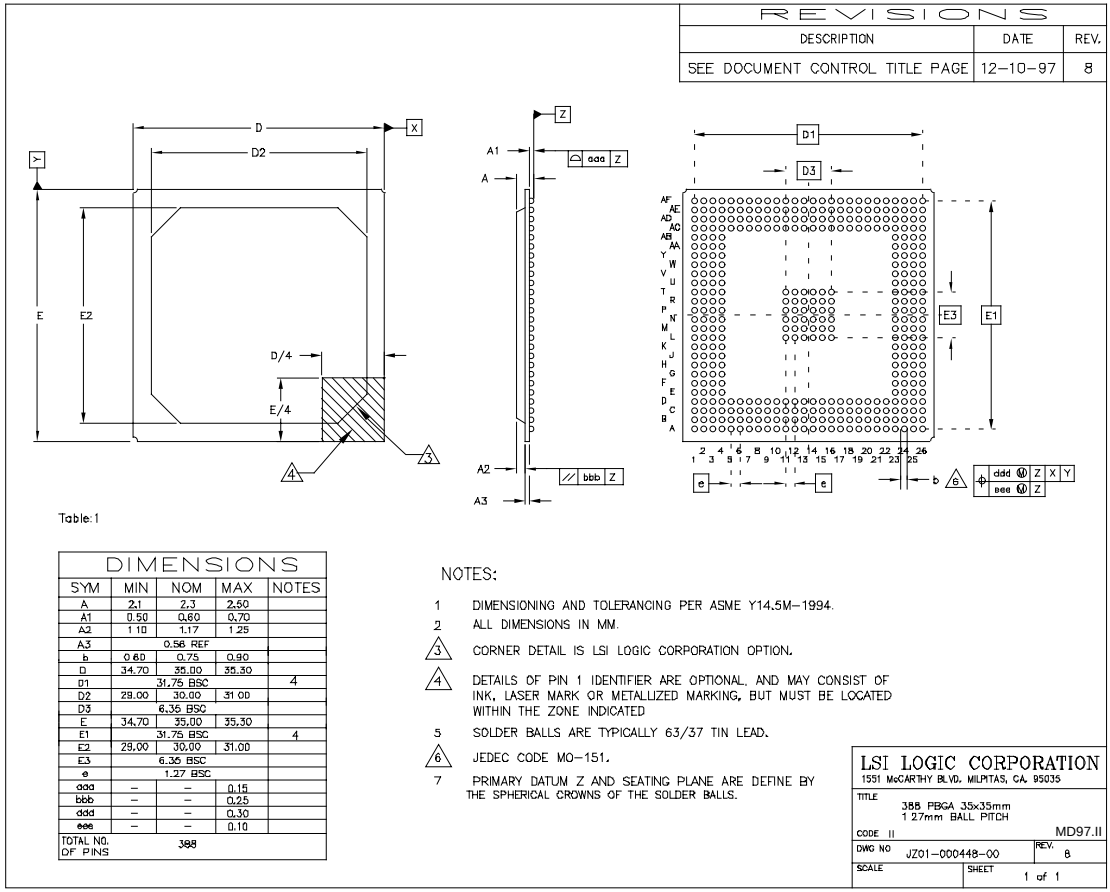


Figure 7.31 388 PBGA (II) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code II.**

Appendix A
Register Summary

Table A.1 lists the LSI53C1510 PCI registers (nonintelligent mode) by register name.

Table A.1 LSI53C1510 PCI Registers (Nonintelligent Mode) Register Map

Register Name	Address	Read/Write	Page
Base Address Register One (MEMORY)	0x14–0x17	Read/Write	5-18
Base Address Register Two (SCRIPTS RAM)	0x18–0x1B	Read/Write	5-18
Base Address Register Zero (I/O)	0x10–0x13	Read/Write	5-17
Bridge Support Extensions	0x46	Read Only	5-26
Cache Line Size	0x0C	Read/Write	5-15
Capabilities Pointer	0x34	Read Only	5-21
Capability ID	0x40	Read Only	5-23
Class Code	0x09–0x0B	Read Only	5-15
Command	0x02–0x03	Read/Write	5-11
Data	0x47	Read Only	5-26
Device ID	0x02–0x03	Read Only	5-11
Expansion ROM Base Address	0x30–0x33	Read/Write	5-20
Header Type	0x0E	Read Only	5-17
Interrupt Line	0x3C	Read/Write	5-22
Interrupt Pin	0x3D	Read Only	5-22
Latency Timer	0x0D	Read/Write	5-16
Max_Lat	0x3F	Read Only	5-23

Table A.1 LSI53C1510 PCI Registers (Nonintelligent Mode) Register Map (Cont.)

Register Name	Address	Read/Write	Page
Min_Gnt	0x3E	Read Only	5-23
Next Item Pointer	0x41	Read Only	5-24
Not Supported	0x0F	–	5-17
Power Management Capabilities	0x42–0x43	Read Only	5-24
Power Management Control/Status	0x44–0x45	Read/Write	5-25
Reserved	0x1C–0x2B	–	5-18
Reserved	0x35–0x3B	–	5-21
Revision ID (Rev ID)	0x08	Read Only	5-15
Status	0x06–0x07	Read/Write	5-13
Subsystem ID	0x2E–0x2F	Read Only	5-20
Subsystem Vendor ID	0x2C–0x2D	Read Only	5-19
Vendor ID	0x00–0x01	Read Only	5-11

Table A.2 lists the LSI53C1510 PCI registers (intelligent mode) registers by register name.

Table A.2 LSI53C1510 PCI Registers (Intelligent Mode) Register Map

Register Name	Address	Read/Write	Page
Base Address Register One (Shared MEMORY)	0x14–0x17	Read/Write	6-12
Base Address Register Zero (I/O)	0x10–0x13	Read/Write	6-11
BIST (Built-In Self Test)	0x0F	Read/Write	6-11
Bridge Support Extensions (PMCSR_BSE)	0x46	Read Only	6-18
Cache Line Size	0x0C	Read/Write	6-9
Capabilities Pointer	0x34	Read Only	6-14
Capability ID	0x40	Read Only	6-16
Class Code	0x09–0x0B	Read Only	6-9
Command	0x04–0x05	Read/Write	6-5

Table A.2 LSI53C1510 PCI Registers (Intelligent Mode) Register Map (Cont.)

Register Name	Address	Read/Write	Page
Data	0x47	Read Only	6-18
Device ID	0x02–0x03	Read Only	6-5
Expansion ROM Base Address	0x30–0x33	Read/Write	6-13
Header Type	0x0E	Read Only	6-10
Interrupt Line	0x3C	Read/Write	6-14
Interrupt Pin	0x3D	Read Only	6-15
Latency Timer	0x0D	Read/Write	6-10
Max_Lat	0x3F	Read Only	6-15
Min_Gnt	0x3E	Read Only	6-15
Next Item Pointer	0x41	Read Only	6-16
Power Management Capabilities (PMC)	0x42–0x43	Read Only	6-16
Power Management Control/Status (PMCSR)	0x44–0x45	Read/Write	6-17
Reserved	0x18–0x2B	–	6-12
Reserved	0x35–0x3B	–	6-14
Revision ID (Rev ID)	0x08	Read Only	6-8
Status	0x06–0x07	Read/Write	6-7
Subsystem ID	0x2E–0x2F	Read Only	6-13
Subsystem Vendor ID	0x2C–0x2D	Read Only	6-12
Vendor ID	0x00–0x01	Read Only	6-5

Table A.3 lists the LSI53C1510 Host Interface Registers (intelligent mode) by register name.

Table A.3 LSI53C1510 Host Interface Registers (Intelligent Mode)

Register Name	Address	Read/Write	Page
Data	0x08	Read/Write	6-18
DiagINT	0x00	Read/Write	6-20
Host Doorbell	0x20	Read/Write	6-24
Reply Interrupt Mask	0x34	Read/Write	6-25
Reply Interrupt Status	0x30	Read Only	6-25
Test Base Address	0x0C	Read/Write	6-23
WRSEQ	0x04	Write Only	6-21

Index

Symbols

A

B

C

D

E

F

G

H

I

L

M

N

O

P

R

S

T

U

V

W

X

Z

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