

TECHNICAL MANUAL

LSI53C860 PCI to Ultra SCSI I/O Processor

Version 2.1

April 2001

This document contains proprietary information of LSI Logic Corporation. The information contained herein is not to be used by or disclosed to third parties without the express written permission of an officer of LSI Logic Corporation.

LSI Logic products are not intended for use in life-support appliances, devices, or systems. Use of any LSI Logic product in such applications without written consent of the appropriate LSI Logic officer is prohibited.

Document DB14-000171-00, First Edition (April 2001)

This document describes the LSI Logic LSI53C860 PCI to Ultra SCSI I/O Processor and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

To receive product literature, visit us at <http://www.lsillogic.com>.

LSI Logic Corporation reserves the right to make changes to any products herein at any time without notice. LSI Logic does not assume any responsibility or liability arising out of the application or use of any product described herein, except as expressly agreed to in writing by LSI Logic; nor does the purchase or use of a product from LSI Logic convey a license under any patent rights, copyrights, trademark rights, or any other of the intellectual property rights of LSI Logic or third parties.

Copyright © 1995–2001 by LSI Logic Corporation. All rights reserved.

TRADEMARK ACKNOWLEDGMENT

The LSI Logic logo design, TolerANT, SDMS, and SCRIPTS are registered trademarks or trademarks of LSI Logic Corporation. All other brand and product names may be trademarks of their respective companies.

Preface

This book is the primary reference and technical manual for the LSI Logic LSI53C860 PCI to Ultra SCSI I/O Processor. It contains a complete functional description for the product and includes complete physical and electrical specifications.

Audience

This technical manual provides reference information on the LSI53C860 PCI to Ultra SCSI I/O Processor. It is intended for system designers and programmers who are using this device to design a SCSI port for PCI-based personal computers, workstations, or embedded applications.

Organization

This document has the following chapters and appendix:

- **Chapter 1, General Description**, includes general information about the LSI53C860 and other members of the LSI53C8XX family of PCI to SCSI I/O Processors.
- **Chapter 2, Functional Description**, describes the main functional areas of the chip in more detail, including the interfaces to the SCSI bus.
- **Chapter 3, PCI Functional Description**, describes the chip's connection to the PCI bus, including the PCI commands and configuration registers supported.
- **Chapter 4, Signal Descriptions**, contains the pin diagrams and definitions of each signal.
- **Chapter 5, Operating Registers**, describes each bit in the operating registers, organized by address.

- [Chapter 6, Instruction Set of the I/O Processor](#), defines all of the SCSI SCRIPTS instructions that are supported by the LSI53C860.
- [Chapter 7, Electrical Characteristics](#), contains the electrical characteristics and AC timings for the chip.
- [Appendix A, Register Summary](#), is a register summary of the LSI53C860.

Related Publications

For background please contact:

ANSI

11 West 42nd Street

New York, NY 10036

(212) 642-4900

Ask for document number X3.131-199X (SCSI-2)

Global Engineering Documents

15 Inverness Way East

Englewood, CO 80112

(800) 854-7179 or (303) 397-7956 (outside U.S.) FAX (303) 397-2740

Ask for document number X3.131-1994 (SCSI-2) or X3.253

(SCSI-3 Parallel Interface)

ENDL Publications

14426 Black Walnut Court

Saratoga, CA 95070

(408) 867-6642

Document names: *SCSI Bench Reference*, *SCSI Encyclopedia*,
SCSI Tutor

Prentice Hall

113 Sylvan Avenue

Englewood Cliffs, NJ 07632

(800) 947-7700

Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

LSI Logic World Wide Web Home Page

www.lsil.com

PCI Special Interest Group

2575 N. E. Katherine

Hillsboro, OR 97214

(800) 433-5177; (503) 693-6232 (International); FAX (503) 693-8344

SCSI SCRIPTS™ Processors Programming Guide, Order Number
S14044.A

Conventions Used in This Manual

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

Hexadecimal numbers are indicated by the prefix “0x” —for example, 0x32CF. Binary numbers are indicated by the prefix “0b” —for example, 0b0011.0010.1100.1111.

Revision Record

Revision	Date	Remarks
1.0	6/95	First version.
2.0	6/96	Revised technical manual.
2.1	4/01	All product names changed from SYM to LSI.

Contents

Chapter 1	General Description	
1.1	Benefits of Ultra SCSI	1-2
1.2	TolerANT® Technology	1-2
1.3	LSI53C860 Benefits Summary	1-3
1.3.1	SCSI Performance	1-4
1.3.2	PCI Performance	1-4
1.3.3	Integration	1-5
1.3.4	Ease of Use	1-5
1.3.5	Flexibility	1-5
1.3.6	Reliability	1-6
1.3.7	Testability	1-7

Chapter 2	Functional Description	
2.1	SCSI Core	2-1
2.1.1	DMA Core	2-2
2.2	SCRIPTS Processor	2-2
2.2.1	SDMS Software: The Total SCSI Solution	2-3
2.2.2	Designing an Ultra SCSI System	2-3
2.3	Prefetching SCRIPTS Instructions	2-4
2.3.1	Opcode Fetch Burst Capability	2-5
2.4	PCI Cache Mode	2-5
2.4.1	Load and Store Instructions	2-5
2.4.2	3.3 V/5 V PCI Interface	2-6
2.4.3	Loopback Mode	2-6
2.5	Parity Options	2-6
2.5.1	DMA FIFO	2-9
2.6	SCSI Bus Interface	2-11
2.6.1	Terminator Networks	2-12
2.6.2	Select/Reselect During Selection/Reselection	2-12

	2.6.3	Synchronous Operation	2-13
2.7		Interrupt Handling	2-15
	2.7.1	Polling and Hardware Interrupts	2-16
Chapter 3	PCI Functional Description		
	3.1	PCI Addressing	3-1
	3.1.1	Configuration Space	3-1
	3.1.2	PCI Bus Commands and Functions Supported	3-2
	3.2	PCI Cache Mode	3-3
	3.2.1	Support for PCI Cache Line Size Register	3-3
	3.2.2	Selection of Cache Line Size	3-4
	3.2.3	Alignment	3-4
	3.2.4	Memory Read Multiple Command	3-7
	3.2.5	Unsupported PCI Commands	3-8
	3.3	Configuration Registers	3-9
Chapter 4	Signal Descriptions		
	4.1	PCI Bus Interface Signals	5-5
	4.1.1	System Signals	5-5
	4.1.2	Address and Data Signals	5-6
	4.1.3	Interface Control Signals	5-7
	4.1.4	Arbitration Signals	5-8
	4.1.5	Error Reporting Signals	5-8
	4.2	SCSI Bus Interface Signals	5-9
	4.2.1	SCSI Bus Interface Signals	5-9
	4.2.2	Additional Interface Signals	5-10
Chapter 5	Operating Registers		
Chapter 6	Instruction Set of the I/O Processor		
	6.1	Low Level Register Interface Mode	7-1
	6.2	SCSI SCRIPTS	7-2
	6.2.1	Sample Operation	7-3
	6.3	Block Move Instructions	7-5
	6.3.1	First Dword	7-6
	6.3.2	Second Dword	7-12

6.4	I/O Instructions	7-13
6.4.1	First Dword	7-13
6.4.2	Second Dword	7-22
6.5	Read/Write Instructions	7-22
6.5.1	First Dword	7-22
6.5.2	Second Dword	7-23
6.5.3	Read-Modify-Write Cycles	7-23
6.5.4	Move To/From SFBR Cycles	7-23
6.6	Transfer Control Instructions	7-27
6.6.1	First Dword	7-27
6.6.2	Second Dword	7-35
6.7	Memory Move Instructions	7-35
6.7.1	First Dword	7-38
6.7.2	Second Dword	7-38
6.7.3	Third Dword	7-38
6.7.4	Read/Write System Memory from a SCRIPTS Instruction	7-39
6.8	Load and Store Instructions	7-39
6.8.1	First Dword	7-40
6.8.2	Second Dword	7-41

Chapter 7

Electrical Characteristics

7.1	DC Characteristics	8-1
7.2	TolerANT Technology	8-6
7.3	AC Characteristics	8-10
7.4	PCI Interface Timing Diagrams	8-12
7.4.1	Target Timing	8-13
7.4.2	Initiator Timing	8-17
7.5	PCI Interface Timing	8-25
7.6	SCSI Timing	8-26
7.7	Package Drawings	8-30

Appendix A

Register Summary

Index

Customer Feedback

Figures

1.1	LSI53C860 System Diagram	1-7
1.2	LSI53C860 Chip Diagram	1-8
2.1	DMA FIFO Sections	2-9
2.2	LSI53C860 Host Interface Data Paths	2-11
2.3	Active or Regulated Termination	2-13
4.1	LSI53C860 Pin Diagram	5-2
4.2	Functional Signal Grouping	5-4
6.1	SCRIPTS Overview	7-5
6.2	Block Move Instruction Register	7-8
6.3	I/O Instruction Register	7-16
6.4	Read/Write Register Instruction	7-25
6.5	Transfer Control Instruction	7-30
6.6	Memory to Memory Move Instruction	7-37
6.7	Load and Store Instruction Format	7-42
7.1	Rise and Fall Time Test Conditions	8-8
7.2	SCSI Input Filtering	8-8
7.3	Hysteresis of SCSI Receiver	8-8
7.4	Input Current as a Function of Input Voltage	8-9
7.5	Output Current as a Function of Output Voltage	8-9
7.6	Clock Timing Waveform	8-10
7.7	Reset Input Waveforms	8-11
7.8	Interrupt Output Waveforms	8-11
7.9	PCI Configuration Register Read	8-13
7.10	PCI Configuration Register Write	8-14
7.11	Target Read	8-15
7.12	Target Write	8-16
7.13	OpCode Fetch, Nonburst	8-17
7.14	Burst OpCode Fetch	8-18
7.15	Back-to-Back Read	8-19
7.16	Back-to-Back Write	8-20
7.17	Burst Read	8-21
7.18	Burst Write	8-23
7.19	Initiator Asynchronous Send	8-26

7.20	Initiator Asynchronous Receive	8-27
7.21	Target Asynchronous Send	8-27
7.22	Target Asynchronous Receive	8-28
7.23	Initiator and Target Synchronous Transfers	8-28
7.24	100 LD PQFP (UD) Mechanical Drawing (Sheet 1 of 2)	8-31

Tables

2.1	Bits Used for Parity Control and Observation	2-7
2.2	SCSI Parity Control	2-8
2.3	SCSI Parity Errors and Interrupts	2-8
3.1	PCI Bus Commands and Encoding Types	3-9
3.2	PCI Configuration Register Map	3-10
4.1	Power and Ground Signals	5-3
4.2	System Signals	5-5
4.3	Address and Data Signals	5-6
4.4	Interface Control Signals	5-7
4.5	Arbitration Signals	5-8
4.6	Error Reporting Signals	5-8
4.7	SCSI Bus Interface Signals	5-9
4.8	Additional Interface Signals	5-10
5.1	LSI53C860 Register Address Map	6-2
5.2	Synchronous Clock Conversion Factor	6-11
5.3	Asynchronous Clock Conversion Factor	6-12
5.4	Examples of Synchronous Transfer Periods and Rates for SCSI-1	6-14
5.5	Examples of Synchronous Transfer Periods and Rates for Fast SCSI	6-15
5.6	SCSI Synchronous Offset Values	6-16
6.1	SCRIPTS Instructions	7-3
6.2	Read/Write Instructions	7-26
7.1	Absolute Maximum Stress Ratings	8-2
7.2	Operating Conditions	8-2
7.3	SCSI Signals—SD[7:0]/, SDP/, SREQ/, SACK/	8-3
7.4	SCSI Signals—MSG, SI_O/, SC_D/, SATN/, SBSY/, SSEL/, SRST/	8-3
7.5	Input Signals—CLK, SCLK, GNT/, IDSEL, RST/, TESTIN	8-3
7.6	Capacitance	8-4
7.7	Output Signals—MAC/_TESTOUT, REQ/	8-4

7.8	Output Signal—IRQ/	8-4
7.9	Output Signal—SERR/	8-5
7.10	Bidirectional Signals—AD[31:0], C_BE/[3:0], FRAME/, IRDY/, TRDY/, DEVSEL/, STOP/, PERR/, PAR/	8-5
7.11	Bidirectional Signals—GPIO0_FETCH/, GPIO1_MASTER/	8-6
7.12	TolerANT Technology Electrical Characteristics	8-7
7.13	Clock Timing	8-10
7.14	Reset Input	8-11
7.15	Interrupt Output	8-11
7.16	PCI Timing	8-25
7.17	Initiator Asynchronous Send (5 Mbytes/s)	8-26
7.18	Initiator Asynchronous Receive (5 Mbytes/s)	8-27
7.19	Target Asynchronous Send (5 Mbytes/s)	8-27
7.20	Target Asynchronous Receive (5 Mbytes/s)	8-28
7.21	SCSI-1 Transfers (SE, 5.0 Mbytes/s)	8-29
7.22	SCSI-2 Fast Transfers (10.0 Mbytes/s (8-Bit Transfers), 40 MHz Clock)	8-29
7.23	Ultra SCSI Transfers (20.0 Mbytes/s (8-Bit Transfers), 80 MHz Clock)	8-30
A.1	Configuration Registers	A-1
A.2	SCSI Registers	A-2

Chapter 1

General Description

Chapter 1 is divided into the following sections:

- [Section 1.1, "Benefits of Ultra SCSI"](#)
- [Section 1.2, "TolerANT® Technology"](#)
- [Section 1.3, "LSI53C860 Benefits Summary"](#)

The LSI53C860 PCI to Ultra SCSI I/O Processor brings high-performance I/O solutions to host adapter, workstation, and general computer designs, making it easy to add SCSI to any PCI system.

The LSI53C860 is a pin-for-pin replacement for the LSI53C810 PCI to SCSI I/O processor. It performs Ultra SCSI transfers or Fast SCSI transfers in Single-Ended (SE) mode and improves performance by optimizing PCI bus utilization.

The LSI53C860 integrates a high-performance SCSI core, a PCI bus master DMA core, and the LSI Logic SCSI SCRIPTS™ processor to meet the flexibility requirements of SCSI-1, SCSI-2, and Ultra SCSI standards. It is designed to implement multithreaded I/O algorithms with a minimum of processor intervention, solving the protocol overhead problems of previous intelligent and nonintelligent adapter designs.

The LSI53C860 is fully supported by the LSI Logic Storage Device Management System (SDMS™), a software package that supports the Advanced SCSI Protocol Interface (ASPI). SDMS software provides BIOS and driver support for hard disk, tape, removable media products, and CD-ROM under the major PC operating systems.

The LSI53C860 is packaged in a compact rectangular 100-pin Plastic Quad Flat Pack (PQFP) package to minimize board space requirements. It operates the SCSI bus at 5 Mbytes/s asynchronously or up to 20 Mbytes/s synchronously and bursts data to the host at full PCI

speeds. The LSI53C860 increases SCRIPTS performance and reduces PCI bus overhead by allowing instruction prefetches of four or eight Dwords.

Software development tools are available to developers who use the SCSI SCRIPTS language to create customized SCSI software applications. The LSI53C860 allows easy firmware upgrades and is supported by advanced SCRIPTS commands.

1.1 Benefits of Ultra SCSI

Ultra SCSI is an extension of the SCSI-3 standard that expands the bandwidth of the SCSI bus and allows faster synchronous SCSI transfer rates. When enabled, Ultra SCSI performs 20 megatransfers during an I/O operation, resulting in approximately twice the synchronous transfer rates of fast SCSI-2. The LSI53C860 can perform 8-bit, Ultra SCSI synchronous transfers as fast as 20 Mbytes/s. This advantage is most noticeable in heavily loaded systems or with applications with large block requirements, such as video on-demand and image processing.

An advantage of Ultra SCSI is that it significantly improves SCSI bandwidth while preserving existing hardware and software investments. The primary software changes required enable the chip to perform synchronous negotiations for Ultra SCSI rates. The LSI53C860 uses the same board socket as an LSI53C810, with the addition of an 80 MHz SCLK. Some changes to existing cabling or system designs may be needed to maintain signal integrity at Ultra SCSI synchronous transfer rates. These design issues are discussed in [Chapter 2, "Functional Description."](#)

1.2 TolerANT[®] Technology

The LSI53C860 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation actively drives the SCSI Request, Acknowledge, Data, and Parity signals HIGH rather than allowing them to be passively pulled up by terminators. Active negation is enabled by setting bit 7 in the [SCSI Test Three \(STEST3\)](#) register.

TolerANT receiver technology improves data integrity in unreliable cabling environments where other devices would be subject to data corruption. TolerANT receivers filter the SCSI bus signals to eliminate unwanted transitions, without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps eliminate double clocking of data, the single biggest reliability issue with SCSI operations. TolerANT input signal filtering is a built in feature of all LSI Logic fast SCSI devices. On the LSI53C8XX family products, the user may select a filtering period of 30 or 60 ns, with bit 1 in the [SCSI Test Two \(STEST2\)](#) register. During Ultra SCSI transfers, the filtering period is automatically set at 15 ns. This period cannot be extended with the Extend SREQ/SACK Filtering bit.

The benefits of TolerANT technology include increased immunity to noise when the signal is going HIGH, better performance due to balanced duty cycles, and improved fast SCSI transfer rates. In addition, TolerANT SCSI devices do not cause glitches on the SCSI bus at power-up or power-down, so other devices on the bus are also protected from data corruption. TolerANT technology is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

1.3 LSI53C860 Benefits Summary

This section provides an overview of the LSI53C860 features and benefits. It contains these topics:

- [SCSI Performance](#)
- [PCI Performance](#)
- [Integration](#)
- [Ease of Use](#)
- [Flexibility](#)
- [Reliability](#)
- [Testability](#)

1.3.1 SCSI Performance

To improve SCSI performance, the LSI53C860:

- Complies with PCI 2.1 specification
- Performs Ultra SCSI synchronous transfers as fast as 20 Mbytes/s
- Supports variable block size and scatter/gather data transfers
- Minimizes SCSI I/O start latency
- Performs complex bus sequences without interrupts, including restore data pointers
- Reduces ISR overhead through a unique interrupt status reporting method
- Performs fast SCSI bus transfers in SE mode
 - up to 7 Mbytes/s asynchronous
 - 10 Mbytes/s synchronous, or 20 Mbytes/s synchronous with Ultra SCSI
- Increases performance of data transfers to and from the chip registers with new Load and Store SCRIPTS instruction
- Supports target disconnect and later reselect with no interrupt to the system processor
- Supports execution of multithreaded I/O algorithms in SCSI SCRIPTS with fast I/O context switching

1.3.2 PCI Performance

To improve PCI performance, the LSI53C860:

- Bursts 2, 4, 8, or 16 Dwords across PCI bus with 80-byte DMA FIFO
- Prefetches up to 8 Dwords of SCRIPTS instructions
- Supports 32-bit word data bursts with variable burst lengths
- Bursts SCRIPTS opcode fetches across the PCI bus
- Performs zero wait-state bus master data bursts faster than 110 Mbytes/s (@ 33 MHz)
- Supports PCI [Cache Line Size](#) register

1.3.3 Integration

Features of the LSI53C860 which ease integration include:

- 3.3 V/5 V PCI interface
- Full 32-bit PCI DMA bus master
- DMA controller using Memory-to-Memory Move instructions
- High-performance SCSI core
- Integrated SCRIPTS processor
- Compact 100-pin PQFP packaging

1.3.4 Ease of Use

The LSI53C860 provides:

- Direct PCI-to-SCSI connection
- Reduced SCSI development effort
- Support for the ASPI software standard using SDMS software
- Compatibility with existing LSI53C7XX and LSI53C8XX family SCRIPTS
- Direct connection to PCI and SCSI SE bus
- Development tools and sample SCSI SCRIPTS
- Maskable and pollable interrupts
- Three programmable SCSI timers: Select/Reselect, Handshake-to-Handshake, and General Purpose. The time-out period is programmable from 100 μ s to greater than 1.6 seconds
- SDMS software for complete PC-based operating system support
- Support for relative jumps
- SCSI Selected As ID bits for responding with multiple IDs

1.3.5 Flexibility

The LSI53C860 provides:

- High level programming interface (SCSI SCRIPTS)

- Support for execution of tailored SCSI sequences from main system RAM
- Flexible programming interface to tune I/O performance or to adapt to unique SCSI devices
- Flexibility to accommodate changes in the logical I/O interface definition
- Low level access to all registers and all SCSI bus signals
- Fetch, Master, and Memory Access control pins
- Support for indirect fetching of DMA address and byte counts so that SCRIPTS can be placed in a PROM
- Separate SCSI and system clocks
- Selectable IRQ pin disable bit
- Ability to route system clock to SCSI clock

1.3.6 Reliability

Enhanced reliability features of the LSI53C860 include:

- 2 kV ESD protection on SCSI signals
- Typical 300 mV SCSI bus hysteresis
- Average operating supply current of 50 mA
- Protection against bus reflections due to impedance mismatches
- Controlled bus assertion times (reduces RFI, improves reliability, and eases FCC certification)
- Latch-up protection greater than 150 mA
- Voltage feed-through protection (minimum leakage current through SCSI pads)
- High proportion (> 25%) of device pins are power and ground
- Power and ground isolation of I/O pads and internal chip logic
- TolerANT technology, which provides:
 - Active negation of SCSI Data, Parity, Request, and Acknowledge signals for improved fast SCSI transfer rates.
 - Input signal filtering on SCSI receivers improves data integrity, even in noisy cabling environments.

1.3.7 Testability

The LSI53C860 provides improved testability through:

- Access to all SCSI signals through programmed I/O
- SCSI loopback diagnostics
- SCSI bus signal continuity checking
- Support for single step mode operation
- Test mode (AND tree) to check pin continuity to the board

A system diagram showing the connections of the LSI53C860 in a PCI system is pictured in [Figure 1.1](#). A block diagram of the LSI53C860 is pictured in [Figure 1.2](#).

Figure 1.1 LSI53C860 System Diagram

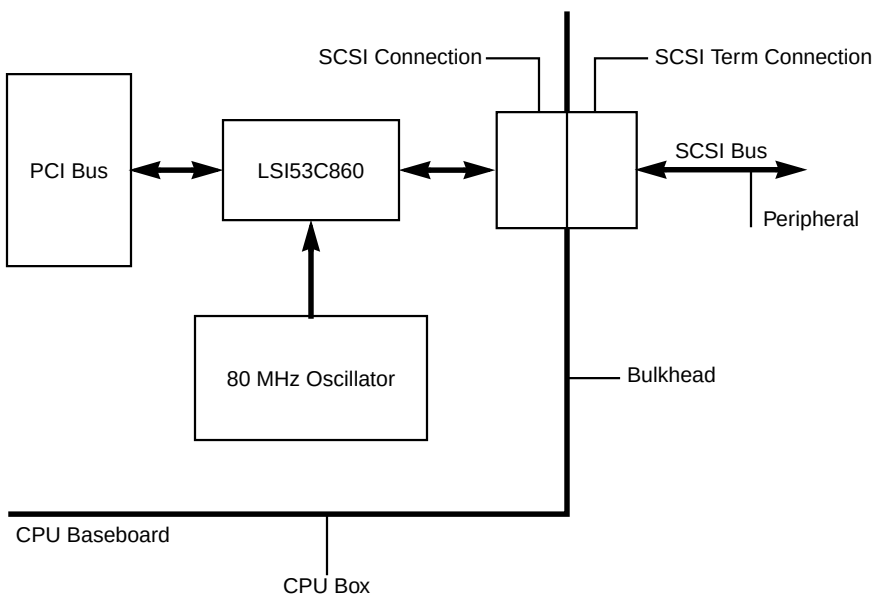
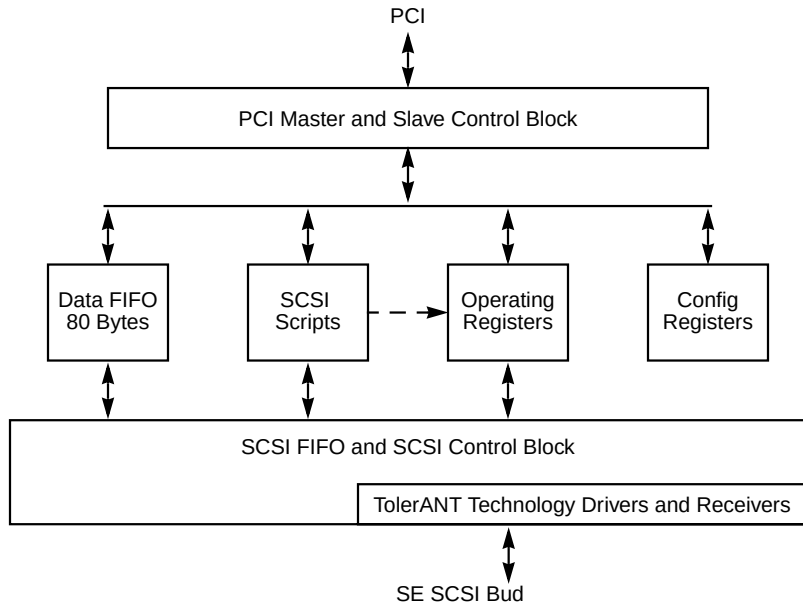


Figure 1.2 LSI53C860 Chip Diagram



Chapter 2

Functional Description

Chapter 2 is divided into the following sections:

- Section 2.1, “SCSI Core”
- Section 2.2, “SCRIPTS Processor”
- Section 2.3, “Prefetching SCRIPTS Instructions”
- Section 2.4, “PCI Cache Mode”
- Section 2.5, “Parity Options”
- Section 2.6, “SCSI Bus Interface”
- Section 2.7, “Interrupt Handling”

The LSI53C860 contains three functional blocks: the SCSI Core, the DMA Core, and the SCRIPTS Processor. The LSI53C860 is fully supported by SDMS software, a complete software package that supports the LSI Logic product line of SCSI processors and controllers.

2.1 SCSI Core

The SCSI core supports Ultra SCSI synchronous transfer rates up to 20 Mbytes/s, Fast SCSI synchronous transfer rates up to 10 Mbytes/s, and asynchronous transfer rates up to 7 Mbytes/s on an 8-bit SCSI bus. The SCSI core can be programmed with SCSI SCRIPTS, making it easy to fine tune the system for specific mass storage devices or advanced SCSI requirements.

The SCSI core offers low-level register access or a high-level control interface. Like first generation SCSI devices, the LSI53C860 is accessed as a register-oriented device. Error recovery and/or diagnostic

procedures use the ability to sample and/or assert any signal on the SCSI bus. In support of loopback diagnostics, the SCSI core may perform a self-selection and operate as both an initiator and a target.

The LSI53C860 is controlled by the integrated SCRIPTS processor through a high-level logical interface. Commands controlling the SCSI core are fetched out of the main host memory or local memory. These commands instruct the SCSI core to Select, Reselect, Disconnect, Wait for a Disconnect, Transfer Information, Change Bus Phases and, in general, implement all aspects of the SCSI protocol. The SCRIPTS processor is a special high-speed processor optimized for SCSI protocol.

2.1.1 DMA Core

The DMA core is a bus master DMA device that attaches directly to the industry standard PCI bus. The DMA core is tightly coupled to the SCSI core through the SCRIPTS processor, which supports uninterrupted scatter/gather memory operations.

The LSI53C860 supports 32-bit memory and automatically supports misaligned DMA transfers. An 80-byte FIFO allows two, four, eight, or sixteen Dword bursts across the PCI bus interface to run efficiently without throttling the bus during PCI bus latency.

2.2 SCRIPTS Processor

The SCSI SCRIPTS processor allows both DMA and SCSI commands to be fetched from host memory. Algorithms written in SCSI SCRIPTS control the actions of the SCSI and DMA cores. The SCRIPTS processor executes complex SCSI bus sequences independently of the host CPU.

The SCRIPTS processor can begin a SCSI I/O operation in approximately 500 ns. This compares with 2–8 ms required for traditional intelligent host adapters. Algorithms may be designed to tune SCSI bus performance, to adjust to new bus device types (such as scanners, communication gateways, etc.), or to incorporate changes in the SCSI-2 or SCSI-3 logical bus definitions without sacrificing I/O performance. SCSI SCRIPTS are hardware independent, so they can be used interchangeably on any host or CPU system bus.

A complete set of development tools is available for writing custom drivers with SCSI SCRIPTS. For more information on SCSI SCRIPTS instructions supported by the LSI53C860, see [Chapter 6, “Instruction Set of the I/O Processor.”](#)

2.2.1 SDMS Software: The Total SCSI Solution

For users who do not need to develop custom drivers, LSI Logic provides a total SCSI solution in PC environments with SDMS software. SDMS software provides BIOS and driver support for hard disk, tape, and removable media peripherals for the major PC-based operating systems.

SDMS software includes a SCSI BIOS to manage all SCSI functions related to the device. It also provides a series of SCSI device drivers that support most major operating systems. SDMS software supports a multithreaded I/O application programming interface (API) for user-developed SCSI applications. SDMS software supports both the ASPI and CAM SCSI software specifications.

2.2.2 Designing an Ultra SCSI System

Migrating an existing SE SCSI design from Fast SCSI to Ultra SCSI requires minor software modifications as well as consideration for some hardware design guidelines. Since Ultra SCSI is based on existing SCSI standards, it can use existing software programs as long as the software is able to negotiate for Ultra SCSI synchronous transfer rates.

In the area of hardware, the primary area of concern in SE systems is to maintain signal integrity at high data transfer rates. To assure reliable operation at Ultra SCSI transfer speeds, follow the system design parameters recommended in the SCSI-3 Ultra SCSI Parallel Interface draft standard. [Chapter 7, “Electrical Characteristics,”](#) contains Ultra SCSI timing information. In addition to the guidelines in the draft standard, make the following hardware and software adjustments to accommodate Ultra SCSI transfers:

- Set the Ultra SCSI Enable bit to enable Ultra SCSI transfers.
- Set the TolerANT Enable bit, bit 7 in the [SCSI Test Three \(STEST3\)](#) register, whenever the Fast-20 Enable bit is set.

- Do not extend the SREQ/SACK filtering period with [SCSI Test Two \(STEST2\)](#), bit 1.
- Use an 80 MHz SCLK.

2.3 Prefetching SCRIPTS Instructions

When enabled by setting the Prefetch Enable bit in the [DMA Control \(DCNTL\)](#) register, the prefetch logic in the LSI53C860 fetches 4 or 8 Dwords of instructions. The prefetch logic automatically determines the maximum burst size that it can perform, based on the burst length as determined by the values in the [DMA Mode \(DMODE\)](#) register and the PCI [Cache Line Size](#) register (if cache mode is enabled). If the unit cannot perform bursts of at least four Dwords, it disables itself.

The LSI53C860 may flush the contents of the prefetch unit under certain conditions, listed below, to ensure that the chip always operates from the most current version of the software. When one of these conditions apply, the contents of the prefetch unit are automatically flushed.

- On every Memory Move instruction. The Memory Move (MMOV) instruction is often used to place modified code directly into memory. To make sure that the chip executes all recent modifications, the prefetch unit flushes its contents and loads the modified code every time a MMOV instruction is issued. To avoid inadvertently flushing the prefetch unit contents, use the No Flush Memory to Memory Move (NFMMOV) instruction for all MMOV operations that do not modify code within the next 4 to 8 Dwords. For more information on this instruction, refer to [Chapter 6, "Instruction Set of the I/O Processor."](#)
- On every Store instruction. The Store instruction may also be used to place modified code directly into memory. To avoid inadvertently flushing the prefetch unit contents use the No Flush option for all Store operations that do not modify code within the next 8 Dwords.
- On every write to the [DMA SCRIPTS Pointer \(DSP\)](#) register.
- On all Transfer Control instructions when the transfer conditions are met. This is necessary because the next instruction to execute is not the sequential next instruction in the prefetch unit.

- When the Prefetch Flush bit ([DMA Control \(DCNTL\)](#) register, bit 5) is set. The unit flushes whenever this bit is set. The bit is self-clearing.

2.3.1 Opcode Fetch Burst Capability

Setting the Burst Opcode Fetch Enable bit (bit 1) in the [DMA Mode \(DMODE\)](#) register (0x38) causes the LSI53C860 to burst in the first two Dwords of all instruction fetches. If the instruction is a Memory-to-Memory Move, the third Dword is accessed in a separate ownership. If the instruction is an indirect type, the additional Dword is accessed in a subsequent bus ownership. If the instruction is a Table Indirect Block Move, the chip uses two accesses to obtain the four Dwords required, in two bursts of two Dwords each.

Note: This feature is only useful if SCRIPTS prefetching is disabled.

2.4 PCI Cache Mode

The LSI53C860 supports the PCI specification for an 8-bit [Cache Line Size](#) register located in PCI configuration space. The [Cache Line Size](#) register provides the ability to sense and react to nonaligned addresses corresponding to cache line boundaries. In conjunction with the [Cache Line Size](#) register, the PCI commands Read Line, Read Multiple, and Write and Invalidate are each software enabled or disabled to allow the user full flexibility in using these commands. For more information on PCI cache mode operations, refer to [Chapter 3, “PCI Functional Description.”](#)

2.4.1 Load and Store Instructions

The LSI53C860 supports the Load and Store instruction type, which simplifies the movement of data between memory and the internal chip registers. It also enables the chip to transfer bytes to addresses relative to the [Data Structure Address \(DSA\)](#) register. For more information on the Load and Store instructions, refer to [Chapter 6, “Instruction Set of the I/O Processor.”](#)

2.4.2 3.3 V/5 V PCI Interface

The LSI53C860 can attach directly to a 3.3 V or a 5 V PCI interface, due to separate V_{DD} pins for the PCI bus drivers. This allows the devices to be used on the universal board recommended by the PCI Special Interest Group.

2.4.3 Loopback Mode

The LSI53C860 loopback mode allows testing of both initiator and target functions and, in effect, lets the chip communicate with itself. When the Loopback Enable bit is set in the [SCSI Test One \(STEST1\)](#) register, the LSI53C860 allows control of all SCSI signals whether the chip is operating in the initiator or target mode. For more information on this mode of operation, refer to the *SCSI SCRIPTS Processors Programming Guide*.

2.5 Parity Options

The LSI53C860 implements a flexible parity scheme that allows control of the parity sense, allows parity checking to be turned on or off, and has the ability to deliberately send a byte with bad parity over the SCSI bus to test parity error recovery procedures. [Table 2.1](#) defines the bits that are involved in parity control and observation. [Table 2.2](#) describes the parity control function of the Enable Parity Checking and Assert SCSI Even Parity bits in the [SCSI Control Zero \(SCNTL0\)](#) register. [Table 2.3](#) describes the options available when a parity error occurs.

Table 2.1 Bits Used for Parity Control and Observation

Bit Name	Location	Description
Assert SATN/ on Parity Errors	SCSI Control Zero (SCNTL0) , Bit 1	Causes the LSI53C860 to automatically assert SATN/ when it detects a parity error while operating as an initiator.
Enable Parity Checking	SCSI Control Zero (SCNTL0) , Bit 3	Enables the LSI53C860 to check for parity errors. The LSI53C860 checks for odd parity.
Assert Even SCSI Parity	SCSI Control One (SCNTL1) , Bit 2	Determines the SCSI parity sense generated by the LSI53C860 to the SCSI bus.
Disable Halt on SATN/ or a Parity Error (Target Mode Only)	SCSI Control One (SCNTL1) , Bit 5	Causes the LSI53C860 not to halt operations when a SCSI parity error is detected in target mode.
Enable Parity Error Interrupt	SCSI Interrupt Enable Zero (SIEN0) , Bit 0	Determines whether the LSI53C860 generates an interrupt when it detects a SCSI parity error.
Parity Error	SCSI Interrupt Status Zero (SIST0) , Bit 0	This status bit is set whenever the LSI53C860 detects a parity error on the SCSI bus.
Status of SCSI Parity Signal	SCSI Status Zero (SSTAT0) , Bit 0	This status bit represents the live SCSI Parity Signal (SDP).
Latched SCSI Parity	SCSI Status One (SSTAT1) , Bit 3	This bit reflects the SCSI odd parity signal corresponding to the data latched into the SCSI Input Data Latch (SIDL) register.
Master Parity Error Enable	Chip Test Four (CTEST4) , Bit 3	Enables parity checking during PCI master data phases.
Master Data Parity Error	DMA Status (DSTAT) , Bit 6	Set when the LSI53C860, as a PCI master, detects a target device signaling a parity error during a data phase.
Master Data Parity Error Interrupt Enable	DMA Interrupt Enable (DIEN) , Bit 6	By clearing this bit, a Master Data Parity Error does not cause assertion of IRQ/, but the status bit is set in the DMA Status (DSTAT) register.

Table 2.2 SCSI Parity Control

EPC	AESP	Description
0	0	Does not check for parity errors. Parity is generated when sending SCSI data. Asserts odd parity when sending SCSI data.
0	1	Does not check for parity errors. Parity is generated when sending SCSI data. Asserts even parity when sending SCSI data.
1	0	Checks for odd parity on SCSI data received. Parity is generated when sending SCSI data. Asserts odd parity when sending SCSI data.
1	1	Checks for odd parity on SCSI data received. Parity is generated when sending SCSI data. Asserts even parity when sending SCSI data.

1. EPC = Enable Parity Checking (bit 3 [SCSI Control Zero \(SCNTL0\)](#)).
2. ASEP = Assert SCSI Even Parity (bit 2 [SCSI Control One \(SCNTL1\)](#)).

Table 2.3 SCSI Parity Errors and Interrupts

DHP	PAR	Description
0	0	Halts when a parity error occurs in the target or initiator mode and does NOT generate an interrupt.
0	1	Halts when a parity error occurs in target mode and generates an interrupt in target or initiator mode.
1	0	Does not halt in target mode when a parity error occurs until the end of the transfer. An interrupt is not generated.
1	1	Does not halt in target mode when a parity error occurs until the end of the transfer. An interrupt is generated.

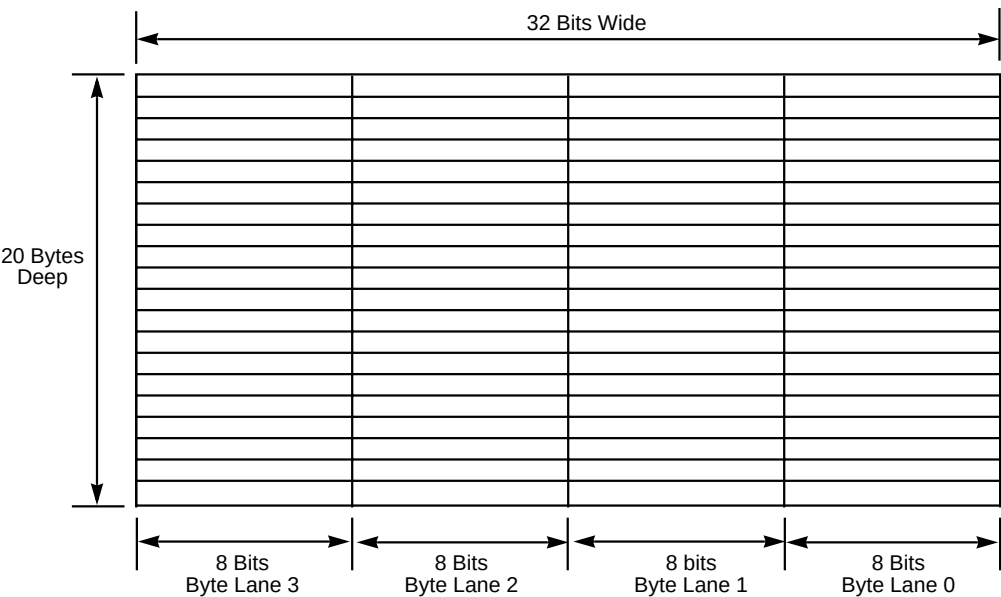
1. DHP = Disable Halt on SATN/ or Parity Error (bit 5 [SCSI Control One \(SCNTL1\)](#)).
2. PAR = Parity Error (bit 0 [SCSI Interrupt Enable Zero \(SIEN0\)](#)).

Note: This table only applies when the Enable Parity Checking bit is set.

2.5.1 DMA FIFO

The DMA FIFO is divided into four sections, each one byte wide and 20 transfers deep. The DMA FIFO is illustrated in [Figure 2.1](#).

Figure 2.1 DMA FIFO Sections



2.5.1.1 Data Paths

The data path through the LSI53C860 is dependent on whether data is being moved into or out of the chip, and whether SCSI data is being transferred asynchronously or synchronously.

[Figure 2.2](#) shows how data is moved to/from the SCSI bus in each of the different modes.

The following steps determine if any bytes remain in the data path when the chip halts an operation:

Asynchronous SCSI Send –

- Step 1. Look at the [DMA FIFO \(DFIFO\)](#) and [DMA Byte Counter \(DBC\)](#) registers and calculate if there are bytes left in the DMA FIFO. To make this calculation, subtract the seven least significant bits

of the [DMA Byte Counter \(DBC\)](#) register from the 7-bit value of the [DMA FIFO \(DFIFO\)](#) register. AND the result with 0x7F for a byte count between zero and 80.

- Step 2. Read bit 5 in the [SCSI Status Zero \(SSTAT0\)](#) register to determine if any bytes are left in the [SCSI Output Data Latch \(SODL\)](#) register. If bit 5 is set in the SSTAT0 register, then the [SCSI Output Data Latch \(SODL\)](#) register is full.

Synchronous SCSI Send –

- Step 1. Look at the [DMA FIFO \(DFIFO\)](#) and [DMA Byte Counter \(DBC\)](#) registers and calculate if there are bytes left in the DMA FIFO. To make this calculation, subtract the seven least significant bits of the [DMA Byte Counter \(DBC\)](#) register from the 7-bit value of the [DMA FIFO \(DFIFO\)](#) register. AND the result with 0x7F for a byte count between zero and 80.
- Step 2. Read bit 5 in the [SCSI Status Zero \(SSTAT0\)](#) register to determine if any bytes are left in the [SCSI Output Data Latch \(SODL\)](#) register. If bit 5 is set in the SSTAT0 register, then the [SCSI Output Data Latch \(SODL\)](#) register is full.
- Step 3. Read bit 6 in the [SCSI Status Zero \(SSTAT0\)](#) register to determine if any bytes are left in the SODR register. If bit 6 is set in the SSTAT0 register, then the SODR register is full.

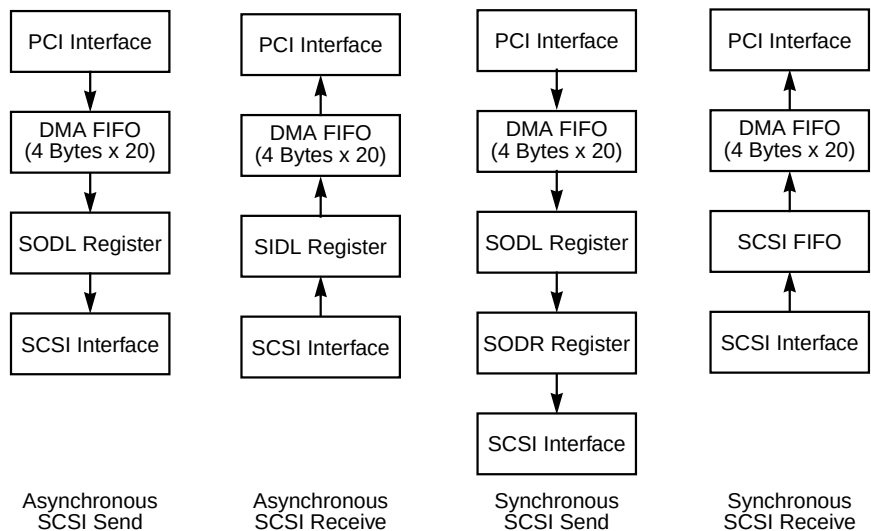
Asynchronous SCSI Receive –

- Step 1. Look at the [DMA FIFO \(DFIFO\)](#) and [DMA Byte Counter \(DBC\)](#) registers and calculate if there are bytes left in the DMA FIFO. To make this calculation, subtract the seven least significant bits of the [DMA Byte Counter \(DBC\)](#) register from the 7-bit value of the [DMA FIFO \(DFIFO\)](#) register. AND the result with 0x7F for a byte count between zero and 80.
- Step 2. Read bit 7 in the [SCSI Status Zero \(SSTAT0\)](#) register to determine if any bytes are left in the [SCSI Input Data Latch \(SIDL\)](#) register. If bit 7 is set in the SSTAT0 register, then the [SCSI Input Data Latch \(SIDL\)](#) register is full.

Synchronous SCSI Receive –

- Step 1. Subtract the seven least significant bits of the [DMA Byte Counter \(DBC\)](#) register from the 7-bit value of the [DMA FIFO \(DFIFO\)](#) register. AND the result with 0x7F for a byte count between 0 and 80.
- Step 2. Read the [SCSI Status One \(SSTAT1\)](#) register and examine bits [7:4], the binary representation of the number of valid bytes in the SCSI FIFO, to determine if any bytes are left in the SCSI FIFO.

Figure 2.2 LSI53C860 Host Interface Data Paths



2.6 SCSI Bus Interface

The LSI53C860 supports SE operation only. All SCSI signals are active LOW. The LSI53C860 contains the SE output drivers and can be connected directly to the SCSI bus. Each output is isolated from the power supply to ensure that a powered-down LSI53C860 has no effect on an active SCSI bus (CMOS “voltage feed-through” phenomena). TolerANT technology provides signal filtering at the inputs of SREQ/ and SACK/ to increase immunity to signal reflections.

2.6.1 Terminator Networks

The terminator networks provide the biasing needed to pull signals to an inactive voltage level, and to match the impedance seen at the end of the cable with the characteristic impedance of the cable. Terminators must be installed at the extreme ends of the SCSI chain, and only at the ends. No system should ever have more or less than two terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. There should be a means of disabling the termination.

SE cables can use a 220 Ω pull-up to the terminator power supply (Term Power) line and a 330 Ω pull-down resistor to ground. Because of the high-performance nature of the LSI53C860, regulated (or active) termination is recommended. [Figure 2.3](#) shows a Unitorde active terminator. For additional information, refer to the SCSI-2 Specification. TolerANT technology active negation can be used with any ANSI-approved termination network.

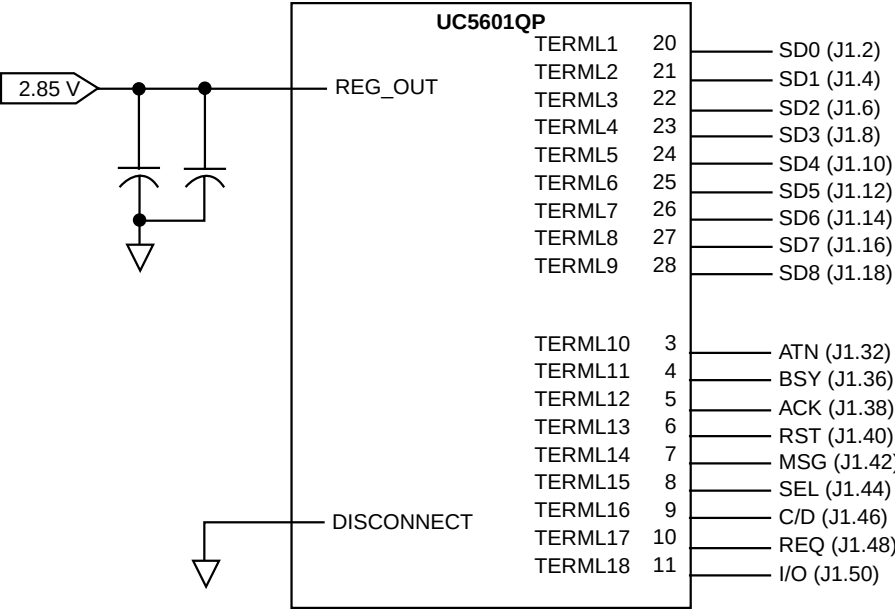
Note: Active termination is required in Ultra SCSI systems.

2.6.2 Select/Reselect During Selection/Reselection

In multithreaded SCSI I/O environments, it is not uncommon to be selected or reselected while trying to perform selection/reselection. This situation may occur when a SCSI controller (operating in the initiator mode) tries to select a target and is reselected by another. The Select SCRIPTS instruction has an alternate address to which the SCRIPTS will jump when this situation occurs. The analogous situation for target devices is being selected while trying to perform a reselection.

Once a change in operating mode occurs, the initiator SCRIPTS should start with a Set Initiator instruction or the target SCRIPTS should start with a Set Target instruction. The Selection and Reselection Enable bits ([SCSI Chip ID \(SCID\)](#) bits 5 and 6, respectively) should both be asserted so that the LSI53C860 may respond as an initiator or as a target. If only selection is enabled, the LSI53C860 cannot be reselected as an initiator. There are also status and interrupt bits in the [SCSI Interrupt Status Zero \(SIST0\)](#) and [SCSI Interrupt Enable Zero \(SIEN0\)](#) registers, respectively, indicating that the LSI53C860 has been selected (bit 5) or reselected (bit 4).

Figure 2.3 Active or Regulated Termination



Key	
C1	10 μ F SMT
C2	0.1 μ F SMT
J1	68-pin, high density "P" connector

2.6.3 Synchronous Operation

The LSI53C860 can transfer synchronous SCSI data in both the initiator and target modes. The [SCSI Transfer \(SXFER\)](#) register controls both the synchronous offset and the transfer period. It may be loaded by the CPU before SCRIPTS execution begins, from within SCRIPTS using a Table Indirect I/O instruction, or with a Read-Modify-Write instruction.

The LSI53C860 can receive data from the SCSI bus at a synchronous transfer period as short as 50 ns, regardless of the transfer period used to send data. The LSI53C860 can receive data at one-fourth of the

divided SCLK frequency. Depending on the SCLK frequency, the negotiated transfer period, and the synchronous clock divider, the LSI53C860 can send synchronous data at intervals as short as 50 ns for Ultra SCSI, 100 ns for fast SCSI-2, and 200 ns for SCSI-1.

2.6.3.1 Determining the Data Transfer Rate

Synchronous data transfer rates are controlled by bits in two different registers of the LSI53C860. Following is a brief description of the bits.

2.6.3.2 **SCSI Control Three (SCNTL3) Register, Bits [6:4] (SCF[2:0])**

The SCF[2:0] bits select the factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. The output from this divider controls the rate at which data can be received; this rate must not exceed 80 MHz. The receive rate is one-fourth of the divider output. For example, if SCLK is 40 MHz and the SCF value is set to divide by one, then the maximum rate at which data can be received is 10 Mbytes/s ($40/(1*4) = 10$).

For synchronous send, the output of the SCF divider is divided by the transfer period (XFERP) bits in the **SCSI Transfer (SXFER)** register. For valid combinations of the SCF and the XFERP, see [Table 5.4](#) and [Table 5.5](#), under the description of the XFERP bits [7:5] in the **SCSI Transfer (SXFER)** register.

2.6.3.3 **SCSI Control Three (SCNTL3) Register, Bits [2:0] (CCF[2:0])**

The CCF[2:0] bits select the frequency of the SCLK for asynchronous SCSI operations. To meet the SCSI timings as defined by the ANSI specification, these bits need to be set properly.

2.6.3.4 **SCSI Transfer (SXFER) Register, Bits [7:5] (TP[2:0])**

The TP[2:0] divider (XFERP) bits determine the SCSI synchronous send rate in either initiator or target mode. This value further divides the output from the SCF divider.

2.6.3.5 Achieving Optimal SCSI Send Rates

To achieve optimal synchronous SCSI send timings, the SCF divisor value should be set high, to divide the clock as much as possible before presenting the clock to the TP divider bits in the [SCSI Transfer \(SXFER\)](#) register. The TP[2:0] divider value should be as low as possible. For example, with an 80 MHz clock to achieve a 10 Mbytes/s send rate, the SCF bits can be set to divide by 1 and the TP bits to divide by 8; or the SCF bits can be set to divide by 2 and the TP bits set to divide by 4. Use the second option to achieve optimal SCSI timings.

2.6.3.6 Ultra SCSI Synchronous Data Transfers

Ultra SCSI is an extension of the current fast SCSI synchronous transfer specifications. It allows synchronous transfer periods to be negotiated down as low as 50 ns, which is half the 100 ns period allowed under fast SCSI. This will allow a maximum transfer rate of 20 Mbytes/s on an 8-bit SCSI bus. The LSI53C860 requires an 80 MHz SCSI clock input to perform Ultra SCSI transfers. In addition, the following bit values affect the chip's ability to support Ultra SCSI synchronous transfer rates:

- Clock Conversion Factor bits, [SCSI Control Three \(SCNTL3\)](#) register bits [2:0] and Synchronous Clock Conversion Factor bits, [SCSI Control Three \(SCNTL3\)](#) register bits [6:4]. These fields support the value of 101b which sets the CCF to work with 80 MHz and the SCF to be divided by 4 to run Ultra SCSI rates.
- Ultra Enable bit, [SCSI Control Three \(SCNTL3\)](#) register, bit 7. Setting this bit enables Ultra SCSI synchronous transfers in systems that have an 80 MHz clock.
- Tolerant Enable bit [SCSI Test Three \(STEST3\)](#), bit 7. Active negation must be enabled for Ultra SCSI operation.

2.7 Interrupt Handling

The SCRIPTS processor in the LSI53C860 performs most functions independently of the host microprocessor. However, certain interrupt situations must be handled by the external microprocessor. This section explains all aspects of interrupts as they apply to the LSI53C860.

2.7.1 Polling and Hardware Interrupts

The external microprocessor is informed of an interrupt condition by polling or hardware interrupts. Polling means that the microprocessor must continually loop and read a register until it detects a bit set that indicates an interrupt. This method is the fastest, but it wastes CPU time that could be used for other system tasks. The preferred method of detecting interrupts in most systems is hardware interrupts. In this case, the LSI53C860 asserts the Interrupt Request (IRQ/) line that interrupts the microprocessor, causing the microprocessor to execute an interrupt service routine. A hybrid approach would use hardware interrupts for long waits, and use polling for short waits.

2.7.1.1 Registers

The registers in the LSI53C860 that are used for detecting or defining interrupts are the [Interrupt Status \(ISTAT\)](#), [SCSI Interrupt Status Zero \(SIST0\)](#), [SCSI Interrupt Status One \(SIST1\)](#), [DMA Status \(DSTAT\)](#), [SCSI Interrupt Enable Zero \(SIEN0\)](#), [SCSI Interrupt Enable One \(SIEN1\)](#), [DMA Control \(DCNTL\)](#), and [DMA Interrupt Enable \(DIEN\)](#).

ISTAT – The [Interrupt Status \(ISTAT\)](#) is the only register that can be accessed as a slave during SCRIPTS operation. Therefore it is the register that is polled when polled interrupts are used. It is also the first register that should be read when the IRQ/ pin is asserted in association with a hardware interrupt. The INTF (Interrupt-on-the-Fly) bit should be the first interrupt serviced. It must be written to one to be cleared. This interrupt must be cleared before servicing any other interrupts.

If the SIP bit in the [Interrupt Status \(ISTAT\)](#) register is set, then a SCSI-type interrupt has occurred and the [SCSI Interrupt Status Zero \(SIST0\)](#) and [SCSI Interrupt Status One \(SIST1\)](#) registers should be read.

If the DIP bit in the [Interrupt Status \(ISTAT\)](#) register is set, then a DMA-type interrupt has occurred and the [DMA Status \(DSTAT\)](#) register should be read.

SCSI-type and DMA-type interrupts may occur simultaneously, so in some cases both SIP and DIP may be set.

SIST0 and SIST1 – The [SCSI Interrupt Status Zero \(SIST0\)](#) and [SCSI Interrupt Status One \(SIST1\)](#) registers contain SCSI-type interrupt bits. Reading these registers determines which condition or conditions caused the SCSI-type interrupt, and clears that SCSI interrupt condition.

If the LSI53C860 is receiving data from the SCSI bus and a fatal interrupt condition occurs, the chip attempts to send the contents of the DMA FIFO to memory before generating the interrupt.

If the LSI53C860 is sending data to the SCSI bus and a fatal SCSI interrupt condition occurs, data could be left in the DMA FIFO. Because of this the DMA FIFO Empty (DFE) bit in [DMA Status \(DSTAT\)](#) should be checked.

If this bit is cleared, set the CLF (Clear DMA FIFO) and CSF (Clear SCSI FIFO) bits before continuing. The CLF bit is bit 2 in [Chip Test Three \(CTEST3\)](#). The CSF bit is bit 1 in [SCSI Test Three \(STEST3\)](#).

DSTAT – The [DMA Status \(DSTAT\)](#) register contains the DMA-type interrupt bits. Reading this register determines which condition or conditions caused the DMA-type interrupt, and clears that DMA interrupt condition. The DFE bit, bit 7 in [DMA Status \(DSTAT\)](#), is purely a status bit. It will not generate an interrupt under any circumstances and will not be cleared when read. DMA interrupts flush neither the DMA nor SCSI FIFOs before generating the interrupt, so the DFE bit in the [DMA Status \(DSTAT\)](#) register should be checked after any DMA interrupt.

If the DFE bit is cleared, then the FIFOs must be cleared by setting the CLF (Clear DMA FIFO) and CSF (Clear SCSI FIFO) bits, or flushed by setting the FLF (Flush DMA FIFO) bit.

SIEN0 and SIEN1 – The [SCSI Interrupt Enable Zero \(SIEN0\)](#) and [SCSI Interrupt Enable One \(SIEN1\)](#) registers are the interrupt enable registers for the SCSI interrupts in [SCSI Interrupt Status Zero \(SIST0\)](#) and [SCSI Interrupt Status One \(SIST1\)](#).

DIEN – The [DMA Interrupt Enable \(DIEN\)](#) register is the interrupt enable register for DMA interrupts in [DMA Status \(DSTAT\)](#).

DCNTL – When bit 1 in [DMA Control \(DCNTL\)](#) is set, the IRQ/ pin is not asserted when an interrupt condition occurs. The interrupt is not lost or ignored, but merely masked at the pin. Clearing this bit when an interrupt

is pending immediately causes the IRQ/ pin to assert. As with any register other than [Interrupt Status \(ISTAT\)](#), this register cannot be accessed except by a SCRIPTS instruction during SCRIPTS execution.

2.7.1.2 Fatal vs. Nonfatal Interrupts

A fatal interrupt, as the name implies, always causes the SCRIPTS to stop running. All nonfatal interrupts become fatal when they are enabled by setting the appropriate interrupt enable bit. Interrupt masking is discussed in [Section 2.7.1.3, “Masking.”](#) All DMA interrupts (indicated by the DIP bit in [Interrupt Status \(ISTAT\)](#) and one or more bits in [DMA Status \(DSTAT\)](#) being set) are fatal.

Some SCSI interrupts (indicated by the SIP bit in the [Interrupt Status \(ISTAT\)](#) and one or more bits in [SCSI Interrupt Status Zero \(SIST0\)](#) or [SCSI Interrupt Status One \(SIST1\)](#) being set) are nonfatal.

When the LSI53C860 is operating in the Initiator mode, only the Function Complete (CMP), Selected (SEL), Reselected (RSL), General Purpose Timer Expired (GEN), and Handshake-to-Handshake Timer Expired (HTH) interrupts are nonfatal.

When operating in the target mode, CMP, SEL, RSL, Target mode: SATN/ active (M/A), GEN, and HTH are nonfatal. Refer to the description for the Disable Halt on a Parity Error or SATN/ active (Target Mode Only) (DHP) bit in the [SCSI Control One \(SCNTL1\)](#) register to configure the chip's behavior when the SATN/ interrupt is enabled during Target mode operation. The Interrupt-on-the-Fly interrupt is also nonfatal, since SCRIPTS can continue when it occurs.

The reason for nonfatal interrupts is to prevent SCRIPTS from stopping when an interrupt occurs that does not require service from the CPU. This prevents an interrupt when arbitration is complete (CMP set), when the LSI53C860 has been selected or reselected (SEL or RSL set), when the initiator asserts ATN (target mode: SATN/ active), or when the General Purpose or Handshake-to-Handshake timers expire. These interrupts are not needed for events that occur during high-level SCRIPTS operation.

2.7.1.3 Masking

Masking an interrupt means disabling or ignoring that interrupt. Interrupts can be masked by clearing bits in the [SCSI Interrupt Enable Zero \(SIEN0\)](#) and [SCSI Interrupt Enable One \(SIEN1\)](#) (for SCSI interrupts) registers or the [DMA Interrupt Enable \(DIEN\)](#) (for DMA interrupts) register. How the chip responds to masked interrupts depends on: whether polling or hardware interrupts are being used; whether the interrupt is fatal or nonfatal; and whether the chip is operating in the Initiator or Target mode.

If a nonfatal interrupt is masked and that condition occurs, the SCRIPTS do not stop, the appropriate bit in the [SCSI Interrupt Status Zero \(SIST0\)](#) or [SCSI Interrupt Status One \(SIST1\)](#) is still set, the SIP bit in the [Interrupt Status \(ISTAT\)](#) is not set, and the IRQ/ pin is not asserted. See [Section 2.7.1.2, “Fatal vs. Nonfatal Interrupts,”](#) for a list of the nonfatal interrupts.

If a fatal interrupt is masked and that condition occurs, then the SCRIPTS still stop, the appropriate bit in the [DMA Status \(DSTAT\)](#), [SCSI Interrupt Status Zero \(SIST0\)](#), or [SCSI Interrupt Status One \(SIST1\)](#) register is set, and the SIP or DIP bits in the [Interrupt Status \(ISTAT\)](#) register is set, but the IRQ/ pin is not asserted.

When the chip is initialized, enable all fatal interrupts if you are using hardware interrupts. If a fatal interrupt is disabled and that interrupt condition occurs, the SCRIPTS halt and the system never knows it unless it times out and checks the [Interrupt Status \(ISTAT\)](#) register after a certain period of inactivity.

If you are polling the [Interrupt Status \(ISTAT\)](#) instead of using hardware interrupts, then masking a fatal interrupt makes no difference since the SIP and DIP bits in the [Interrupt Status \(ISTAT\)](#) inform the system of interrupts, not the IRQ/ pin.

Masking an interrupt after IRQ/ is asserted does not cause deassertion of IRQ/.

2.7.1.4 Stacked Interrupts

The LSI53C860 will stack interrupts if they occur one after the other. If the SIP or DIP bits in the [Interrupt Status \(ISTAT\)](#) register are set (first level), then there is already at least one pending interrupt, and any future

interrupts are stacked in extra registers behind the [SCSI Interrupt Status Zero \(SIST0\)](#), [SCSI Interrupt Status One \(SIST1\)](#), and [DMA Status \(DSTAT\)](#) registers (second level). When two interrupts have occurred and the two levels of the stack are full, any further interrupts set additional bits in the extra registers behind [SCSI Interrupt Status Zero \(SIST0\)](#), [SCSI Interrupt Status One \(SIST1\)](#), and [DMA Status \(DSTAT\)](#). When the first level of interrupts are cleared, all the interrupts that came in afterward move into the [SCSI Interrupt Status Zero \(SIST0\)](#), [SCSI Interrupt Status One \(SIST1\)](#), and [DMA Status \(DSTAT\)](#). After the first interrupt is cleared by reading the appropriate register, the IRQ/ pin is deasserted for a minimum of three CLKs; the stacked interrupts move into the [SCSI Interrupt Status Zero \(SIST0\)](#), [SCSI Interrupt Status One \(SIST1\)](#), or [DMA Status \(DSTAT\)](#); and the IRQ/ pin is asserted once again.

Since a masked nonfatal interrupt does not set the SIP or DIP bits, interrupt stacking does not occur. A masked, nonfatal interrupt still posts the interrupt in [SCSI Interrupt Status Zero \(SIST0\)](#), but does not assert the IRQ/ pin. Since no interrupt is generated, future interrupts move right into the [SCSI Interrupt Status Zero \(SIST0\)](#) or [SCSI Interrupt Status One \(SIST1\)](#) instead of being stacked behind another interrupt. When another condition occurs that generates an interrupt, the bit corresponding to the earlier masked nonfatal interrupt is still set.

A related situation to interrupt stacking is when two interrupts occur simultaneously. Since stacking does not occur until the SIP or DIP bits are set, there is a small timing window in which multiple interrupts can occur but are not stacked. These could be multiple SCSI interrupts (SIP set), multiple DMA interrupts (DIP set), or multiple SCSI and multiple DMA interrupts (both SIP and DIP set).

As previously mentioned, DMA interrupts do not attempt to flush the FIFOs before generating the interrupt. It is important to set the Clear DMA FIFO (CLF) and Clear SCSI FIFO (CSF) bits if a DMA interrupt occurs and the DMA FIFO Empty (DFE) bit is not set. This is because any future SCSI interrupts are not posted until the DMA FIFO is cleared of data. These 'locked out' SCSI interrupts are posted as soon as the DMA FIFO is empty.

2.7.1.5 Halting in an Orderly Fashion

When an interrupt occurs, the LSI53C860 attempts to halt in an orderly fashion.

- If the interrupt occurs in the middle of an instruction fetch, the fetch is completed, except in the case of a Bus Fault. Execution does not begin, but the [DMA SCRIPTS Pointer \(DSP\)](#) points to the next instruction since it is updated when the current instruction is fetched.
- If the DMA direction is a write to memory and a SCSI interrupt occurs, the LSI53C860 attempts to flush the DMA FIFO to memory before halting. Under any other circumstances only the current cycle is completed before halting, so the DFE bit in [DMA Status \(DSTAT\)](#) register should be checked to see if any data remains in the DMA FIFO.
- SCSI SREQ/SACK handshakes that have begun are completed before halting.
- The LSI53C860 attempts to clean up any outstanding synchronous offset before halting.
- In the case of Transfer Control Instructions, once instruction execution begins it continues to completion before halting.
- If the instruction is a JUMP/CALL WHEN/IF <phase>, the [DMA SCRIPTS Pointer \(DSP\)](#) is updated to the transfer address before halting.
- All other instructions may halt before completion.

2.7.1.6 Sample Interrupt Service Routine

The following is a sample of an interrupt service routine for the LSI53C860. It can be repeated during polling or should be called when the IRQ/ pin is asserted if hardware interrupts.

1. Read [Interrupt Status \(ISTAT\)](#).
2. If the INTF bit is set, it must be written to a one to clear this status.
3. If only the SIP bit is set, read [SCSI Interrupt Status Zero \(SIST0\)](#) and [SCSI Interrupt Status One \(SIST1\)](#) to clear the SCSI interrupt condition and get the SCSI interrupt status. The bits in the [SCSI](#)

Interrupt Status Zero (SIST0) and SCSI Interrupt Status One (SIST1) tell which SCSI interrupts occurred and determine what action is required to service the interrupts.

4. If only the DIP bit is set, read the DMA Status (DSTAT) to clear the interrupt condition and get the DMA interrupt status. The bits in the DMA Status (DSTAT) tells which DMA interrupts occurred and determine what action is required to service the interrupts.
5. If both the SIP and DIP bits are set, read SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), and DMA Status (DSTAT) to clear the SCSI and DMA interrupt condition and get the interrupt status. If using 8-bit reads of the SCSI Interrupt Status Zero (SIST0), SCSI Interrupt Status One (SIST1), and DMA Status (DSTAT) registers to clear interrupts, insert a 12 CLK delay between the consecutive reads to ensure that the interrupts clear properly. Both the SCSI and DMA interrupt conditions should be handled before leaving the ISR. It is recommended that the DMA interrupt is serviced before the SCSI interrupt, because a serious DMA interrupt condition could influence how the SCSI interrupt is acted upon.
6. When using polled interrupts, go back to Step 1 before leaving the interrupt service routine, in case any stacked interrupts moved in when the first interrupt was cleared. When using hardware interrupts, the IRQ/ pin is asserted again if there are any stacked interrupts. This should cause the system to re-enter the interrupt service routine.

Chapter 3

PCI Functional Description

Chapter 3 is divided into the following sections:

- [Section 3.1, “PCI Addressing”](#)
- [Section 3.2, “PCI Cache Mode”](#)
- [Section 3.3, “Configuration Registers”](#)

3.1 PCI Addressing

There are three types of PCI-defined address space:

- Configuration space
- Memory space
- I/O space

3.1.1 Configuration Space

The configuration space is a contiguous 256-byte set of addresses dedicated to each “slot” or “stub” on the bus. Decoding C_BE/[3:0] determines if a PCI cycle is intended to access configuration register space. The IDSEL bus signal is a chip select that allows access to the configuration register space only. A configuration read/write cycle without IDSEL is ignored. The eight lower order address lines and byte enables select a specific 8-bit register. The host processor uses this configuration space to initialize the LSI53C860.

The lower 128 bytes of the LSI53C860 configuration space hold system parameters while the upper 128 bytes map into the LSI53C860 operating registers. For all PCI cycles except configuration cycles, the LSI53C860 registers are located on the 256-byte block boundary defined by the base

address assigned through the configured register. The LSI53C860 operating registers are available in both the upper and lower 128-byte portions of the 256-byte space selected.

At initialization time, each PCI device is assigned a base address (in the case of the LSI53C860, the upper 24 bits of the address are used) for memory accesses and I/O accesses. On every access, the LSI53C860 compares its assigned base addresses with the value on the Address/Data bus during the PCI address phase. If there is a match of the upper 24 bits, the access is for the LSI53C860 and the low order eight bits define the register to be accessed. A decode of C_BE/[3:0] determines which registers and what type of access is to be performed.

PCI defines memory space as a contiguous 32-bit memory address that is shared by all system resources, including the LSI53C860. [Base Address One \(Memory\)](#) determines which 256-byte memory area this device will occupy.

PCI defines I/O space as a contiguous 32-bit I/O address that is shared by all system resources, including the LSI53C860. [Base Address Zero \(I/O\)](#) determines which 256-byte I/O area this device will occupy.

3.1.2 PCI Bus Commands and Functions Supported

Bus commands indicate to the target the type of transaction the master is requesting. Bus commands are encoded on the C_BE/[3:0] lines during the address phase. PCI bus command encoding and types appear in [Table 3.1](#).

3.1.2.1 I/O Read Command

The I/O Read command reads data from an agent mapped in I/O address space. All 32 address bits are decoded.

3.1.2.2 I/O Write Command

The I/O Write command writes data to an agent when mapped in I/O address space. All 32 address bits are decoded.

3.1.2.3 Memory Read Command

The Memory Read command reads data from an agent mapped in memory address space. All 32 address bits are decoded.

3.1.2.4 Memory Read Multiple Command

The Memory Read Multiple command reads data from an agent mapped in memory address space. All 32 address bits are decoded.

3.1.2.5 Memory Read Line Command

The Memory Read Line command reads data from an agent mapped in memory address space. All 32 address bits are decoded.

3.1.2.6 Memory Write Command

The Memory Write command writes data to an agent when mapped in memory address space. All 32 address bits are decoded.

3.1.2.7 Memory Write and Invalidate Command

The Memory Write and Invalidate command writes data to an agent when mapped in memory address space. All 32 address bits are decoded.

3.2 PCI Cache Mode

The LSI53C860 supports the PCI specification for an 8-bit [Cache Line Size](#) register located in PCI configuration space. The [Cache Line Size](#) register provides the ability to sense and react to nonaligned addresses corresponding to cache line boundaries. In conjunction with the [Cache Line Size](#) register, the PCI commands Read Line, Read Multiple, and Write and Invalidate are each software enabled or disabled to allow the user full flexibility in using these commands.

3.2.1 Support for PCI Cache Line Size Register

The LSI53C860 supports the PCI specification for an 8-bit [Cache Line Size](#) register in PCI configuration space. It can sense and react to nonaligned addresses corresponding to cache line boundaries.

3.2.2 Selection of Cache Line Size

The cache logic will select a cache line size based on the values for the burst size in the [DMA Mode \(DMODE\)](#) register and the PCI [Cache Line Size](#) register.

Note: The LSI53C860 will not automatically use the value in the PCI [Cache Line Size](#) register as the cache line size value. The chip scales the value of the [Cache Line Size](#) register down to the nearest binary burst size allowed by the chip (2, 4, 8 or 16), compares this value to the [DMA Mode \(DMODE\)](#) burst size, then selects the smallest as the value for the cache line size. The LSI53C860 will use this value for all burst data transfers.

3.2.3 Alignment

The LSI53C860 uses the calculated burst size value to monitor the current address for alignment to the cache line size. When it is not aligned the chip disables bursting, allowing only single Dword transfers until a cache line boundary is reached. When the chip is aligned, bursting is re-enabled. It will burst in increments specified by the [Cache Line Size](#) register as explained above. If the [Cache Line Size](#) register is not set (default = 0x00), the [DMA Mode \(DMODE\)](#) burst size is automatically used as the cache line size.

3.2.3.1 MMIO Misalignment

The LSI53C860 will not operate in a cache alignment mode when a MMIO instruction is issued and the read and write addresses are different distances from the nearest cache line boundary. For example, if the read address is 0x21F and the write address is 0x42F, and the cache line size is eight (8), the addresses are byte aligned, but they are not the same distance from the nearest cache boundary. The read address is 1 byte from the cache boundary 0x220 and the write address is 17 bytes from the cache boundary 0x440. In this situation, the chip will not align to cache boundaries and will operate as an LSI53C810.

3.2.3.2 Memory Write and Invalidate Command

The Memory Write and Invalidate command is identical to the Memory Write command, except that it additionally guarantees a minimum transfer of one complete cache line; in other words, the master intends to write all bytes within the addressed cache line in a single PCI transaction unless interrupted by the target. This command requires implementation of the PCI [Cache Line Size](#) register at address 0x0C in PCI configuration space. The LSI53C860 enables Memory Write and Invalidate cycles when bit 0 in the [Chip Test Three \(CTEST3\)](#) register (WRIE) and bit 4 in the PCI [Command](#) register are set. This will cause Memory Write and Invalidate commands to be issued when the following conditions are met:

- The CLSE bit, WRIE bit, and PCI Configuration [Command](#) register, bit 4 must be set.
- The [Cache Line Size](#) register must contain a legal burst size (2, 4, 8 or 16) value AND that value must be less than or equal to the [DMA Mode \(DMODE\)](#) burst size.
- The chip must have enough bytes in the DMA FIFO to complete at least one full cache line burst.
- The chip must be aligned to a cache line boundary.

When these conditions have been met, the LSI53C860 will issue a Write and Invalidate command instead of a Memory Write command during all PCI write cycles.

Multiple Cache Transfers – When multiple cache lines of data have been read in during a MMIOV instruction (see the description for the Read Multiple command), the LSI53C860 will issue a Write and Invalidate command using the burst size necessary to transfer all the data in one transfer. For example, if the cache line size is 4, and the chip read in 16 Dwords of data using a Read Multiple command, the chip will switch the burst size to 16, and issue a Write and Invalidate to transfer all 16 Dwords in one bus ownership.

Latency – In accordance with the PCI specification, the chip's latency timer will be ignored when issuing a Write and Invalidate command such that when a latency time-out has occurred, the LSI53C860 will continue to transfer up until a cache line boundary. At that point, the chip will

relinquish the bus, and finish the transfer at a later time using another bus ownership. If the chip is transferring multiple cache lines it will continue to transfer until the next cache boundary is reached.

PCI Target Retry – During a Write and Invalidate transfer, if the target device issues a retry (STOP with no TRDY, indicating that no data was transferred), the LSI53C860 will relinquish the bus and immediately try to finish the transfer on another bus ownership. The chip will issue another Write and Invalidate command on the next ownership, in accordance with the PCI specification.

PCI Target Disconnect – During a Write and Invalidate transfer, if the target device issues a disconnect the LSI53C860 will relinquish the bus and immediately try to finish the transfer on another bus ownership. The chip will not issue another Write and Invalidate command on the next ownership.

3.2.3.3 Memory Read Line Command

This command is identical to the Memory Read command, except that it additionally indicates that the master intends to fetch a complete cache line. This command is intended to be used with bulk sequential data transfers where the memory system and the requesting master might gain some performance advantage by reading up to a cache line boundary rather than a single memory cycle. The Read Line Mode function that exists in the previous LSI53C8XX chips has been modified in the LSI53C860 to reflect the PCI [Cache Line Size](#) register specifications. The functionality of the Enable Read Line bit (bit 3 in [DMA Mode \(DMODE\)](#)) has been modified to more resemble the Write and Invalidate mode in terms of conditions that must be met before a Read Line command will be issued. However, the Read Line option will operate exactly like the previous LSI53C8XX chips when cache mode has been disabled by a CLSE bit reset or when certain conditions exist in the chip (explained below).

The Read Line mode is enabled by setting bit 3 in the [DMA Mode \(DMODE\)](#) register. If cache mode is disabled, Read Line commands will be issued on every read data transfer, except opcode fetches, as in previous LSI53C8XX chips.

If cache mode has been enabled, a Read Line command will be issued on all read cycles, except opcode fetches, when the following conditions have been met:

- The CLSE and Enable Read Line bits must be set.
- The [Cache Line Size](#) register must contain a legal burst size value (2, 4, 8 or 16) AND that value must be less than or equal to the DMODE burst size.
- The number of bytes to be transferred at the time a cache boundary has been reached must be equal to or greater than a full cache line size.
- The chip must be aligned to a cache line boundary.

When these conditions have been met, the chip will issue a Read Line command instead of a Memory Read during all PCI read cycles. Otherwise, it will issue a normal Memory Read command.

3.2.4 Memory Read Multiple Command

This command is identical to the Memory read command except that it additionally indicates that the master may intend to fetch more than one cache line before disconnecting. The LSI53C860 supports PCI Read Multiple functionality and will issue Read Multiple commands on the PCI bus when the Read Multiple Mode is enabled. This mode is enabled by setting bit 2 of the [DMA Mode \(DMODE\)](#) register (ERMP). The command will be issued when certain conditions have been met.

If cache mode has been enabled, a Read Multiple command will be issued on all read cycles, except opcode fetches, when the following conditions have been met:

1. The CLSE and ERMP bits must be set.
2. The [Cache Line Size](#) register must contain a legal burst size value (2, 4, 8 or 16) AND that value must be less than or equal to the DMODE burst size.
3. The number of bytes to be transferred at the time a cache boundary has been reached must be equal to or greater than the [DMA Mode \(DMODE\)](#) burst size.
4. The chip must be aligned to a cache line boundary.

When these conditions have been met, the chip will issue a Read Multiple command instead of a Memory Read during all PCI read cycles.

Burst Size Selection – The Read Multiple command reads in multiple cache lines of data in a single bus ownership. The number of cache lines to be read is determined by the [DMA Mode \(DMODE\)](#) burst size bits. In other words, the chip will switch its normal operating burst size to reflect the [DMA Mode \(DMODE\)](#) burst size settings for the Read Multiple command. For example, if the cache line size is 4, and the [DMA Mode \(DMODE\)](#) burst size is 16, the chip will switch the current burst size from 4 to 16, and issue a Read Multiple. After the transfer, the chip will then switch the burst size back to the normal operating burst size of 4.

Read Multiple with Read Line Enabled – When both the Read Multiple and Read Line modes have been enabled, the Read Line command will not be issued if the above conditions are met. Instead, a Read Multiple command will be issued, even though the conditions for Read Line have been met.

If the Read Multiple mode is enabled and the Read Line mode has been disabled, Read Multiple commands will still be issued if the Read Multiple conditions are met.

3.2.5 Unsupported PCI Commands

The LSI53C860 does not respond to reserved commands, special cycle, dual address cycle, or interrupt acknowledge commands as a slave. It will never generate these commands as a master.

The PCI bus commands and encoding types appear in [Table 3.1](#).

Table 3.1 PCI Bus Commands and Encoding Types

C_BE[3:0]	Command Type	Supported as Master	Supported as Slave
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read Cycle	Yes	Yes
0011	I/O Write Cycle	Yes	Yes
0100	Reserved	N/A	N/A
0101	Reserved	N/A	N/A
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	N/A	N/A
1001	Reserved	N/A	N/A
1010	Configuration Read	No	Yes
1011	Configuration Write	No	Yes
1100	Memory Read Multiple	Yes	No (defaults to 0110)
1101	Dual Address Cycle	No	No
1110	Memory Read Line	Yes	No (defaults to 0110)
1111	Memory Write and Invalidate	Yes	No (defaults to 0111)

3.3 Configuration Registers

The Configuration registers are accessible only by system BIOS during PCI configuration cycles, and are not available to the user at any time. No other cycles, including SCRIPTS operations, can access these registers.

The lower 128 bytes hold configuration data while the upper 128 bytes hold the LSI53C860 operating registers, which are described in [Chapter 5, “Operating Registers.”](#) The operating registers can be accessed by SCRIPTS or the host processor.

Note: The configuration register descriptions are provided for general information only, to indicate which PCI configuration addresses are supported in the LSI53C860.

For detailed information, refer to the PCI Specification.

All PCI-compliant devices, such as the LSI53C860, must support the [Vendor ID](#), [Device ID](#), [Command](#), and [Status](#) registers. Support of other PCI-compliant registers is optional. In the LSI53C860, registers that are not supported are not writable and return all zeros when read. Only those registers and bits that are currently supported by the LSI53C860 are described in this chapter. For more detailed information on PCI registers, please see the PCI Specification.

[Table 3.2](#) shows the PCI configuration registers implemented by the LSI53C860. Addresses 0x40 through 0x7F are not defined.

Table 3.2 PCI Configuration Register Map

31		16 15		0
Device ID		Vendor ID		0x00
Status		Command		0x04
Class Code			Revision ID	0x08
Not Supported	Header Type	Latency Timer	Cache Line Size	0x0C
Base Address Zero (I/O)¹				0x10
Base Address One (Memory)²				0x14
Not Supported				0x18
Not Supported				0x1C
Not Supported				0x20
Not Supported				0x24
Reserved				0x28
Reserved				0x2C
Reserved				0x30
Reserved				0x34
Reserved				0x38
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	0x3C

1. I/O Base is supported.

2. Memory Base is supported.

Note: Addresses 0x40 to 0x7F are not defined. All unsupported registers are not writable and return all zeros when read. Reserved registers also return zeros when read.

Register: 0x00**Vendor ID****Read Only**

15															0
VID															
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

VID**Vendor ID****[15:0]**

This field identifies the manufacturer of the device. The Vendor ID is 0x1000.

Register: 0x02**Device ID****Read Only**

15															0
DID															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DID**Device ID****[15:0]**

This field identifies the particular device. The LSI53C860 device ID is 0x0006.

Register: 0x04**Command****Read/Write**

15								9	8	7	6	5	4	3	2	1	0
R								SE	R	EPER	R	WIE	R	EBM	EMS	EIS	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles. When a zero is written to this register, the LSI53C860 is logically disconnected from the PCI bus for all accesses except configuration accesses.

In the LSI53C860, bits 3, 5, 7, and 9 are not implemented. Bits 10 through 15 are reserved.

R	Reserved	[15:10]
SE	SERR/ Enable This bit enables the SERR/ driver. SERR/ is disabled when this bit is clear. The default value of this bit is zero. This bit and bit 6 must be set to report address parity errors.	8
EPER	Enable Parity Error Response This bit allows the LSI53C860 to detect parity errors on the PCI bus and report these errors to the system. Only data parity checking is enabled. The LSI53C860 always generates parity for the PCI bus.	6
WIE	Write and Invalidate Mode This bit, when set, will cause Memory Write and Invalidate cycles to be issued on the PCI bus after certain conditions have been met. For more information on these conditions, refer to the section Section 3.2.3.2, “Memory Write and Invalidate Command.” To enable Write and Invalidate Mode, bit 0 in the Chip Test Three (CTEST3) register (Operating registers) must also be set.	4
EBM	Enable Bus Mastering This bit controls the LSI53C860’s ability to act as a master on the PCI bus. A value of zero disables the device from generating PCI bus master accesses. A value of one allows the LSI53C860 to behave as a bus master. The LSI53C860 must be a bus master in order to fetch SCRIPTS instructions and transfer data.	2
EMS	Enable Memory Space This bit controls the LSI53C860’s response to memory space accesses. A value of zero disables the device response. A value of one allows the LSI53C860 to respond to memory space accesses at the address specified by Base Address One (Memory) .	1
EIS	Enable I/O Space This bit controls the LSI53C860’s response to I/O space accesses. A value of zero disables the response. A value of one allows the LSI53C860 to respond to I/O space accesses at the address specified in Base Address Zero (I/O) .	0

Register: 0x06

Status

Read/Write

15	14	13	12	11	10	9	8	7								0
DPE	SSE	RMA	RTA	R	DT[1:0]		DPR	R								
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

The Status register is used to record status information for PCI bus related events.

In the LSI53C860, bits 0 through 4 are reserved and bits 5, 6, 7, and 11 are not implemented by the LSI53C860.

Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a one. For instance, to clear bit 15 and not affect any other bits, write the value 0x8000 to the register.

DPE	Detected Parity Error (from Slave)	16
	This bit will be set by the LSI53C860 whenever it detects a data parity error, even if parity error handling is disabled.	
SSE	Signaled System Error	14
	This bit is set whenever a device asserts the SERR/ signal.	
RMA	Master Abort (from Master)	13
	This bit should be set by a master device whenever its transaction (except for Special Cycle) is terminated with master-abort. All master devices should implement this bit.	
RTA	Received Target Abort (from Master)	12
	This bit should be set by a master device whenever its transaction is terminated with a target abort. All master devices should implement this bit.	
DT[1:0]	DEVSEL/ Timing	[10:9]
	These bits encode the timing of DEVSEL/.	

0b00	Fast
0b01	Medium
0b10	Slow
0b11	Reserved

These bits are read only and should indicate the slowest time that a device asserts DEVSEL/ for any bus command except Configuration Read and Configuration Write. The LSI53C860 supports 0b01.

DPR Data Parity Reported 8

This bit is set when the following three conditions are met:

- the bus agent asserted PERR/ itself or observed PERR/ asserted;
- the agent setting this bit acted as the bus master for the operation in which the error occurred; and
- the Parity Error Response bit in the [Command](#) register is set.

R Reserved [7:0]

Register: 0x08

Revision ID

Read Only

7						0	
RID							
LSI53C810A							
0	0	1	0	0	1	1	0
LSI53C810							
0	0	0	1	0	1	0	0

RID Revision ID [7:0]

This register specifies device and revision identifiers. In the LSI53C860, the upper nibble is 0000b. The lower nibble represents the current revision level of the device. It should have the same value as the Chip Revision Level bits in the [Chip Test Three \(CTEST3\)](#) register.

Register: 0x09**Class Code****Read Only**

23 0																							
CC																							
0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CC**Class Code****[23:0]**

This register is used to identify the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register-level programming interface. The value of this register is 0x010000, which indicates a SCSI controller.

Register: 0x0C**Cache Line Size****Read/Write**

7 0							
CLS							
0	0	0	0	0	0	0	0

CLS**Cache Line Size****[7:0]**

This register specifies the system cache line size in units of 32-bit words. Cache mode is enabled and disabled by the Cache Line Size Enable (CLSE) bit, bit 7 in the [DMA Control \(DCNTL\)](#) register. Setting this bit causes the LSI53C860 to align to cache line boundaries before allowing any bursting, except during MMOVs in which the read and write addresses are Burst Size boundary misaligned. For more information see [Section 3.2.1, "Support for PCI Cache Line Size Register."](#)

Register: 0x0D**Latency Timer****Read/Write**

7				0			
LT							
0	0	0	0	0	0	0	0

LT**Latency Timer****[7:0]**

The Latency Timer register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. The LSI53C860 supports this timer. All eight bits are writable, allowing latency values of 0–255 PCI clocks. Use the following equation to calculate an optimum latency value for the LSI53C860:

$\text{Latency} = 2 + (\text{Burst Size} * (\text{typical wait states} + 1))$.

Values greater than optimum are also acceptable.

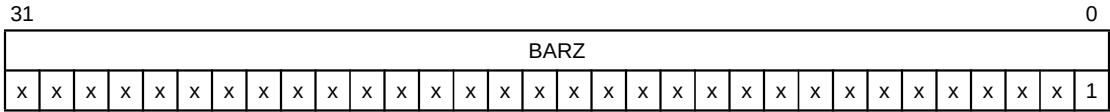
Register: 0x0E**Header Type****Read Only**

7				0			
HT							
0	0	0	0	0	0	0	0

HT**Header Type****[7:0]**

This register identifies the layout of bytes 0x10 through 0x3F in configuration space and also whether or not the device contains multiple functions. The value of this register is 0x00.

Register: 0x10
Base Address Zero (I/O)
Read/Write



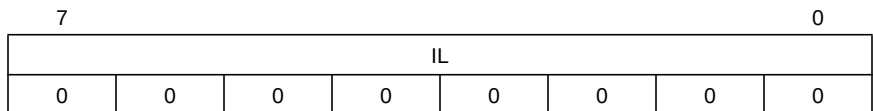
BARZ **Base Address Register Zero (I/O)** **[31:0]**
 This 32-bit register has bit zero hardwired to one. Bit 1 is reserved and must return a zero on all reads, and the other bits are used to map the device into I/O space.

Register: 0x14
Base Address One (Memory)
Read/Write



BARO **Base Address Register One** **[31:0]**
 This register has bit 0 hardwired to zero. For detailed information on the operation of this register, refer to the PCI Specification.

Register: 0x3C
Interrupt Line
Read/Write



IL **Interrupt Line** **[7:0]**
 This register is used to communicate interrupt line routing information. POST software will write the routing information into this register as it initiates and configures the system. The value in this register tells which input of

the system interrupt controller(s) has been connected to the device's interrupt pin. Values in this register are specified by system architecture.

Register: 0x3D

Interrupt Pin

Read Only

7							0
IP							
0	0	0	0	0	0	0	1

IP

Interrupt Pin

[7:0]

This register tells which interrupt pin the device uses. Its value is set to 0x01, for the INTA/ signal.

Register: 0x3E

Min_Gnt

Read Only

7								0
MG								
0	0	0	1	0	0	0	1	

MG

Min_Gnt

[7:0]

This register is used to specify the desired settings for Latency Timer values. Min_Gnt is used to specify how long a burst period the device needs. The value specified in this register is in units of 0.25 microseconds. Values of zero indicate that the device has no major requirements for the settings of Latency Timers. The LSI53C810A sets the Min_Gnt register to 0x11.

Register: 0x3F

Max_Lat

Read Only

7				0			
ML							
0	1	0	0	0	0	0	0

ML **Max_Lat** **[7:0]**

This register is used to specify the desired settings for Latency Timer values. Max_Lat is used to specify how often the device needs to gain access to the PCI bus. The value specified in these registers is in units of 0.25 microseconds. Values of zero indicate that the device has no major requirements for the settings of Latency Timers. The LSI53C810A sets the Max_Lat register to 0x40.

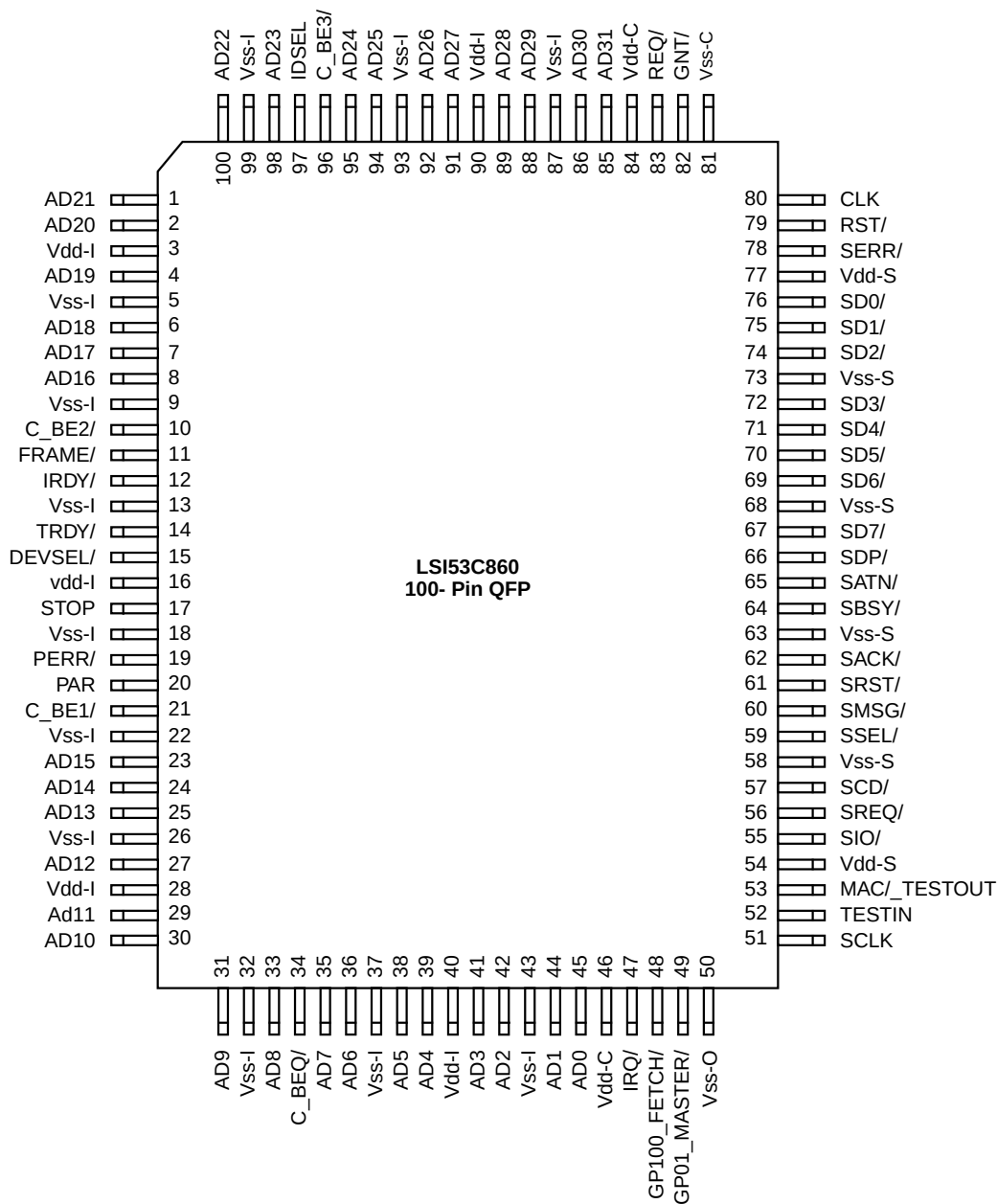
Chapter 4

Signal Descriptions

This chapter presents the LSI53C860 pin configuration and signal definitions using tables and illustrations. [Figure 4.1](#) is the pin diagram and [Figure 4.2](#) is a functional signal grouping. The pin definitions are presented in [Table 4.1](#) through [Table 4.8](#). This chapter is divided into the following sections:

- [Section 4.1, “PCI Bus Interface Signals”](#)
- [Section 4.2, “SCSI Bus Interface Signals”](#)

Figure 4.1 LSI53C860 Pin Diagram



Note: NC pins are not connected.

Note: The decoupling capacitor arrangement shown above is recommended to maximize the benefits of the internal split ground system. Capacitor values between 0.01 and 0.1 μF should provide adequate noise isolation. Because of the number of high current drivers on the LSI53C860, a multilayer PC board with power and ground planes is required.

A slash (/) at the end of the signal name indicates that the active state occurs when the signal is at a LOW voltage. When the slash is absent, the signal is active at a HIGH voltage.

There are four signal type definitions:

- I** Input, a standard input only signal.
- O** Output, a standard output driver (typically a Totem Pole Output).
- T/S** 3-state, a bidirectional, 3-state input/output signal.
- S/T/S** Sustained 3-state, an active LOW 3-state signal owned and driven by one and only one agent at a time.

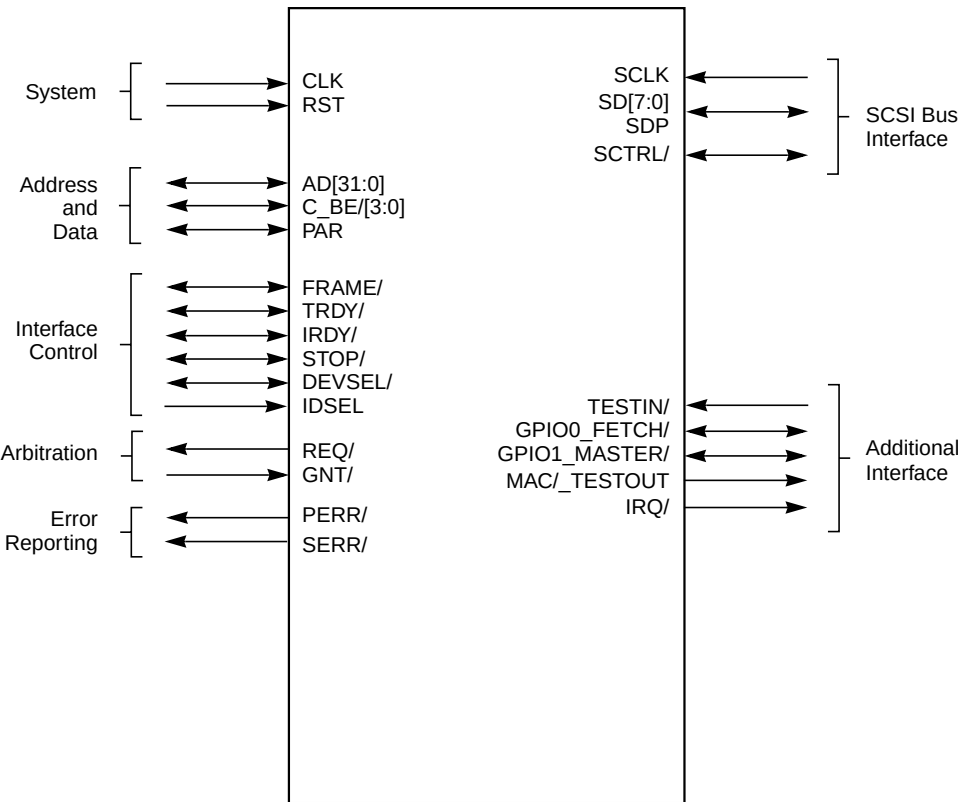
Table 4.1 describes the Power and Ground Signals group.

Table 4.1 Power and Ground Signals

Name	Pin No.	Description
V_{SS-I}	5, 9, 13, 18, 22, 26, 32, 37, 43, 87, 93, 99	Power supplies to the PCI I/O pins.
V_{DD-I}^1	3, 16, 28, 40, 90	Power supplies to the PCI I/O pins.
V_{SS-S}	58, 63, 68, 73	Power supplies to the SCSI bus I/O pins.
V_{DD-S}	54, 77	Power supplies to the SCSI bus I/O pins.
V_{SS-C}	50, 81	Power supplies to the internal logic core.
V_{DD-C}	46, 84	Power supplies to the internal logic core.

1. These pins can accept a V_{DD} source of 3.3 or 5 V. All other V_{DD} pins must be supplied 5 V.

Figure 4.2 Functional Signal Grouping



4.1 PCI Bus Interface Signals

The PCI signal definitions are organized into the following functional groups: [Power and Ground Signals](#), [System Signals](#), [Address and Data Signals](#), [Interface Control Signals](#), [Arbitration Signals](#), and [Error Reporting Signals](#).

4.1.1 System Signals

[Table 4.2](#) describes the System Signals group.

Table 4.2 System Signals

Name	Pin No.	Type	Description
CLK	80	I	Clock provides timing for all transactions on the PCI bus and is an input to every PCI device. All other PCI signals are sampled on the rising edge of CLK, and other timing parameters are defined with respect to this edge. Clock can optionally serve as the SCSI core clock, but this may effect fast SCSI transfer rates.
RST/	79	I	Reset forces the PCI sequencer of each device to a known state. All T/S and S/T/S signals are forced to a high impedance state, and all internal logic is reset. The RST/ input is synchronized internally to the rising edge of CLK. The CLK input must be active while RST/ is active to properly reset the device.

4.1.2 Address and Data Signals

Table 4.3 describes the Address and Data Signals group.

Table 4.3 Address and Data Signals

Name	Pin No.	Type	Description
AD[31:0]	85, 86, 88, 89, 91, 92, 94, 95, 98, 100, 1, 2, 4, 6, 7, 8, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36, 38, 39, 41, 42, 44, 45	T/S	Physical Dword Address and Data are multiplexed on the same PCI pins. During the first clock of a transaction, AD[31:0] contain a physical byte address. During subsequent clocks, AD[31:0] contain data. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. AD[7:0] define the least significant byte, and AD[31:24] define the most significant byte.
C_BE/[3:0]	96, 10, 21, 34	T/S	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C_BE/[3:0] define the bus command. During the data phase, C_BE/[3:0] are used as byte enables. The byte enables determine which byte lanes carry meaningful data. C_BE/[0] applies to byte 0, and C_BE/[3] to byte 3.
PAR	20	T/S	Parity is the even parity bit that protects the AD[31:0] and C_BE/[3:0] lines. During address phase, both the address and command bits are covered. During data phase, both data and byte enables are covered.

4.1.3 Interface Control Signals

Table 4.4 describes the Interface Control Signals group.

Table 4.4 Interface Control Signals

Name	Pin No.	Type	Description
FRAME/	11	S/T/S	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME/ is asserted to indicate that a bus transaction is beginning. While FRAME/ is asserted, data transfers continue. While FRAME/ is deasserted, either the transaction is in the final data phase or the bus is idle.
TRDY/	14	S/T/S	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY/ is used with IRDY/. A data phase is completed on any clock when used with IRDY/. A data phase is completed on any clock when both TRDY/ and IRDY/ are sampled asserted. During a read, TRDY/ indicates that valid data is present on AD[31:0]. During a write, it indicates that the target is prepared to accept data. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together.
IRDY/	12	S/T/S	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY/ is used with TRDY/. A data phase is completed on any clock when both IRDY/ and TRDY/ are sampled asserted. During a write, IRDY/ indicates that valid data is present on AD[31:0]. During a read, it indicates that the master is prepared to accept data. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together.
STOP/	17	S/T/S	Stop indicates that the selected target is requesting the master to stop the current transaction.
DEVSEL/	15	S/T/S	Device Select indicates that the driving device has decoded its address as the target of the current access. As an input, it indicates to a master whether any device on the bus has been selected.
IDSEL	97	I	Initialization Device Select is used as a chip select in place of the upper 24 address lines during configuration read and write transactions.

4.1.4 Arbitration Signals

[Table 4.5](#) describes the Arbitration Signals group.

Table 4.5 Arbitration Signals

Name	Pin No.	Type	Description
REQ/	83	O	Request indicates to the system arbiter that this agent desires use of the PCI bus. This is a point-to-point signal. Every master has its own REQ/ signal.
GNT/	82	I	Grant indicates to the agent that access to the PCI bus has been granted. This is a point-to-point signal. Every master has its own GNT/ signal.

4.1.5 Error Reporting Signals

[Table 4.6](#) describes the Error Reporting Signals group.

Table 4.6 Error Reporting Signals

Name	Pin No.	Type	Description
PERR/	19	S/T/S	Parity Error may be pulsed active by an agent that detects a data parity error. PERR/ can be used by any agent to signal data corruption. However, on detection of a PERR/ pulse, the central resource may generate a nonmaskable interrupt to the host CPU, which often implies the system is unable to continue operation once error processing is complete.
SERR/	78	O	System Error is an open drain output used to report address parity errors.

4.2 SCSI Bus Interface Signals

The SCSI signal definitions are organized into the following functional groups: [SCSI Bus Interface Signals](#) and [Additional Interface Signals](#).

4.2.1 SCSI Bus Interface Signals

[Table 4.7](#) describes the SCSI Bus Interface Signals group.

Table 4.7 SCSI Bus Interface Signals

Name	Pin No.	Type	Description
SCLK	51	I	SCSI Clock is used to derive all SCSI-related timings. The speed of this clock is determined by the application requirements. In some applications, SCLK may be sourced internally from the PCI bus clock (CLK). If SCLK is internally sourced, tie the SCLK pin LOW.
SD[7:0], SDP	67, 69, 70, 71, 72, 74, 75, 76, 66	I/O	SCSI Data includes the following data lines and parity signals: SD[7:0] (8-bit SCSI data bus), and SDP (SCSI data parity bit).
SCTRL/	57, 55, 60, 56, 62, 64, 65, 61, 59	I/O	SCSI Control includes the following signals: SCD/ SCSI phase line, command/data SIO/ SCSI phase line, input/output SMSG/ SCSI phase line, message SREQ/ Data handshake signal from target device SACK/ Data handshake signal from initiator device SBSY/ SCSI bus arbitration signal, busy SATN/ SCSI Attention, the initiator is requesting a message out phase SRST/ SCSI bus reset SSEL/ SCSI bus arbitration signal, select device

4.2.2 Additional Interface Signals

Table 4.8 describes the Additional Interface Signals group.

Table 4.8 Additional Interface Signals

Name	Pin No.	Type	Description
TESTIN/	52	I	Test In. When this pin is driven LOW, the LSI53C860 connects all inputs and outputs to an “AND tree.” The SCSI control signals and data lines are not connected to the “AND tree.” The output of the “AND tree” is connected to the Test Out pin. This allows manufacturers to verify chip connectivity and determine exactly which pins are not properly attached. When the TESTIN pin is driven LOW, internal pull-ups are enabled on all input, output, and bidirectional pins, all outputs and bidirectional signals will be 3-stated, and the MAC/_TESTOUT pin will be enabled. Connectivity can be tested by driving one of the LSI53C860 pins LOW. The MAC/_TESTOUT pin should respond by also driving LOW.
GPIO0_FETCH/	48	I/O	General Purpose I/O pin. Optionally, when driven LOW, this pin indicates that the next bus request will be for an opcode fetch. This pin powers up as a general purpose input. This pin has two specific purposes in the LSI Logic SDMS software. SDMS software uses it to toggle SCSI device LEDs, turning on the LED whenever the LSI53C860 is on the SCSI bus. SDMS software drives this pin LOW to turn on the LED, or drives it HIGH to turn off the LED. This signal can also be used as data I/O for serial EEPROM access. In this case it is used with the GPIO0 pin, which serves as a clock, and the pin can be controlled from PCI configuration register 0x35 or observed from the General Purpose (GPREG) operating register, at address 0x07.
GPIO1_MASTER/	49	I/O	General Purpose I/O pin. Optionally, when driven LOW, indicates that the LSI53C860 is bus master. This pin powers up as a general purpose input. LSI Logic SDMS software supports use of this signal in serial EEPROM applications, when enabled, in combination with the GPIO0 pin. When this signal is used as a clock for serial EEPROM access, the GPIO1 pin serves as data, and the pin is controlled from PCI configuration register 0x35.

Table 4.8 Additional Interface Signals (Cont.)

Name	Pin No.	Type	Description
MAC/_ TESTOUT	53	T/S	Memory Access Control. This pin can be programmed to indicate local or system memory accesses (non-PCI applications). It is also used to test the connectivity of the LSI53C860 signals using an “AND tree” scheme. The MAC/_TESTOUT pin is only driven as the Test Out function when the TESTIN/ pin is driven LOW.
IRQ/	47	O	Interrupt. This signal, when asserted LOW, indicates that an interrupting condition has occurred and that service is required from the host CPU. The output drive of this pin is programmed as either open drain with an internal weak pull-up or, optionally, as a totem pole driver. Refer to the description of DMA Control (DCNTL) register, bit 3, for additional information.

Chapter 5

Operating Registers

This section contains descriptions of all LSI53C860 operating registers. [Table 5.1](#), the register map, lists registers by operating and configuration addresses. The terms “set” and “assert” are used to refer to bits that are programmed to a binary one. Similarly, the terms “deassert,” “clear,” and “reset” are used to refer to bits that are programmed to a binary zero. Any bits marked as reserved should always be written to zero; mask all information read from them. Reserved bit functions may be changed at any time. Unless otherwise indicated, all bits in registers are active high, that is, the feature is enabled by setting the bit. The bottom row of every register diagram shows the default register values, which are enabled after the chip is powered on or reset.

Note: The only register that the host CPU can access while the LSI53C860 is executing SCRIPTS is the [Interrupt Status \(ISTAT\)](#) register. Attempts to access other registers will interfere with the operation of the chip. However, all operating registers are accessible with SCRIPTS. All read data is synchronized and stable when presented to the PCI bus.

The LSI53C860 cannot fetch SCRIPTS instructions from the operating register space. Instructions must be fetched from system memory.

Table 5.1 LSI53C860 Register Address Map

31	16 15			0	Mem I/O	Config
SCNTL3	SCNTL2	SCNTL1	SCNTL0	0x00	0x80	
GPREG	SDID	SXFER	SCID	0x04	0x84	
SBCL	SSID	SOCL	SFBR	0x08	0x88	
SSTAT2	SSTAT1	SSTAT0	DSTAT	0x0C	0x8C	
DSA				0x10	0x90	
Reserved			ISTAT	0x14	0x94	
CTEST3	CTEST2	CTEST1	Reserved	0x18	0x98	
TEMP				0x1C	0x9C	
CTEST6	CTEST5	CTEST4	DFIFO	0x20	0xA0	
DCMD	DBC			0x24	0xA4	
DNAD				0x28	0xA8	
DSP				0x2C	0xAC	
DSPS				0x30	0xB0	
SCRATCHA				0x34	0xB4	
DCNTL	SBR	DIEN	DMODE	0x38	0xB8	
ADDER				0x3C	0xBC	
SIST1	SIST0	SIEN1	SIEN0	0x40	0xC0	
GPCNTL	MACNTL	SWIDE	SLPAR	0x44	0xC4	
Reserved	RESPID	STIME1	STIME0	0x48	0xC8	
STEST3	STEST2	STEST1	STEST0	0x4C	0xCC	
Reserved		SIDL		0x50	0xD0	
Reserved		SODL		0x54	0xD4	
Reserved		SBDL		0x58	0xD8	
SCRATCH B				0x5C	0xDC	

Register: 0x00 (0x80)
SCSI Control Zero (SCNTL0)
Read/Write

7	6	5	4	3	2	1	0
ARB[1:0]		START	WATN	EPC	R	AAP	TRG
1	1	0	0	0	x	0	0

ARB[1:0]

Arbitration Mode Bits 1 and 0

[7:6]

ARB1	ARB0	Arbitration Mode
0	0	Simple arbitration
0	1	Reserved
1	0	Reserved
1	1	Full arbitration, selection/reselection

Simple Arbitration

1. The LSI53C860 waits for a bus free condition to occur.
2. It asserts SBSY/ and its SCSI ID (contained in the [SCSI Chip ID \(SCID\)](#) register) onto the SCSI bus. If the SSEL/ signal is asserted by another SCSI device, the LSI53C860 deasserts SBSY/, deasserts its ID, and sets the Lost Arbitration bit (bit 3) in the [SCSI Status Zero \(SSTAT0\)](#) register.
3. After an arbitration delay, the CPU should read the [SCSI Bus Data Lines \(SBDL\)](#) register to check if a higher priority SCSI ID is present. If no higher priority ID bit is set, and the Lost Arbitration bit is not set, the LSI53C860 has won arbitration.
4. Once the LSI53C860 has won arbitration, SSEL/ must be asserted using the [SCSI Output Control Latch \(SOCL\)](#) for a bus clear plus a bus settle delay (1.2 μ s) before a low level selection can be performed.

Full Arbitration, Selection/Reselection

1. The LSI53C860 waits for a bus free condition.
2. It asserts SBSY/ and its SCSI ID (the highest priority ID stored in the [SCSI Chip ID \(SCID\)](#) register) onto the SCSI bus.
3. If the SSEL/ signal is asserted by another SCSI device or if the LSI53C860 detects a higher priority ID, the LSI53C860 deasserts BSY, deasserts its ID, and waits until the next bus free state to try arbitration again.
4. The LSI53C860 repeats arbitration until it wins control of the SCSI bus. When it has won, the Won Arbitration bit is set in the [SCSI Status Zero \(SSTAT0\)](#) register, bit 2.
5. The LSI53C860 performs selection by asserting the following onto the SCSI bus: SSEL/, the target's ID (stored in the [SCSI Destination ID \(SDID\)](#) register), and the LSI53C860's ID (stored in the [SCSI Chip ID \(SCID\)](#) register).
6. After a selection is complete, the Function Complete bit is set in the [SCSI Interrupt Status Zero \(SIST0\)](#) register, bit 6.
7. If a selection time-out occurs, the Selection Time-Out bit is set in the [SCSI Interrupt Status One \(SIST1\)](#) register, bit 2.

START

Start Sequence

5

When this bit is set, the LSI53C860 will start the arbitration sequence indicated by the Arbitration Mode bits. The Start Sequence bit is accessed directly in low-level mode; during SCSI SCRIPTS operations, this bit is controlled by the SCRIPTS processor. An arbitration sequence should not be started if the connected (CON) bit in the [SCSI Control One \(SCNTL1\)](#) register, bit 4, indicates that the LSI53C860 is already connected to the SCSI bus. This bit is automatically cleared when the arbitration sequence is complete. If a sequence is aborted, bit 4 in the [SCSI Control One \(SCNTL1\)](#) register should be checked to verify that the LSI53C860 did not connect to the SCSI bus.

WATN	Select with SATN/ on a Start Sequence 4 When this bit is set and the LSI53C860 is in initiator mode, the SATN/ signal will be asserted during LSI53C860 selection of a SCSI target device. This is to inform the target that the LSI53C860 has a message to send. If a selection time-out occurs while attempting to select a target device, SATN/ will be deasserted at the same time SSEL/ is deasserted. When this bit is clear, the SATN/ signal will not be asserted during selection. When executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor, but it may be set manually in low level mode.
EPC	Enable Parity Checking 3 When this bit is set, the SCSI data bus is checked for odd parity when data is received from the SCSI bus in either initiator or target mode. If a parity error is detected, bit 0 of the SCSI Interrupt Status Zero (SISTO) register is set and an interrupt may be generated. If the LSI53C860 is operating in initiator mode and a parity error is detected, SATN/ can optionally be asserted, but the transfer continues until the target changes phase. When this bit is cleared, parity errors are not reported.
R	Reserved 2
AAP	Assert SATN/ on Parity error 1 When this bit is set, the LSI53C860 automatically asserts the SATN/ signal upon detection of a parity error. SATN/ is only asserted in initiator mode. The SATN/ signal is asserted before deasserting SACK/ during the byte transfer with the parity error. The Enable Parity Checking bit must also be set for the LSI53C860 to assert SATN/ in this manner. A parity error is detected on data received from the SCSI bus. If the Assert SATN/ on Parity Error bit is cleared or the Enable Parity Checking bit is cleared, SATN/ will not be automatically asserted on the SCSI bus when a parity error is received.
TRG	Target Role 0 This bit determines the default operating role of the LSI53C860. The user must manually set target or initiator

role. This can be done using the SCRIPTS language (SET TARGET or CLEAR TARGET). When this bit is set, the chip is a target device by default. When this bit is cleared, the LSI53C860 is an initiator device by default.

Caution: Writing this bit while not connected may cause the loss of a selection or reselection due to the changing of target or initiator roles.

Register: 0x01 (0x81)
SCSI Control One (SCNTL1)
Read/Write

7	6	5	4	3	2	1	0
EXC	ADB	DHP	CON	RST	AESP	IARB	SST
0	0	0	0	0	0	0	0

- EXC** **Extra Clock Cycle of Data Setup** **7**
 When this bit is set, an extra clock period of data setup is added to each SCSI data send transfer. The extra data setup time can provide additional system design margin, though it will affect the SCSI transfer rates. Clearing this bit disables the extra clock cycle of data setup time. Setting this bit only affects SCSI send operations.
- ADB** **Assert SCSI Data Bus** **6**
 When this bit is set, the LSI53C860 drives the contents of the [SCSI Output Data Latch \(SODL\)](#) register onto the SCSI data bus. When the LSI53C860 is an initiator, the SCSI I/O signal must be inactive to assert the SODL contents onto the SCSI bus. When the LSI53C860 is a target, the SCSI I/O signal must be active for the SODL contents to be asserted onto the SCSI bus. The contents of the [SCSI Output Data Latch \(SODL\)](#) register can be asserted at any time, even before the LSI53C860 is connected to the SCSI bus. This bit should be cleared when executing SCSI SCRIPTS. It is normally used only for diagnostics testing or operation in low level mode.
- DHP** **Disable Halt on Parity Error or ATN (Target Only)** **5**
 The DHP bit is only defined for target role. When this bit is cleared, the LSI53C860 halts the SCSI data transfer when a parity error is detected or when the SATN/ signal is asserted. If SATN/ or a parity error is received in the

middle of a data transfer, the LSI53C860 may transfer up to three additional bytes before halting to synchronize between internal core cells. During synchronous operation, the LSI53C860 transfers data until there are no outstanding synchronous offsets. If the LSI53C860 is receiving data, any data residing in the DMA FIFO is sent to memory before halting.

When this bit is set, the LSI53C860 does not halt the SCSI transfer when SATN/ or a parity error is received.

CON	Connected 4
	This bit is automatically set any time the LSI53C860 is connected to the SCSI bus as an initiator or as a target. It is set after the LSI53C860 successfully completes arbitration or when it has responded to a bus initiated selection or reselection. This bit is also set after the chip wins simple arbitration when operating in low level mode. When this bit is clear, the LSI53C860 is not connected to the SCSI bus. The CPU can force a connected or disconnected condition by setting or clearing this bit. This feature would be used primarily during loopback mode.
RST	Assert SCSI RST/ Signal 3
	Setting this bit asserts the SRST/ signal. The SRST/ output remains asserted until this bit is cleared. The 25 μs minimum assertion time defined in the SCSI specification must be timed out by the controlling microprocessor or a SCRIPTS loop.
AESP	Assert Even SCSI Parity (force bad parity) 2
	When this bit is set, the LSI53C860 asserts even parity. It forces a SCSI parity error on each byte sent to the SCSI bus from the LSI53C860. If parity checking is enabled, then the LSI53C860 checks data received for odd parity. This bit is used for diagnostic testing and should be clear for normal operation. It can be used to generate parity errors to test error handling functions.
IARB	Immediate Arbitration 1
	Setting this bit causes the SCSI core to immediately begin arbitration once a Bus Free phase is detected following an expected SCSI disconnect. This bit is useful

for multithreaded applications. The ARB[1:0] bits in [SCSI Control Zero \(SCNTL0\)](#) should be set for full arbitration and selection before setting this bit.

Arbitration will be retried until won. At that point, the LSI53C860 will hold BSY and SEL asserted, and wait for a select or reselect sequence to be requested. The Immediate Arbitration bit will be reset automatically when the selection or reselection sequence is completed, or times out. Interrupts will not occur until after this bit is reset.

An unexpected disconnect condition will clear IARB without attempting arbitration. See the SCSI Disconnect Unexpected bit ([SCSI Control Two \(SCNTL2\)](#), bit 7) for more information on expected versus unexpected disconnects.

An immediate arbitration sequence can be aborted. First, the Abort bit in the [Interrupt Status \(ISTAT\)](#) register should be set. Then one of two things will eventually happen:

- The Won Arbitration bit ([SCSI Status Zero \(SSTAT0\)](#), bit 2) will be set. In this case, the Immediate Arbitration bit needs to be reset. This will complete the abort sequence and disconnect the LSI53C860 from the SCSI bus. If it is not acceptable to go to Bus Free phase immediately following the arbitration phase, a low level selection may be performed instead.
- The abort will complete because the LSI53C860 loses arbitration. This can be detected by the Immediate Arbitration bit being cleared. The Lost Arbitration bit ([SCSI Status Zero \(SSTAT0\)](#), bit 3) should not be used to detect this condition. No further action needs to be taken in this case.

SST

Start SCSI Transfer

0

This bit is automatically set during SCRIPTS execution, and should not be used. It causes the SCSI core to begin a SCSI transfer, including SREQ/SACK handshaking. The determination of whether the transfer is a send or receive is made according to the value written to the I/O bit in [SCSI Output Control Latch \(SOCL\)](#). This bit is self-clearing. It should not be set for low level operation.

Caution: Writing to this register while not connected may cause the loss of a selection/reselection by resetting the Connected bit.

Register: 0x02 (0x82)
SCSI Control Two (SCNTL2)
Read/Write

7	6						0
SDU	R						
0	x	x	x	x	x	x	x

SDU	SCSI Disconnect Unexpected	7
	This bit is valid in initiator mode only. When this bit is set, the SCSI core is not expecting the SCSI bus to enter the Bus Free phase. If it does, an unexpected disconnect error will be generated (see the Unexpected Disconnect bit in the SCSI Interrupt Status Zero (SIST0) register, bit 2). During normal SCRIPTS mode operation, this bit is set automatically whenever the SCSI core is reselected or successfully selects another SCSI device. The SDU bit should be reset with a register write (Move 0x7f and SCNTL2 TO SCNTL2) before the SCSI core expects a disconnect to occur, normally prior to sending an Abort, Abort Tag, Bus Device Reset, Clear Queue or Release Recovery message, or before deasserting SACK/ after receiving a Disconnect command or Command Complete message.	
R	Reserved	[6:0]

Register: 0x03 (0x83)
SCSI Control Three (SCNTL3)
Read/Write

7	6	4	3	2	0
Ultra	SCF[2:0]			R	CCF[2:0]
0x	0	0	0	x	0 0 0

ULTRA	ULTRA Enable	7
	Setting this bit enables Ultra SCSI synchronous SCSI transfers in systems that have an 80 MHz clock. The default value of this bit is 0. This bit should remain cleared in systems that have a 40 MHz clock.	
	When this bit is set, the signal filtering period for SREQ/ and SACK/ automatically changes to 15 ns, regardless of the value of the Extend REQ/ACK Filtering bit in the SCSI Test Two (STEST2) register.	
SCF[2:0]	Synchronous Clock Conversion Factor	[6:4]
	These bits select the factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. The bits are encoded as per Table 5.2 . For synchronous receive, the output of this divider is always divided by 4 and that value determines the transfer rate. For example, if SCLK is 80 MHz, and the SCF value is set to divide by one, then the maximum synchronous receive rate is 20 Mbytes/s $((80/1)/4 = 20$.	
	For synchronous send, the output of this divider gets divided by the transfer period (XFERP) bits in the SCSI Transfer (SXFER) register, and that value determines the transfer rate. For valid combinations of the SCF and XFERP, see Table 5.4 and Table 5.5 .	

Table 5.2 Synchronous Clock Conversion Factor

SCF2	SCF1	SCF0	Factor Frequency
0	0	0	SCLK/3
0	0	1	SCLK/1
0	1	0	SCLK/1.5
0	1	1	SCLK/2
1	0	0	SCLK/3
1	0	1	SCLK/4
1	1	0	Reserved
1	1	1	Reserved

Note: To migrate from a Fast SCSI-2 system with a 40 MHz clock, divide the clock by a factor of two or more to achieve the same synchronous transfer rate in a system with an 80 MHz clock.

For additional information on how the synchronous transfer rate is determined, see [Section 2.6.3, “Synchronous Operation,” page 2-13](#).

R **Reserved** **3**

CCF[2:0] **Clock Conversion Factor** **[2:0]**

These bits select the frequency of the SCLK for asynchronous SCSI operations. The bits are encoded as per the following table. All other combinations are reserved and should never be used.

Table 5.3 Asynchronous Clock Conversion Factor

CCF2	CCF1	CCF0	SCSI Clock (MHz)
0	0	0	50.01–66.00
0	0	1	16.67–25.00
0	1	0	25.01–37.50
0	1	1	37.51–50.00
1	0	0	50.01–66.00
1	0	1	75.01–80.00
1	1	0	Reserved
1	1	1	Reserved

Register: 0x04 (0x84)**SCSI Chip ID (SCID)****Read/Write**

7	6	5	4	3	2	0	
R	RRE	SRE	R		ENC[2:0]		
x	0	0	x	0	0	0	0

R **Reserved** **7****RRE** **Enable Response to Reselection** **6**

When this bit is set, the LSI53C860 is enabled to respond to bus-initiated reselection at the chip ID in the [Response ID \(RESPID\)](#) register. Note that the LSI53C860 will not automatically reconfigure itself to initiator mode as a result of being reselected.

SRE **Enable Response to Selection** **5**

When this bit is set, the LSI53C860 is able to respond to bus-initiated selection at the chip ID in the [Response ID \(RESPID\)](#) register. Note that the LSI53C860 will not automatically reconfigure itself to target mode as a result of being selected.

R **Reserved** **[4:3]**

ENC{2:0} **Encoded LSI53C860 Chip SCSI ID** **[2:0]**

These bits are used to store the LSI53C860 encoded SCSI ID. This is the ID which the chip will assert when arbitrating for the SCSI bus. The IDs that the LSI53C860 will respond to when being selected or reselected are configured in the [Response ID \(RESPID\)](#) register. The priority of the 8 possible IDs, in descending order is:

Highest				Lowest			
7	6	5	4	3	2	1	0

Register: 0x05 (0x85)

SCSI Transfer (SXFER)

Read/Write

7			5		4	3		0	
TP[2:0]			R		MO[3:0]				
0	0	0	x		0	0	0	0	

Note: When using Table Indirect I/O commands, bits [7:0] of this register will be loaded from the I/O data structure.

For additional information on how the synchronous transfer rate is determined, refer to [Chapter 2, “Functional Description.”](#)

TP[2:0] **SCSI Synchronous Transfer Period** **[7:5]**

These bits determine the SCSI synchronous transfer period (XFERP) used by the LSI53C860 when sending synchronous SCSI data in either initiator or target mode. These bits control the programmable dividers in the chip.

Note: For Ultra SCSI transfers, the ideal transfer period is 4, and 5 is acceptable. Setting the transfer period to a value greater than 5 is not recommended.

TP2	TP1	TP0	XFERP
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11

Use the following formula to calculate the synchronous send and receive rates. [Table 5.4](#) and [Table 5.5](#) show examples of possible bit combinations.

Synchronous Send Rate = (SCLK/SCF)/XFERP

Synchronous Receive Rate = (SCLK/SCF) /4

Where:

SCLK SCSI clock

SCF Synchronous Clock Conversion Factor,
SCNTL3 register, bits [6:4]

XFERP Transfer period, SXFER register, bits [7:5]

Table 5.4 Examples of Synchronous Transfer Periods and Rates for SCSI-1

SCLK (MHz)	SCF ÷ SCNTL3 Bits [6:4]	XFERP SXFER Bits [7:5]	Synch. Send Rate (Mbytes/s)	Synch. Send Period (ns)	Synch. Receive Rate (Mbytes/s)	Synch. Receive Period (ns)
80	4	4	5	200	5	200
80	4	5	4	250	5	200
66.67	3	4	5.55	180	5.55	180
66.67	3	5	4.44	225	5.55	180
50	2	4	6.25	160	6.25	160
50	2	5	5	200	6.25	160

Table 5.4 Examples of Synchronous Transfer Periods and Rates for SCSI-1 (Cont.)

SCLK (MHz)	SCF ÷ SCNTL3 Bits [6:4]	XFERP SXFER Bits [7:5]	Synch. Send Rate (Mbytes/s)	Synch. Send Period (ns)	Synch. Receive Rate (Mbytes/s)	Synch. Receive Period (ns)
40	2	4	5	200	5	200
37.50	1.5	4	6.25	160	6.25	160
33.33	1.5	4	5.55	180	5.55	180
25	1	4	6.25	160	6.25	160
20	1	4	5	200	5	200
16.67	1	4	4.17	240	4.17	240

Table 5.5 Examples of Synchronous Transfer Periods and Rates for Fast SCSI

SCLK (MHz)	SCF ÷ SCNTL3 Bits [6:4]	XFERP SXFER Bits [7:5]	Synch. Send Rate (Mbytes/s)	Synch. Send Period (ns)	Synch. Receive Rate (Mbytes)	Synch. Receive Period (ns)
80	1	4	20	50	20	50
80	2	4	10	100	10	100
66.67	1.5	4	11.11	90	11.11	90
66.67	1	5	8.88	112.5	11.11	90
50	1	4	12.5	80	12.5	80
50	1	5	10	100	12.5	80
40	1	4	10	100	10.0	100
37.50	1	4	9.375	106.67	9.375	106.67
33.33	1	4	8.33	120	8.33	120
25	1	4	6.25	160	6.25	160
20	1	4	5	200	5	200
16.67	1	4	4.17	240	4.17	240

R **Reserved** **4**

MO[3:0] **Max SCSI Synchronous Offset** **[3:0]**
 These bits describe the maximum SCSI synchronous offset used by the LSI53C860 when transferring synchronous SCSI data in either initiator or target mode.

The following table describes the possible combinations and their relationship to the synchronous data offset used by the LSI53C860. These bits determine the LSI53C860's method of transfer for Data-In and Data-Out phases only. All other information transfers will occur asynchronously.

Table 5.6 SCSI Synchronous Offset Values

MO3	MO2	MO1	MO0	Synchronous Offset
0	0	0	0	0-Asynchronous
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	x	x	1	Reserved
1	x	1	x	Reserved
1	1	x	x	Reserved

Register: 0x06 (0x86)
SCSI Destination ID (SDID)
Read/Write

7					3		2		0	
R					ENC[3:0]					
x	x	x	x	x	0	0	0			

R **Reserved** **[7:3]**

ENC[2:0] **Encoded Destination SCSI ID** **[2:0]**

Writing these bits sets the SCSI ID of the intended initiator or target during SCSI reselection or selection phases, respectively. When executing SCRIPTS, the SCRIPTS processor writes the destination SCSI ID to this register. The SCSI ID is defined by the user in a SCRIPTS SELECT or RESELECT instruction. The value written should be the binary-encoded ID value. The priority of the 8 possible IDs, in descending order, is:

Register: 0x08 (0x88)
SCSI First Byte Received (SFBR)
Read/Write

7						0	
IB							
0	0	0	0	0	0	0	0

This register contains the first byte received in any asynchronous information transfer phase. For example, when the LSI53C860 is operating in initiator role, this register contains the first byte received in Message In, Status Phase, Reserved In and Data In.

When a Block Move instruction is executed for a particular phase, the first byte received is stored in this register—even if the present phase is the same as the last phase. The first byte-received value for a particular input phase is not valid until after a MOVE instruction is executed.

This register is also the accumulator for register read-modify-writes with the [SCSI First Byte Received \(SFBR\)](#) as the destination. This allows bit testing after an operation.

The [SCSI First Byte Received \(SFBR\)](#) cannot be written to using the CPU, and therefore not by a Memory Move. Additionally, the Load instruction cannot be used to write to this register. However, the [SCSI First Byte Received \(SFBR\)](#) can be loaded using SCRIPTS Read/Write operations. To load the [SCSI First Byte Received \(SFBR\)](#) with a byte stored in system memory, the byte must first be moved to an intermediate LSI53C860 register (such as the SCRATCH register), and then to the [SCSI First Byte Received \(SFBR\)](#).

This register will also contain the state of the lower eight bits of the SCSI data bus during the selection phase if the COM bit in the [DMA Control \(DCNTL\)](#) register is clear.

Register: 0x09 (0x89)
SCSI Output Control Latch (SOCL)
Read /Write

7	6	5	4	3	2	1	0
REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
0	0	0	0	0	0	0	0

REQ	Assert SCSI REQ/ Signal	7
ACK	Assert SCSI ACK/ Signal	6
BSY	Assert SCSI BSY/ Signal	5
SEL	Assert SCSI SEL/ Signal	4
ATN	Assert SCSI ATN/ Signal	3
MSG	Assert SCSI MSG/ Signal	2
C/D	Assert SCSI C_D/ Signal	1
I/O	Assert SCSI I_O/ Signal	0

This register is used primarily for diagnostic testing or programmed I/O operation. It is controlled by the SCRIPTS processor when executing SCSI SCRIPTS. [SCSI Output Control Latch \(SOCL\)](#) should only be used when transferring data using programmed I/O. Some bits are set (1) or reset (0) when executing SCSI SCRIPTS. Do not write to the register once the LSI53C860 starts executing normal SCSI SCRIPTS.

Register: 0x0A (0x8A)
SCSI Selector ID (SSID)
Read Only

7	6		3		2	0	
VAL	R				ENID[2:0]		
0	x	x	x	x	0	0	0

- VAL

SCSI Valid Bit

7
- If VAL is asserted, the two SCSI IDs were detected on the bus during a bus-initiated selection or reselection, and the encoded destination SCSI ID bits below are valid. If VAL is deasserted, only one ID was present and the contents of the encoded destination ID are meaningless.
- R

Reserved

[6:3]
- ENID[2:0]

Encoded Destination SCSI ID

[2:0]
- Reading the SSID register immediately after the LSI53C860 has been selected or reselected returns the binary-encoded SCSI ID of the device that performed the operation. These bits are invalid for targets that are selected under the single initiator option of the SCSI-1 specification. This condition can be detected by examining the VAL bit above.

Register: 0x0B (0x8B)
SCSI Bus Control Lines (SBCL)
Read Only

7	6	5	4	3	2	1	0
REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
x	x	x	x	x	x	x	x

REQ	SREQ/ Status	7
ACK	SACK/ Status	6
BSY	SBSY/ Status	5
SEL	SSEL/ Status	4
ATN	SATN/ Status	3
MSG	SMSG/ Status	2
C/D	SC_D/ Status	1
I/O	SI_O/ Status	0

When read, this register returns the SCSI control line status. A bit will be set when the corresponding SCSI control line is asserted. These bits are not latched. They are a true representation of what is on the SCSI bus at the time the register is read. The resulting read data is synchronized before being presented to the PCI bus to prevent parity errors from being passed to the system. This register can be used for diagnostics testing or operation in low level mode.

Register: 0x0C (0x8C)
DMA Status (DSTAT)
Read Only

7	6	5	4	3	2	1	0
DFE	MDPE	BF	ABRT	SSI	SIR	R	IID
1	0	0	0	0	0	x	0

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the LSI53C860 stacks interrupts).

The DIP bit in the [Interrupt Status \(ISTAT\)](#) register will also be cleared. DMA interrupt conditions may be individually masked through the [DMA Interrupt Enable \(DIEN\)](#) register.

When performing consecutive 8-bit reads of the [DMA Status \(DSTAT\)](#), [SCSI Interrupt Status Zero \(SIST0\)](#) and [SCSI Interrupt Status One \(SIST1\)](#) registers (in any order), insert a delay equivalent to 12 CLK periods between the reads to ensure that the interrupts clear properly. See [Chapter 2, “Functional Description,”](#) for more information on interrupts.

DFE	DMA FIFO Empty 7 This status bit is set when the DMA FIFO is empty. It may be used to determine if any data resides in the FIFO when an error occurs and an interrupt is generated. This bit is a pure status bit and will not cause an interrupt.
MDPE	Master Data Parity Error 6 This bit is set when the LSI53C860 as a master detects a data parity error, or a target device signals a parity error during a data phase. This bit is completely disabled by the Master Parity Error Enable bit (bit 3 of Chip Test Four (CTEST4)).
BF	Bus Fault 5 This bit is set when a PCI bus fault condition is detected. A PCI bus fault can only occur when the LSI53C860 is bus master. A PCI bus fault occurs when a cycle ends with a Bad Address or Target Abort Condition.
ABRT	Aborted This bit is set when an abort condition occurs. An abort condition occurs when a software abort command is issued by setting bit 7 of the Interrupt Status (ISTAT) register.
SSI	Single Step Interrupt 3 If the Single-Step Mode bit in the DMA Control (DCNTL) register is set, this bit will be set and an interrupt generated after successful execution of each SCRIPTS instruction.
SIR	SCRIPTS Interrupt Instruction Received 2 This status bit is set whenever an Interrupt instruction is evaluated as true.

R	Reserved	1
IID	Illegal Instruction Detected This status bit is set any time an illegal instruction is detected, whether the LSI53C860 is operating in single-step mode or automatically executing SCSI SCRIPTS. This bit will also be set if one of the following conditions occurs: • If the LSI53C860 is executing a Wait Disconnect instruction and the SCSI REQ line is asserted without a disconnect occurring. • If a Move, Chained Move, or Memory Move command with a byte count of zero is fetched. • If a Load/Store memory address maps back into chip register space.	0

Register: 0x0D (0x8D)
SCSI Status Zero (SSTAT0)
Read Only

7	6	5	4	3	2	1	0
ILF	ORF	OLF	AIP	LOA	WOA	RST/	SDP/
0	0	0	0	0	0	0	0

ILF	SIDL Full This bit is set when the SCSI Input Data Latch (SIDL) register contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SCSI Input Data Latch (SIDL) register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.	7
ORF	SODR Full This bit is set when the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It cannot be read or written by the user. This bit can be used to determine how many bytes reside in the chip when an error occurs.	6

OLF	SODL Full This bit is set when SCSI Output Data Latch (SODL) contains data. The SCSI Output Data Latch (SODL) register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SCSI Output Data Latch (SODL) register, and then to the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SCSI Output Data Latch (SODL) register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. This bit can be used to determine how many bytes reside in the chip when an error occurs.	5
AIP	Arbitration in Progress Arbitration in Progress (AIP = 1) indicates that the LSI53C860 has detected a Bus Free condition, asserted BSY, and asserted its SCSI ID onto the SCSI bus.	4
LOA	Lost Arbitration When set, LOA indicates that the LSI53C860 has detected a bus free condition, arbitrated for the SCSI bus, and lost arbitration due to another SCSI device asserting the SEL/ signal.	3
WOA	Won Arbitration When set, WOA indicates that the LSI53C860 has detected a Bus Free condition, arbitrated for the SCSI bus and won arbitration. The arbitration mode selected in the SCSI Control Zero (SCNTL0) register must be full arbitration and selection for this bit to be set.	
RST/	SCSI RST/ Signal This bit reports the current status of the SCSI RST/ signal, and the SRST bit (bit 6) in the Interrupt Status (ISTAT) register.	1
SDP/	SCSI SDP/ Parity Signal This bit represents the active high current status of the SCSI SDP/ parity signal.	0

Register: 0x0E (0x8E)
SCSI Status One (SSTAT1)
Read Only

7				4	3	2	1	0
FF[3:0]				SDPL	MSG	C/D	I/O	
0	0	0	0	x	x	x	x	

FF[3:0]

FIFO Flags

[7:4]

These four bits define the number of bytes that currently reside in the LSI53C860's SCSI synchronous data FIFO. These bits are not latched and they will change as data moves through the FIFO. Because the FIFO can only hold nine bytes, values over nine will not occur.

FF3	FF2	FF1	FF0	Bytes or Words in the SCSI FIFO
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

SDPL

Latched SCSI Parity

3

This bit reflects the SCSI parity signal (SDP/), corresponding to the data latched in the [SCSI Input Data Latch \(SIDL\)](#). It changes when a new byte is latched into the [SCSI Input Data Latch \(SIDL\)](#) register. This bit is active HIGH, in other words, it is set when the parity signal is active.

MSG	SCSI MSG/ signal	2
C/D	SCSI C_D/ signal	1
I/O	SCSI I_O/ signal	0

These SCSI phase status bits are latched on the asserting edge of SREQ/ when operating in either initiator or target mode. These bits are set when the corresponding signal is active. They are useful when operating in low level mode.

Register: 0x0F (0x8F)
SCSI Status Two (SSTAT2)
Read Only

7						2	1	0
R						LDSC	R	
x	x	x	x	x	x	1	x	

R **Reserved** **[7:2]**

LDSC **Last Disconnect** **1**

This bit is used in conjunction with the Connected (CON) bit in [SCSI Control One \(SCNTL1\)](#). It allows the user to detect the case in which a target device disconnects, and then some SCSI device selects or reselects the LSI53C860. If the Connected bit is asserted and the LDSC bit is asserted, a disconnect has occurred. This bit is set when the Connected bit in [SCSI Control One \(SCNTL1\)](#) is clear. This bit is cleared when a Block Move instruction executes while the Connected bit in [SCSI Control One \(SCNTL1\)](#) is on.

R **Reserved** **0**

Registers: 0x10–0x13 (0x90–0x93)

Data Structure Address (DSA)

Read/Write

31																													0	
DSA																														
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSA

Data Structure Address

[31:0]

This 32-bit register contains the base address used for all table indirect calculations. The DSA register is usually loaded prior to starting an I/O, but it is possible for a SCRIPTS Memory Move to load the DSA during the I/O.

During any Memory-to-Memory Move operation, the contents of this register are preserved. The power-up value of this register is indeterminate.

Register: 0x14 (0x94)

Interrupt Status (ISTAT)

Read/Write

7	6	5	4	3	2	1	0
ABRT	SRST	SIGP	SEM	CON	INTF	SIP	DIP
0	0	0	0	0	0	0	0

This is the only register that can be accessed by the host CPU while the LSI53C860 is executing SCRIPTS (without interfering in the operation of the LSI53C860). It may be used to poll for interrupts if hardware interrupts are disabled. There may be stacked interrupts pending. Read this register after servicing an interrupt to check for stacked interrupts. For more information on interrupt handling refer to [Chapter 2, “Functional Description.”](#)

ABRT

Abort Operation

7

Setting this bit aborts the current operation being executed by the LSI53C860. If this bit is set and an interrupt is received, reset this bit before reading the [DMA Status \(DSTAT\)](#) register to prevent further aborted interrupts from being generated. The sequence to abort any operation is:

1. Set this bit.

2. Wait for an interrupt.
3. Read the [Interrupt Status \(ISTAT\)](#) register.
4. If the SCSI Interrupt Pending bit is set, then read the [SCSI Interrupt Status Zero \(SIST0\)](#) or [SCSI Interrupt Status One \(SIST1\)](#) register to determine the cause of the SCSI Interrupt and go back to Step 2.
5. If the SCSI Interrupt Pending bit is clear, and the DMA Interrupt Pending bit is set, then write 0x00 value to this register.
6. Read the [DMA Status \(DSTAT\)](#) register to verify the aborted interrupt and to see if any other interrupting conditions have occurred.

SRST	Software Reset 6 Setting this bit resets the LSI53C860. All operating registers are cleared to their default values and all SCSI signals are deasserted. Setting this bit does not cause the SCSI RST/ signal to be asserted. This reset will not clear the LSI53C700 compatibility bit or any of the PCI configuration registers. This bit is not self-clearing; it must be cleared to clear the reset condition (a hardware reset will also clear this bit).
SIGP	Signal Process 5 SIGP is a R/W bit that can be written at any time, and polled and reset using Chip Test Two (CTEST2) . The SIGP bit can be used in various ways to pass a flag to or from a running SCRIPTS instruction. The only SCRIPTS instruction directly affected by the SIGP bit is Wait For Selection/Reselection. Setting this bit causes that instruction to jump to the alternate address immediately. The instructions at the alternate jump address should check the status of SIGP to determine the cause of the jump. The SIGP bit may be used at any time and is not restricted to the wait for selection/ reselection condition.
SEM	Semaphore 4 This bit can be set by the SCRIPTS processor using a SCRIPTS register write instruction. The bit may also be set by an external processor while the LSI53C860 is executing a SCRIPTS operation. This bit enables the

LSI53C860 to notify an external processor of a predefined condition while SCRIPTS are running. The external processor may also notify the LSI53C860 of a predefined condition and the SCRIPTS processor may take action while SCRIPTS are executing.

CON	Connected 3 This bit is automatically set any time the LSI53C860 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing selection or when the LSI53C860 has responded to a bus-initiated selection or reselection. It will also be set after the LSI53C860 wins arbitration when operating in low level mode. When this bit is clear, the LSI53C860 is not connected to the SCSI bus.
INTF	Interrupt-on-the-Fly 2 This bit is asserted by an INTFLY instruction during SCRIPTS execution. SCRIPTS programs will not halt when the interrupt occurs. This bit can be used to notify a service routine, running on the main processor while the SCRIPTS processor is still executing a SCRIPTS program. If this bit is set, when the Interrupt Status (ISTAT) register is read it will not automatically be cleared. To clear this bit, it must be written to a one. The reset operation is self-clearing. <u>Note:</u> If the INTF bit is set but SIP or DIP is not set, do not attempt to read the other chip status registers. An interrupt-on-the-fly interrupt must be cleared before servicing any other interrupts indicated by SIP or DIP. This bit must be written to one in order to clear it after it has been set.
SIP	SCSI Interrupt Pending 1 This status bit is set when an interrupt condition is detected in the SCSI portion of the LSI53C860. The following conditions will cause a SCSI interrupt. • A phase mismatch occurs (initiator mode) or SATN/ becomes active (target mode) • An arbitration sequence completes • A selection or reselection time-out occurs

- The LSI53C860 was selected
- The LSI53C860 was reselected
- A SCSI gross error occurs
- An unexpected disconnect occurs
- A SCSI reset occurs
- A parity error is detected
- The handshake-to-handshake timer is expired
- The general purpose timer is expired

To determine exactly which condition(s) caused the interrupt, read the [SCSI Interrupt Status Zero \(SIST0\)](#) and [SCSI Interrupt Status One \(SIST1\)](#) registers.

DIP

DMA Interrupt Pending

0

This status bit is set when an interrupt condition is detected in the DMA portion of the LSI53C860. The following conditions will cause a DMA interrupt.

- A PCI parity error is detected
- A bus fault is detected
- An abort condition is detected
- A SCRIPTS instruction is executed in single-step mode
- A SCRIPTS interrupt instruction is executed
- An illegal instruction is detected

To determine exactly which condition(s) caused the interrupt, read the [DMA Status \(DSTAT\)](#) register.

Register: 0x18 (0x98)
Chip Test Zero (CTEST0)
Read/Write

7							0
FMT							
1	1	1	1	1	1	1	1

FMT **Byte Empty in DMA FIFO** **[7:0]**
This was a general purpose read/write register in previous LSI53C8XX family chips. Although it is still a read/write register, LSI Logic reserves the right to use these bits for future LSI53C8XX family enhancements.

Register: 0x19 (0x99)
Chip Test One (CTEST1)
Read Only

7			4	3			0
FMT[3:0]				FFL[3:0]			
1	1	1	1	0	0	0	0

FMT[3:0] **Byte Empty in DMA FIFO** **[7:4]**
These bits identify the bottom bytes in the DMA FIFO that are empty. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is empty, then FMT3 will be set. Since the FMT flags indicate the status of bytes at the bottom of the FIFO, if all FMT bits are set, the DMA FIFO is empty.

FFL[3:0] **Byte Full in DMA FIFO** **[3:0]**
These status bits identify the top bytes in the DMA FIFO that are full. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is full then FFL3 will be set. Since the FFL flags indicate the status of bytes at the top of the FIFO, if all FFL bits are set, the DMA FIFO is full.

Register: 0x1A (0x9A)
Chip Test Two (CTEST2)
Read Only

7	6	5	4	3	2	1	0
DDIR	SIGP	CIO	CM	R	TEOP	DREQ	DACK
0	0	x	x	0	0	0	1

- DDIR** **Data Transfer Direction** **7**
This status bit indicates which direction data is being transferred. When this bit is set, the data will be transferred from the SCSI bus to the host bus. When this bit is clear, the data will be transferred from the host bus to the SCSI bus.
- SIGP** **Signal Process** **6**
This bit is a copy of the SIGP bit in the [Interrupt Status \(ISTAT\)](#) register (bit 5). The SIGP bit is used to signal a running SCRIPTS instruction. When this register is read, the SIGP bit in the [Interrupt Status \(ISTAT\)](#) register is cleared.
- CIO** **Configured as I/O** **5**
This bit is defined as the Configuration I/O Enable Status bit. This read only bit indicates if the chip is currently enabled as I/O space.
- Note: Both bits 4 and 5 may be set if the chip is dual-mapped.
- CM** **Configured as Memory** **4**
This bit is defined as the configuration memory enable status bit. This read only bit indicates if the chip is currently enabled as memory space.
- Note: Both bits 4 and 5 may be set if the chip is dual-mapped.
- R** **Reserved** **3**
- TEOP** **SCSI True End of Process** **2**
This bit indicates the status of the LSI53C860's internal TEOP signal. The TEOP signal acknowledges the completion of a transfer through the SCSI portion of the LSI53C860. When this bit is set, TEOP is active. When this bit is clear, TEOP is inactive.

- DREQ** **Data Request Status** **1**
This bit indicates the status of the LSI53C860's internal Data Request signal (DREQ). When this bit is set, DREQ is active. When this bit is clear, DREQ is inactive.
- DACK** **Data Acknowledge Status** **0**
This bit indicates the status of the LSI53C860's internal Data Acknowledge signal (DACK/). When this bit is set, DACK/ is inactive. When this bit is clear, DACK/ is active.

Register: 0x1B (0x9B)
Chip Test Three (CTEST3)
Read/Write

7				4	3	2	1	0
V[3:0]				FLF	CLF	FM	WRIE	
x	x	x	x	0	0	0	0	

- V[3:0]** **Chip Revision Level** **[7:4]**
These bits identify the chip revision level for software purposes.

- FLF** **Flush DMA FIFO** **3**
When this bit is set, data residing in the DMA FIFO is transferred to memory, starting at the address in the [DMA Next Address \(DNAD\)](#) register. The internal DMAWR signal, controlled by the [Chip Test Five \(CTEST5\)](#) register, determines the direction of the transfer. This bit is not self-clearing; once the LSI53C860 has successfully transferred the data, this bit should be reset.

Note: Polling of FIFO flags is allowed during flush operations.

- CLF** **Clear DMA FIFO** **2**
When this bit is set, all data pointers for the DMA FIFO are cleared. Any data in the FIFO is lost. This bit automatically resets after the LSI53C860 has successfully cleared the appropriate FIFO pointers and registers.

Note: This bit does not clear the data visible at the bottom of the FIFO.

- FM

Fetch Pin Mode

1

When set, this bit causes the FETCH/ pin to deassert during indirect and table indirect read operations. FETCH/ will only be active during the opcode portion of an instruction fetch. This allows SCRIPTS to be stored in a PROM while data tables are stored in RAM.

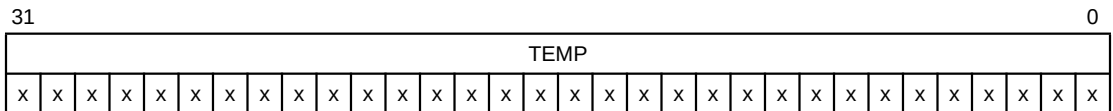
If this bit is not set, FETCH/ will be asserted for all bus cycles during instruction fetches.
- WRIE

Write and Invalidate Enable

0

This bit, when set, causes Memory Write and Invalidate commands to be issued on the PCI bus after certain conditions have been met. These conditions are described in more detail in [Chapter 3, “PCI Functional Description.”](#)

Registers: 0x1C–0x1F (0x9C–0x9F)
Temporary (TEMP)
Read/Write



- TEMP

Temporary

[31:0]

This 32-bit register stores the Return instruction address pointer from the Call instruction. The address pointer stored in this register is loaded into the [DMA SCRIPTS Pointer \(DSP\)](#) register when a Return instruction is executed. This address points to the next instruction to be executed. Do not write to this register while the LSI53C860 is executing SCRIPTS.

During any Memory-to-Memory Move operation, the contents of this register are preserved. The power-up value of this register is indeterminate.

Read/Write

Register: 0x21 (0xA1)
Chip Test Four (CTEST4)
Read/Write

7	6	5	4	3	2	0
BDIS	ZMOD	ZSD	SRTM	MPEE	FBL[2:0]	
0	0	0	0	0	0	0

- BDIS** **Burst Disable** **7**
When set, this bit will cause the LSI53C860 to perform back-to-back cycles for all transfers. When reset, the LSI53C860 performs back-to-back transfers for opcode fetches and burst transfers for data moves. The handling of opcode fetches is dependent on the setting of the Burst OpCode Fetch bit in the [DMA Mode \(DMODE\)](#) register.
- ZMOD** **High Impedance Mode** **6**
Setting this bit causes the LSI53C860 to place all output and bidirectional pins into a high impedance state. In order to read data out of the LSI53C860, this bit must be cleared. This bit is intended for board-level testing only. Do not set this bit during normal system operation.
- ZSD** **SCSI Data High Impedance** **5**
Setting this bit causes the LSI53C860 to place the SCSI data bus SD[7:0] and the parity line (SDP) in a high impedance state. In order to transfer data on the SCSI bus, this bit must be cleared.
- SRTM** **Shadow Register Test Mode** **4**
Setting this bit allows access to the shadow registers used by Memory-to-Memory Move operations. When this bit is set, register accesses to the [Temporary \(TEMP\)](#) and [Data Structure Address \(DSA\)](#) registers are directed to the shadow copies STEMP (Shadow TEMP) and SDSA (Shadow DSA). The registers are shadowed to prevent them from being overwritten during a Memory-to-Memory Move operation. The [Data Structure Address \(DSA\)](#) and [Temporary \(TEMP\)](#) registers contain the base address used for table indirect calculations, and the address pointer for a call or return instruction, respectively. This bit is intended for manufacturing diagnostics only and should not be set during normal operations.

MPEE**Master Parity Error Enable****3**

Setting this bit enables parity checking during master data phases. A parity error during a bus master read is detected by the LSI53C860. A parity error during a bus master write is detected by the target, and the LSI53C860 is informed of the error by the PERR/ pin being asserted by the target. When this bit is reset, the LSI53C860 will not interrupt if a master parity error occurs. This bit is reset at power-up.

FBL[2:0]**FIFO Byte Control****[2:0]**

FBL2	FBL1	FBL0	DMA FIFO Byte Lane	Pins
x	x	x	Disabled	N/A
0	0	0	0	D[7:0]
0	0	1	1	D[15:8]
0	1	0	2	D[23:16]
0	1	1	3	D[31:24]

These bits steer the contents of the [Chip Test Six \(CTEST6\)](#) register to the appropriate byte lane of the 32-bit DMA FIFO. If the FBL2 bit is set, then FBL1 and FBL0 determine which of four byte lanes can be read or written. When cleared, the byte lane read or written is determined by the current contents of the DNAD and [DMA Byte Counter \(DBC\)](#) registers. Each of the four bytes that make up the 32-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL2 must equal zero.

Register: 0x22 (0xA2)**Chip Test Five (CTEST5)****Read/Write**

7	6	5	4	3	2	1	0
ADCK	BBCK	R	MASR	DDIR	R		
0	0	x	0	0	x	x	x

ADCK**Clock Address Incrementor****7**

Setting this bit increments the address pointer contained in the DNAD register. The DNAD register is incremented

based on the DNAD contents and the current [DMA Byte Counter \(DBC\)](#) value. This bit automatically clears itself after incrementing the DNAD register.

BBCK	Clock Byte Counter	6
	Setting this bit decrements the byte count contained in the 24-bit DMA Byte Counter (DBC) register. It is decremented based on the DMA Byte Counter (DBC) contents and the current DNAD value. This bit automatically clears itself after decrementing the DMA Byte Counter (DBC) register.	
R	Reserved	5
MASR	Master Control for Set or Reset Pulses	4
	This bit controls the operation of bit 3. When this bit is set, bit 3 asserts the corresponding signals. When this bit is reset, bit 3 deasserts the corresponding signals. This bit and bit 3 should not be changed in the same write cycle.	
DDIR	DMA Direction	3
	Setting this bit either asserts or deasserts the internal DMA Write (DMAWR) direction signal depending on the current status of the MASR bit in this register. Asserting the DMAWR signal indicates that data will be transferred from the SCSI bus to the host bus. Deasserting the DMAWR signal transfers data from the host bus to the SCSI bus.	
R	Reserved	[2:0]

Register: 0x23 (0xA3)
Chip Test Six (CTEST6)
Read/Write

7							0
DF							
0	0	0	0	0	0	0	0

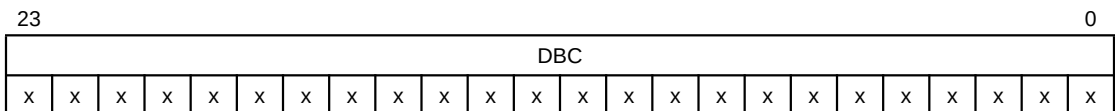
DF	DMA FIFO	[7:0]
	Writing to this register writes data to the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the Chip Test Four (CTEST4) register. Reading this register unloads data from the appropriate byte lane of	

the DMA FIFO as determined by the FBL bits in the [Chip Test Four \(CTEST4\)](#) register. Data written to the FIFO is loaded into the top of the FIFO. Data read out of the FIFO is taken from the bottom. To prevent DMA data from being corrupted, this register should not be accessed before starting or restarting SCRIPTS operation. This register should only be written when testing the DMA FIFO using the [Chip Test Four \(CTEST4\)](#) register. Writes to this register while the test mode is not enabled will have unexpected results.

Register: 0x24–0x26 (0xA4–0xA6)

DMA Byte Counter (DBC)

Read/Write



DBC

DMA Byte Counter

[23:0]

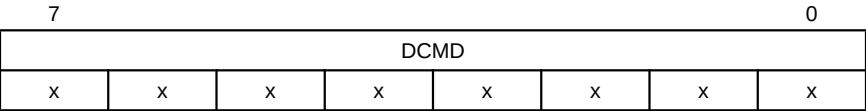
This 24-bit register determines the number of bytes to be transferred in a Block Move instruction. While sending data to the SCSI bus, the counter is decremented as data is moved into the DMA FIFO from memory. While receiving data from the SCSI bus, the counter is decremented as data is written to memory from the LSI53C860. The [DMA Byte Counter \(DBC\)](#) counter is decremented each time that data is transferred on the PCI bus. It is decremented by an amount equal to the number of bytes that were transferred.

The maximum number of bytes that can be transferred in any one Block Move command is 16,777,215 bytes. The maximum value that can be loaded into the [DMA Byte Counter \(DBC\)](#) register is 0xFFFFFFFF. If the instruction is a Block Move and a value of 0x000000 is loaded into the [DMA Byte Counter \(DBC\)](#) register, an illegal instruction interrupt will occur if the LSI53C860 is not in target role, Command phase.

The [DMA Byte Counter \(DBC\)](#) register is also used to hold the least significant 24 bits of the first Dword of a SCRIPTS fetch, and to hold the offset value during table

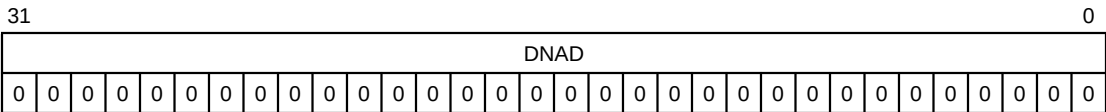
indirect I/O SCRIPTS. For a complete description, see [Chapter 6, “Instruction Set of the I/O Processor.”](#) The power-up value of this register is indeterminate.

Register: 0x27 (0xA7)
DMA Command (DCMD)
Read/Write



DCMD **DMA Command** **[7:0]**
This 8-bit register determines the instruction for the LSI53C860 to execute. This register has a different format for each instruction. For a complete description, see [Chapter 6, “Instruction Set of the I/O Processor.”](#)

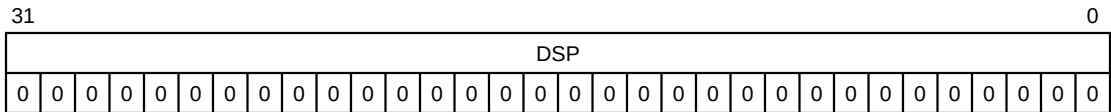
Register: 0x28–0x2B (0xA8–0xAB)
DMA Next Address (DNAD)
Read/Write



DNAD **DMA Next Address** **[31:0]**
This 32-bit register contains the general purpose address pointer. At the start of some SCRIPTS operations, its value is copied from the [DMA SCRIPTS Pointer Save \(DSPS\)](#) register. Its value may not be valid except in certain abort conditions. The default value of this register is zero.

Register: 0x2C–0x2F (0xAC–0xAF)**DMA SCRIPTS Pointer (DSP)**

Read/Write

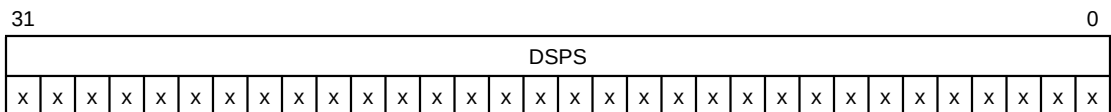
**DSP****DMA SCRIPTS Pointer****[31:0]**

The CPU writes the address of the first SCRIPTS instruction to this register to begin SCSI SCRIPTS operation. In normal SCRIPTS operation, once the starting address of the first SCRIPTS instruction is written to this register, SCRIPTS instructions are automatically fetched and executed until an interrupt condition occurs.

In single-step mode, there is a single step interrupt after each instruction is executed. The [DMA SCRIPTS Pointer \(DSP\)](#) register does not need to be written with the next address, but the Start DMA bit (bit 2, [DMA Control \(DCNTL\)](#) register) must be set each time the step interrupt occurs to fetch and execute the next SCRIPTS command. When writing this register eight bits at a time, writing the upper eight bits begins execution of the SCSI SCRIPTS. The default value of this register is zero.

Register: 0x30–0x33 (0xB0–0xB3)**DMA SCRIPTS Pointer Save (DSPS)**

Read/Write

**DSPS****DMA SCRIPTS Pointer Save****[31:0]**

This register contains the second Dword of a SCRIPTS instruction. It is overwritten each time a SCRIPTS instruction is fetched. When a SCRIPTS interrupt instruction is executed, this register holds the interrupt vector. The power-up value of this register is indeterminate.

Register: 0x34–0x37 (0xB4–0xB7)

Scratch Register A (SCRATCHA)

Read/Write

31																															0																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
SCRATCHA																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																		
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

SCRATCHA Scratch Register A [31:0]

This is a general purpose, user-definable scratch pad register. Apart from CPU access, only Register Read/Write and Memory Moves into the SCRATCH register will alter its contents. The power-up value of this register is indeterminate.

The LSI53C860 cannot fetch SCRIPTS instructions from this location.

Register: 0x38 (0xB8)

DMA Mode (DMODE)

Read/Write

7	6	5	4	3	2	1	0
BL[1:0]		SIOM	DIOM	ER	ERMP	BOF	MAN
0	0	0	0	0	0	0	0

BL[1:0] Burst Length [7:6]

These bits control the maximum number of transfers performed per bus ownership, regardless of whether the transfers are back-to-back, burst, or a combination of both. The LSI53C860 asserts the Bus Request (REQ/) output when the DMA FIFO can accommodate a transfer of at least one burst size of data. Bus Request (REQ/) is also asserted during start-of-transfer and end-of-transfer cleanup and alignment, even though less than a full burst of transfers may be performed. The LSI53C860 inserts a “fairness delay” of four CLKs between burst-length transfers (as set in BL[1:0]) during normal operation. The fairness delay is not inserted during PCI retry cycles. This gives the CPU and other bus master devices the opportunity to access the PCI bus between bursts.

BL1	BL0	Burst Length
0	0	2-transfer burst
0	1	4-transfer burst
1	0	8-transfer burst
1	1	16-transfer burst

SIOM

Source I/O-Memory Enable

5

This bit is defined as an I/O Memory Enable bit for the source address of a Memory Move or Block Move Command. If this bit is set, then the source address is in I/O space; and if reset, then the source address is in memory space.

This function is useful for register-to-memory operations using the Memory Move instruction when the LSI53C860 is I/O mapped. Bits 4 and 5 of the [Chip Test Two \(CTEST2\)](#) register can be used to determine the configuration status of the LSI53C860.

DIOM

Destination I/O-Memory Enable

4

This bit is defined as an I/O Memory Enable bit for the destination address of a Memory Move or Block Move Command. If this bit is set, then the destination address is in I/O space; and if reset, then the destination address is in memory space.

This function is useful for memory-to-register operations using the Memory Move instruction when the LSI53C860 is I/O mapped. Bits 4 and 5 of the [Chip Test Two \(CTEST2\)](#) register can be used to determine the configuration status of the LSI53C860.

ERL

Enable Read Line

3

This bit enables a PCI Read Line command. If PCI cache mode is enabled by setting bits in the PCI [Cache Line Size](#) register, the chip issues a Read Line command on all read cycles if other conditions are met. For more information on these conditions, refer to [Chapter 3, "PCI Functional Description."](#)

ERMP	Enable Read Multiple	2
	This bit, when set, will cause Read Multiple commands to be issued on the PCI bus after certain conditions have been met. These conditions are described in Chapter 3, “PCI Functional Description.”	
BOF	Burst OpCode Fetch Enable	1
	Setting this bit causes the LSI53C860 to fetch instructions in burst mode, if the Burst Disable bit (Chip Test Four (CTEST4) , bit7) is cleared. Specifically, the chip will burst in the first two Dwords of all instructions using a single bus ownership. If the instruction is a memory-to-memory move type, the third Dword will be accessed in a subsequent bus ownership. If the instruction is an indirect type, the additional Dword will be accessed in a subsequent bus ownership. If the instruction is a table indirect block move type, the chip will access the remaining two Dwords in a subsequent bus ownership, thereby fetching the four Dwords required in two bursts of two Dwords each.	
MAN	Manual Start Mode	0
	Setting this bit prevents the LSI53C860 from automatically fetching and executing SCSI SCRIPTS when the DMA SCRIPTS Pointer (DSP) register is written. When this bit is set, the Start DMA bit in the DMA Control (DCNTL) register must be set to begin SCRIPTS execution. Clearing this bit causes the LSI53C860 to automatically begin fetching and executing SCSI SCRIPTS when the DMA SCRIPTS Pointer (DSP) register is written. This bit is not normally used for SCSI SCRIPTS operations.	

Register: 0x39 (0xB9)
DMA Interrupt Enable (DIEN)
Read/Write

7	6	5	4	3	2	1	0
R	MDPE	BF	ABRT	SSI	SIR	R	IID
x	0	0	0	0	0	x	0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the [DMA Status \(DSTAT\)](#) register. An interrupt is masked by clearing the appropriate mask bit. Masking an

interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the [DMA Status \(DSTAT\)](#) register. Masking an interrupt will not prevent the ISTAT DIP from being set. All DMA interrupts are considered fatal, therefore SCRIPTS will stop running when a DMA interrupt occurs, whether or not the interrupt is masked. Setting a mask bit enables the assertion of IRQ/ for the corresponding interrupt. (A masked nonfatal interrupt will not prevent unmasked or fatal interrupts from getting through; interrupt stacking begins when either the ISTAT SIP or DIP bit is set.)

The LSI53C860 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted.

For more information on interrupts, see [Chapter 2, "Functional Description."](#)

R	Reserved	7
MDPE	Master Data Parity Error	6
BF	Bus fault	5
ABRT	Aborted	4
SSI	Single step interrupt	3
SIR	SCRIPTS interrupt instruction received	2
R	Reserved	1
IID	Illegal instruction detected	0

Register: 0x3A (0xBA)
Scratch Byte Register (SBR)
Read/Write

7							0
SBR							
0	0	0	0	0	0	0	0

SBR **Scratch Byte Register** **[7:0]**

This is a general purpose register. Apart from CPU access, only Register Read/Write and Memory Moves into this register will alter its contents. The default value of this register is zero. This register was called the DMA Watchdog Timer on previous LSI53C8XX family products.

Register: 0x3B (0xBB)
DMA Control (DCNTL)
Read/Write

7	6	5	4	3	2	1	0
CLSE	PFF	PFEN	SSM	IRQM	STD	IRQD	COM
0	0	0	0	0	0	0	0

CLSE **Cache Line Size Enable** **7**

Setting this bit enables the LSI53C860 to sense and react to cache line boundaries set up by the [DMA Mode \(DMODE\)](#) or PCI Cache Line Size register, whichever contains the smaller value. Clearing this bit disables the cache line size logic and the LSI53C860 monitors the cache line size using the [DMA Mode \(DMODE\)](#) register.

PFF **Prefetch Flush** **6**

Setting this bit will cause the prefetch unit to flush its contents. The bit will reset after the flush is complete.

PFEN **Prefetch Enable** **5**

Setting this bit enables the prefetch unit if the burst size is equal to or greater than four. For more information on SCRIPTS instruction prefetching, see [Chapter 2, "Functional Description."](#)

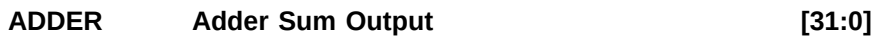
SSM	Single-Step Mode 4 Setting this bit causes the LSI53C860 to stop after executing each SCRIPTS instruction, and generate a single step interrupt. When this bit is clear the LSI53C860 will not stop after each instruction; instead it continues fetching and executing instructions until an interrupt condition occurs. This bit should be clear for normal SCSI SCRIPTS operation. To restart the LSI53C860 after it generates a SCRIPTS Step interrupt, read the Interrupt Status (ISTAT) and DMA Status (DSTAT) registers to recognize and clear the interrupt; then set the START DMA bit in this register.
IRQM	IRQ Mode 3 When set, this bit enables a totem pole driver for the IRQ pin. When reset, this bit enables an open drain driver for the IRQ pin with a internal weak pull-up. This bit is reset at power-up.
STD	Start DMA operation 2 The LSI53C860 fetches a SCSI SCRIPTS instruction from the address contained in the DMA SCRIPTS Pointer (DSP) register when this bit is set. This bit is required if the LSI53C860 is in one of the following modes: • Manual start mode – Bit 0 in the DMA Mode (DMODE) register is set • Single-step mode – Bit 4 in the DMA Control (DCNTL) register is set When the LSI53C860 is executing SCRIPTS in manual start mode, the Start DMA bit needs to be set to start instruction fetches. This bit will remain set until an interrupt occurs. When the LSI53C860 is in single-step mode, the Start DMA bit needs to be set to restart execution of SCRIPTS after a single-step interrupt.
IRQD	IRQ Disable 1 Setting this bit 3-states the IRQ pin; clearing the bit enables normal operation. When bit 1 in this register is set, the IRQ/ pin will not be asserted when an interrupt condition occurs. The interrupt is not lost or ignored, but merely masked at the pin. Clearing this bit when an interrupt is pending will immediately cause the IRQ/ pin

COM	LSI53C700 Family Compatibility	0
-----	--------------------------------	---

When this bit is set, the ID will be stored only in the SSID register, protecting the **SCSI First Byte Received (SFBR)** from being overwritten if a selection/reselection occurs during a DMA register-to-register operation.

Register: 0x3C–0x3F (0xBC–0xBF)

Read Only



Register: 0x40 (0xC0)

Read/Write

This register contains the interrupt mask bits that correspond to the interrupting conditions described in the [SCSI Interrupt Status Zero \(SIST0\)](#) register. An interrupt is masked by clearing the appropriate mask bit. For more information on interrupts, see [Chapter 2, “Functional Description.”](#)

M/A	SCSI Phase Mismatch - Initiator Mode; SCSI ATN Condition - Target Mode In initiator mode, this bit controls whether an interrupt occurs when the SCSI phase asserted by the target and sampled during SREQ/ does not match the expected phase in the SCSI Output Control Latch (SOCL) register. This expected phase is automatically written by the SCSI SCRIPTS program. In target mode, this bit is set when the initiator has asserted SATN/. See the Disable Halt on Parity Error or SATN/ Condition bit in the SCSI Control One (SCNTL1) register for more information on when this status is actually raised.	7
CMP	Function Complete This bit controls whether an interrupt occurs when full arbitration and selection sequence has completed.	6
SEL	Selected This bit controls whether an interrupt occurs when the LSI53C860 has been selected by a SCSI target device. The Enable Response to Selection bit in the SCSI Chip ID (SCID) register must be set for this to occur.	5
RSL	Reselected This bit controls whether an interrupt occurs when the LSI53C860 has been reselected by a SCSI initiator device. The Enable Response to Reselection bit in the SCSI Chip ID (SCID) register must be set for this to occur.	4
SGE	SCSI Gross Error This bit controls whether an interrupt occurs when the LSI53C860 detects a SCSI Gross Error. The following conditions are considered SCSI Gross Errors: • Data underflow – the SCSI FIFO was read when no data was present. • Data overflow – the SCSI FIFO was written to while full. • Offset underflow – in target mode, a SACK/ pulse was received before the corresponding SREQ/ was sent.	3

- Offset overflow – in initiator mode, an SREQ/ pulse was received which caused the maximum offset (defined by the MO[3:0] bits in the [SCSI Transfer \(SXFER\)](#) register) to be exceeded.
- In initiator mode, a phase change occurred with an outstanding SREQ/SACK offset.
- Residual data in SCSI FIFO – a transfer other than synchronous data receive was started with data left in the SCSI synchronous receive FIFO.

UDC	Unexpected Disconnect	2
	This bit controls whether an interrupt occurs in the case of an unexpected disconnect. This condition only occurs in initiator mode. It happens when the target to which the LSI53C860 is connected disconnects from the SCSI bus unexpectedly. See the SCSI Disconnect Unexpected bit in the SCSI Control Two (SCNTL2) register for more information on expected versus unexpected disconnects. Any disconnect in low level mode causes this condition.	
RST	SCSI Reset Condition	1
	This bit controls whether an interrupt occurs when the SRST/ signal has been asserted by the LSI53C860 or any other SCSI device. Note that this condition is edge-triggered, so that multiple interrupts cannot occur because of a single SRST/ pulse.	
PAR	SCSI Parity Error	0
	This bit controls whether an interrupt occurs when the LSI53C860 detects a parity error while receiving or sending SCSI data. See the Disable Halt on Parity Error or SATN/ Condition bits in the SCSI Control One (SCNTL1) register for more information on when this condition will actually be raised.	

Register: 0x41 (0xC1)

SCSI Interrupt Enable One (SIEN1)

Read/Write

7					3	2	1	0
R					STO	GEN	HTH	
x	x	x	x	x	0	0	0	

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the [SCSI Interrupt Status One \(SIST1\)](#) register. An interrupt is masked by clearing the appropriate mask bit. For more information on interrupts, refer to [Chapter 2, “Functional Description.”](#)

R	Reserved	[7:3]
STO	Selection or Reselection Time-out	2
This bit controls whether an interrupt occurs when the SCSI device which the LSI53C860 was attempting to select or reselect did not respond within the programmed time-out period. See the description of the SCSI Timer Zero (STIME0) register bits [3:0] for more information on the time-out timer.		
GEN	General Purpose Timer Expired	1
This bit controls whether an interrupt occurs when the general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the SCSI Timer One (STIME1) register, bits [3:0], for more information on the general purpose timer.		
HTH	Handshake to Handshake timer Expired	0
This bit controls whether an interrupt occurs when the handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the SCSI Timer Zero (STIME0) register, bits [7:4], for more information on the handshake-to-handshake timer.		

Register: 0x42 (0xC2)
SCSI Interrupt Status Zero (SIST0)
Read Only

7	6	5	4	3	2	1	0
M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
0	0	0	0	0	0	0	0

Reading the [SCSI Interrupt Status Zero \(SIST0\)](#) register returns the status of the various interrupt conditions, whether or not they are enabled in the [SCSI Interrupt Enable Zero \(SIEN0\)](#) register. Each bit set indicates that the corresponding condition has occurred. Reading the [SCSI Interrupt Status Zero \(SIST0\)](#) will clear the interrupt status.

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the LSI53C860 stacks interrupts). SCSI interrupt conditions may be individually masked through the [SCSI Interrupt Enable Zero \(SIEN0\)](#) register.

When performing consecutive 8-bit reads of the [DMA Status \(DSTAT\)](#), [SCSI Interrupt Status Zero \(SIST0\)](#), and [SCSI Interrupt Status One \(SIST1\)](#) registers (in any order), insert a delay equivalent to 12 CLK periods between the reads to ensure the interrupts clear properly. Also, if reading the registers when both the ISTAT SIP and DIP bits may not be set, the [SCSI Interrupt Status Zero \(SIST0\)](#) and [SCSI Interrupt Status One \(SIST1\)](#) registers should be read before the [DMA Status \(DSTAT\)](#) register to avoid missing a SCSI interrupt. For more information on interrupts, refer to [Chapter 2, "Functional Description."](#)

M/A	Initiator Mode: Phase Mismatch; Target Mode: SATN/ Active	7
	In initiator mode, this bit is set if the SCSI phase asserted by the target does not match the instruction. The phase is sampled when SREQ/ is asserted by the target. In target mode, this bit is set when the SATN/ signal is asserted by the initiator.	
CMP	Function Complete	6
	This bit is set when an arbitration only or full arbitration sequence has completed.	

SEL	Selected 5 This bit is set when the LSI53C860 is selected by another SCSI device. The Enable Response to Selection bit must have been set in the SCSI Chip ID (SCID) register (and the Response ID (RESPID) register must hold the chip's ID) for the LSI53C860 to respond to selection attempts.
RSL	Reselected 4 This bit is set when the LSI53C860 is reselected by another SCSI device. The Enable Response to Reselection bit must have been set in the SCSI Chip ID (SCID) register (and the Response ID (RESPID) register must hold the chip's ID) for the LSI53C860 to respond to reselection attempts.
SGE	SCSI Gross Error 3 This bit is set when the LSI53C860 encounters a SCSI Gross Error Condition. The following conditions can result in a SCSI Gross Error Condition: • Data Underflow – the SCSI FIFO register was read when no data was present. • Data Overflow – too many bytes were written to the SCSI FIFO or the synchronous offset caused the SCSI FIFO to be overwritten. • Offset Underflow – the LSI53C860 is operating in target mode and a SACK/ pulse is received when the outstanding offset is zero. • Offset Overflow – the other SCSI device sent a SREQ/ or SACK/ pulse with data which exceeded the maximum synchronous offset defined by the SCSI Transfer (SXFER) register. • A phase change occurred with an outstanding synchronous offset when the LSI53C860 was operating as an initiator. • Residual data in the Synchronous data FIFO – a transfer other than synchronous data receive was started with data left in the synchronous data FIFO.
UDC	Unexpected Disconnect 2 This bit is set when the LSI53C860 is operating in initiator mode and the target device unexpectedly disconnects from the SCSI bus. This bit is only valid when the

LSI53C860 operates in the initiator mode. When the LSI53C860 operates in low level mode, any disconnect will cause an interrupt, even a valid SCSI disconnect. This bit will also be set if a selection time-out occurs (it may occur before, at the same time, or stacked after the STO interrupt, since this is not considered an expected disconnect).

- RST

SCSI RST/ Received

1

This bit is set when the LSI53C860 detects an active SRST/ signal, whether the reset was generated external to the chip or caused by the Assert SRST/ bit in the [SCSI Control One \(SCNTL1\)](#) register. This LSI53C860 SCSI reset detection logic is edge-sensitive, so that multiple interrupts will not be generated for a single assertion of the SRST/ signal.
- PAR

Parity Error

0

This bit is set when the LSI53C860 detects a parity error while receiving SCSI data. The Enable Parity Checking bit (bit 3 in the [SCSI Control Zero \(SCNTL0\)](#) register) must be set for this bit to become active. The LSI53C860 always generates parity when sending SCSI data.

Register: 0x43 (0xC3)
SCSI Interrupt Status One (SIST1)
Read Only

7					3	2	1	0
R					STO	GEN	HTH	
x	x	x	x	x	0	0	0	

Reading the [SCSI Interrupt Status One \(SIST1\)](#) register returns the status of the various interrupt conditions, whether or not they are enabled in the [SCSI Interrupt Enable One \(SIEN1\)](#) register. Each bit that is set indicates the corresponding condition has occurred.

Reading the [SCSI Interrupt Status One \(SIST1\)](#) register will clear the interrupt condition.

R	Reserved	[7:3]
STO	Selection or Reselection Time-out 2 This bit is set when the SCSI device which the LSI53C860 was attempting to select or reselect did not respond within the programmed time-out period. See the description of the SCSI Timer Zero (STIME0) register, bits [3:0], for more information on the time-out timer.	
GEN	General Purpose Timer Expired 1 This bit is set when the general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the SCSI Timer One (STIME1) register, bits [3:0], for more information on the general purpose timer.	
HTH	Handshake-to-Handshake Timer Expired 0 This bit is set when the handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the SCSI Timer Zero (STIME0) register, bits [7:4], for more information on the handshake-to-handshake timer.	

Register: 0x44 (0xC4)
SCSI Longitudinal Parity (SLPAR)
 Read/Write

7							0
SLPAR							
x	x	x	x	x	x	x	x

SLPAR	SCSI Longitudinal Parity [7:0] This register performs a bitwise longitudinal parity check on all SCSI data received or sent through the SCSI core. If one of the bytes received or sent (usually the last) is the set of correct even parity bits, SCSI Longitudinal Parity (SLPAR) should go to zero (assuming it started at zero). As an example, suppose that the following three data bytes and one check byte are received from the SCSI bus (all signals are shown active HIGH):
--------------	---

Data Bytes	Running SLPAR
–	00000000
1. 11001100	11001100 (XOR of word 1)
2. 01010101	10011001 (XOR of word 1 and 2)
3. 00001111	10010110 (XOR of word 1, 2 and 3) Even parity >>> 10010110
4. 10010110	00000000

A one in any bit position of the final [SCSI Longitudinal Parity \(SLPAR\)](#) value would indicate a transmission error.

The [SCSI Longitudinal Parity \(SLPAR\)](#) register can also be used to generate the check bytes for SCSI send operations. If the [SCSI Longitudinal Parity \(SLPAR\)](#) register contains all zeros prior to sending a block move, it will contain the appropriate check byte at the end of the block move. This byte must then be sent across the SCSI bus.

Note: Writing any value to this register resets it to zero.

The longitudinal parity checks are meant to provide an added measure of SCSI data integrity and are entirely optional. This register does not latch SCSI selection/reselection IDs under any circumstances. The default value of this register is zero.

Register: 0x46 (0xC6)
Memory Access Control (MACNTL)
Read/Write

7				4	3	2	1	0
TYP[3:0]				DWR	DRD	PSCPT	SCPTS	
0	1	1	0	0	0	0	0	

TYP[3:0]	Chip Type	[7:4]
	These bits identify the chip type for software purposes.	
	Bits 3 through 0 of this register are used to determine if an external bus master access is to local or far memory. When bits 3 through 0 are set, the corresponding access is considered local and the MAC/_TESTOUT pin is driven high. When these bits are clear, the corresponding access is to far memory and the MAC/_TESTOUT pin is driven low. This function is enabled after a Transfer Control SCRIPTS instruction is executed.	
DWR	DataWR	3
	This bit is used to define if a data write is considered local memory access.	
DRD	DataRD	2
	This bit is used to define if a data read is considered local memory access.	
PSCPT	Pointer SCRIPTS	1
	This bit is used to define if a pointer to a SCRIPTS indirect or table indirect fetch is considered local memory access.	
SCPTS	SCRIPTS	0
	This bit is used to define if a SCRIPTS fetch is considered local memory access.	

Register: 0x47 (0xC7)
General Purpose Pin Control (GPCNTL)
Read/Write

7	6	5	4	3	2	1	0
ME	FE	R				GPIO[1:0]	
0	0	x	0	1	1	1	1

This register is used to determine if the pins controlled by the [General Purpose \(GPREG\)](#) register are inputs or outputs. Bits [1:0] in [General Purpose Pin Control \(GPCNTL\)](#) correspond to bits [1:0] in the [General Purpose \(GPREG\)](#) register. When the bits are enabled as inputs, an internal pull-up is also enabled.

ME	Master Enable	7
	The internal bus master signal will be presented on GPIO1 if this bit is set, regardless of the state of Bit 1 (GPIO1_EN).	
FE	Fetch Enable	6
	The internal opcode fetch signal will be presented on GPIO0 if this bit is set, regardless of the state of Bit 0 (GPIO0_EN).	
R	Reserved	[5:2]
GPIO[1:0]	GPIO Enable	[1:0]
	These bits power-up set, causing the GPIO1 and GPIO0 pins to become inputs. Resetting these bits causes GPIO[1:0] to become outputs.	

Register: 0x48 (0xC8)
SCSI Timer Zero (STIME0)
Read/Write

7				4		3		0	
HTH[3:0]				SEL[3:0]					
0	0	0	0	0	0	0	0	0	0

HTH **Handshake-to-Handshake Timer Period** **[7:4]**

These bits select the handshake-to-handshake time-out period, the maximum time between SCSI handshakes (SREQ/ to SREQ/ in target mode, or SACK/ to SACK/ in initiator mode). When this timing is exceeded, an interrupt is generated and the HTH bit in the [SCSI Interrupt Status One \(SIST1\)](#) register is set. The following table contains time-out periods for the Handshake-to-Handshake Timer, the Selection/Reselection Timer (bits [3:0]), and the General Purpose Timer ([SCSI Timer One \(STIME1\)](#) bits [3:0]). For a more detailed explanation of interrupts, refer to [Chapter 2, “Functional Description.”](#)

HTH[7:4], SEL[3:0], GEN[3:0] ¹	Minimum Timeout (40 MHz)	Minimum Timeout (50 MHz)
0000	Disabled	Disabled
0001	125 μ s	100 μ s
0010	250 μ s	200 μ s
0011	500 μ s	400 μ s
0100	1 ms	800 μ s
0101	2 ms	1.6 ms
0110	4 ms	3.2 ms
0111	8 ms	6.4 ms
1000	16 ms	12.8 ms
1001	32 ms	25.6 ms
1010	64 ms	51.2 ms
1011	128 ms	102.4 ms
1100	256 ms	204.8 ms
1101	512 ms	409.6 ms
1110	1.024 s	819.2 ms
1111	2.048 s	1.6384 s

1. These values are correct if the CCF bits in the [SCSI Control Three \(SCNTL3\)](#) register are set according to the valid combinations in the bit description.

SEL

Selection Time-Out

[3:0]

These bits select the SCSI selection/reselection time-out period. When this timing (plus the 200 μ s selection abort time) is exceeded, the STO bit in the [SCSI Interrupt Status One \(SIST1\)](#) register is set. For a more detailed explanation of interrupts, refer to [Chapter 2, "Functional Description."](#)

Register: 0x49 (0xC9)
SCSI Timer One (STIME1)
Read/Write

7			4		3		0
R				GEN[3:0]			
x	x	x	x	0	0	0	0

R **Reserved** **[7:4]**

GEN[3:0] **General Purpose Timer Period** **[3:0]**

These bits select the period of the general purpose timer. The time measured is the time between enabling and disabling of the timer. When this timing is exceeded, the GEN bit in the [SCSI Interrupt Status One \(SIST1\)](#) register is set. Refer to the table under [SCSI Timer Zero \(STIME0\)](#), bits [3:0], for the available time-out periods.

Note: To reset a timer before it has expired and to obtain repeatable delays, the time value must be written to zero first, and then written back to the desired value. This is also required when changing from one time value to another. [Chapter 2, “Functional Description,”](#) for an explanation of how interrupts are generated when the timers expire.

Register: 0x4A (0xCA)
Response ID (RESPID)
Read/Write

7							0
ID							
x	x	x	x	x	x	x	x

RESPID **Response ID** **[7:0]**

This register contains the IDs that the chip responds to on the SCSI bus. Each bit represents one possible ID with the most significant bit representing ID 7 and the least significant bit representing ID 0. The [SCSI Chip ID \(SCID\)](#) register still contains the chip ID used during arbitration. The chip can respond to more than one ID because more than one bit can be set in the [Response](#)

ID (RESPID) register. However, the chip can arbitrate with only one ID value in the **SCSI Chip ID (SCID)** register.

Register: 0x4C (0xCC)

SCSI Test Zero (STEST0)

Read Only

7	6	4	3	2	1	0
R	SSAID			SLT	ART	SOM
x	x	x	x	0	x	1

R	Reserved	7
SSAID	SCSI Selected As ID [6:4] These bits contain the encoded value of the SCSI ID that the LSI53C860 was selected or reselected as during a SCSI selection or reselection phase. These bits are read only and contain the encoded value of 0–7 possible IDs that could be used to select the LSI53C860. During a SCSI selection or reselection phase when a valid ID has been put on the bus, and the LSI53C860 responds to that ID, the “selected as” ID is written into these bits.	
SLT	Selection Response Logic Test 3 This bit is set when the LSI53C860 is ready to be selected or reselected. This does not take into account the bus settle delay of 400 ns. This bit is used for functional test and fault purposes.	
ART	Arbitration Priority Encoder Test 2 This bit will always be set when the LSI53C860 exhibits the highest priority ID asserted on the SCSI bus during arbitration. It is primarily used for chip level testing, but it may be used during low level mode operation to determine if the LSI53C860 has won arbitration.	
SOZ	SCSI Synchronous Offset Zero 1 This bit indicates that the current synchronous SREQ/SACK offset is zero. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set, the	

LSI53C860, as an initiator, is waiting for the target to request data transfers. If the LSI53C860 is a target, then the initiator has sent the offset number of acknowledges.

SOM SCSI Synchronous Offset Maximum 0

This bit indicates that the current synchronous SREQ/SACK offset is the maximum specified by bits [3:0] in the SCSI Transfer register. This bit is not latched and may change at any time. It is used in low level synchronous SCSI operations. When this bit is set, the LSI53C860, as a target, is waiting for the initiator to acknowledge the data transfers. If the LSI53C860 is an initiator, then the target has sent the offset number of requests.

Register: 0x4D (0xCD)

SCSI Test One (STEST1)

Read/Write

7	6	5	0				
SCLK	SISO	R					
0	0	x	x	x	x	x	x

SCLK SCSI Clock 7

This bit, when set, disables the external SCLK (SCSI Clock) pin, and causes the chip to use the PCI clock as the internal SCSI clock. If a transfer rate of 10 Mbytes/s is to be achieved on the SCSI bus, this bit must be cleared and the chip must be connected to at least a 40 MHz external SCLK. To achieve Ultra SCSI synchronous transfer rates, this bit must be cleared and the chip must be connected to an 80 MHz external SCLK.

SISO SCSI Isolation Mode 6

This bit allows the LSI53C860 to put the SCSI bidirectional and input pins into a low power mode when the SCSI bus is not in use. When this bit is set, the SCSI bus inputs are logically isolated from the SCSI bus.

R Reserved [5:0]

Register: 0x4E (0xCE)

SCSI Test Two (STEST2)

Read/Write

7	6	5	4	3	2	1	0
SCE	ROF	R	SLB	SZM	R	EXT	LOW
0	0	x	0	0	x	0	0

SCE	SCSI Control Enable	7
	This bit, when set, allows all SCSI control and data lines to be asserted through the SCSI Output Control Latch (SOCL) and SCSI Output Data Latch (SODL) registers regardless of whether the LSI53C860 is configured as a target or initiator.	
	<u>Note:</u> This bit should not be set during normal operation, since it could cause contention on the SCSI bus. It is included for diagnostic purposes only.	
ROF	Reset SCSI Offset	6
	Setting this bit clears any outstanding synchronous SREQ/SACK offset. This bit should be set if a SCSI gross error condition occurs, to clear the offset when a synchronous transfer does not complete successfully. The bit automatically clears itself after resetting the synchronous offset.	
R	Reserved	5
SLB	SCSI Loopback Mode	4
	Setting this bit allows the LSI53C860 to perform SCSI loopback diagnostics. That is, it enables the SCSI core to simultaneously perform as both initiator and target.	
SZM	SCSI High Impedance Mode	3
	Setting this bit places all the open-drain 48 mA SCSI drivers into a high impedance state. This is to allow internal loopback mode operation without affecting the SCSI bus.	
R	Reserved	2
EXT	Extend SREQ/SACK filtering	1
	LSI Logic TolerANT SCSI receiver technology includes a special digital filter on the SREQ/ and SACK/ pins which	

will cause glitches on deasserting edges to be disregarded. Setting this bit will increase the filtering period from 30 ns to 60 ns on the deasserting edge of the SREQ/ and SACK/ signals.

Note: This bit must never be set during fast SCSI (greater than 5 M transfers per second) operations, because a valid assertion could be treated as a glitch.

This bit does not affect the filtering period when the Fast-20 Enable bit in the [SCSI Control Three \(SCNTL3\)](#) register is set. When the LSI53C860 is executing Ultra SCSI transfers, the filtering period is automatically set at 15 ns.

LOW **SCSI Low level Mode** **0**

Setting this bit places the LSI53C860 in low level mode. In this mode, no DMA operations occur, and no SCRIPTS execute. Arbitration and selection may be performed by setting the start sequence bit as described in the [SCSI Control Zero \(SCNTL0\)](#) register. SCSI bus transfers are performed by manually asserting and polling SCSI signals. Clearing this bit allows instructions to be executed in SCSI SCRIPTS mode.

Note: It is not necessary to set this bit for access to the SCSI bit-level registers ([SCSI Output Data Latch \(SODL\)](#), [SCSI Bus Control Lines \(SBCL\)](#), and input registers).

Register: 0x4F (0xCF)
SCSI Test Three (STEST3)
Read/Write

7	6	5	4	3	2	1	0
TE	STR	HSC	DSI	R	TTM	CSF	STW
0	0	0	0	x	0	0	0

TE **TolerANT Enable** **7**

Setting this bit enables the active negation portion of TolerANT technology. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively deasserted, instead of relying on external pull-ups, when the LSI53C860 is driving these signals.

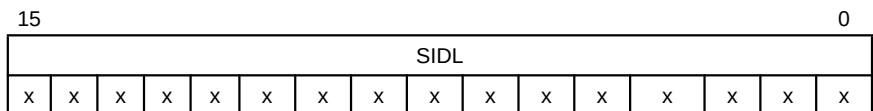
Active deassertion of these signals will occur only when the LSI53C860 is in an information transfer phase. TolerANT active negation should be enabled to improve setup and deassertion times at fast SCSI timings. Active negation is disabled after reset or when this bit is cleared. For more information on TolerANT technology, refer to [Chapter 1, “General Description.”](#)

Note: This bit must be set if the Enable Fast 20 bit in [SCSI Control Three \(SCNTL3\)](#) is set.

STR	SCSI FIFO Test Read 6 Setting this bit places the SCSI core into a test mode in which the SCSI FIFO can be easily read. Reading the SCSI Output Data Latch (SODL) register will cause the FIFO to unload.
HSC	Halt SCSI Clock 5 Asserting this bit causes the internal divided SCSI clock to come to a stop in a glitchless manner. This bit may be used for test purposes or to lower I _{DD} during a power down mode.
DSI	Disable Single Initiator Response 4 If this bit is set, the LSI53C860 will ignore all bus-initiated selection attempts that employ the single-initiator option from SCSI-1. In order to select the LSI53C860 while this bit is set, the LSI53C860's SCSI ID and the initiator's SCSI ID must both be asserted. This bit should be asserted in SCSI-2 systems so that a single bit error on the SCSI bus will not be interpreted as a single initiator response.
R	Reserved 3
TTM	Timer Test Mode 2 Setting this bit facilitates testing of the selection time-out, general purpose, and handshake-to-handshake timers by greatly reducing all three time-out periods. Setting this bit starts all three timers and, if the respective bits in the SCSI Interrupt Enable One (SIEN1) register are set, causes the LSI53C860 to generate interrupts at time-out. This bit is intended for internal manufacturing diagnosis and should not be used.

- CSF** **Clear SCSI FIFO** **1**
 Setting this bit will cause the “full flags” for the SCSI FIFO to be cleared. This empties the FIFO. This bit is self-clearing. In addition, the SCSI FIFO pointers, the [SCSI Input Data Latch \(SIDL\)](#), [SCSI Output Data Latch \(SODL\)](#), and SODR Full bits in the [SCSI Status Zero \(SSTAT0\)](#) register are cleared.
- STW** **SCSI FIFO Test Write** **0**
 Setting this bit places the SCSI core into a test mode in which the FIFO can easily be written. While this bit is set, writes to the [SCSI Output Data Latch \(SODL\)](#) register will cause the entire word contained in this register to be loaded into the FIFO. Writing the least significant byte of the [SCSI Output Data Latch \(SODL\)](#) register will cause the FIFO to load.

Register: 0x50 (0xD0)
SCSI Input Data Latch (SIDL)
Read Only



- SIDL** **SCSI Input Data Latch** **[15:0]**
 This register is used primarily for diagnostic testing, programmed I/O operation or error recovery. Data received from the SCSI bus can be read from this register. Data can be written to the [SCSI Output Data Latch \(SODL\)](#) register and then read back into the LSI53C860 by reading this register to allow loopback testing. When receiving SCSI data, the data will flow into this register and out to the host FIFO. This register differs from the [SCSI Bus Data Lines \(SBDL\)](#) register; SIDL contains latched data and the SBDL always contains exactly what is currently on the SCSI data bus. Reading this register causes the SCSI parity bit to be checked, and will cause a parity error interrupt if the data is not valid. The power-up values are indeterminate.

Register: 0x54 (0xD4)
SCSI Output Data Latch (SODL)
Read/Write

15															0
SODL															
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

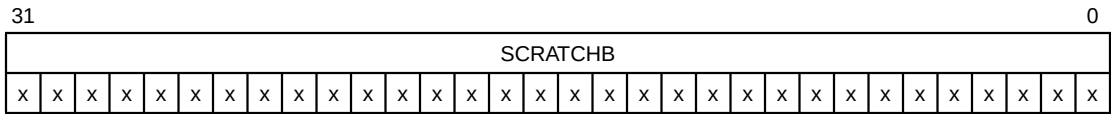
SODL **SCSI Output Data Latch** **[15:0]**
This register is used primarily for diagnostic testing or programmed I/O operation. Data written to this register is asserted onto the SCSI data bus by setting the Assert Data Bus bit in the [SCSI Control One \(SCNTL1\)](#) register. This register is used to send data using programmed I/O. Data flows through this register when sending data in any mode. It is also used to write to the synchronous data FIFO when testing the chip. The power-up value of this register is indeterminate.

Register: 0x58 (0xD8)
SCSI Bus Data Lines (SBDL)
Read Only

15															0
SBDL															
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

SBDL **SCSI Bus Data Lines** **[15:0]**
This register contains the SCSI data bus status. Even though the SCSI data bus is active low, these bits are active high. The signal status is not latched and is a true representation of exactly what is on the data bus at the time the register is read. This register is used when receiving data using programmed I/O. This register can also be used for diagnostic testing or in low level mode. The power-up value of this register is indeterminate.

Register: 0x5C–0x5F (0xDC–0xDF)
Scratch Register B (SCRATCHB)
 Read/Write



SCRATCHB Scratch Register B **[31:0]**

This is a general purpose user definable scratch pad register. Apart from CPU access, only Register Read/Write and Memory Moves directed at the SCRATCH register will alter its contents. The power-up values are indeterminate.

The LSI53C860 cannot fetch SCRIPTS instructions from this location.

Chapter 6

Instruction Set of the I/O Processor

This chapter is divided into the following sections:

- Section 6.1, “Low Level Register Interface Mode”
- Section 6.2, “SCSI SCRIPTS”
- Section 6.3, “Block Move Instructions”
- Section 6.4, “I/O Instructions”
- Section 6.5, “Read/Write Instructions”
- Section 6.6, “Transfer Control Instructions”
- Section 6.7, “Memory Move Instructions”
- Section 6.8, “Load and Store Instructions”

After power-up and initialization of the LSI53C860, the chip can operate in the low level register interface mode, or use SCSI SCRIPTS.

6.1 Low Level Register Interface Mode

With the low level register interface, the user has access to the DMA control logic and the SCSI bus control logic. An external processor has access to the SCSI bus signals and the low level DMA signals, which allows creation of complicated board level test algorithms. The low level interface is useful for backward compatibility with SCSI devices that require certain unique timings or bus sequences to operate properly. Another feature allowed at the low level is loopback testing. In loopback mode, the SCSI core can be directed to talk to the DMA core to test internal data paths all the way out to the chip's pins.

6.2 SCSI SCRIPTS

To operate in the SCSI SCRIPTS mode, the LSI53C860 requires only a SCRIPTS start address. The start address must be at a Dword (four byte) boundary. This aligns the following SCRIPTS at a Dword boundary, since all SCRIPTS are 8 or 12 bytes long. All instructions are fetched from external memory. The LSI53C860 fetches and executes its own instructions by becoming a bus master on the host bus and fetching two or three 32-bit words into its registers. Instructions are fetched until an interrupt instruction is encountered, or until an unexpected event (such as a hardware error) causes an interrupt to the external processor.

Once an interrupt is generated, the LSI53C860 halts all operations until the interrupt is serviced. Then, the start address of the next SCRIPTS instruction may be written to the [DMA SCRIPTS Pointer \(DSP\)](#) register to restart the automatic fetching and execution of instructions.

The SCSI SCRIPTS mode of execution allows the LSI53C860 to make decisions based on the status of the SCSI bus, so that the microprocessor does not have to service all of the interrupts inherent in I/O operations.

Given the rich set of SCSI oriented features included in the instruction set, and the ability to re-enter the SCSI algorithm at any point, this high level interface is all that is required for both normal and exception conditions. There is no need to switch to low level mode for error recovery.

The following types of SCRIPTS instructions are implemented in the LSI53C860 as shown in [Table 6.1](#):

Table 6.1 SCRIPTS Instructions

Instruction	Description
Block Move	Block Move instruction moves data between the SCSI bus and memory.
I/O or Read/Write	I/O or Read/Write instructions cause the LSI53C860 to trigger common SCSI hardware sequences, or to move registers.
Transfer Control	Transfer Control instruction allows SCRIPTS instructions to make decisions based on real time SCSI bus conditions.
Memory Move	Memory Move instruction causes the LSI53C860 to execute block moves between different parts of main memory.
Load and Store	Load and Store instructions provide a more efficient way to move data to/from memory from/to an internal register in the chip without using the Memory Move instruction.

Each instruction consists of two or three 32-bit words. The first 32-bit word is always loaded into the [DMA Command \(DCMD\)](#) and [DMA Byte Counter \(DBC\)](#) registers, the second into the [DMA SCRIPTS Pointer Save \(DSPS\)](#) register. The third word, used only by Memory Move instructions, is loaded into the [Temporary \(TEMP\)](#) shadow register. In an indirect I/O or Move instruction, the first two 32-bit opcode fetches will be followed by one or two more 32-bit fetch cycles.

6.2.1 Sample Operation

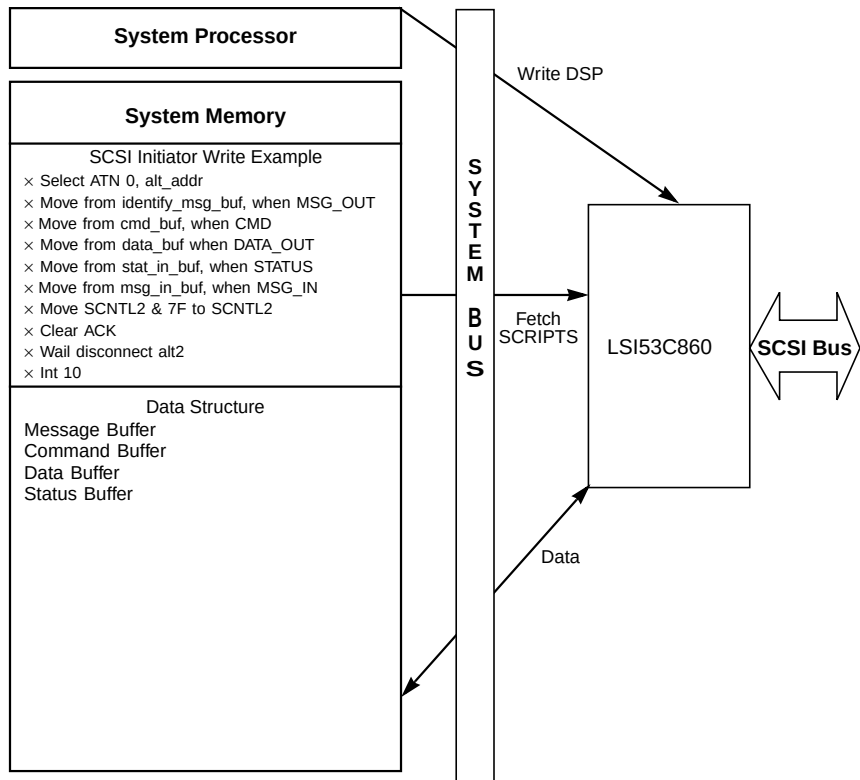
The following example describes execution of a SCRIPTS instruction. This sample operation is for a Block Move instruction. [Figure 6.1](#) illustrates a SCRIPTS Initiator Write operation, which uses several Block Move instructions.

- The host CPU, through programmed I/O, gives the [DMA SCRIPTS Pointer \(DSP\)](#) register (in the Operating Register file) the starting address in main memory that points to a SCSI SCRIPTS program for execution.

- Loading the [DMA SCRIPTS Pointer \(DSP\)](#) register causes the LSI53C860 to request use of the PCI bus to fetch its first instruction from main memory at the address just loaded.
- The LSI53C860 typically fetches two Dwords (64 bits) and decodes the high order byte of the first Dword as a SCRIPTS instruction. If the instruction is a Block Move, the lower three bytes of the first Dword are stored and interpreted as the number of bytes to be moved. The second Dword is stored and interpreted as the 32-bit beginning address in main memory to which the move is directed.
- For a SCSI send operation, the LSI53C860 waits until there is enough space in the DMA FIFO to transfer a programmable size block of data. For a SCSI receive operation, it waits until enough data is collected in the DMA FIFO for transfer to memory.
- LSI53C860 requests use of the PCI bus again, this time for data transfers.
- When the LSI53C860 is again granted the PCI bus, it will execute (as a bus master) a burst transfer (programmable size) of data, decrement the internally stored remaining byte count, increment the address pointer, and then release the PCI bus. The LSI53C860 stays off the PCI bus until the FIFO can again hold (for a write) or has collected (for a read) enough data to repeat the process.

The process repeats until the internally stored byte count has reached zero. The LSI53C860 releases the PCI bus and then requests use of the PCI bus again for another SCRIPTS instruction fetch cycle, using the incremented stored address maintained in the [DMA SCRIPTS Pointer \(DSP\)](#) register. Execution of SCRIPTS instructions continues until an error condition occurs or an interrupt SCRIPTS instruction is received. At this point, the LSI53C860 interrupts the host CPU and waits for further servicing by the host system. It can execute independent Block Move instructions, specifying new byte counts and starting locations in main memory. In this manner, the LSI53C860 performs scatter/gather operations on data without requiring help from the host program, generating a host interrupt, or requiring an external DMA controller to be programmed. [Figure 6.1](#) illustrates a SCRIPTS Initiator Write operation, which uses several Block Move instructions.

Figure 6.1 SCRIPTS Overview



6.3 Block Move Instructions

The Block Move SCRIPTS instruction is used to move data between the SCSI bus and memory. For a Block Move instruction, the LSI53C860 operates much like a chaining DMA device with a SCSI controller attached. Figure 6.2 illustrates the register bit values that represent a Block Move instruction. In Block Move instructions, bits 5 and 4 (SIOM and DIOM) in the **DMA Mode (DMODE)** register determine whether the source/destination address resides in memory or I/O space. When data is being moved onto the SCSI bus, SIOM controls whether that data comes from I/O or memory space. When data is being moved off of the SCSI bus, DIOM controls whether that data goes to I/O or memory space.

6.3.1 First Dword

IT[1:0] **Instruction Type-Block Move** [31:30]

IA **Indirect Addressing** 29

When this bit is cleared, user data is moved to or from the 32-bit data start address for the Block Move instruction. The value is loaded into the chip's address register and incremented as data is transferred. The address of data to be moved is in the second Dword of this instruction.

When set, the 32-bit user data start address for the Block Move is the address of a pointer to the actual data buffer address. The value at the 32-bit start address is loaded into the chip's [DMA Next Address \(DNAD\)](#) register using a third Dword fetch (4-byte transfer across the host computer bus).

Direct Addressing

The byte count and absolute address are:

Command	Byte Count
Address of Data	

Indirect Addressing

Use the fetched byte count, but fetch the data address from the address in the instruction.

Command	Byte Count
Address of Pointer to Data	

Once the data pointer address is loaded, it is executed as when the chip operates in the direct mode. This indirect feature allows a table of data buffer addresses to be specified. Using the SCSI SCRIPTS assembler, the table offset is placed in the SCRIPTS file when the program is assembled. Then at the actual data transfer time, the offsets are added to the base address of the data address table by the external processor. The logical I/O driver builds a structure of addresses for an I/O rather than treating each address individually. This feature makes it possible to locate SCSI SCRIPTS in a PROM.

Note: Indirect and table indirect addressing cannot be used simultaneously; only one addressing method can be used at a time.

TIA

Table Indirect

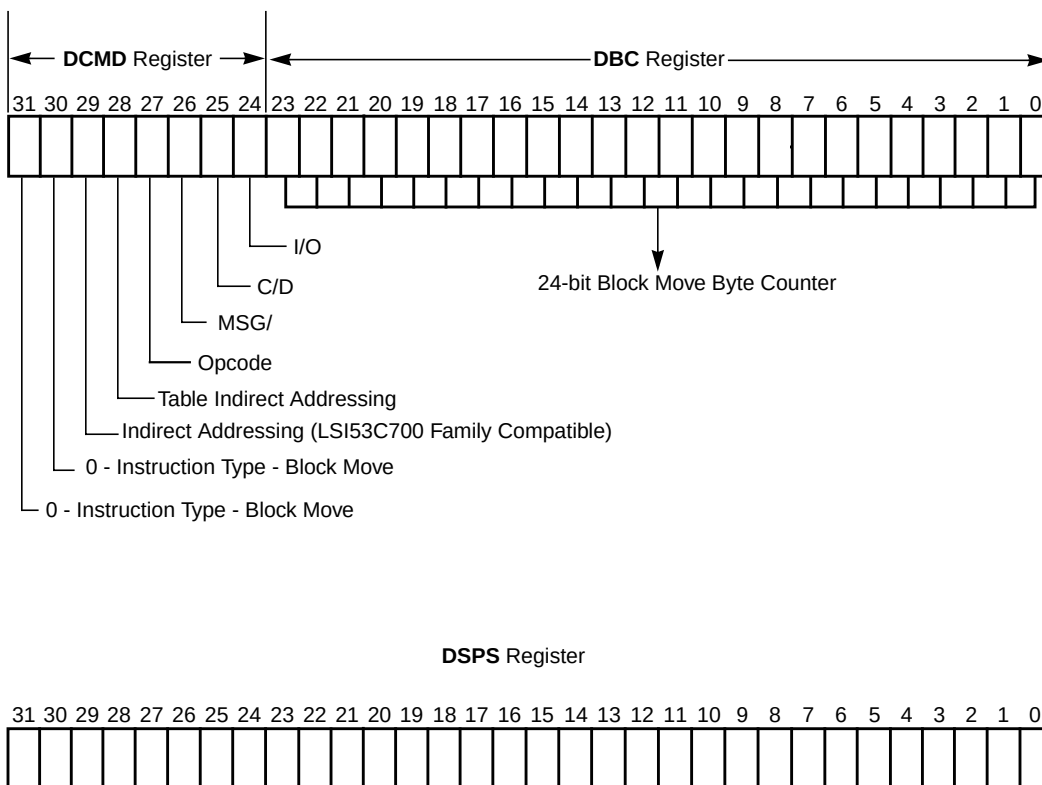
28

When this bit is set, the 24-bit signed value in the start address of the move is treated as a relative displacement from the value in the [Data Structure Address \(DSA\)](#) register. Both the transfer count and the source/destination address are fetched from this address.

Use the signed integer offset in bits [23:0] of the second four bytes of the instruction, added to the value in the [Data Structure Address \(DSA\)](#) register, to fetch first the byte count and then the data address. The signed value is combined with the data structure base address to generate the physical address used to fetch values from the data structure. Sign-extended values of all ones for negative values are allowed, but bits [31:24] are ignored.

Command	Not Used
Don't Care	Table Offset

Figure 6.2 Block Move Instruction Register



Prior to the start of an I/O, the [Data Structure Address \(DSA\)](#) register should be loaded with the base address of the I/O data structure. The address may be any address on a Dword boundary.

After a Table Indirect opcode is fetched, the DSA is added to the 24-bit signed offset value from the opcode to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from that address brings the data values into the chip.

For a MOVE instruction, the 24-bit byte count is fetched from system memory. Then the 32-bit physical address is brought into the LSI53C860. Execution of the move begins at this point.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any Dword boundary and may cross system segment boundaries.

There are two restrictions on the placement of pointer data in system memory:

- the eight bytes of data in the MOVE instruction must be contiguous, as shown below; and
- indirect data fetches are not available during execution of a Memory-to-Memory DMA operation.

00	Byte Count
Physical Data Address	

OpCode 27

This 1-bit field defines the instruction to be executed as a block move (MOVE).

Target Mode

OPC	Instruction Defined
0	MOVE
1	Reserved

These instructions perform the following steps:

1. The LSI53C860 verifies that it is connected to the SCSI bus as a Target before executing this instruction.
2. The LSI53C860 asserts the SCSI phase signals (MSG/, SC_D/, and SI_O/) as defined by the Phase Field bits in the instruction.
3. If the instruction is for the command phase, the LSI53C860 receives the first command byte and decodes its SCSI Group Code.
 - If the SCSI Group Code is either Group 0, Group 1, Group 2, or Group 5, then the LSI53C860 overwrites the [DMA Byte Counter \(DBC\)](#) register with the length of the Command Descriptor Block: 6, 10, or 12 bytes.

- If any other Group Code is received, the [DMA Byte Counter \(DBC\)](#) register is not modified and the LSI53C860 will request the number of bytes specified in the [DMA Byte Counter \(DBC\)](#) register. If the [DMA Byte Counter \(DBC\)](#) register contains 0x000000, an illegal instruction interrupt is generated.
- 4. The LSI53C860 transfers the number of bytes specified in the [DMA Byte Counter \(DBC\)](#) register starting at the address specified in the [DMA Next Address \(DNAD\)](#) register.
- 5. If the SATN/ signal is asserted by the Initiator or a parity error occurred during the transfer, the transfer can optionally be halted and an interrupt generated. The Disable Halt on Parity Error or ATN bit in the [SCSI Control One \(SCNTL1\)](#) register controls whether the LSI53C860 halts on these conditions immediately, or waits until completion of the current Move.

Initiator Mode

OPC	Instruction Defined
0	Reserved
1	MOVE

These instructions perform the following steps:

1. The LSI53C860 verifies that it is connected to the SCSI bus as an Initiator before executing this instruction.
2. The LSI53C860 waits for an unserviced phase to occur. An unserviced phase is any phase (with SREQ/ asserted) for which the LSI53C860 has not yet transferred data by responding with a SACK/.

3. The LSI53C860 compares the SCSI phase bits in the [DMA Command \(DCMD\)](#) register with the latched SCSI phase lines stored in the [SCSI Status One \(SSTAT1\)](#) register. These phase lines are latched when SREQ/ is asserted.
4. If the SCSI phase bits match the value stored in the SCSI [SCSI Status One \(SSTAT1\)](#) register, the LSI53C860 transfers the number of bytes specified in the [DMA Byte Counter \(DBC\)](#) register starting at the address pointed to by the [DMA Next Address \(DNAD\)](#) register.
5. If the SCSI phase bits do not match the value stored in the [SCSI Status One \(SSTAT1\)](#) register, the LSI53C860 generates a phase mismatch interrupt and the instruction is not executed.
6. During a Message-Out phase, after the LSI53C860 has performed a select with Attention (or SATN/ is manually asserted with a Set ATN instruction), the LSI53C860 deasserts SATN/ during the final SREQ/SACK/ handshake of the first move of Message-Out bytes after SATN/ was set.
7. When the LSI53C860 is performing a block move for Message-In phase, it does not deassert the SACK/ signal for the last SREQ/SACK/ handshake. Clear the SACK/ signal using the Clear SACK I/O instruction.

SCSIP[2:0]

SCSI Phase

[26:24]

This 3-bit field defines the desired SCSI information transfer phase. When the LSI53C860 operates in initiator mode, these bits are compared with the latched SCSI phase bits in the [SCSI Status One \(SSTAT1\)](#) register. When the LSI53C860 operates in target mode, the LSI53C860 asserts the phase defined in this field. The following table describes the possible combinations and the corresponding SCSI phase.

MSG	C_D	I_O	SCSI Phase
0	0	0	Data-Out
0	0	1	Data-In
0	1	0	Command
0	1	1	Status
1	0	0	Reserved-Out
1	0	1	Reserved-In
1	1	0	Message-Out
1	1	1	Message-In

TC[23:0]

Transfer Counter

[23:0]

This 24-bit field specifies the number of data bytes to be moved between the LSI53C860 and system memory. The field is stored in the [DMA Byte Counter \(DBC\)](#) register. When the LSI53C860 transfers data to/from memory, the [DMA Byte Counter \(DBC\)](#) register is decremented by the number of bytes transferred. In addition, the [DMA Next Address \(DNAD\)](#) register is incremented by the number of bytes transferred. This process is repeated until the [DMA Byte Counter \(DBC\)](#) register has been decremented to zero. At that time, the LSI53C860 fetches the next instruction.

If bit 28 is set, indicating table indirect addressing, this field is not used. The byte count is instead fetched from a table pointed to by the [Data Structure Address \(DSA\)](#) register.

6.3.2 Second Dword

Start Address

[31:0]

This 32-bit field specifies the starting address of the data to be moved to/from memory. This field is copied to the [DMA Next Address \(DNAD\)](#) register. When the LSI53C860 transfers data to or from memory, the [DMA Next Address \(DNAD\)](#) register is incremented by the number of bytes transferred.

When bit 29 is set, indicating indirect addressing, this address is a pointer to an address in memory that points to the data location. When bit 28 is set, indicating table

indirect addressing, the value in this field is an offset into a table pointed to by the DSA. The table entry contains byte count and address information.

6.4 I/O Instructions

The I/O SCRIPTS instruction causes the LSI53C860 to trigger common SCSI hardware sequences such as Set/Clear ACK, Set/Clear ATN, Set/Clear Target Mode, Select With ATN, or Wait for Reselect.

6.4.1 First Dword

IT[1:0] **Instruction Type - I/O Instruction** **[31:30]**

OPC[2:0] **OpCode** **[29:27]**

The following OpCode bits have different meanings, depending on whether the LSI53C860 is operating in initiator or target mode.

Note: OpCode selections 101–111 are considered Read/Write instructions, and are described in that section.

Target Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Reselect
0	0	1	Disconnect
0	1	0	Wait Select
0	1	1	Set
1	0	0	Clear

Reselect Instruction

1. The LSI53C860 arbitrates for the SCSI bus by asserting the SCSI ID stored in the [SCSI Chip ID \(SCID\)](#) register. If it loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.
2. If the LSI53C860 wins arbitration, it attempts to reselect the SCSI device whose ID is defined in the destination ID field of the instruction. Once the

LSI53C860 wins arbitration, it fetches the next instruction from the address pointed to by the [DMA SCRIPTS Pointer \(DSP\)](#) register. This way the SCRIPTS can move on to the next instruction before the reselection completes. It continues executing SCRIPTS until a SCRIPT that requires a response from the Initiator is encountered.

3. If the LSI53C860 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the [DMA Next Address \(DNAD\)](#) register. Manually set the LSI53C860 to Initiator mode if it is reselected, or to Target mode if it is selected.

Disconnect Instruction

The LSI53C860 disconnects from the SCSI bus by deasserting all SCSI signal outputs.

Wait Select Instruction

1. If the LSI53C860 is selected, it fetches the next instruction from the address pointed to by the [DMA SCRIPTS Pointer \(DSP\)](#) register.
2. If reselected, the LSI53C860 fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the [DMA Next Address \(DNAD\)](#) register. Manually set the LSI53C860 to Initiator mode when it is reselected.
3. If the CPU sets the SIGP bit in the [SCSI Status Zero \(SSTAT0\)](#) register, the LSI53C860 aborts the Wait Select instruction and fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the [DMA Next Address \(DNAD\)](#) register.

Set Instruction

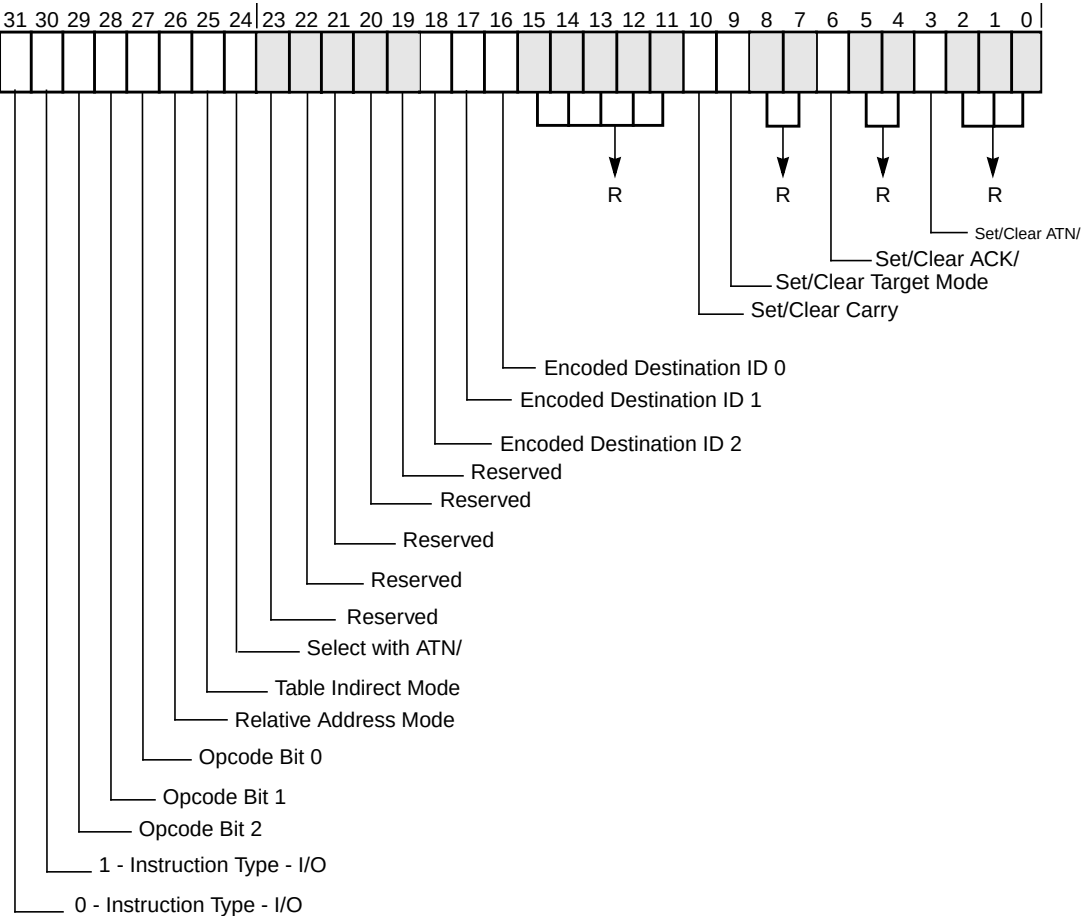
When the SACK/ or SATN/ bits are set, the corresponding bits in the [SCSI Output Control Latch \(SOCL\)](#) register are set. SACK/ or SATN/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the [SCSI Control Zero \(SCNTL0\)](#)

register is also set. When the carry bit is set, the corresponding bit in the Arithmetic Logic Unit (ALU) is set.

Note: None of the signals are set on the SCSI bus in target mode.

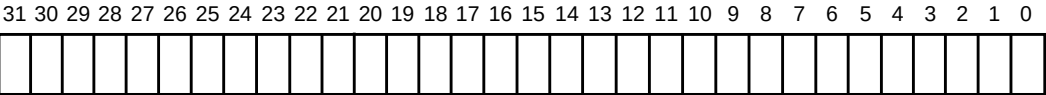
Figure 6.3 illustrates the register bit values that represent an I/O instruction.

Figure 6.3 I/O Instruction Register



Second 32-bit Word of the I/O Instruction

DSPS Register



32-bit Jump Address

Clear Instruction

When the SACK/ or SATN/ bits are set, the corresponding bits are cleared in the [SCSI Output Control Latch \(SOCL\)](#) register. SACK/ or SATN/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the [SCSI Control Zero \(SCNTL0\)](#) register is cleared. When the carry bit is set, the corresponding bit in the ALU is cleared.

Note: None of the signals are reset on the SCSI bus in target mode.

Initiator Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Select
0	0	1	Wait Disconnect
0	1	0	Wait Reselect
0	1	1	Set
1	0	0	Clear

Select Instruction

1. The LSI53C860 arbitrates for the SCSI bus by asserting the SCSI ID stored in the [SCSI Chip ID \(SCID\)](#) register. If it loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.
2. If the LSI53C860 wins arbitration, it attempts to select the SCSI device whose ID is defined in the destination ID field of the instruction. Once the LSI53C860 wins arbitration, it fetches the next instruction from the address pointed to by the [DMA SCRIPTS Pointer \(DSP\)](#) register. This way the SCRIPTS can move to the next instruction before the selection completes. It continues executing SCRIPTS until a SCRIPT that requires a response from the Target is encountered.
3. If the LSI53C860 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the [DMA Next Address \(DNAD\)](#) register.

Manually set the LSI53C860 to Initiator mode if it is reselected, or to Target mode if it is selected.

4. If the Select with SATN/ field is set, the SATN/ signal is asserted during the selection phase.

Wait Disconnect Instruction

1. The LSI53C860 waits for the Target to perform a “legal” disconnect from the SCSI bus. A “legal” disconnect occurs when SBSY/ and SSEL/ are inactive for a minimum of one Bus Free delay (400 ns), after the LSI53C860 has received a Disconnect Message or a Command Complete Message.

Wait Reselect Instruction

1. If the LSI53C860 is selected before being reselected, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the [DMA Next Address \(DNAD\)](#) register. Manually set the LSI53C860 to Target mode when it is selected.
2. If the LSI53C860 is reselected, it fetches the next instruction from the address pointed to by the [DMA SCRIPTS Pointer \(DSP\)](#) register.
3. If the CPU sets the SIGP bit in the [Interrupt Status \(ISTAT\)](#) register, the LSI53C860 aborts the Wait Reselect instruction and fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the [DMA Next Address \(DNAD\)](#) register.

Set Instruction

When the SACK/ or SATN/ bits are set, the corresponding bits in the [SCSI Output Control Latch \(SOCL\)](#) register are set. When the Target bit is set, the corresponding bit in the [SCSI Control Zero \(SCNTL0\)](#) register is also set. When the Carry bit is set, the corresponding bit in the ALU is set.

Clear Instruction

When the SACK/or SATN/ bits are set, the corresponding bits are cleared in the [SCSI Output Control Latch \(SOCL\)](#)

register. When the Target bit is set, the corresponding bit in the [SCSI Control Zero \(SCNTL0\)](#) register is cleared. When the Carry bit is set, the corresponding bit in the ALU is cleared.

RA **Relative Addressing Mode** **26**

When this bit is set, the 24-bit signed value in the [DMA Next Address \(DNAD\)](#) register is used as a relative displacement from the current DSP address. This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. The Select and Reselect instructions can contain an absolute alternate jump address or a relative transfer address.

TI **Table Indirect Mode** **25**

When this bit is set, the 24-bit signed value in the [DMA Byte Counter \(DBC\)](#) register is added to the value in the [Data Structure Address \(DSA\)](#) register, used as an offset relative to the value in the [Data Structure Address \(DSA\)](#) register. The SCNTL3 value, SCSI ID, synchronous offset and synchronous period are loaded from this address. Prior to the start of an I/O, the DSA should be loaded with the base address of the I/O data structure. The address may be any address on a Dword boundary. After a Table Indirect opcode is fetched, the DSA is added to the 24-bit signed offset value from the opcode to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from that address brings the data values into the chip.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any Dword boundary and may cross system segment boundaries. There are two restrictions on the placement of data in system memory:

- The I/O data structure must lie within the 8 Mbytes above or below the base address.
- An I/O command structure must have all four bytes contiguous in system memory, as shown below. The offset/period bits are ordered as in the [SCSI Transfer \(SXFER\)](#) register. The configuration bits are ordered as in the [SCSI Control Three \(SCNTL3\)](#) register.

Config	ID	Offset/period	00
--------	----	---------------	----

This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. Bits 25 and 26 may be set individually or in combination:

	Bit 25	Bit 26
Direct	0	0
Table Indirect	0	1
Relative	1	0
Table Relative	1	1

Direct

Uses the device ID and physical address in the instruction.

Command	ID	Not Used	Not Used
Absolute Alternate Address			

Table Indirect

Uses the physical jump address, but fetches data using the table indirect method.

Command	Table Offset
Absolute Jump Offset	

Relative

Uses the device ID in the instruction, but treats the alternate address as a relative jump.

Command	ID	Not Used	Not Used
Absolute Jump Offset			

Table Relative

Treats the alternate jump address as a relative jump and fetches the device ID, synchronous offset, and synchronous period indirectly. Adds the value in bits

[23:0] of the first four bytes of the SCRIPTS instruction to the data structure base address to form the fetch address.

Command	Table Offset
Absolute Jump Offset	

Sel	Select with ATN/ 24 This bit specifies whether SATN/ will be asserted during the selection phase when the LSI53C860 is executing a Select instruction. When operating in initiator mode, set this bit for the Select instruction. If this bit is set on any other I/O instruction, an illegal instruction interrupt is generated.
ENDID	Encoded SCSI Destination ID [18:16] This 3-bit field specifies the destination SCSI ID for an I/O instruction.
CC	Set/Clear Carry 10 This bit is used in conjunction with a Set or Clear instruction to set or clear the Carry bit. Setting this bit with a Set instruction asserts the Carry bit in the ALU. Setting this bit with a Clear instruction deasserts the Carry bit in the ALU.
TM	Set/Clear Target Mode 9 This bit is used in conjunction with a Set or Clear instruction to set or clear target mode. Setting this bit with a Set instruction configures the LSI53C860 as a target device (this sets bit 0 of the SCSI Control Zero (SCNTL0) register). Clearing this bit with a Clear instruction configures the LSI53C860 as an initiator device (this clears bit 0 of the SCSI Control Zero (SCNTL0) register).
ACK	Set/Clear SACK/ 6
ATN	Set/Clear SATN/ 3 These two bits are used in conjunction with a Set or Clear instruction to assert or deassert the corresponding SCSI control signal. Bit 6 controls the SCSI SACK/ signal; bit 3 controls the SCSI SATN/ signal.

Setting either of these bits will set or reset the corresponding bit in the [SCSI Output Control Latch \(SOCL\)](#) register, depending on the instruction used. The Set instruction is used to assert SACK/ and/or SATN/ on the SCSI bus. The Clear instruction is used to deassert SACK/ and/or SATN/ on the SCSI bus.

Since SACK/ and SATN/ are initiator signals, they will not be asserted on the SCSI bus unless the LSI53C860 is operating as an initiator or the SCSI Loopback Enable bit is set in the [SCSI Test Two \(STEST2\)](#) register.

The Set/Clear SCSI ACK/ATN instruction would be used after message phase Block Move operations to give the initiator the opportunity to assert attention before acknowledging the last message byte. For example, if the initiator wishes to reject a message, an Assert SCSI ATN instruction would be issued before a Clear SCSI ACK instruction.

R	Reserved	[2:0]
----------	-----------------	--------------

6.4.2 Second Dword

SA	Start Address	[31:0]
-----------	----------------------	---------------

This 32-bit field contains the memory address to fetch the next instruction if the selection or reselection fails.

If relative or table relative addressing is used, this value is a 24-bit signed offset relative to the current [DMA SCRIPTS Pointer \(DSP\)](#) register value.

6.5 Read/Write Instructions

The Read/Write Instruction type moves the contents of one register to another, or performs arithmetic operations such as AND, OR, XOR, Addition, and Shift.

6.5.1 First Dword

IT[1:0]	Instruction Type - Read/Write Instruction	[31:30]
----------------	--	----------------

The Read/Write instruction uses operator bits 26 through 24 in conjunction with the opcode bits to determine which instruction is currently selected.

OPC[2:0]	OpCode [29:27] The combinations of these bits determine if the instruction is a Read/Write or an I/O instruction. Opcodes 000 through 100 are considered I/O instructions. Refer to Table 6.2 for field definitions.
O[2:0]	Operator [26:24] These bits are used in conjunction with the opcode bits to determine which instruction is currently selected. Refer to Table 6.2 for field definitions.
A[6:0]	Register Address - A[6:0] [22:16] Register values may be changed from SCRIPTS in read-modify-write cycles or move to/from SFBR cycles. A[6:0] select an 8-bit source/destination register within the LSI53C860.

6.5.2 Second Dword

Destination Address [31:0] This field contains the 32-bit destination address where the data is to be moved.
--

6.5.3 Read-Modify-Write Cycles

During these cycles the register is read, the selected operation is performed, and the result is written back to the source register.

The Add operation can be used to increment or decrement register values (or memory values if used in conjunction with a Memory-to-Register Move operation) for use as loop counters.

6.5.4 Move To/From SFBR Cycles

All operations are read-modify-writes. However, two registers are involved, one of which is always the SFBR. The possible functions of this instruction are:

- Write one byte (value contained within the SCRIPTS instruction) into any chip register.
- Move to/from the [SCSI First Byte Received \(SFBR\)](#) from/to any other register.

- Alter the value of a register with AND, OR, ADD, XOR, SHIFT LEFT, or SHIFT RIGHT operators.
- After moving values to the [SCSI First Byte Received \(SFBR\)](#), the compare and jump, call, or similar instructions may be used to check the value.
- A Move-to-SFBR followed by a Move-from-SFBR can be used to perform a register to register move.

[Figure 6.4](#) illustrates the register bit values that represent a Read/Write instruction.

Figure 6.4 Read/Write Register Instruction

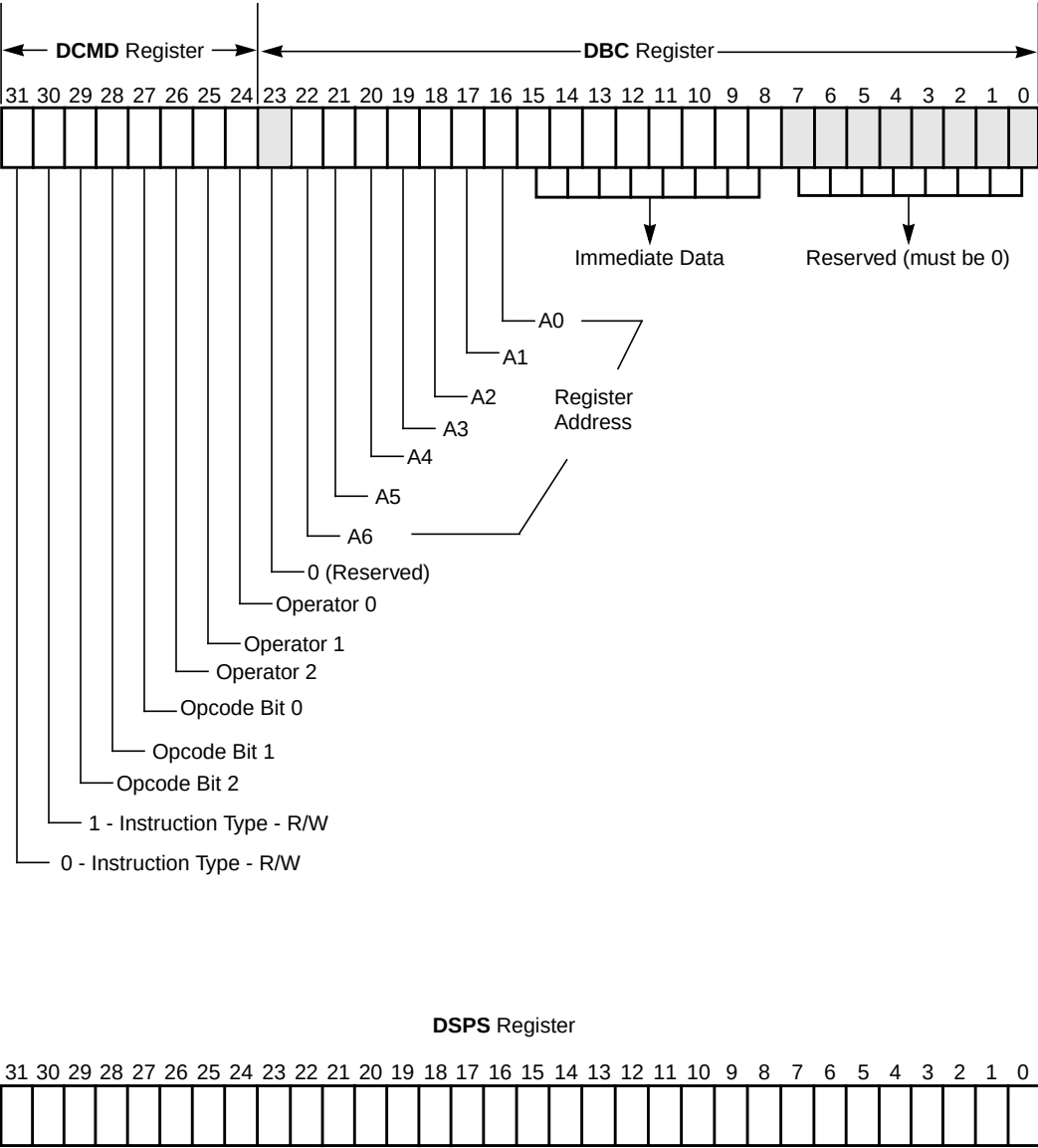


Table 6.2 Read/Write Instructions

Operator	Opcode 111 Read-Modify-Write	Opcode 110 Move to SFBR	Opcode 101 Move from SFBR
000	Move data into register. Syntax: "Move data8 to RegA"	Move data into SCSI First Byte Received (SFBR) register. Syntax: "Move data8 to SFBR"	Move data into register. Syntax: "Move data8 to RegA"
001 ¹	Shift register one bit to the left and place the result in the same register. Syntax: "Move RegA SHL RegA"	Shift register one bit to the left and place the result in the SCSI First Byte Received (SFBR) register. Syntax: "Move RegA SHL SFBR"	Shift the SCSI First Byte Received (SFBR) register one bit to the left and place the result in the register. Syntax: "Move SFBR SHL RegA"
010	OR data with register and place the result in the same register. Syntax: "Move RegA data8 to RegA"	OR data with register and place the result in the SCSI First Byte Received (SFBR) register. Syntax: "Move RegA data8 to SFBR"	OR data with SFBR and place the result in the register. Syntax: "Move SFBR data8 to RegA"
011	XOR data with register and place the result in the same register. Syntax: "Move RegA XOR data8 to RegA"	XOR data with register and place the result in the SCSI First Byte Received (SFBR) register. Syntax: "Move RegA XOR data8 to SFBR"	XOR data with SFBR and place the result in the register. Syntax: "Move SFBR XOR data8 to RegA"
100	AND data with register and place the result in the same register. Syntax: "Move RegA & data8 to RegA"	AND data with register and place the result in the SCSI First Byte Received (SFBR) register. Syntax: "Move RegA & data8 to SFBR"	AND data with SFBR and place the result in the register. Syntax: "Move SFBR & data8 to RegA"
101 ¹	Shift register one bit to the right and place the result in the same register. Syntax: "Move RegA SHR RegA"	Shift register one bit to the right and place the result in the SCSI First Byte Received (SFBR) register. Syntax: "Move RegA SHR SFBR"	Shift the SCSI First Byte Received (SFBR) register one bit to the right and place the result in the register. Syntax: "Move SFBR SHR RegA"

Table 6.2 Read/Write Instructions (Cont.)

Operator	Opcode 111 Read-Modify-Write	Opcode 110 Move to SFBR	Opcode 101 Move from SFBR
110	Add data to register without carry and place the result in the same register. Syntax: "Move RegA + data8 to RegA"	Add data to register without carry and place the result in the SCSI First Byte Received (SFBR) register. Syntax: "Move RegA + data8 to SFBR"	Add data to SFBR without carry and place the result in the register. Syntax: "Move SFBR + data8 to RegA"
111	Add data to register with carry and place the result in the same register. Syntax: "Move RegA + data8 to RegA with carry"	Add data to register with carry and place the result in the SCSI First Byte Received (SFBR) register. Syntax: "Move RegA + data8 to SFBR with carry"	Add data to SFBR with carry and place the result in the register. Syntax: "Move SFBR + data8 to RegA with carry"

1. Data is shifted through the Carry bit and the Carry bit is shifted into the data byte.

Miscellaneous Notes:

- ~ Substitute the desired register name or address for "RegA" in the syntax examples.
- ~ data8 indicates eight bits of data.

6.6 Transfer Control Instructions

The Transfer Control or Conditional Jump instruction allows you to write SCRIPTS that make decisions based on real time conditions on the SCSI bus, such as phase or data. This instruction type includes Jump, Call, Return, and Interrupt instructions.

6.6.1 First Dword

IT[2:0]	Instruction Type - Transfer Control Instruction	[31:30]
OPC[2:0]	OpCode This 3-bit field specifies the type of transfer control instruction to be executed. All transfer control instructions can be conditional. They can be dependent on a true/false comparison of the ALU Carry bit or a comparison of the SCSI information transfer phase with the Phase field, and/or a comparison of the First Byte Received with the Data Compare field. Each instruction can operate in initiator or target mode.	[29:27]

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Jump
0	0	1	Call
0	1	0	Return
0	1	1	Interrupt
1	x	x	Reserved

Jump Instruction

The LSI53C860 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare and True/False bit fields. If the comparisons are true, the LSI53C860 loads the [DMA SCRIPTS Pointer \(DSP\)](#) register with the contents of the [DMA SCRIPTS Pointer Save \(DSPS\)](#) register. The [DMA SCRIPTS Pointer \(DSP\)](#) register now contains the address of the next instruction.

If the comparisons are false, the LSI53C860 fetches the next instruction from the address pointed to by the [DMA SCRIPTS Pointer \(DSP\)](#) register, leaving the instruction pointer unchanged.

Call Instruction

The LSI53C860 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the LSI53C860 loads the [DMA SCRIPTS Pointer \(DSP\)](#) register with the contents of the [DMA SCRIPTS Pointer Save \(DSPS\)](#) register and that address value becomes the address of the next instruction.

When the LSI53C860 executes a Call instruction, the instruction pointer contained in the [DMA SCRIPTS Pointer \(DSP\)](#) register is stored in the [Temporary \(TEMP\)](#) register. Since the [Temporary \(TEMP\)](#) register is not a stack and can only hold one Dword, nested call instructions are not allowed.

If the comparisons are false, the LSI53C860 fetches the next instruction from the address pointed to by the [DMA SCRIPTS Pointer \(DSP\)](#) register and the instruction pointer is not modified.

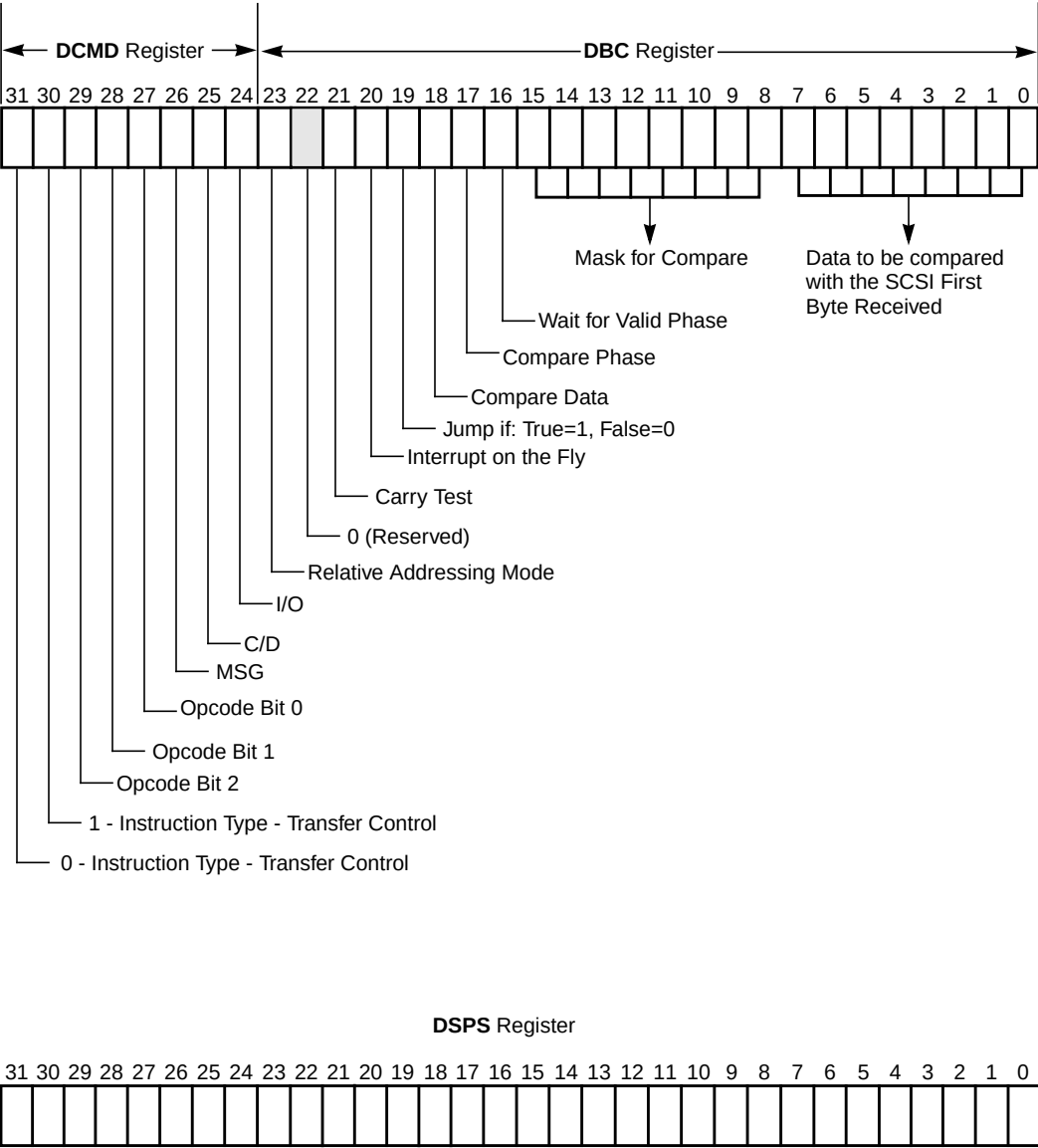
Return Instruction

The LSI53C860 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the LSI53C860 loads the [DMA SCRIPTS Pointer \(DSP\)](#) register with the contents of the [DMA SCRIPTS Pointer Save \(DSPS\)](#) register. That address value becomes the address of the next instruction.

When a Return instruction is executed, the value stored in the [Temporary \(TEMP\)](#) register is returned to the [DMA SCRIPTS Pointer \(DSP\)](#) register. The LSI53C860 does not check to see whether the Call instruction has already been executed. It will not generate an interrupt if a Return instruction is executed without previously executing a Call instruction.

[Figure 6.5](#) illustrates the register bit values that represent a Transfer Control instruction.

Figure 6.5 Transfer Control Instruction



If the comparisons are false, then the LSI53C860 fetches the next instruction from the address pointed to by the [DMA SCRIPTS Pointer \(DSP\)](#) register and the instruction pointer will not be modified.

Interrupt Instruction

The LSI53C860 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the LSI53C860 generates an interrupt by asserting the IRQ/ signal.

The 32-bit address field stored in the [DMA SCRIPTS Pointer Save \(DSPS\)](#) register can contain a unique interrupt service vector. When servicing the interrupt, this unique status code allows the ISR to quickly identify the point at which the interrupt occurred.

The LSI53C860 halts and the [DMA SCRIPTS Pointer \(DSP\)](#) register must be written to start any further operation.

Interrupt on-the-Fly Instruction

The LSI53C860 can do a true/false comparison of the ALU carry bit or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, and the Interrupt-on-the-Fly bit is set (bit 2), the LSI53C860 will assert the Interrupt-on-the-Fly bit ([Interrupt Status \(ISTAT\)](#) bit 2).

SCSIP[2:0]

SCSI Phase

[26:24]

This 3-bit field corresponds to the three SCSI bus phase signals which are compared with the phase lines latched when SREQ/ is asserted. Comparisons can be performed to determine the SCSI phase actually being driven on the SCSI bus. The following table describes the possible combinations and their corresponding SCSI phase. These bits are only valid when the LSI53C860 is operating in initiator mode; when the LSI53C860 is operating in the target mode, these bits should be cleared.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data-Out
0	0	1	Data-In
0	1	0	Command
0	1	1	Status
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Message-Out
1	1	1	Message-In

RA

Relative Addressing Mode

23

When this bit is set, the 24-bit signed value in the [DMA SCRIPTS Pointer Save \(DSPS\)](#) register is used as a relative offset from the current DSP address (which is pointing to the next instruction, not the one currently executing). Relative mode does not apply to Return and Interrupt SCRIPTS.

Jump/Call an Absolute Address

Start execution at the new absolute address.

Command	Condition Codes
Absolute Alternate Address	

Jump/Call a Relative Address

Start execution at the current address plus (or minus) the relative offset.

Command	Condition Codes
Don't Care	Alternate Jump Offset

The SCRIPTS program counter is a 32-bit value pointing to the SCRIPTS instruction currently being executed by the LSI53C860. The next address is formed by adding the 32-bit program counter to the 24-bit signed value of the last 24 bits of the Jump or Call instruction. Because it is signed (2's complement), the jump can be forward or backward.

SCRIPTS programs may contain a mixture of direct jumps and relative jumps to provide maximum versatility when writing SCRIPTS. For example, major sections of code can be accessed with far calls using the 32-bit physical address, then local labels can be called using relative transfers. If a SCRIPTS instruction uses only relative transfers it would not require any run time alteration of physical addresses, and could be stored in and executed from a PROM.

When this bit is set, decisions based on the ALU carry bit can be made. True/False comparisons are legal, but Data Compare and Phase Compare are illegal.

When this bit is set, the Interrupt instruction will not halt the SCRIPTS processor. Once the interrupt occurs, the Interrupt-on-the-Fly bit ([Interrupt Status \(ISTAT\)](#), bit 2) will be asserted.

This bit determines whether the LSI53C860 should branch when a comparison is true or when a comparison is false. This bit applies to phase compares, data compares, and carry tests. If both the Phase Compare and Data Compare bits are set, then both compares must be true to branch on a true condition. Both compares must be false to branch on a false condition.

CD	Compare Data 18 When this bit is set, the first byte received from the SCSI data bus (contained in SCSI First Byte Received (SFBR) register) is compared with the Data to be Compared Field in the Transfer Control instruction. The Wait for Valid Phase bit controls when this compare will occur. The Jump if True/False bit determines the condition (true or false) to branch on.
CP	Compare Phase 17 When the LSI53C860 is in initiator mode, this bit controls phase compare operations. When this bit is set, the SCSI phase signals (latched by SREQ/) are compared to the Phase Field in the Transfer Control instruction; if they match, the comparison is true. The Wait for Valid Phase bit controls when the compare will occur. When the LSI53C860 is operating in target mode this bit, when set, tests for an active SCSI SATN/ signal.
WVP	Wait For Valid Phase 16 If the Wait for Valid Phase bit is set, the LSI53C860 waits for a previously unserviced phase before comparing the SCSI phase and data. If the Wait for Valid Phase bit is clear, the LSI53C860 compares the SCSI phase and data immediately.
DCM	Data Compare Mask [15:8] The Data Compare Mask allows a SCRIPTS instruction to test certain bits within a data byte. During the data compare, any mask bits that are set cause the corresponding bit in the SFBR data byte to be ignored. For instance, a mask of 01111111b and data compare value of 1XXXXXXXb allows the SCRIPTS processor to determine whether or not the high order bit is set while ignoring the remaining bits.
DCV	Data Compare Value [7:0] This 8-bit field is the data to be compared against the SCSI First Byte Received (SFBR) register. These bits are used in conjunction with the Data Compare Mask Field to test for a particular data value.

6.6.2 Second Dword

Jump Address

[31:0]

This 32-bit field contains the address of the next instruction to fetch when a jump is taken. Once the LSI53C860 has fetched the instruction from the address pointed to by these 32 bits, this address is incremented by 4, loaded into the [DMA SCRIPTS Pointer \(DSP\)](#) register and becomes the current instruction pointer.

6.7 Memory Move Instructions

This SCRIPTS Instruction allows the LSI53C860 to execute high performance block moves of 32-bit data from one part of main memory to another. In this mode, the LSI53C860 is an independent, high-performance DMA controller irrespective of SCSI operations. Since the registers of the LSI53C860 can be mapped into system memory, this SCRIPTS instruction also moves an LSI53C860 register to or from memory or another LSI53C860 register.

For Memory Move instructions, bits 5 and 4 (SIOM and DIOM) in the [DMA Mode \(DMODE\)](#) register determine whether the source or destination addresses reside in memory or I/O space. By setting these bits appropriately, data may be moved within memory space, within I/O space, or between the two address spaces.

The Memory Move instruction is used to copy the specified number of bytes from the source address to the destination address.

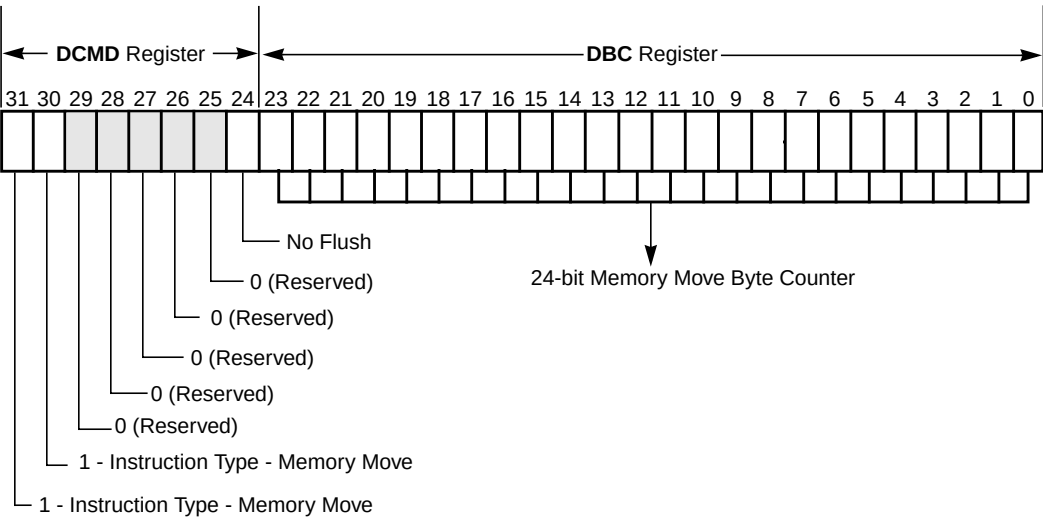
Allowing the LSI53C860 to perform memory moves frees the system processor for other tasks and moves data at higher speeds than available from current DMA controllers. Up to 16 Mbytes may be transferred with one instruction. There are two restrictions:

- Both the source and destination addresses must start with the same address alignment (A[1:0] must be the same). If source and destination are not aligned, then an illegal instruction interrupt will occur.

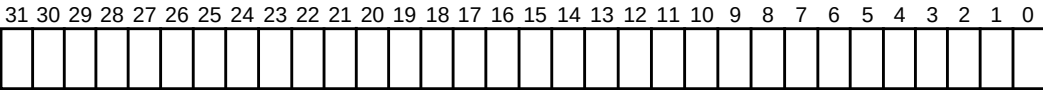
- Indirect addresses are not allowed. A burst of data is fetched from the source address, put into the DMA FIFO and then written out to the destination address. The move continues until the byte count decrements to zero, then another SCRIPTS instruction is fetched from system memory.

Figure 6.6 illustrates the register bit values that represent a Memory Move instruction.

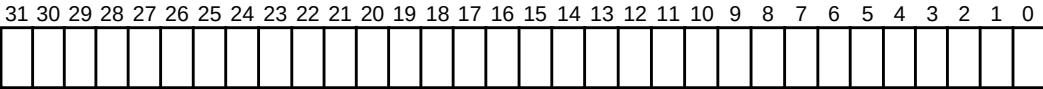
Figure 6.6 Memory to Memory Move Instruction



DSPPS Register



TEMP Register



The [DMA SCRIPTS Pointer Save \(DSPS\)](#) and [Data Structure Address \(DSA\)](#) registers are additional holding registers used during the Memory Move; however, the contents of the [Data Structure Address \(DSA\)](#) register are preserved.

6.7.1 First Dword

IT[1:0]	Instruction Type - Memory Move Instruction	[31:30]
R	Reserved	[29:25]
	These bits are reserved and must be zero. If any of these bits are set, an illegal instruction interrupt will occur.	
NF	No Flush	24

Note: This bit has no effect unless the Prefetch Enable bit in the [DMA Control \(DCNTL\)](#) register is set. For information on SCRIPTS instruction prefetching, see [Chapter 2, "Functional Description."](#)

When this bit is set, the LSI53C860 performs a Memory Move (MMOV) without flushing the prefetch unit (NFMMOV). When this bit is clear, the Memory Move instruction automatically flushes the prefetch unit. NFMMOV should be used if the source and destination are not within four instructions of the current MMOV instruction.

TC[23:0]	Transfer Count	[23:0]
	The number of bytes to be transferred is stored in the lower 24 bits of the first instruction word.	

6.7.2 Second Dword

DSPS Register	[31:0]
These bits contain the source address of the Memory Move.	

6.7.3 Third Dword

TEMP Register	[31:0]
These bits contain the destination address for the Memory Move.	

6.7.4 Read/Write System Memory from a SCRIPTS Instruction

By using the Memory Move instruction, single or multiple register values may be transferred to or from system memory.

Because the LSI53C860 will respond to addresses as defined in the Base I/O or Base Memory registers, it could be accessed during a Memory Move operation if the source or destination address decodes to within the chip's register space. If this occurs, the register indicated by the lower seven bits of the address is taken to be the data source or destination. In this way, register values can be saved to system memory and later restored, and SCRIPTS can make decisions based on data values in system memory.

The SFBR is not writable using the CPU, and therefore not by a Memory Move. However, it can be loaded using SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate LSI53C860 register (for example, a SCRATCH register), and then to the SFBR.

The same address alignment restrictions apply to register access operations as to normal memory-to-memory transfers.

6.8 Load and Store Instructions

The Load and Store instruction provides a more efficient way to move data from/to memory to/from an internal register in the chip without using the normal memory move instruction.

The load and store instructions are represented by two Dword opcodes. The first Dword contains the [DMA Command \(DCMD\)](#) and [DMA Byte Counter \(DBC\)](#) register values. The second Dword contains the [DMA SCRIPTS Pointer Save \(DSPS\)](#) value. This is either the actual memory location of where to load or store, or the offset from the DSA, depending on the value of Bit 28 (DSA Relative).

A maximum of 4 bytes may be moved with these instructions. The register address and memory address must have the same byte alignment, and the count set such that it does not cross Dword boundaries. The destination memory address in the Store instruction and the source address in the Load instruction may not map back to the

operating register set of the chip. If it does, a PCI illegal read/write cycle will occur, and the chip will issue an interrupt (Illegal Instruction Detected) immediately following.

Bits A1, A0	Number of Bytes Allowed to Load/Store
00	One, two, three or four
01	One, two, or three
10	One or two
11	One

The SIOM and DIOM bits in the [DMA Mode \(DMODE\)](#) register determine whether the destination or source address of the instruction is in Memory space or I/O space. The Load/Store utilizes the PCI commands for I/O read and I/O write to access the I/O space.

6.8.1 First Dword

IT[2:0]	Instruction Type [31:29] These bits should be 111, indicating the Load and Store instruction.
DSA	DSA Relative 28 When this bit is clear, the value in the DMA SCRIPTS Pointer Save (DSPS) is the actual 32-bit memory address to perform the load/store to/from. When this bit is set, the chip determines the memory address to perform the load/store to/from by adding the 24-bit signed offset value in the DMA SCRIPTS Pointer Save (DSPS) to the Data Structure Address (DSA) .
R	Reserved [27:26]
NF	No Flush (Store instruction only) 25 When this bit is set, the LSI53C860 performs a Store without flushing the prefetch unit. When this bit is clear, the Store instruction automatically flushes the prefetch unit. No Flush should be used if the source and destination are not within four instructions of the current Store instruction.

Note: This bit has no effect unless the Prefetch Enable bit in the [DMA Control \(DCNTL\)](#) register is set. For information on SCRIPTS instruction prefetching, see [Chapter 2, “Functional Description.”](#)

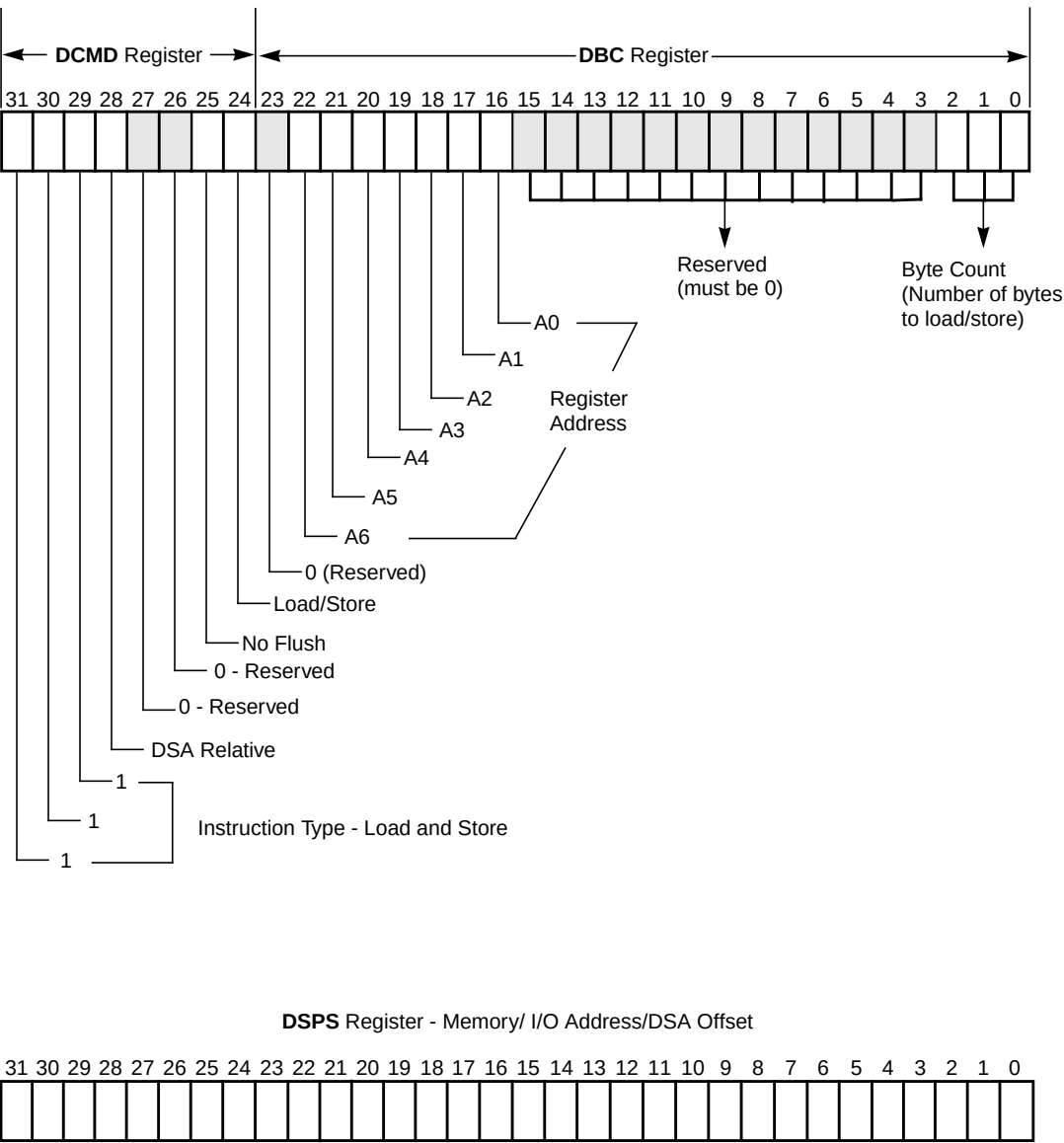
LS	Load and Store	24
	When this bit is set, the instruction is a Load. When cleared, it is a Store.	
R	Reserved	23
RA[6:0]	Register Address	[22:16]
	A[6:0] select the register to load/store to/from within the LSI53C860.	
 <u>Note:</u> It is not possible to load the SCSI First Byte Received (SFBR) register, although the SFBR contents may be stored in another location.		
R	Reserved	[15:3]
BC	Byte Count	[2:0]
	This value is the number of bytes to load/store.	

6.8.2 Second Dword

Memory/IO Address / DSA Offset	[31:0]
This is the actual memory location of where to load or store, or the offset from the Data Structure Address (DSA) register value.	

[Figure 6.7](#) illustrates the register bit values that represent a Load and Store instruction.

Figure 6.7 Load and Store Instruction Format



Chapter 7

Electrical

Characteristics

This chapter specifies the LSI53C860 electrical and mechanical characteristics. It is divided into the following sections:

- [Section 7.1, “DC Characteristics”](#)
 - [Section 7.2, “TolerANT Technology”](#)
 - [Section 7.3, “AC Characteristics”](#)
 - [Section 7.4, “PCI Interface Timing Diagrams”](#)
 - [Section 7.4.1, “Target Timing”](#)
 - [Section 7.5, “PCI Interface Timing”](#)
 - [Section 7.6, “SCSI Timing”](#)
 - [Section 7.7, “Package Drawings”](#)
-

7.1 DC Characteristics

This section of the manual describes the LSI53C860 DC characteristics. [Table 7.1](#) through [Table 7.11](#) give the current and voltage specifications.

Table 7.1 Absolute Maximum Stress Ratings

Symbol	Parameter	Min	Max	Unit	Test Conditions
T_{STG}	Storage temperature	–55	150	°C	–
V_{DD}	Supply voltage	–0.5	7.0	V	–
V_{IN}	Input voltage	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V	–
I_{LP}^1	Latch-up current	±150	–	mA	–
ESD ²	Electrostatic discharge	–	2 K	V	MIL-STD 883C, Method 3015.7

1. $-2\text{ V} < V_{PIN} < 8\text{ V}$.

2. SCSI pins only.

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the [Operating Conditions](#) section of the manual is not implied.

Table 7.2 Operating Conditions

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{DD}	Supply voltage	4.75	5.25	V	–
I_{DD}^1	Supply current (dynamic)	–	130	mA	–
	Supply current (static)	–	1	mA	–
T_A	Operating free air	0	70	°C	–
θ_{JA}	Thermal resistance (junction to ambient air)	–	67	°C/W	–

1. Average operating supply current is 50 mA.

Note: Conditions that exceed the operating limits may cause the device to function incorrectly.

Table 7.3 SCSI Signals—SD[7:0]/, SDP/, SREQ/, SACK/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	$V_{DD} + 0.5$	V	—
V_{IL}	Input low voltage	$V_{SS} - 0.5$	0.8	V	—
V_{OH}^1	Output high voltage	2.5	3.5	V	2.5 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	48 mA
I_{IN}	Input leakage	–10	10	μA	—
I_{OZ}	3-state leakage	–10	10	μA	—

1. TolerANT active negation enabled.

Table 7.4 SCSI Signals—SMSG, SI_O/, SC_D/, SATN/, SBSY/, SSEL/, SRST/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	$V_{DD} + 0.5$	V	—
V_{IL}	Input low voltage	$V_{SS} - 0.5$	0.8	V	—
V_{OL}	Output low voltage	V_{SS}	0.5	V	48 mA
I_{IN}	Input leakage (SRST/ only)	–10 –500	10 –50	μA μA	—
I_{OZ}	3-state leakage	–10	10	μA	—

Table 7.5 Input Signals—CLK, SCLK, GNT/, IDSEL, RST/, TESTIN

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	$V_{DD} + 0.5$	V	—
V_{IL}	Input low voltage	$V_{SS} - 0.5$	0.8	V	—
I_{IN}	Input leakage	–1.0	1.0	μA	—

Note: CLK, SCLK, GNT/ and IDSEL have 100 μA pull-ups that are enabled when TESTIN is low.
TESTIN has a 100 μA pull-up that is always enabled.

Table 7.6 Capacitance

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input capacitance of input pads	–	7	pF	–
C_{IO}	Input capacitance of I/O pads	–	10	pF	–

Table 7.7 Output Signals—MAC/_TESTOUT, REQ/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	–16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OH}	Output high current	–8	–	mA	V_{DD} –0.5 V
I_{OL}	Output low current	16	–	mA	0.4 V
I_{OZ}	3-state leakage	–10	10	μ A	–

Note: REQ/ has a 100 μ A pull-up that is enabled when TESTIN is low.

Table 7.8 Output Signal—IRQ/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	–8 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	8 mA
I_{OH}	Output high current	–4	–	mA	V_{DD} –0.5 V
I_{OL}	Output low current	8	–	mA	0.4 V
I_{OZ}	3-state leakage	–10	10	μ A	–

Note: IRQ/ has a 100 μ A pull-up that is enabled when TESTIN is low. IRQ/ can be enabled with a register as an open drain with an internal 100 μ A pull-up.

Table 7.9 Output Signal—SERR/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OL}	Output low current	16	–	mA	0.4 V
I_{OZ}	3-state leakage	–10	10	μ A	–

Table 7.10 Bidirectional Signals—AD[31:0], C_BE/[3:0], FRAME/, IRDY/, TRDY/, DEVSEL/, STOP/, PERR/, PAR/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	$V_{DD} + 0.5$	V	–
V_{IL}	Input low voltage	$V_{SS} - 0.5$	0.8	V	–
V_{OH}	Output high voltage	2.4	V_{DD}	V	16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OH}	Output high current	–8	–	mA	$V_{DD} - 0.5$
I_{OL}	Output low current	16	–	mA	0.4 V
I_{IN}	Input leakage	–10	10	μ A	$V_{SS} < V_{IN} < V_{DD}$
I_{OZ}	3-state leakage	–10	10	μ A	–

Note: All the signals in this table have 100 μ A pull-ups that are enabled when TESTIN is low.

Table 7.11 Bidirectional Signals—GPIO0_FETCH/, GPIO1_MASTER/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	$V_{DD} + 0.5$	V	–
V_{IL}	Input low voltage	$V_{SS} - 0.5$	0.8	V	–
V_{OH}	Output high voltage	2.4	V_{DD}	V	–16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OH}	Output high current	–8	–	mA	2.4 V
I_{OL}	Output low current	16	–	mA	0.4 V
I_{IN}	Input leakage	–10	10	μ A	–
I_{OZ}	3-state leakage	–10	10	μ A	–

Note: All the signals in this table have 100 μ A pull-ups that are enabled when TESTIN is low.

7.2 TolerANT Technology

The LSI53C860 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation actively drives the SCSI Request, Acknowledge, Data, and Parity signals HIGH rather than allowing them to be passively pulled up by terminators. [Table 7.12](#) provides electrical characteristics for SE SCSI signals. [Figure 7.1](#) through [Figure 7.5](#) show the effect of TolerANT technology on the DC characteristics of the chip.

Table 7.12 TolerANT Technology Electrical Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}^1	Output high voltage	2.5	3.5	V	$I_{OH} = 2.5 \text{ mA}$
V_{OL}	Output low voltage	0.1	0.5	V	$I_{OL} = 48 \text{ mA}$
V_{IH}	Input high voltage	2.0	7.0	V	–
V_{IL}	Input low voltage	–0.5	0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	–0.66	–0.77	V	$V_{DD} = 4.75$; $I_I = -20 \text{ mA}$
V_{TH}	Threshold, HIGH to LOW	1.1	1.3	V	–
V_{TL}	Threshold, LOW to HIGH	1.5	1.7	V	–
$V_{TH}-V_{TL}$	Hysteresis	200	400	mV	–
I_{OH}^1	Output high current	2.5	24	mA	$V_{OH} = 2.5 \text{ V}$
I_{OL}	Output low current	100	200	mA	$V_{OL} = 0.5 \text{ V}$
I_{OSH}^1	Short-circuit output high current	–	625	mA	Output driving low, pin shorted to V_{DD} supply ²
I_{OSL}	Short-circuit output low current	–	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	–	10	μA	$-0.5 < V_{DD} < 5.25$ $V_{PIN} = 2.7 \text{ V}$
I_{LL}	Input low leakage	–	–10	μA	$-0.5 < V_{DD} < 5.25$ $V_{PIN} = 0.5 \text{ V}$
R_I	Input resistance	20	–	$\text{M}\Omega$	SCSI pins ³
C_P	Capacitance per pin	–	10	pF	PQFP
t_R^1	Rise time, 10% to 90%	9.7	18.5	ns	Figure 7.1
t_F	Fall time, 90% to 10%	5.2	14.7	ns	Figure 7.1
dV_H/dt	Slew rate, LOW to HIGH	0.15	0.49	V/ns	Figure 7.1
dV_L/dt	Slew rate, HIGH to LOW	0.19	0.52	V/ns	Figure 7.1
ESD	Electrostatic discharge	2	–	kV	MIL-STD-883C; 3015-7
	Latch-up	100	–	mA	–
	Filter delay	20	30	ns	Figure 7.2
	Extended filter delay	40	60	ns	Figure 7.2

1. Active negation outputs only: Data, Parity, SREQ/, SACK/.

2. Single pin only; irreversible damage may occur if sustained for one second.

3. SCSI RESET pin has 10 k Ω pull-up resistor.

Note: These values are guaranteed by periodic characterization; they are not 100% tested on every device.

Figure 7.1 Rise and Fall Time Test Conditions

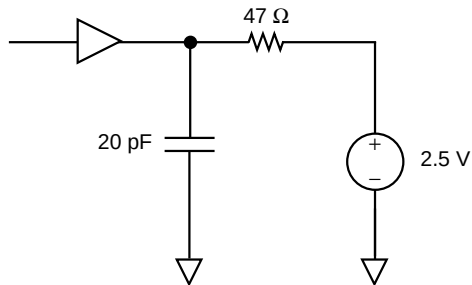
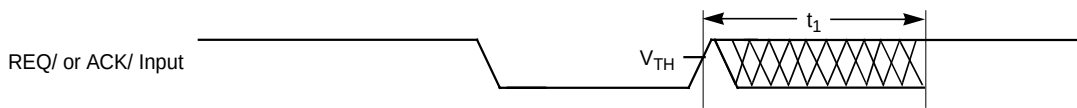


Figure 7.2 SCSI Input Filtering



Note: t_1 is the input filtering period.

Figure 7.3 Hysteresis of SCSI Receiver

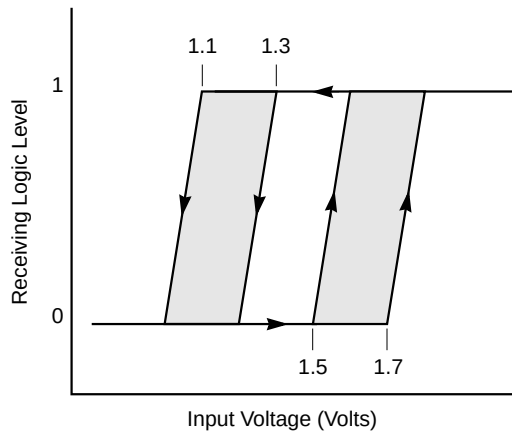


Figure 7.4 Input Current as a Function of Input Voltage

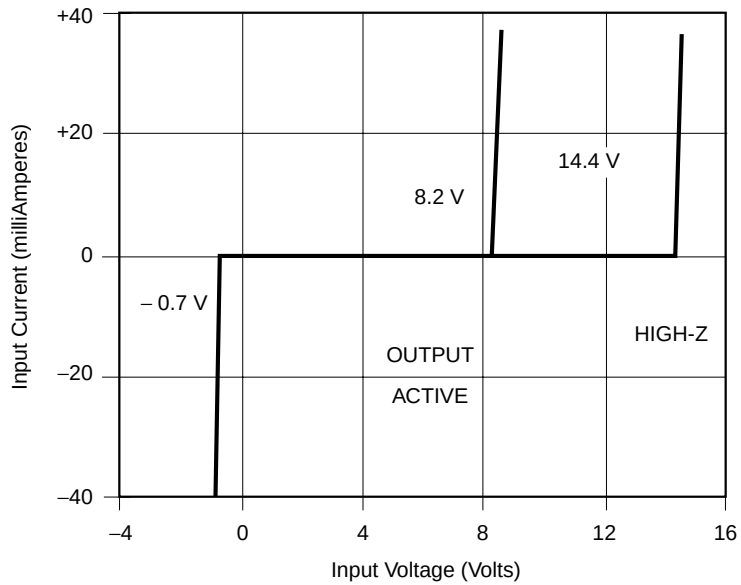
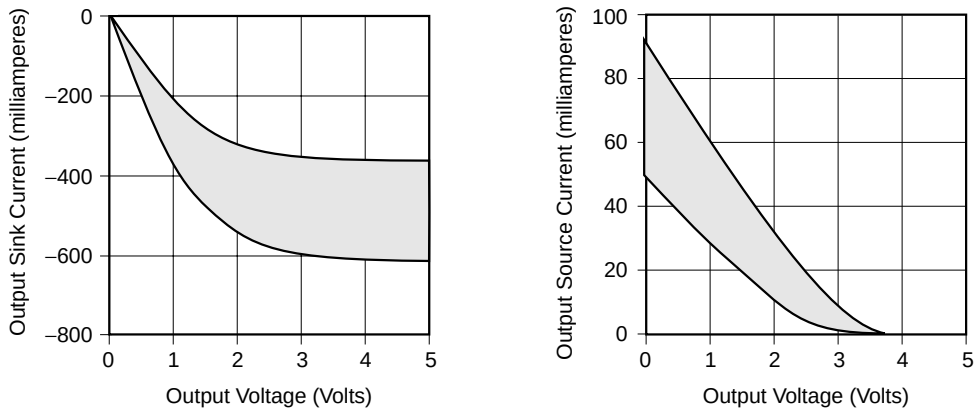


Figure 7.5 Output Current as a Function of Output Voltage



7.3 AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to [Section 7.1, “DC Characteristics”](#)), Chip timings are based on simulation at worst case voltage, temperature, and processing. Timings were developed with a load capacitance of 50 pF. [Table 7.13](#) and [Figure 7.6](#) provide clock timing data.

Table 7.13 Clock Timing

Symbol	Parameter	Min	Max	Unit
t_1	Bus clock cycle time	30	DC	ns
	SCSI clock cycle time (SCLK) ¹	12.5	60	ns
t_2	CLK LOW time ²	12	—	ns
	SCLK LOW time ²	5	33	ns
t_3	CLK HIGH time ²	12	—	ns
	SCLK HIGH time ²	5	33	ns
t_4	CLK slew rate	1	—	V/ns
	SCLK slew rate	1	—	V/ns

1. This parameter must be met to ensure SCSI timings are within specification.
2. Duty cycle not to exceed 60/40.

Figure 7.6 Clock Timing Waveform

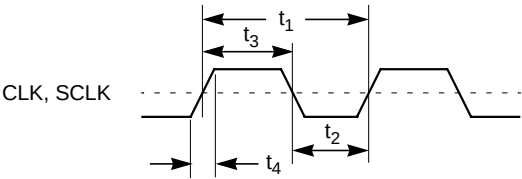
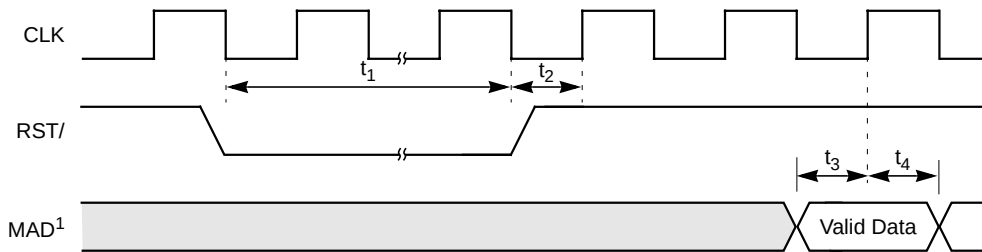


Table 7.14 and Figure 7.7 provide Reset Input timing data.

Table 7.14 Reset Input

Symbol	Parameter	Min	Max	Unit
t_1	Reset pulse width	10	–	t_{CLK}
t_2	Reset deasserted setup to CLK HIGH	0	–	ns

Figure 7.7 Reset Input Waveforms



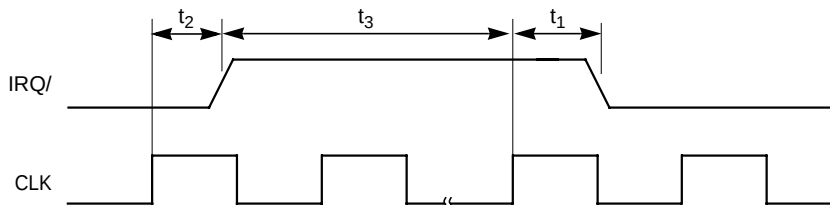
1. When enabled.

Table 7.15 and Figure 7.8 provide Interrupt Output timing data.

Table 7.15 Interrupt Output

Symbol	Parameter	Min	Max	Unit
t_1	CLK HIGH to IRQ/ LOW	–	20	ns
t_2	CLK HIGH to IRQ/ HIGH	–	40	ns
t_3	IRQ/ deassertion time	3	–	CLK

Figure 7.8 Interrupt Output Waveforms



7.4 PCI Interface Timing Diagrams

[Figure 7.9](#) through [Figure 7.18](#) represent signal activity when the LSI53C860 accesses the PCI bus. The timings for the PCI bus interface are listed on [page 7-25](#). The following timing diagrams are included in this section:

Target Timing

- PCI Configuration Register Read
- PCI Configuration Register Write
- Target Read
- Target Write

Initiator Timing

- OpCode Fetch, Nonburst
- Burst OpCode Fetch
- Back-to-Back Read
- Back-to-Back Write
- Burst Read
- Burst Write

7.4.1 Target Timing

Figure 7.9 through Figure 7.12 describe Target timing.

Figure 7.9 PCI Configuration Register Read

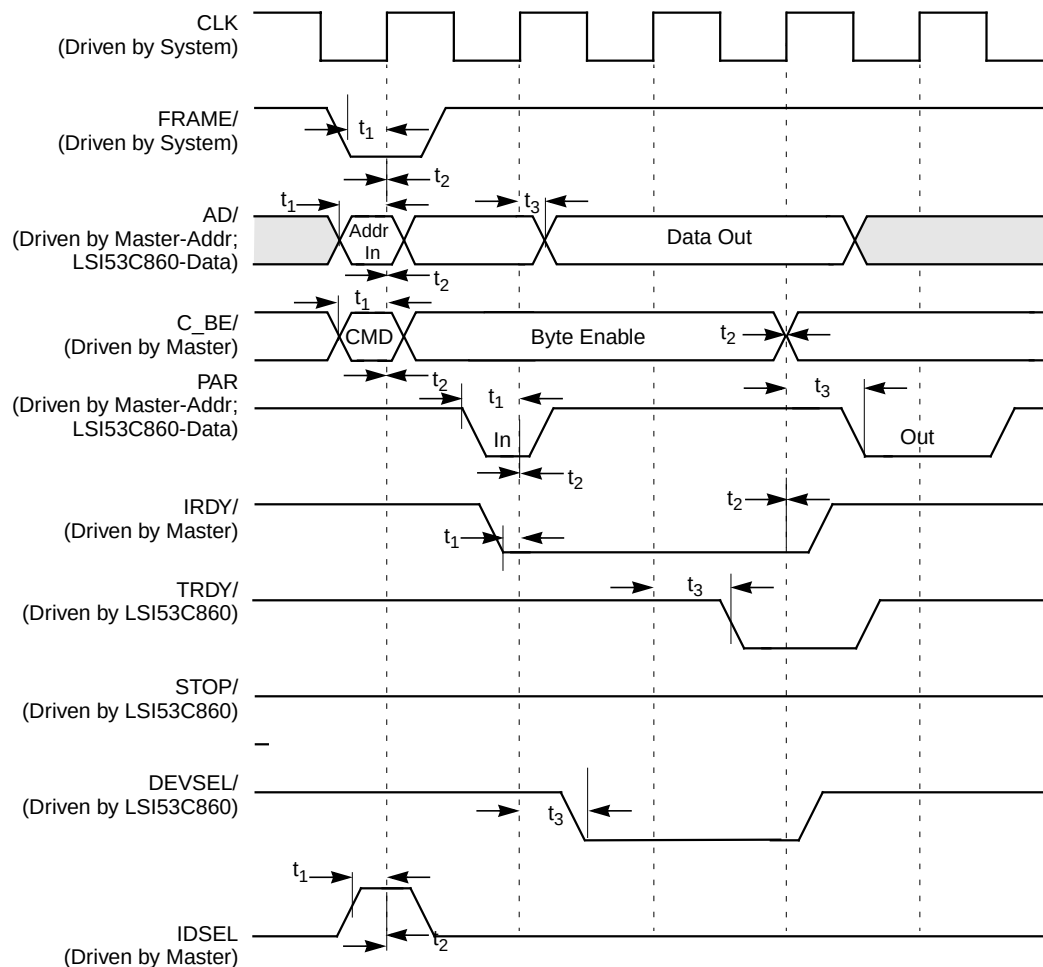


Figure 7.10 PCI Configuration Register Write

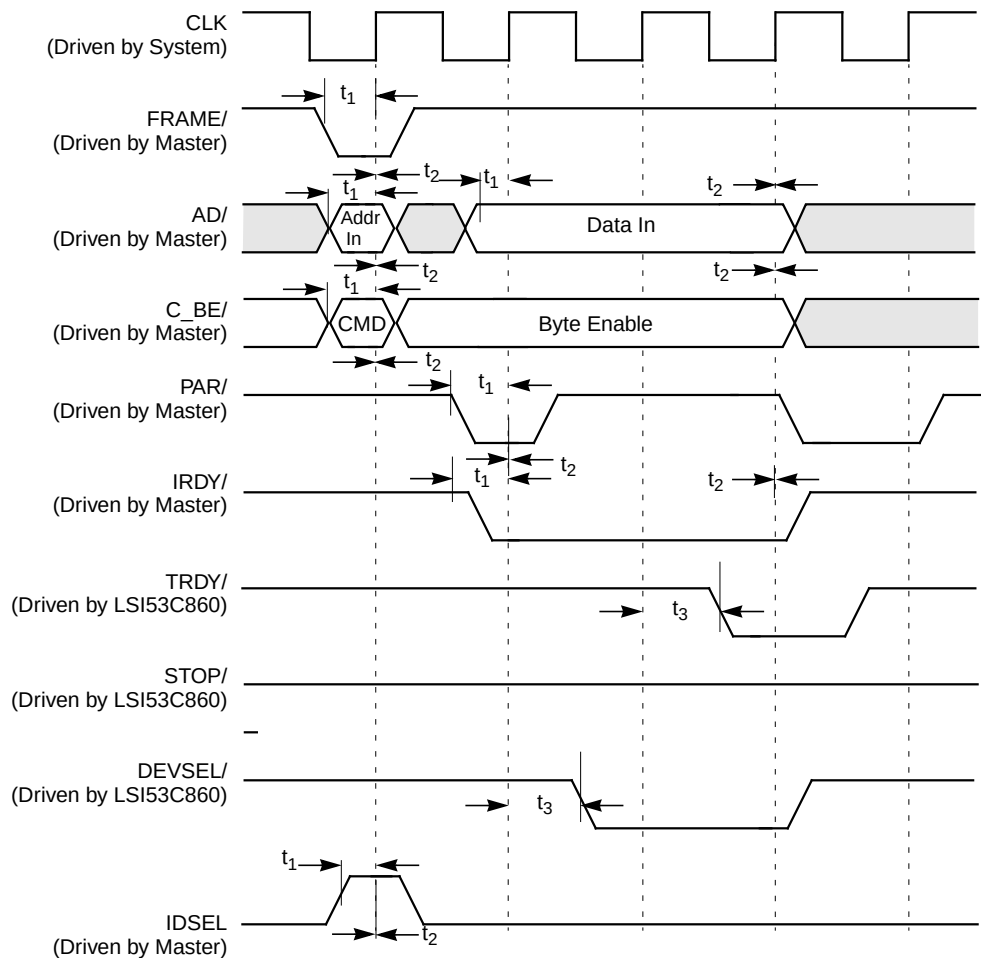


Figure 7.11 Target Read

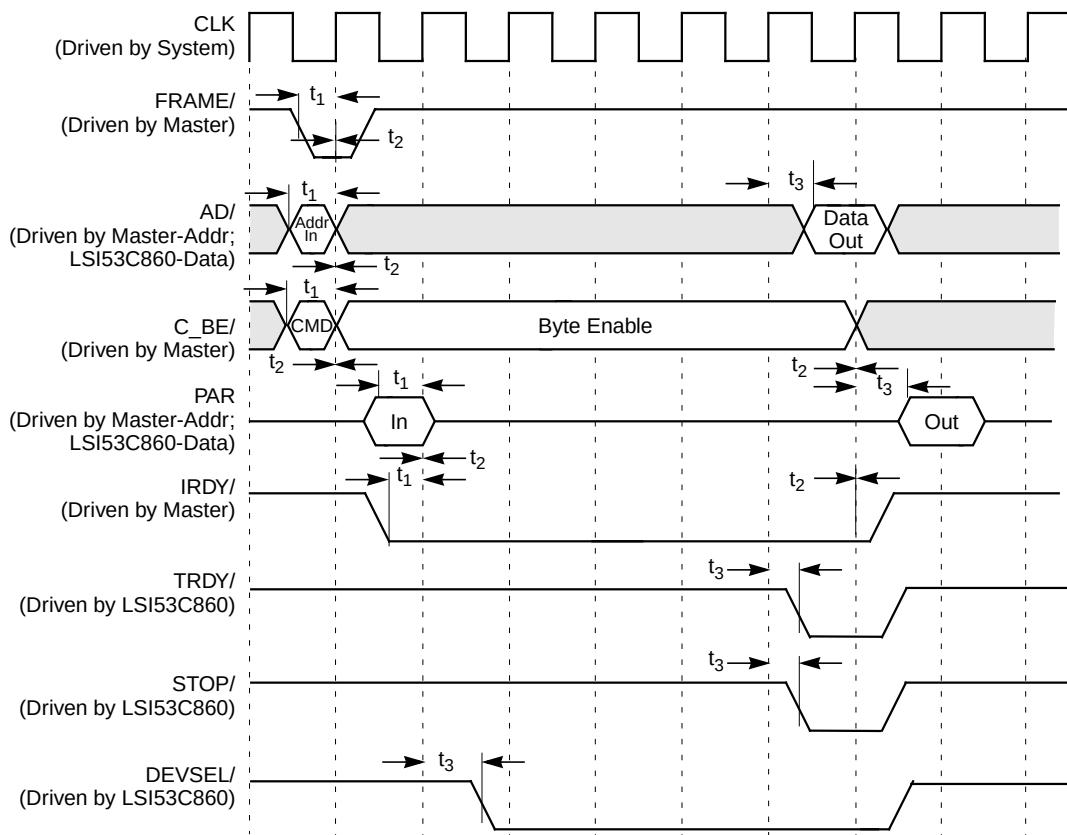
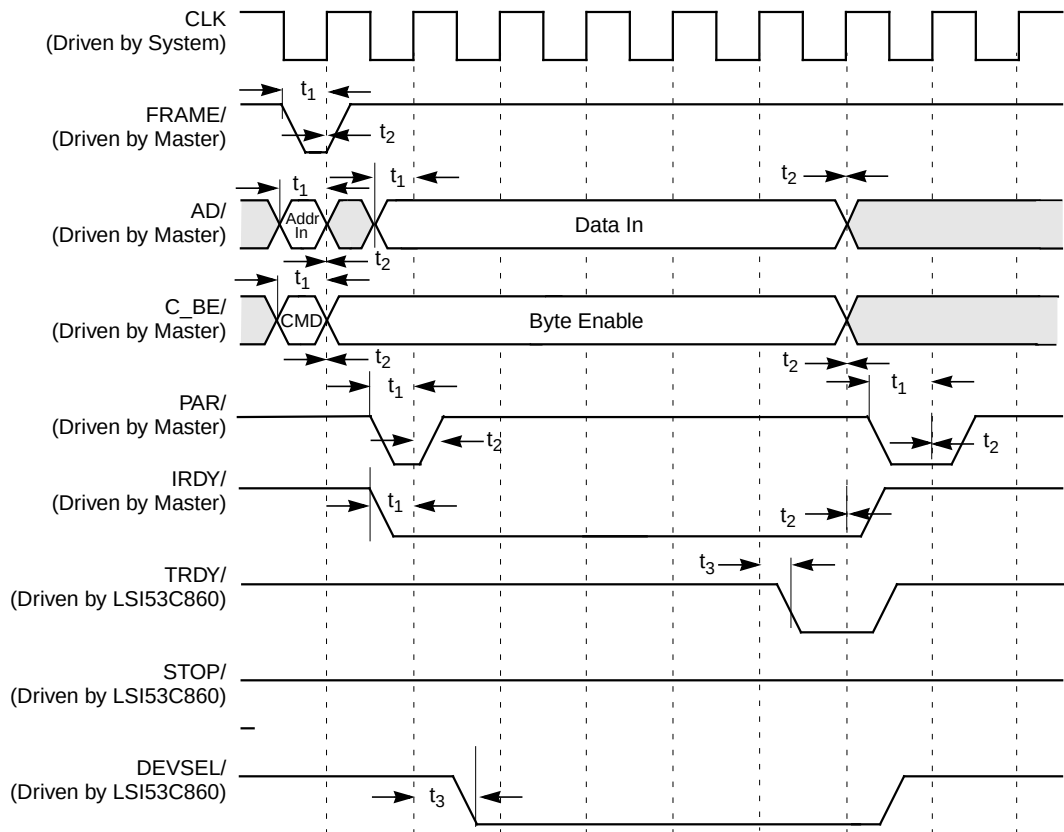


Figure 7.12 Target Write



7.4.2 Initiator Timing

Figure 7.13 through Figure 7.18 describe Initiator timing.

Figure 7.13 OpCode Fetch, Nonburst

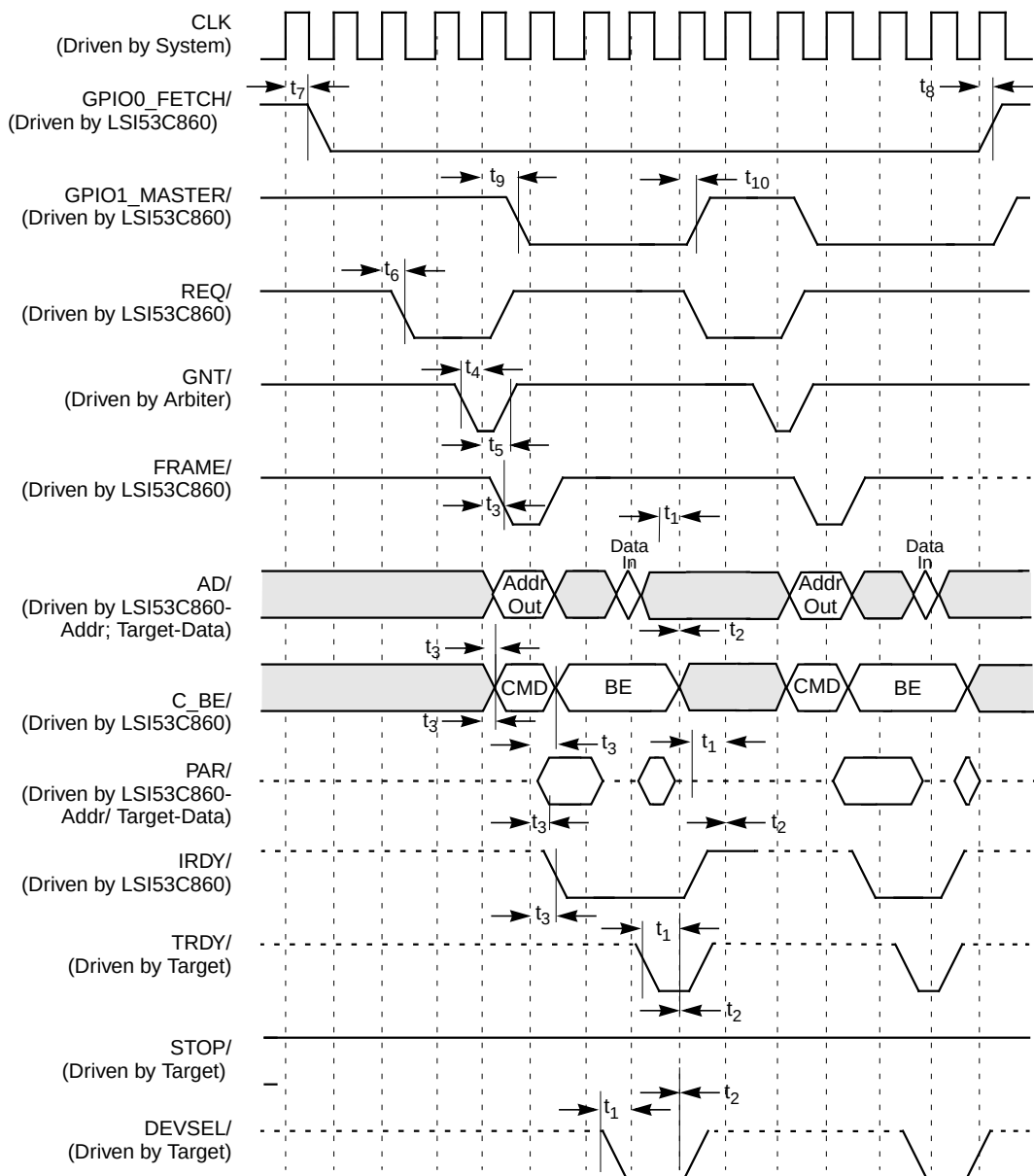


Figure 7.14 Burst OpCode Fetch

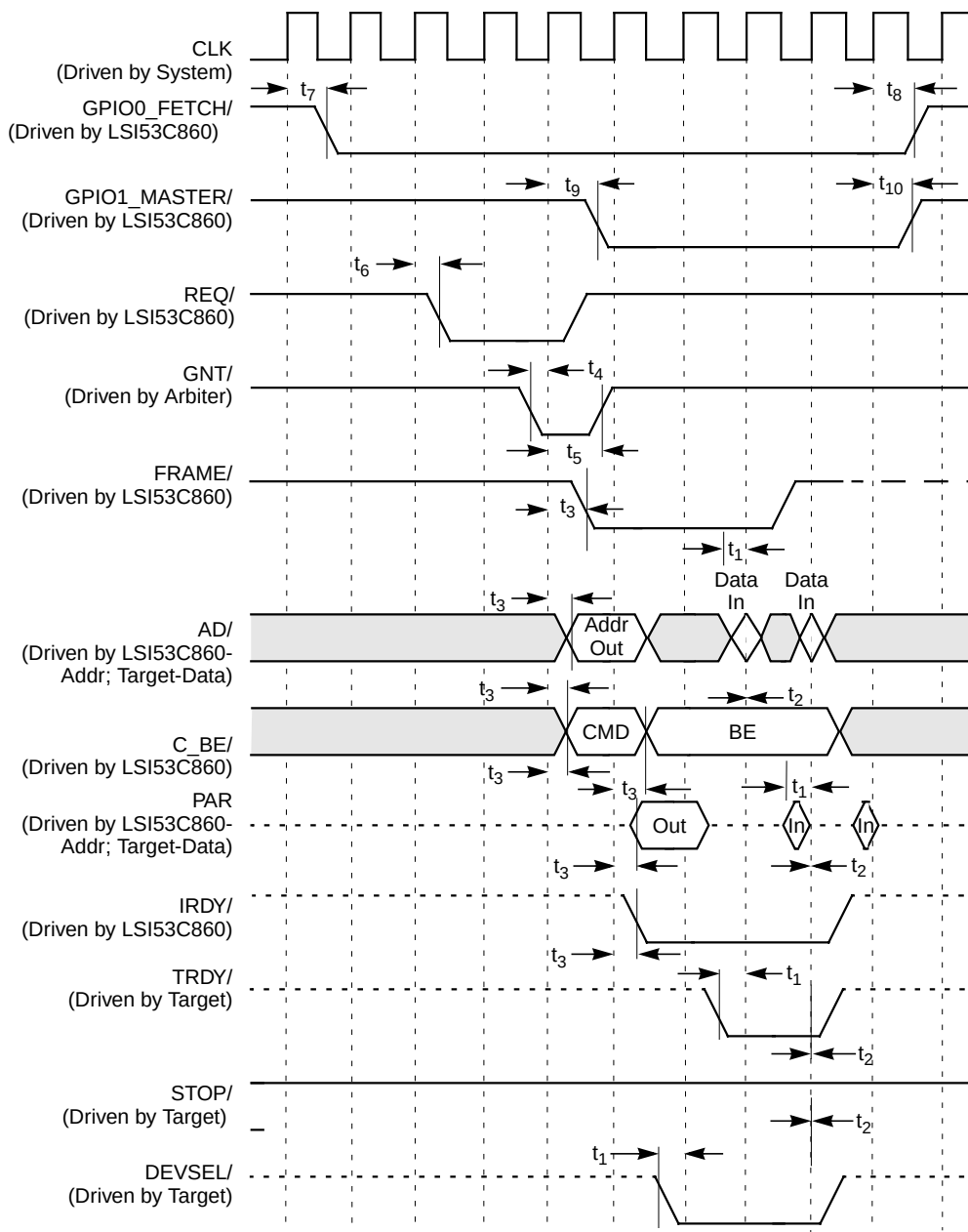


Figure 7.15 Back-to-Back Read

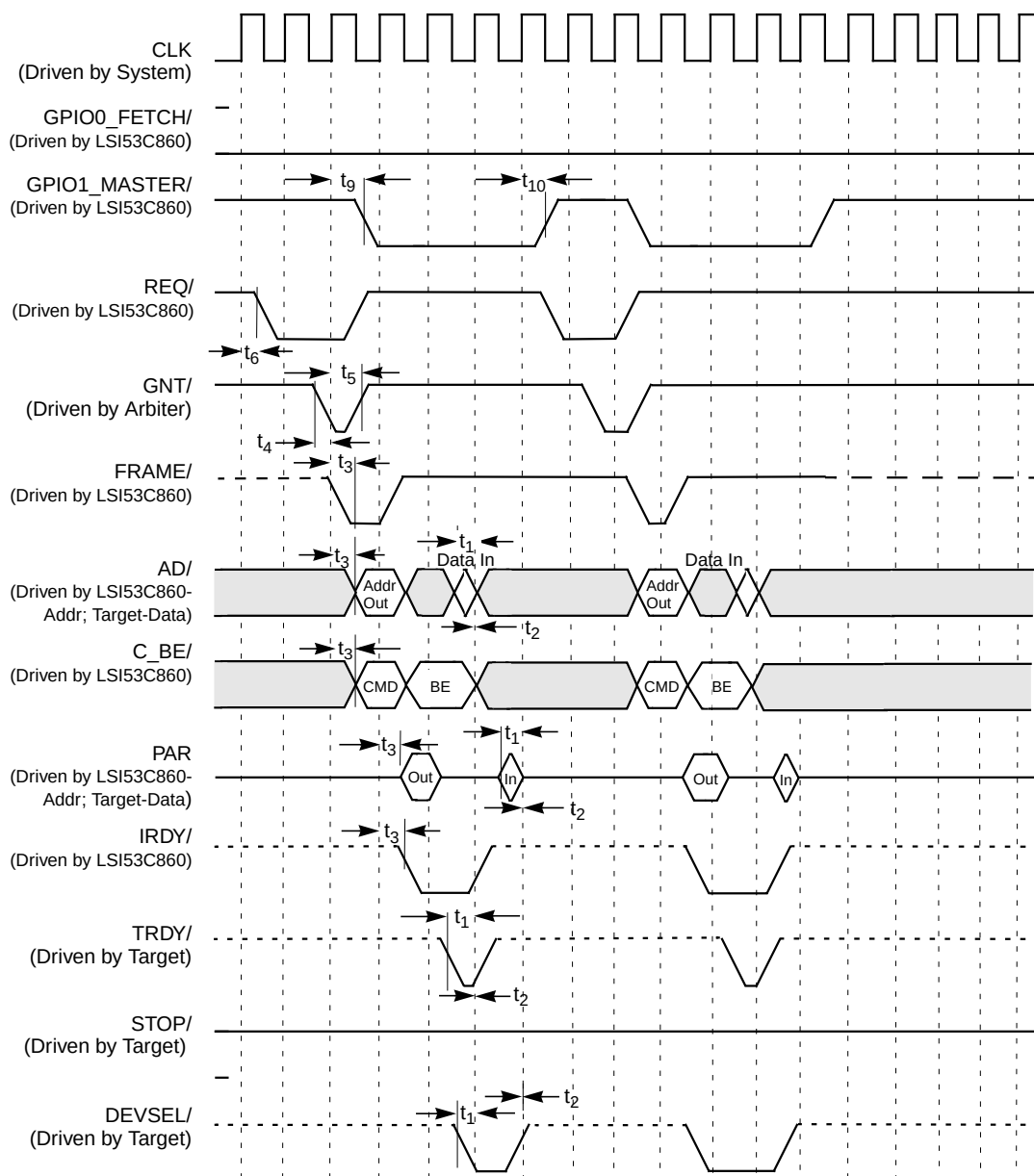


Figure 7.16 Back-to-Back Write

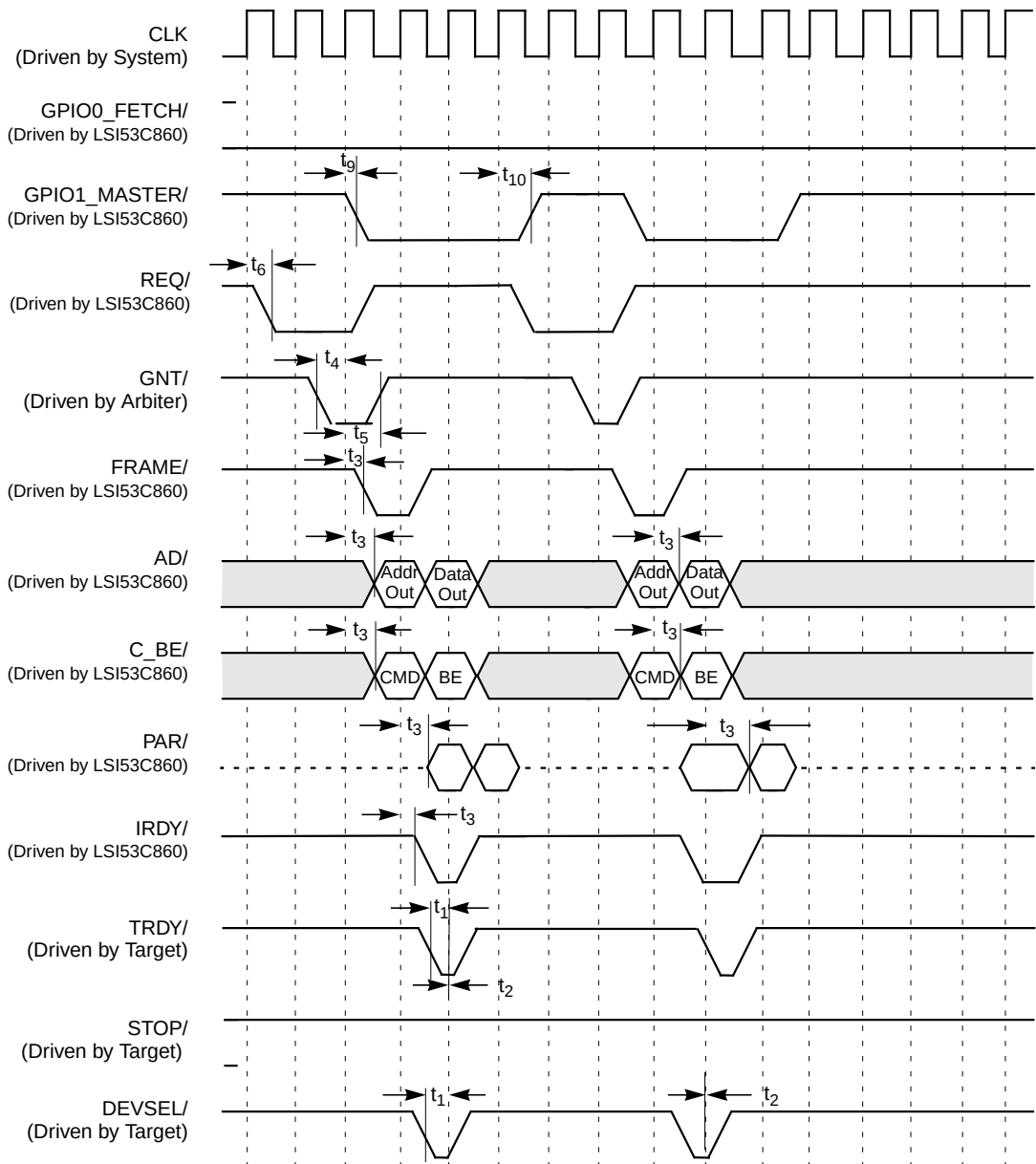


Figure 7.17 Burst Read

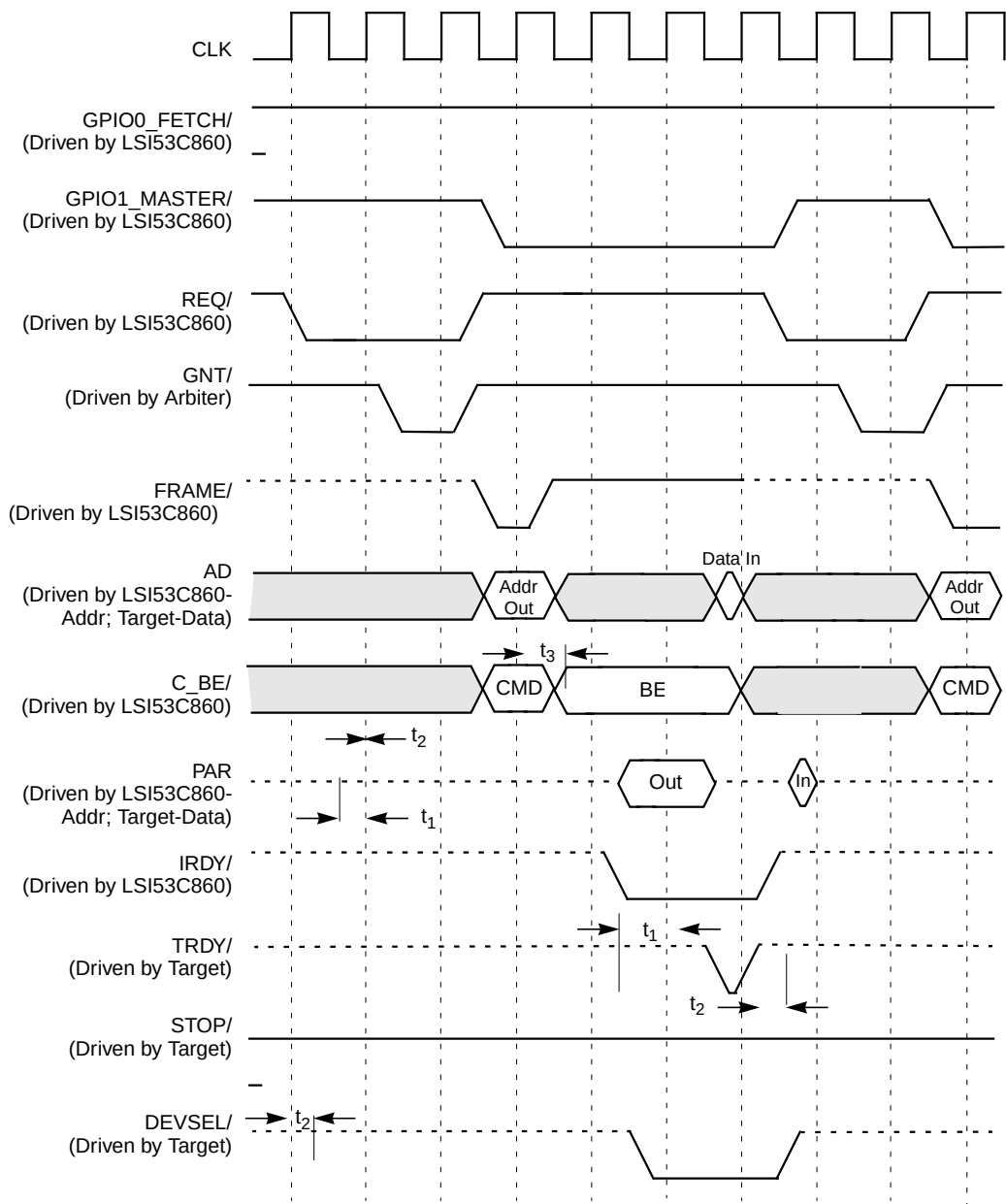


Figure 7.17 Burst Read (Cont.)

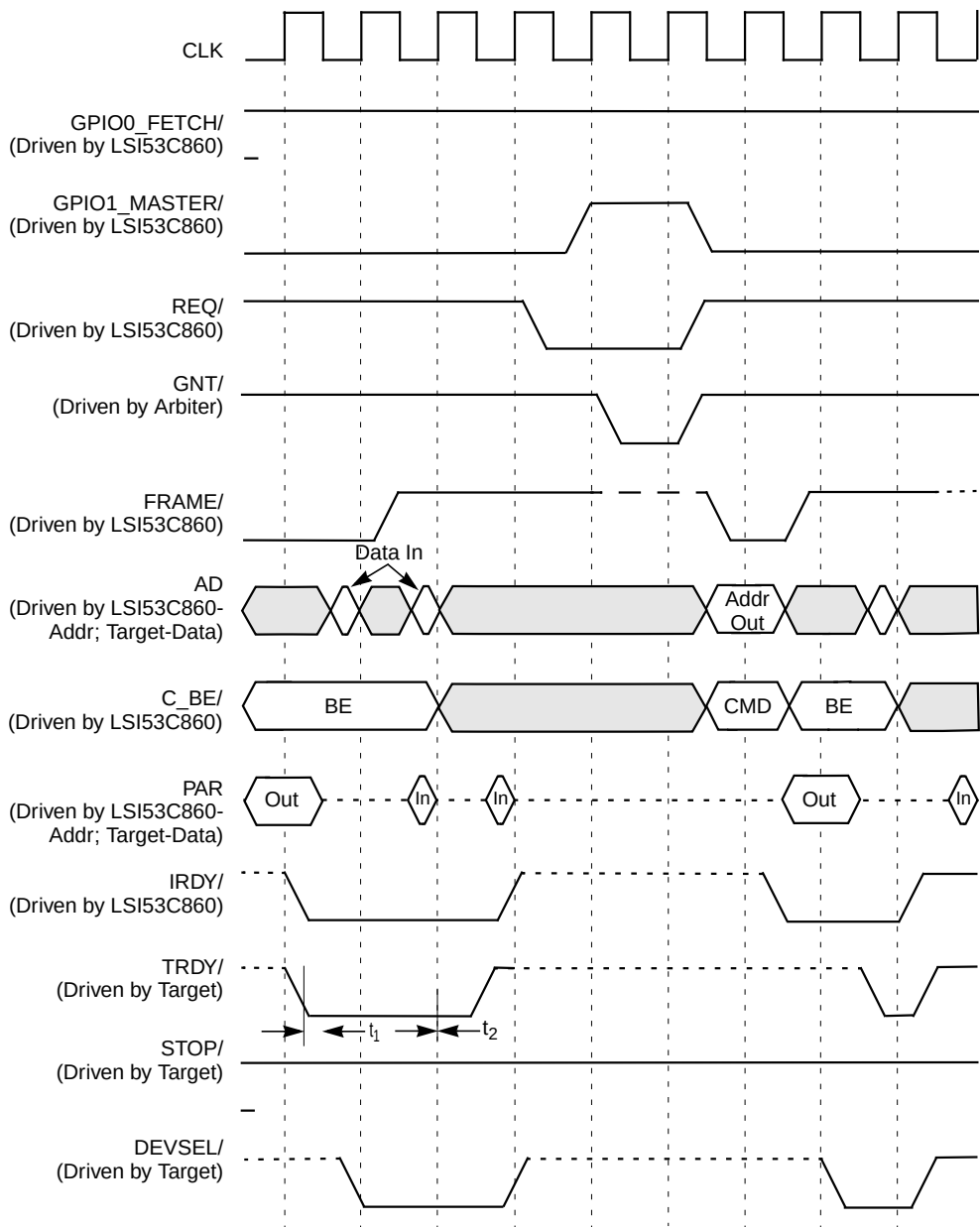


Figure 7.18 Burst Write

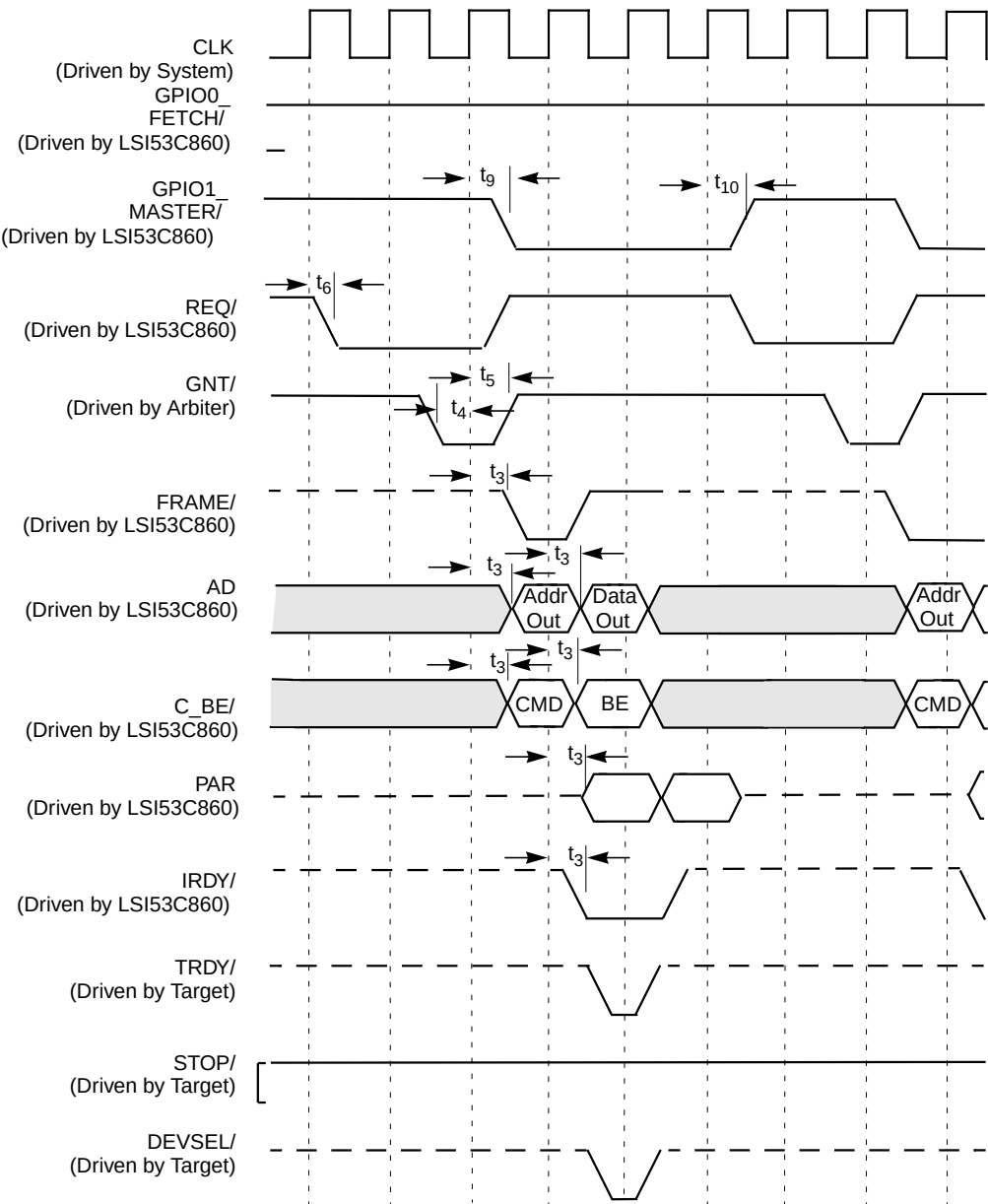
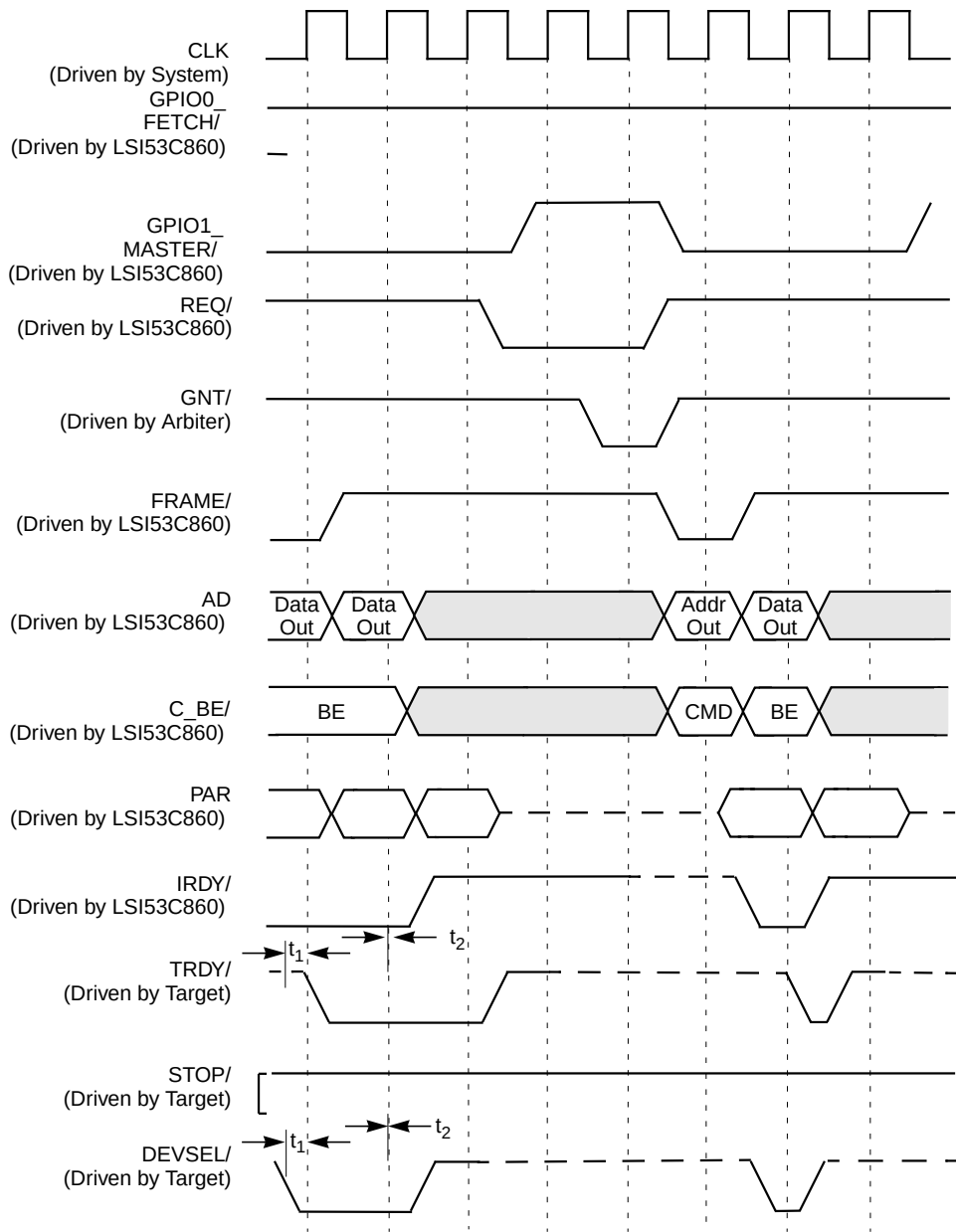


Figure 7.18 Burst Write (Cont.)



7.5 PCI Interface Timing

Table 7.16 describes the PCI timing data for the LSI53C860.

Table 7.16 PCI Timing

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	—	ns
t_2	Shared signal input hold time	0	—	ns
t_3	CLK to shared signal output valid	—	11	ns
t_4	Side signal input setup time	10	—	ns
t_5	Side signal input hold time	0	—	ns
t_6	CLK to side signal output valid	—	12	ns
t_7	CLK high to FETCH/ low	—	20	ns
t_8	CLK high to FETCH/ high	—	20	ns
t_9	CLK high to MASTER/ low	—	20	ns
t_{10}	CLK high to MASTER/ high	—	20	ns

7.6 SCSI Timing

Tables 7.17 through 7.23 and Figures 7.19 through 7.23 describe the LSI53C860 SCSI timing data.

Table 7.17 Initiator Asynchronous Send (5 Mbytes/s)

Symbol	Parameter	Min	Max	Unit
t_1	SACK/ asserted from SREQ/ asserted	10	—	ns
t_2	SACK/ deasserted from SREQ/ deasserted	10	—	ns
t_3	Data setup to SACK/ asserted	55	—	ns
t_4	Data hold from SREQ/ deasserted	20	—	ns

Figure 7.19 Initiator Asynchronous Send

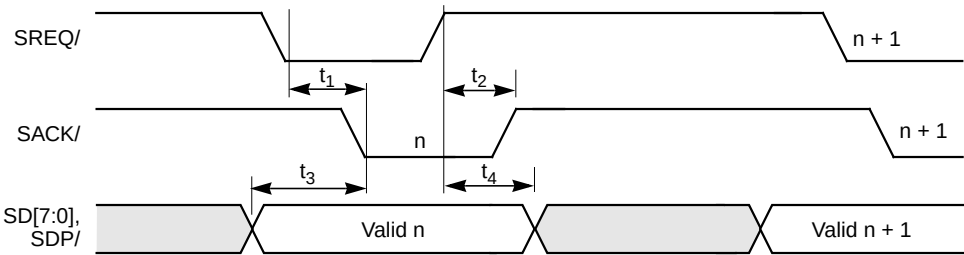
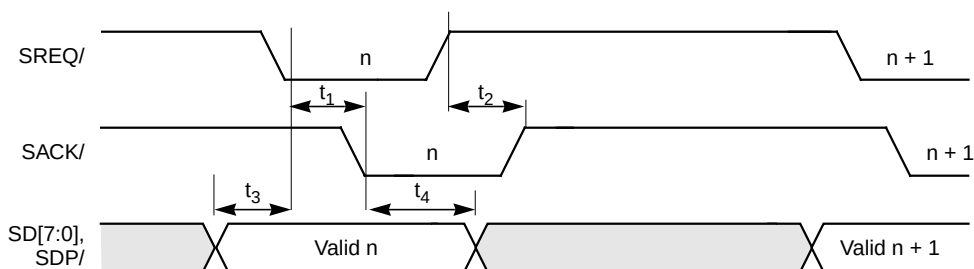


Table 7.18 Initiator Asynchronous Receive (5 Mbytes/s)

Symbol	Parameter	Min	Max	Unit
t_1	SACK/ asserted from SREQ/ asserted	10	–	ns
t_2	SACK/ deasserted from SREQ/ deasserted	10	–	ns
t_3	Data setup to SREQ/ asserted	0	–	ns
t_4	Data hold from SACK/ asserted	0	–	ns

Figure 7.20 Initiator Asynchronous Receive**Table 7.19 Target Asynchronous Send (5 Mbytes/s)**

Symbol	Parameter	Min	Max	Unit
t_1	SACK/ asserted from SREQ/ asserted	10	–	ns
t_2	SACK/ deasserted from SREQ/ deasserted	10	–	ns
t_3	Data setup to SREQ/ asserted	55	–	ns
t_4	Data hold from SACK/ asserted	20	–	ns

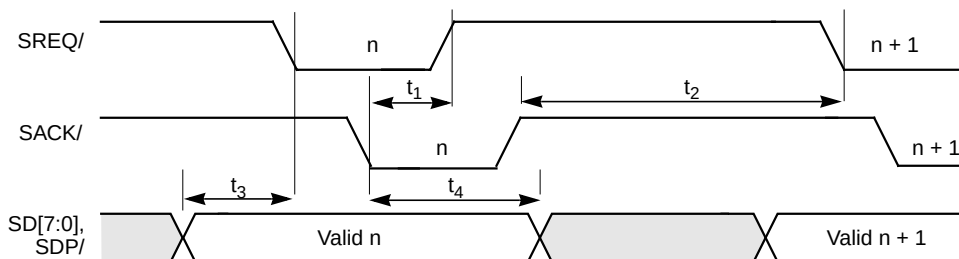
Figure 7.21 Target Asynchronous Send

Table 7.20 Target Asynchronous Receive (5 Mbytes/s)

Symbol	Parameter	Min	Max	Unit
t_1	SREQ/ deasserted from SACK/ asserted	10	–	ns
t_2	SREQ/ asserted from SACK/ deasserted	10	–	ns
t_3	Data setup to SREQ/ asserted	0	–	ns
t_4	Data hold from SACK/ asserted	0	–	ns

Figure 7.22 Target Asynchronous Receive

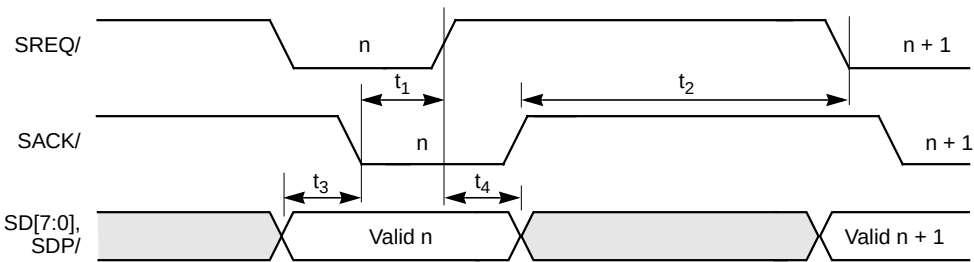


Figure 7.23 Initiator and Target Synchronous Transfers

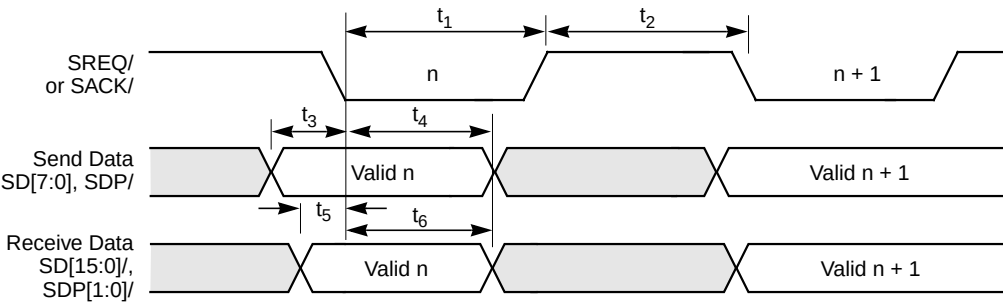


Table 7.21 SCSI-1 Transfers (SE, 5.0 Mbytes/s)

Symbol	Parameter	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	90	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	90	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	90	–	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	90	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	55	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	100	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	45	–	ns

Table 7.22 SCSI-2 Fast Transfers (10.0 Mbytes/s (8-Bit Transfers), 40 MHz Clock)

Symbol	Parameter	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	35	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	35	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	20	–	ns
t_2	Receive SREQ/ or SACK/deassertion pulse width	20	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	33	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	45	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	10	–	ns

Notes: Transfer period bits (bits [7:5] in the [SCSI Transfer \(SXFER\)](#) register) are set to zero and the Extra Clock cycle of Data Setup bit (bit 7 in [SCSI Control One \(SCNTL1\)](#)) is set. Analysis of system configuration is recommended due to reduced driver skew margin in differential systems. For Fast SCSI, set the TolerANT Enable bit (bit 7 in [SCSI Test Three \(STEST3\)](#)).

Table 7.23 Ultra SCSI Transfers (20.0 Mbytes/s (8-Bit Transfers), 80 MHz Clock)

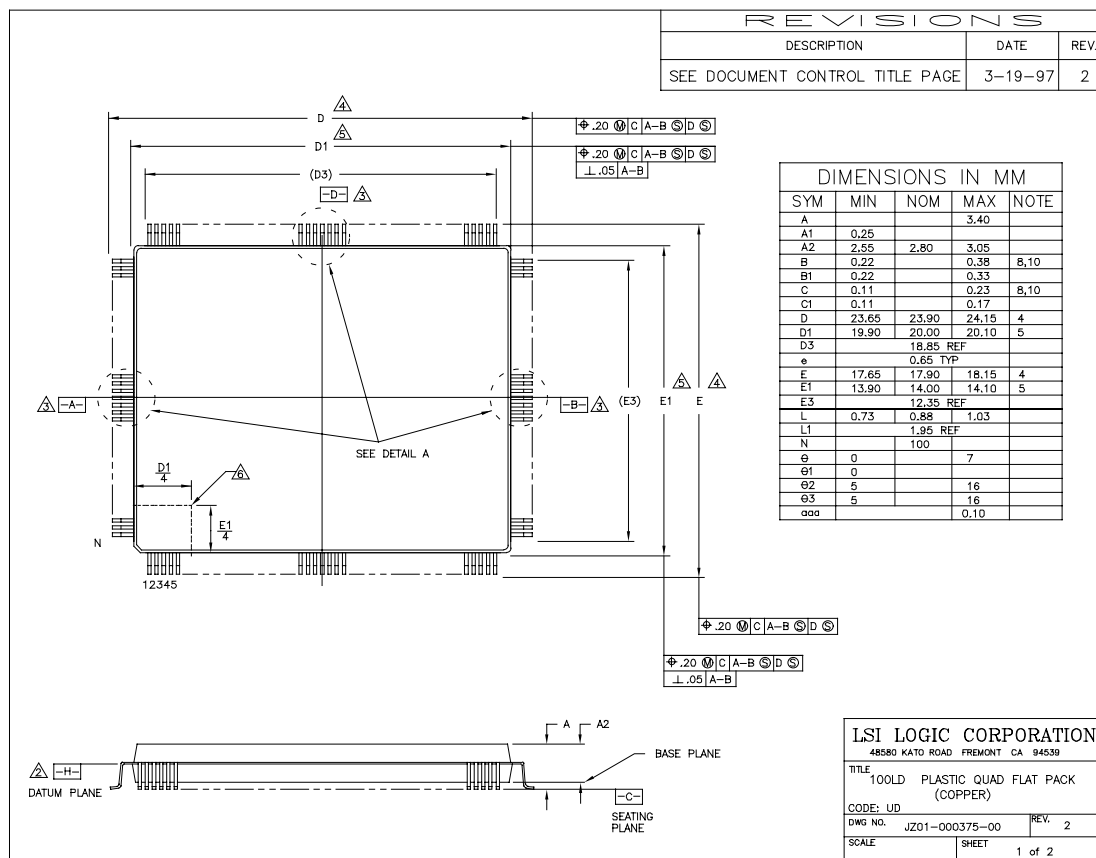
Symbol	Parameter	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	16	–	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	16	–	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	10	–	ns
t_2	Receive SREQ/ or SACK/deassertion pulse width	10	–	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	12	–	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	17	–	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	–	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	6	–	ns

Notes: Transfer period bits (bits [7:5] in the [SCSI Transfer \(SXFER\)](#) register) are set to zero and the Extra Clock cycle of Data Setup bit (bit 7 in [SCSI Control One \(SCNTL1\)](#)) is set. For fast SCSI, set the TolerANT Enable bit (bit 7 in [SCSI Test Three \(STEST3\)](#)). During Ultra SCSI transfers, the value of the Extend REQ/ ACK Filtering bit ([SCSI Test Two \(STEST2\)](#), bit 1) has no effect.

7.7 Package Drawings

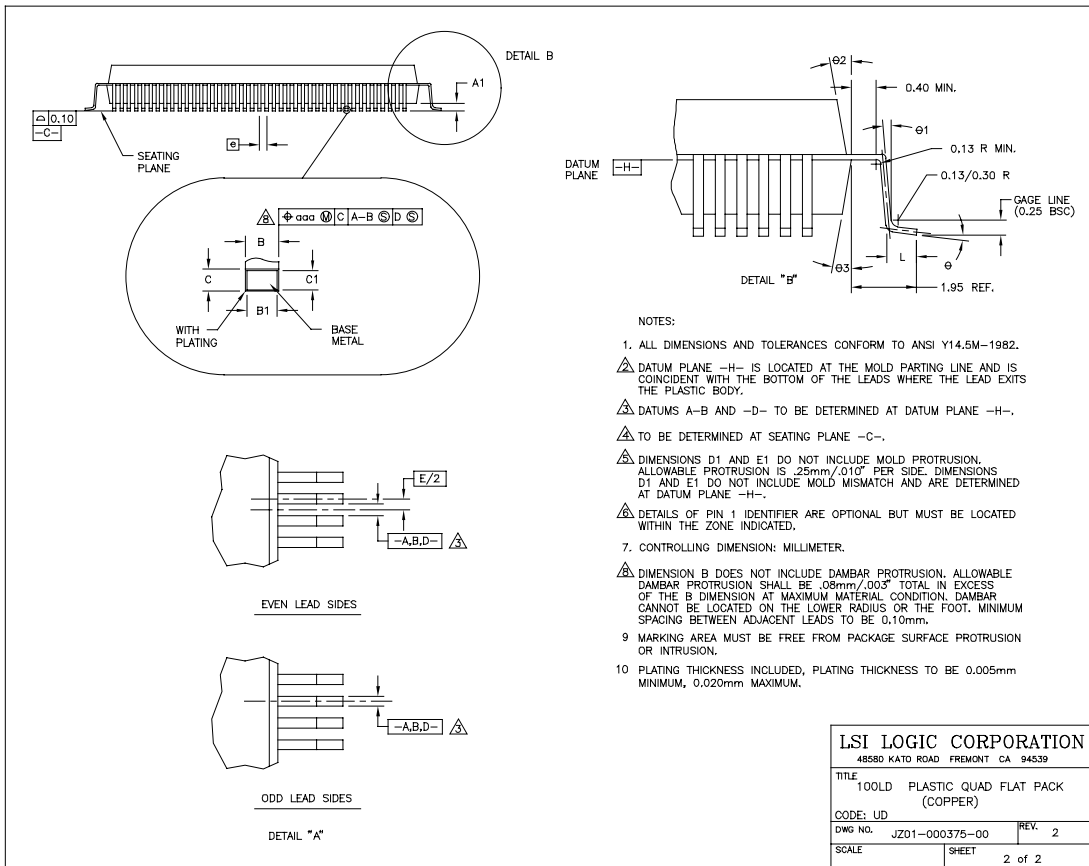
[Figure 7.24](#) illustrates the mechanical drawing for the LSI53C860.

Figure 7.24 100 LD PQFP (UD) Mechanical Drawing (Sheet 1 of 2)



Important: This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UD.

Figure 7.24 100 LD PQFP (UD) Mechanical Drawing (Sheet 2 of 2)



Important: This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UD.

Appendix A

Register Summary

[Table A.1](#) lists the LSI53C860 configuration registers by register name.

Table A.1 Configuration Registers

Register Name	Address	Read/Write	Page
Base Address One (Memory)	0x14	Read/Write	3-17
Base Address Zero (I/O)	0x10	Read/Write	3-17
Cache Line Size	0x0C	Read/Write	3-15
Class Code	0x09	Read Only	3-15
Command	0x04	Read/Write	3-11
Device ID	0x02	Read Only	3-11
Header Type	0x0E	Read Only	3-16
Interrupt Line	0x3C	Read/Write	3-17
Interrupt Pin	0x3D	Read Only	3-18
Latency Timer	0x0D	Read/Write	3-16
Max_Lat	0x3F	Read Only	3-19
Min_Gnt	0x3E	Read Only	3-18
Revision ID	0x08	Read Only	3-14
Status	0x06	Read/Write	3-13
Vendor ID	0x00	Read Only	3-11

Table A.2 lists the LSI53C860 SCSI registers by register name.

Table A.2 SCSI Registers

Register Name	Address	Read/Write	Page
Adder Sum Output (ADDER)	0x3C–0x3F (0xBC–0xBF)	Read Only	5-48
Chip Test Five (CTEST5)	0x22 (0xA2)	Read/Write	5-37
Chip Test Four (CTEST4)	0x21 (0xA1)	Read/Write	5-36
Chip Test One (CTEST1)	0x19 (0x99)	Read Only	5-31
Chip Test Six (CTEST6)	0x23 (0xA3)	Read/Write	5-38
Chip Test Three (CTEST3)	0x1B (0x9B)	Read/Write	5-33
Chip Test Two (CTEST2)	0x1A (0x9A)	Read Only	5-32
Chip Test Zero (CTEST0)	0x18 (0x98)	Read/Write	5-31
Data Structure Address (DSA)	0x10–0x13 (0x90–0x93)	Read/Write	5-27
DMA Byte Counter (DBC)	0x24–0x26 (0xA4–0xA6)	Read/Write	5-39
DMA Command (DCMD)	0x27 (0xA7)	Read/Write	5-40
DMA Control (DCNTL)	0x3B (0xBB)	Read/Write	5-46
DMA FIFO (DFIFO)	0x20 (0xA0)	Read/Write	5-35
DMA Interrupt Enable (DIEN)	0x39 (0xB9)	Read/Write	5-44
DMA Mode (DMODE)	0x38 (0xB8)	Read/Write	5-42
DMA Next Address (DNAD)	0x28–0x2B (0xA8–0xAB)	Read/Write	5-40
DMA SCRIPTS Pointer (DSP)	0x2C–0x2F (0xAC–0xAF)	Read/Write	5-41
DMA SCRIPTS Pointer Save (DSPS)	0x30–0x33 (0xB0–0xB3)	Read/Write	5-41
DMA Status (DSTAT)	0x0C (0x8C)	Read Only	5-21
General Purpose (GPREG)	0x07 (0x87)	Read/Write	5-17
General Purpose Pin Control (GPCNTL)	0x47 (0xC7)	Read/Write	5-58
Interrupt Status (ISTAT)	0x14 (0x94)	Read/Write	5-27
Memory Access Control (MACNTL)	0x46 (0xC6)	Read/Write	5-57
Response ID (RESPID)	0x4A (0xCA)	Read/Write	5-61

Table A.2 SCSI Registers

Register Name	Address	Read/Write	Page
Scratch Byte Register (SBR)	0x3A (0xBA)	Read/Write	5-46
Scratch Register A (SCRATCHA)	0x34–0x37 (0xB4–0xB7)	Read/Write	5-42
Scratch Register B (SCRATCHB)	0x5C–0x5F (0xDC–0xDF)	Read/Write	5-69
SCSI Bus Control Lines (SBCL)	0x0B (0x8B)	Read Only	5-21
SCSI Bus Data Lines (SBDL)	0x58 (0xD8)	Read Only	5-68
SCSI Chip ID (SCID)	0x04 (0x84)	Read/Write	5-12
SCSI Control One (SCNTL1)	0x01 (0x81)	Read/Write	5-6
SCSI Control Three (SCNTL3)	0x03 (0x83)	Read/Write	5-10
SCSI Control Two (SCNTL2)	0x02 (0x82)	Read/Write	5-9
SCSI Control Zero (SCNTL0)	0x00 (0x80)	Read/Write	5-3
SCSI Destination ID (SDID)	0x06 (0x86)	Read/Write	5-16
SCSI First Byte Received (SFBR)	0x08 (0x88)	Read/Write	5-18
SCSI Input Data Latch (SIDL)	0x50 (0xD0)	Read Only	5-67
SCSI Interrupt Enable One (SIEN1)	0x41 (0xC1)	Read/Write	5-51
SCSI Interrupt Enable Zero (SIEN0)	0x40 (0xC0)	Read/Write	5-48
SCSI Interrupt Status One (SIST1)	0x43 (0xC3)	Read Only	5-54
SCSI Interrupt Status Zero (SIST0)	0x42 (0xC2)	Read Only	5-52
SCSI Longitudinal Parity (SLPAR)	0x44 (0xC4)	Read/Write	5-55
SCSI Output Control Latch (SOCL)	0x09 (0x89)	Read /Write	5-19
SCSI Output Data Latch (SODL)	0x54 (0xD4)	Read/Write	5-68
SCSI Selector ID (SSID)	0x0A (0x8A)	Read Only	5-20
SCSI Status One (SSTAT1)	0x0E (0x8E)	Read Only	5-25
SCSI Status Two (SSTAT2)	0x0F (0x8F)	Read Only	5-26
SCSI Status Zero (SSTAT0)	0x0D (0x8D)	Read Only	5-23
SCSI Test One (STEST1)	0x4D (0xCD)	Read/Write	5-63

Table A.2 SCSI Registers

Register Name	Address	Read/Write	Page
SCSI Test Three (STEST3)	0x4F (0xCF)	Read/Write	5-65
SCSI Test Two (STEST2)	0x4E (0xCE)	Read/Write	5-64
SCSI Test Zero (STEST0)	0x4C (0xCC)	Read Only	5-62
SCSI Timer One (STIME1)	0x49 (0xC9)	Read/Write	5-61
SCSI Timer Zero (STIME0)	0x48 (0xC8)	Read/Write	5-59
SCSI Transfer (SXFER)	0x05 (0x85)	Read/Write	5-13
Temporary (TEMP)	0x1C–0x1F (0x9C–0x9F)	Read/Write	5-34

Index

Symbols

(AD[31:0]) 5-6
(BARO[31:0]) 3-17
(BARZ[31:0]) 3-17
(CLS[7:0]) 3-15
(FMT) 6-31
(HT[7:0]) 3-16
(IL[7:0]) 3-17
(IP[7:0]) 3-18
(LT[7:0]) 3-16
(MG[7:0]) 3-18
(ML[7:0]) 3-19

Numerics

3.3/5 volt PCI interface 2-6
3-state 5-3

A

abort operation bit 6-27
aborted bit 6-22, 6-45
ABRT bit 6-22, 6-27, 6-45
AC characteristics 8-10
ACK bit 6-19, 6-21
active negation. See TolerANT
ADCK bit 6-37
ADDER register 6-48
adder sum output register 6-48
AIP bit 6-24
arbitration in progress bit 6-24
arbitration priority encoder test bit 6-62
ART bit 6-62
assert SCSI ACK bit 6-19
assert SCSI ATN/ bit 6-19
assert SCSI BSY/ bit 6-19
assert SCSI C_D/ bit 6-19
assert SCSI I_O/ bit 6-19
assert SCSI MSG/ bit 6-19
assert SCSI REQ/ signal bit 6-19
assert SCSI SEL/ bit 6-19
ATN bit 6-19

B

base address register
 one (BARO[31:0]) 3-17
 zero - I/O (BARZ[31:0]) 3-17
BBCK bit 6-38
BDIS bit 6-36

benefits summary 1-3
BF bit 6-22, 6-45
bidirectional 5-3
BL[1:0] bits 6-42
block move Instructions 7-5
BO[6:0] bits 6-35
BOF bit 6-44
BSY bit 6-19, 6-21
burst disable bit 6-36
burst length bits 6-42
burst mode fetch enable bit 6-44
bus command and byte enables 5-6
bus fault bit 6-22, 6-45
byte
 empty in DMA FIFO (FMT) 6-31
byte empty in DMA FIFO bits 6-31
byte full in DMA FIFO bits 6-31
byte offset counter bits 6-35

C

C_BE/[3:0] 5-6
C_D bit 6-19, 6-21, 6-26
cache line size
 (CLS[7:0]) 3-15
cache line size enable bit 6-46
cache mode, see PCI cache mode 3-3
chip revision level bits 6-33
chip test five register 6-37
chip test four register 6-36
chip test one register 6-31
chip test six register 6-38
chip test two register 6-32
chip test zero register 6-31
chip type bits 6-57
clear SCSI FIFO bit 6-67
CLK 5-5
clock 5-5
clock address incrementor bit 6-37
clock byte counter bit 6-38
CLSE bit 6-46
CM bit 6-32
CMP bit 6-49, 6-52
COM bit 6-48
CON bit 6-29
configuration registers. See PCI configuration registers
configured as memory bit 6-32
connected bit 6-29
CSF bit 6-67
CTEST0 register 6-31
CTEST1 register 6-31

CTEST2 register [6-32](#)
CTEST4 register [6-36](#)
CTEST5 register [6-37](#)
CTEST6 register [6-38](#)
cycle frame [5-7](#)

D

DACK bit [6-33](#)
Data acknowledge status bit [6-33](#)
data path [2-9](#)
Data request status bit [6-33](#)
data structure address register [6-27](#)
data transfer direction bit [6-32](#)
dataRD bit [6-57](#)
dataWR bit
 DWR bit [6-57](#)
DBC register [6-39](#)
DCMD register [6-40](#)
DCNTL register [6-46](#)
DDIR bit [6-32](#), [6-38](#)
destination I/O-memory enable bit [6-43](#)
determining the data transfer rate [2-14](#)
device select [5-7](#)
DEVSEL/ [5-7](#)
DF[7:0] bits [6-38](#)
DFE bit [6-22](#)
DFIFO register [6-35](#)
DIEN register [6-44](#)
DIFFSENS SCSI signal [8-3](#)
DIOM bit [6-43](#)
disable single initiator response bit [6-66](#)
DMA byte counter register [6-39](#)
DMA command register [6-40](#)
DMA control register [6-46](#)
DMA core [2-2](#)
DMA direction bit [6-38](#)
DMA FIFO [2-9](#)
DMA FIFO bits [6-38](#)
DMA FIFO empty bit [6-22](#)
DMA FIFO register [6-35](#)
DMA interrupt enable register [6-44](#)
DMA mode register [6-42](#)
DMA next address register [6-40](#)
DMA SCRIPTS pointer register [6-41](#)
DMA SCRIPTS pointer save register [6-41](#)
DMA status register [6-21](#)
DMODE register [6-42](#)
DNAD register [6-40](#)
DRD bit [6-57](#)
DREQ bit [6-33](#)
DSA register [6-27](#)
DSI bit [6-66](#)
DSP register [6-41](#)
DSPS register [6-41](#)
DSTAT register [6-21](#)

E

ease of use [1-5](#)
enable read line bit [6-43](#)
enable read multiple bit [6-44](#)
enable response to reselection bit [6-12](#)
enable response to selection bit [6-12](#)
encoded chip SCSI ID, bits[2:0] [6-13](#)
encoded destination SCSI ID bits [6-16](#), [6-20](#)

ERL bit [6-43](#)
EXT bit [6-64](#)
extend SREQ/SACK filtering bit [6-64](#)

F

FBL[2:0] bits [6-37](#)
fetch enable bit [6-58](#)
fetch opcode bursting [2-5](#)
FFL[3:0] bits [6-31](#)
FIFO byte control bits [6-37](#)
FMT[3:0] bits [6-31](#)
FRAME/ [5-7](#)
full arbitration, selection/reselection [6-4](#)
function complete bit [6-49](#), [6-52](#)

G

GEN bit [6-51](#), [6-55](#)
GEN[3:0] bits [6-61](#)
general purpose pin control register [6-58](#)
general purpose register [6-17](#)
general purpose timer expired bit [6-51](#), [6-55](#)
general purpose timer period bits [6-61](#)
GNT/ [5-8](#)
GPCNTL register [6-58](#)
GPIO enable bits [6-58](#)
GPIO[1:0] bits [6-58](#)
GPREG register [6-17](#)
grant [5-8](#)

H

halt SCSI clock bit
 HSC bit [6-66](#)
handshake-to-handshake timer expired bit [6-51](#), [6-55](#)
header type (HT[7:0]) [3-16](#)
high impedance mode bit [6-36](#)
HTH bit [6-51](#), [6-55](#)

I

I/O bit [6-26](#)
I/O instructions [7-13](#)
I_O bit [6-19](#)
IDSEL [5-7](#)
IID bit [6-45](#)
illegal instruction detected bit [6-45](#)
initialization device select [5-7](#)
initiator ready [5-7](#)
input [5-3](#)
instruction prefetch. See SCRIPTS instruction prefetching
instruction set [7-1](#) to [7-42](#)
instructions
 block move [7-5](#)
 I/O [7-13](#)
 load and store [7-39](#)
 memory move [7-35](#)
 read/write [7-22](#)
 transfer control [7-27](#)
interrupt
 line [3-17](#)
 pin (IP[7:0]) [3-18](#)
interrupt output timings [8-11](#)
interrupt status register [6-27](#)

interrupt-on-the-fly bit [6-29](#)

interrupts

fatal vs. nonfatal interrupts [2-18](#)

halting [2-21](#)

IRQ disable bit [2-17](#), [6-47](#)

masking [2-19](#)

polling vs. hardware [2-16](#)

registers [2-16](#)

stacked interrupts [2-19](#)

INTF bit [6-29](#)

IRDY/ [5-7](#)

IRQ disable bit [6-47](#)

IRQ mode bit [6-47](#)

IRQD bit [6-47](#)

IRQM bit [6-47](#)

ISTAT register [6-27](#)

L

last disconnect bit [6-26](#)

latched SCSI parity bit [6-25](#)

latency

timer (LT[7:0]) [3-16](#)

LDSC bit [6-26](#)

load and store instructions [7-39](#)

no flush option [7-40](#)

prefetch unit and store instructions [2-4](#), [7-41](#)

LOW bit [6-65](#)

LSI53C700 family compatibility bit [6-48](#)

LSI53C810A

ease of use [1-5](#)

LSI53C860

ease of use [1-5](#)

flexibility [1-5](#)

integration [1-5](#)

performance [1-4](#)

testability [1-7](#)

M

M/A bit [6-49](#)

MACNTL register [6-57](#)

MAN bit [6-44](#)

manual start mode bit [6-44](#)

MASR bit [6-38](#)

master control for set or reset pulses bit [6-38](#)

master data parity error bit [6-22](#)

MDPE bit [6-45](#)

master enable bit [6-58](#)

master parity error enable bit [6-37](#)

max SCSI synchronous offset bits [6-15](#)

max_lat (ML[7:0]) [3-19](#)

MDPE bit [6-22](#)

memory access control register [6-57](#)

memory move instructions [7-35](#)

and SCRIPTS instruction prefetching [2-4](#)

no flush option [7-38](#)

memory read line command [3-6](#)

memory read multiple command [3-7](#)

memory write and invalidate command [3-5](#)

write and invalidate mode bit [3-12](#)

min_gnt (MG[7:0]) [3-18](#)

move to/from SFBR cycles [7-23](#)

MPEE bit [6-37](#)

MSG bit [6-19](#), [6-21](#), [6-26](#)

N

NFMMOV instruction [7-38](#)

no flush memory-to-memory move [7-38](#)

O

OLF bit [6-24](#)

opcode fetch bursting [2-5](#)

operating registers

adder sum output [6-48](#)

chip test five [6-37](#)

chip test four [6-36](#)

chip test one [6-31](#)

chip test six [6-38](#)

chip test three [6-33](#)

chip test two [6-32](#)

chip test zero [6-31](#)

data structure address [6-27](#)

DMA byte counter [6-39](#)

DMA command [6-40](#)

DMA control [6-46](#)

DMA FIFO [6-35](#)

DMA interrupt enable [6-44](#)

DMA mode [6-42](#)

DMA next address [6-40](#)

DMA SCRIPTS pointer [6-41](#)

DMA SCRIPTS pointer save [6-41](#)

DMA status [6-21](#)

general purpose [6-17](#)

general purpose pin control [6-58](#)

interrupt status [6-27](#)

memory access control [6-57](#)

response ID zero [6-61](#)

scratch register A [6-42](#)

scratch register B [6-69](#)

SCSI bus control lines [6-21](#)

SCSI bus data lines [6-68](#)

SCSI chip ID [6-12](#)

SCSI destination ID [6-16](#)

SCSI first byte received [6-18](#)

SCSI input data latch [6-67](#)

SCSI interrupt enable one [6-51](#)

SCSI interrupt enable zero [6-48](#)

SCSI interrupt status one [6-54](#)

SCSI interrupt status zero [6-52](#)

SCSI longitudinal parity [6-55](#)

SCSI output control latch [6-19](#)

SCSI output data latch [6-68](#)

SCSI selector ID [6-20](#)

SCSI Status One [6-25](#)

SCSI status two [6-26](#)

SCSI status zero [6-23](#)

SCSI test one [6-63](#)

SCSI test three [6-65](#)

SCSI test two [6-64](#)

SCSI test zero [6-62](#)

SCSI timer one [6-61](#)

SCSI timer zero [6-59](#)

SCSI transfer [6-13](#)

temporary stack [6-34](#)

ORF bit [6-23](#)

P

PAR 5-6
PAR bit 6-50, 6-54
parity 2-6 to 2-8, 5-6
 master data parity error bit 6-45
 master parity error enable bit 6-37
 parity error bit 6-54
 SCSI parity error bit 6-50
parity error 5-8
parity error bit 6-54
PCI
 addressing 3-1
 bus commands and functions supported 3-2
PCI addressing 3-1
PCI bus commands and functions supported 3-2
PCI cache mode 2-5, 3-3
 cache line size enable bit 6-46
 enable read line bit 6-43
 enable read multiple bit 6-44
 memory read line command 3-6
 memory read multiple command 3-7
 memory write and invalidate command 3-5
 write and invalidate mode bit 3-12
 write and invalidate enable bit 6-34
PCI commands 3-2
PCI configuration registers 3-9, 3-18
 command 3-11
 device ID 3-11
 status 3-13
 vendor ID 3-11
PCI configuration space 3-1
PCI I/O space 3-2
PCI memory space 3-2
PERR/ 5-8
PFEN bit 6-46
PFF bit 6-46
physical dword address and data 5-6
pointer SCRIPTS bit
 PSCPT bit 6-57
prefetch enable bit 6-46
prefetch flush bit 6-46
prefetching
prefetching. See SCRIPTS instruction

R

read multiple commands
 enable read multiple bit 6-44
read/write instructions 7-22
register addresses
 operating registers
 0x04 6-12
 0x06 6-16
 0x07 6-17
 0x08 6-18
 0x09 6-19
 0x0A 6-20
 0x0B 6-21
 0x0C 6-21
 0x0D 6-23
 0x0E 6-25
 0x0F 6-26
 0x10–0x13 6-27
 0x14 6-27
 0x18 6-31

0x19 6-31
0x1A 6-32
0x1C–0x1F 6-34
0x20 6-35
0x21 6-36
0x22 6-37
0x23 6-38
0x24h–0x26 6-39
0x27 6-40
0x28–0x2B 6-40
0x2C–0x2F 6-41
0x30–0x33 6-41
0x34–0x37 6-42
0x38 6-42
0x39 6-44
0x3B 6-46
0x3C–0x3F 6-48
0x40 6-48
0x41 6-51
0x42 6-52
0x43 6-54
0x44 6-55
0x46 6-57
0x47 6-58
0x48 6-59
0x49 6-61
0x4A 6-61
0x4C 6-62
0x4D 6-63
0x4E 6-64
0x4F 6-65
0x50 6-67
0x54 6-68
0x58 6-68
0x5C–0x5F 6-69
PCI configuration registers
 0x00 3-11
 0x02 3-11
 0x04 3-11
 0x06 3-13
register bits
 abort operation 6-27
 aborted 6-22, 6-45
 arbitration in progress 6-24
 arbitration priority encoder test 6-62
 assert SCSI ACK 6-19
 assert SCSI ATN/ 6-19
 assert SCSI BSY/ 6-19
 assert SCSI C_D/ 6-19
 assert SCSI I_O/ 6-19
 assert SCSI MSG/ 6-19
 assert SCSI REQ/ signal 6-19
 assert SCSI SEL/ 6-19
 burst disable 6-36
 burst length 6-42
 burst mode fetch enable 6-44
 bus fault 6-45
 byte empty in DMA FIFO 6-31
 byte full in DMA FIFO 6-31
 byte offset counter 6-35
 cache line size enable 6-46
 chip revision level 6-33
 chip type 6-57
 clear DMA FIFO 6-33
 clear SCSI FIFO 6-67
 clock address incrementor 6-37

register bits (Cont.)

- clock byte counter 6-38
- configured as memory 6-32
- connected 6-29
- DACK 6-33
- data transfer direction 6-32
- dataRD 6-57
- dataWR 6-57
- destination I/O-memory enable 6-43
- disable single initiator response 6-66
- DMA direction 6-38
- DMA FIFO 6-38
- DMA FIFO empty bit 6-22
- DREQ 6-33
- enable read line 6-43
- enable read multiple 6-44
- enable response to reselection 6-12
- enable response to selection 6-12
- encoded chip SCSI ID, bits[2:0] 6-13
- encoded destination ID 6-16
- encoded destination SCSI ID 6-20
- extend SREQ/SACK filtering 6-64
- fetch enable 6-58
- fetch pin mode 6-34
- FIFO byte control 6-37
- flush DMA FIFO 6-33
- function complete 6-49, 6-52
- general purpose timer expired 6-51, 6-55
- general purpose timer period 6-61
- GPIO enable 6-58
- GPIO[1:0] 6-17
- halt SCSI clock 6-66
- handshake-to-handshake timer expired 6-51, 6-55
- high impedance mode 6-36
- illegal instruction detected 6-45
- interrupt-on-the-fly 6-29
- IRQ disable 6-47
- IRQ mode 6-47
- last disconnect 6-26
- latched SCSI parity 6-25
- LSI53C700 family compatibility 6-48
- manual start mode 6-44
- master control for set or reset pulses 6-38
- master data parity error 6-22, 6-45
- master enable 6-58
- master parity error enable 6-37
- max SCSI synchronous offset 6-15
- parity error 6-54
- pointer SCRIPTS 6-57
- prefetch enable 6-46
- prefetch flush 6-46
- reselected 6-53
- reset SCSI offset 6-64
- SACK/ status 6-21
- SATN/ status 6-21
- SBSY/ status 6-21
- SC_D/ status 6-21
- SCLK 6-63
- SCRIPTS 6-57
- SCSI C_D/ signal 6-26
- SCSI Data high impedance 6-36
- SCSI FIFO test read 6-66
- SCSI FIFO test write 6-67
- SCSI gross error 6-49, 6-53
- SCSI high impedance mode 6-64
- SCSI I_O/ signal 6-26

- SCSI interrupt pending 6-29
- SCSI isolation 6-63
- SCSI loopback mode 6-64
- SCSI low level mode 6-65
- SCSI MSG/ signal 6-26
- SCSI parity error 6-50
- SCSI phase mismatch or SCSI ATN condition 6-49
- SCSI RST/ signal 6-24
- SCSI selected as ID 6-62
- SCSI synchronous offset maximum 6-63
- SCSI synchronous offset zero 6-62
- SCSI synchronous transfer period 6-13
- SCSI true end of process 6-32
- SCSI valid 6-20
- selected 6-49, 6-53
- selection or reselection time-out 6-51, 6-55
- selection response logic test 6-62
- selection time-out 6-60
- semaphore 6-28
- shadow register test mode 6-36
- SI_O/ status 6-21
- SIDL full 6-23
- signal process 6-32
- single step interrupt 6-22, 6-45
- single-step mode 6-47
- SMSG/ status 6-21
- SODL full 6-24
- SODR full 6-23
- software reset 6-28
- source I/O-memory enable 6-43
- SREQ/ status 6-21
- SSEL/ status 6-21
- start DMA operation 6-47
- unexpected disconnect 6-50, 6-53
- won arbitration 6-24
- write and invalidate enable 6-34
- REQ bit 6-19, 6-21
- REQ/ 5-8
- request 5-8
- reselect
 - during reselection 2-12
 - response to 2-12
- reselected bit 6-53
- reset 5-5
- reset SCSI offset bit 6-64
- RESPID0 register 6-61
- response ID zero register 6-61
- revision level bits 6-33
- ROF bit 6-64
- RRE bit 6-12
- RSL bit 6-53
- RST/ 5-5
- RST/ bit 6-24

S

- SACK/ 5-9
- SACK/ status bit 6-21
- SAT bit 6-21
- SATN/ 5-9
- SATN/ status bit 6-21
- SBCL register 6-21
- SBDL register 6-68
- SBSY/ 5-9
- SBSY/ status bit 6-21
- SC_D/ status bit 6-21

SCD/ 5-9
 SCF[2:0] bits 6-10
 SCID register 6-12
 SCLK 5-9
 SCLK bit 6-63
 SCPTS bit 6-57
 SCRATCHA register 6-42
 SCRATCHB register 6-69
 SCRIPTS
 sample operation 7-3
 SCRIPTS bit 6-57
 SCRIPTS instruction prefetching
 no flush memory move instruction 7-38
 prefetch enable bit 6-46
 prefetch flush bit 6-46
 SCRIPTS processor 2-2
 performance 2-2
 SCSI
 termination 2-12
 SCSI ATN condition - target mode 6-49
 SCSI bus control lines register 6-21
 SCSI bus data lines register 6-68
 SCSI bus interface 2-11 to 2-12
 SCSI C_D/ signal 6-26
 SCSI chip ID register 6-12
 SCSI clock 5-9
 SCSI control 5-9
 SCSI core 2-1
 SCSI data high impedance bit 6-36
 SCSI destination ID register 6-16
 SCSI FIFO test read bit 6-66
 SCSI FIFO test write bit 6-67
 SCSI first byte received register 6-18
 SCSI gross error bit 6-49, 6-53
 SCSI high impedance mode bit 6-64
 SCSI I_O/ bit 6-26
 SCSI input data latch register 6-67
 SCSI instructions
 block move 7-5
 I/O 7-13
 load/store 7-39
 memory move 7-35
 read/write 7-22
 SCSI interrupt enable one register 6-51
 SCSI interrupt enable zero register 6-48
 SCSI interrupt pending bit 6-29
 SCSI interrupt status one register 6-54
 SCSI interrupt status zero register 6-52
 SCSI isolation bit 6-63
 SCSI longitudinal parity register 6-55
 SCSI loopback mode bit 6-64
 SCSI low level mode 6-65
 SCSI MSG/ bit 6-26
 SCSI output control latch register 6-19
 SCSI output data latch register 6-68
 SCSI parity error bit 6-50
 SCSI phase mismatch - initiator mode bit 6-49
 SCSI RST/ signal bit 6-24
 SCSI SCRIPTS operation 7-2
 SCSI selected as ID bits 6-62
 SCSI selector ID register 6-20
 SCSI status one register 6-25
 SCSI status two register 6-26
 SCSI status zero register 6-23
 SCSI synchronous offset maximum bit 6-63
 SCSI synchronous offset zero bit 6-62
 SCSI synchronous transfer period bits 6-13
 SCSI test one register 6-63
 SCSI test three register 6-65
 SCSI test two register 6-64
 SCSI test zero register 6-62
 SCSI timer one register 6-61
 SCSI timer zero register 6-59
 SCSI timings 8-26
 SCSI true end of process bit 6-32
 SCSI valid Bit 6-20
 SCTRL/ 5-9
 SD/[15:0] 5-9
 SDID register 6-16
 SDP/[1:0] 5-9
 SDPL bit 6-25
 SEL bit 6-19, 6-21, 6-49, 6-53
 SEL bits 6-60
 selected bit 6-49, 6-53
 selection
 during reselection 2-12
 during selection 2-12
 response to 2-12
 selection or reselection time-out bit 6-51
 STO bit 6-55
 selection response logic test bit 6-62
 selection time-out bits 6-60
 SEM bit 6-28
 semaphore bit 6-28
 SERR/ 5-8
 SFBR register 6-18
 SGE bit 6-49, 6-53
 shadow register test mode bit 6-36
 SI_O bit 6-21
 SI_O/ status bit 6-21
 SIDL bit 6-23
 SIDL least significant byte full bit 6-23
 SIDL register 6-67
 SIEN0 register 6-48
 SIEN1 register 6-51
 signal process bit 6-32
 SIGP bit 6-32
 single step interrupt bit 6-22, 6-45
 single-ended operation 2-11
 single-step mode bit 6-47
 SIO/ 5-9
 SIOM bit 6-43
 SIP bit 6-29
 SISO bit 6-63
 SIST0 register 6-52
 SIST1 register 6-54
 SLB bit 6-64
 SLPAR register 6-55
 SLT bit 6-62
 MSG/ 5-9
 MSG/ status bit 6-21
 SOCL register 6-19
 SODL least significant byte full bit 6-24
 SODL register 6-68
 SODR least significant byte full bit 6-23
 software reset bit 6-28
 SOM bit 6-63
 source I/O-memory enable bit 6-43
 SOZ bit 6-62
 SRE bit 6-12
 SREQ/ 5-9
 SREQ/ status bit 6-21

- SRST bit [6-28](#)
- SRST/ [5-9](#)
- SRTM bit [6-36](#)
- SSAID bits [6-62](#)
- SSEL/ [5-9](#)
- SSEL/ status bit [6-21](#)
- SSI bit [6-22](#), [6-45](#)
- SSID register [6-20](#)
- SSM bit [6-47](#)
- SSTAT0 register [6-23](#)
- SSTAT1 register [6-25](#)
- SSTAT2 register [6-26](#)
- stacked interrupts [2-19](#)
- start DMA operation bit [6-47](#)
- STD bit [6-47](#)
- STEST0 register [6-62](#)
- STEST1 register [6-63](#)
- STEST2 register [6-64](#)
- STEST3 register [6-65](#)
- STIME0 register [6-59](#)
- STIME1 register [6-61](#)
- STO bit [6-51](#)
- stop [5-7](#)
- Storage Device Management System (SDMS) [2-3](#)
- STR bit [6-66](#)
- STW bit [6-67](#)
- synchronous clock conversion factor bits [6-10](#)
- synchronous data transfer rate [2-14](#)
- synchronous operation [2-13](#)
- SZM bit [6-64](#)

T

- target ready [5-7](#)
- TE bit [6-65](#)
- TEMP register [6-34](#)
- temporary register [6-34](#)
- TEOP bit [6-32](#)
- termination [2-12](#)
- timer test mode bit [6-66](#)
- timing diagrams [8-12](#) to [8-28](#)
 - interrupt output [8-11](#)
 - PCI interface [8-25](#)
 - SCSI timings [8-26](#)
- timings
 - PCI [8-25](#)
 - SCSI [8-26](#)
- TolerANT [1-2](#)
 - extend SREQ/SACK filtering bit [6-64](#)
 - TolerANT enable bit [6-65](#)
- TolerANT enable bit [6-65](#)
- totem pole output [5-3](#)
- TP[2:0] bits [6-13](#)
- transfer control instructions [7-27](#)
 - prefetch unit flushing [2-4](#)
- transfer rate [1-4](#)
 - synchronous [2-14](#)
- TRDY/ [5-7](#)
- TTM bit [6-66](#)
- TYP[3:0] bits [6-57](#)

U

- UDC bit [6-50](#), [6-53](#)
- Ultra SCSI
 - SCSI termination requirements [2-12](#)
 - synchronous clock conversion factor bits [6-10](#)
- unexpected disconnect bit [6-50](#), [6-53](#)

V

- VAL bit [6-20](#)
- VDD [5-3](#)
- VDD-C [5-3](#)
- VSS [5-3](#)
- VSS-C [5-3](#)
- VSS-S [5-3](#)

W

- WOA bit [6-24](#)
- won arbitration bit [6-24](#)
- write and invalidate command
 - write and invalidate enable bit [6-34](#)

Z

- ZMOD bit [6-36](#)
- ZSD bit [6-36](#)

Customer Feedback

We would appreciate your feedback on this document. Please copy the following page, add your comments, and fax it to us at the number shown.

If appropriate, please also fax copies of any marked-up pages from this document.

Important: Please include your name, phone number, fax number, and company address so that we may contact you directly for clarification or additional information.

Thank you for your help in improving the quality of our documents.

Reader's Comments

Fax your comments to: LSI Logic Corporation
Technical Publications
M/S E-198
Fax: 408.433.4333

Please tell us how you rate this document: *LSI53C860 PCI to Ultra SCSI I/O Processor Technical Manual*. Place a check mark in the appropriate blank for each category.

	Excellent	Good	Average	Fair	Poor
Completeness of information	_____	_____	_____	_____	_____
Clarity of information	_____	_____	_____	_____	_____
Ease of finding information	_____	_____	_____	_____	_____
Technical content	_____	_____	_____	_____	_____
Usefulness of examples and illustrations	_____	_____	_____	_____	_____
Overall manual	_____	_____	_____	_____	_____

What could we do to improve this document?

If you found errors in this document, please specify the error and page number. If appropriate, please fax a marked-up copy of the page(s).

Please complete the information below so that we may contact you directly for clarification or additional information.

Name _____ Date _____
Telephone _____ Fax _____
Title _____
Department _____ Mail Stop _____
Company Name _____
Street _____
City, State, Zip _____

U.S. Distributors by State

A. E. Avnet Electronics
<http://www.hh.avnet.com>
B. M. Bell Microproducts,
Inc. (for HAB's)
<http://www.bellmicro.com>
I. E. Insight Electronics
<http://www.insight-electronics.com>
W. E. Wyle Electronics
<http://www.wyle.com>

Alabama

Daphne
I. E. Tel: 334.626.6190
Huntsville
A. E. Tel: 256.837.8700
I. E. Tel: 256.830.1222
W. E. Tel: 800.964.9953

Alaska

A. E. Tel: 800.332.8638

Arkansas

W. E. Tel: 972.235.9953

Arizona

Phoenix
A. E. Tel: 480.736.7000
B. M. Tel: 602.267.9551
W. E. Tel: 800.528.4040
Tempe
I. E. Tel: 480.829.1800
Tucson
A. E. Tel: 520.742.0515

California

Agoura Hills
B. M. Tel: 818.865.0266
Irvine
A. E. Tel: 949.789.4100
B. M. Tel: 949.470.2900
I. E. Tel: 949.727.3291
W. E. Tel: 800.626.9953
Los Angeles
A. E. Tel: 818.594.0404
W. E. Tel: 800.288.9953
Sacramento
A. E. Tel: 916.632.4500
W. E. Tel: 800.627.9953
San Diego
A. E. Tel: 858.385.7500
B. M. Tel: 858.597.3010
I. E. Tel: 800.677.6011
W. E. Tel: 800.829.9953
San Jose
A. E. Tel: 408.435.3500
B. M. Tel: 408.436.0881
I. E. Tel: 408.952.7000
Santa Clara
W. E. Tel: 800.866.9953
Woodland Hills
A. E. Tel: 818.594.0404
Westlake Village
I. E. Tel: 818.707.2101

Colorado

Denver
A. E. Tel: 303.790.1662
B. M. Tel: 303.846.3065
W. E. Tel: 800.933.9953
Englewood
I. E. Tel: 303.649.1800

Connecticut

Cheshire
A. E. Tel: 203.271.5700
I. E. Tel: 203.272.5843
Wallingford
W. E. Tel: 800.605.9953

Delaware

North/South
A. E. Tel: 800.526.4812
Tel: 800.638.5988
B. M. Tel: 302.328.8968
W. E. Tel: 856.439.9110

Florida

Altamonte Springs
B. M. Tel: 407.682.1199
I. E. Tel: 407.834.6310
Boca Raton
I. E. Tel: 561.997.2540
Clearwater
I. E. Tel: 727.524.8850
Fort Lauderdale
A. E. Tel: 954.484.5482
W. E. Tel: 800.568.9953
Miami
B. M. Tel: 305.477.6406
Orlando
A. E. Tel: 407.657.3300
W. E. Tel: 407.740.7450
Tampa
W. E. Tel: 800.395.9953
St. Petersburg
A. E. Tel: 727.507.5000

Georgia

Atlanta
A. E. Tel: 770.623.4400
B. M. Tel: 770.980.4922
W. E. Tel: 800.876.9953
Duluth
I. E. Tel: 678.584.0812

Hawaii

A. E. Tel: 800.851.2282

Idaho

A. E. Tel: 801.365.3800
W. E. Tel: 801.974.9953

Illinois

North/South
A. E. Tel: 847.797.7300
Tel: 314.291.5350
Chicago
B. M. Tel: 847.413.8530
W. E. Tel: 800.853.9953
Schaumburg
I. E. Tel: 847.885.9700

Indiana

Fort Wayne
I. E. Tel: 219.436.4250
W. E. Tel: 888.358.9953
Indianapolis
A. E. Tel: 317.575.3500

Iowa

W. E. Tel: 612.853.2280
Cedar Rapids
A. E. Tel: 319.393.0033

Kansas

W. E. Tel: 303.457.9953
Kansas City
A. E. Tel: 913.663.7900
Lenexa
I. E. Tel: 913.492.0408

Kentucky

W. E. Tel: 937.436.9953
Central/Northern/ Western
A. E. Tel: 800.984.9503
Tel: 800.767.0329
Tel: 800.829.0146

Louisiana

W. E. Tel: 713.854.9953
North/South
A. E. Tel: 800.231.0253
Tel: 800.231.5575

Maine

A. E. Tel: 800.272.9255
W. E. Tel: 781.271.9953

Maryland

Baltimore
A. E. Tel: 410.720.3400
W. E. Tel: 800.863.9953
Columbia
B. M. Tel: 800.673.7461
I. E. Tel: 410.381.3131

Massachusetts

Boston
A. E. Tel: 978.532.9808
W. E. Tel: 800.444.9953
Burlington
I. E. Tel: 781.270.9400
Marlborough
B. M. Tel: 508.480.9099
Woburn
B. M. Tel: 781.933.9010

Michigan

Brighton
I. E. Tel: 810.229.7710
Detroit
A. E. Tel: 734.416.5800
W. E. Tel: 888.318.9953

Minnesota

Champlin
B. M. Tel: 800.557.2566
Eden Prairie
B. M. Tel: 800.255.1469
Minneapolis
A. E. Tel: 612.346.3000
W. E. Tel: 800.860.9953
St. Louis Park
I. E. Tel: 612.525.9999

Mississippi

A. E. Tel: 800.633.2918
W. E. Tel: 256.830.1119

Missouri

W. E. Tel: 630.620.0969
St. Louis
A. E. Tel: 314.291.5350
I. E. Tel: 314.872.2182

Montana

A. E. Tel: 800.526.1741
W. E. Tel: 801.974.9953

Nebraska

A. E. Tel: 800.332.4375
W. E. Tel: 303.457.9953

Nevada

Las Vegas
A. E. Tel: 800.528.8471
W. E. Tel: 702.765.7117

New Hampshire

A. E. Tel: 800.272.9255
W. E. Tel: 781.271.9953

New Jersey

North/South
A. E. Tel: 201.515.1641
Tel: 609.222.6400
Mt. Laurel
I. E. Tel: 609.222.9566
Pine Brook
W. E. Tel: 800.862.9953
Parsippany
I. E. Tel: 973.299.4425
Wayne
W. E. Tel: 973.237.9010

New Mexico

W. E. Tel: 480.804.7000
Albuquerque
A. E. Tel: 505.293.5119

U.S. Distributors

by State

(Continued)

New York

Hauppauge
I. E. Tel: 516.761.0960
Long Island
A. E. Tel: 516.434.7400
W. E. Tel: 800.861.9953
Rochester
A. E. Tel: 716.475.9130
I. E. Tel: 716.242.7790
W. E. Tel: 800.319.9953
Smithtown
B. M. Tel: 800.543.2008
Syracuse
A. E. Tel: 315.449.4927

North Carolina

Raleigh
A. E. Tel: 919.859.9159
I. E. Tel: 919.873.9922
W. E. Tel: 800.560.9953

North Dakota

A. E. Tel: 800.829.0116
W. E. Tel: 612.853.2280

Ohio

Cleveland
A. E. Tel: 216.498.1100
W. E. Tel: 800.763.9953
Dayton
A. E. Tel: 614.888.3313
I. E. Tel: 937.253.7501
W. E. Tel: 800.575.9953
Strongsville
B. M. Tel: 440.238.0404
Valley View
I. E. Tel: 216.520.4333

Oklahoma

W. E. Tel: 972.235.9953
Tulsa
A. E. Tel: 918.459.6000
I. E. Tel: 918.665.4664

Oregon

Beaverton
B. M. Tel: 503.524.0787
I. E. Tel: 503.644.3300
Portland
A. E. Tel: 503.526.6200
W. E. Tel: 800.879.9953

Pennsylvania

Mercer
I. E. Tel: 412.662.2707
Pittsburgh
A. E. Tel: 412.281.4150
W. E. Tel: 440.248.9996
Philadelphia
A. E. Tel: 800.526.4812
B. M. Tel: 215.741.4080
W. E. Tel: 800.871.9953

Rhode Island

A. E. 800.272.9255
W. E. Tel: 781.271.9953

South Carolina

A. E. Tel: 919.872.0712
W. E. Tel: 919.469.1502

South Dakota

A. E. Tel: 800.829.0116
W. E. Tel: 612.853.2280

Tennessee

W. E. Tel: 256.830.1119
East/West
A. E. Tel: 800.241.8182
Tel: 800.633.2918

Texas

Austin
A. E. Tel: 512.219.3700
B. M. Tel: 512.258.0725
I. E. Tel: 512.719.3090
W. E. Tel: 800.365.9953
Dallas
A. E. Tel: 214.553.4300
B. M. Tel: 972.783.4191
W. E. Tel: 800.955.9953
El Paso
A. E. Tel: 800.526.9238
Houston
A. E. Tel: 713.781.6100
B. M. Tel: 713.917.0663
W. E. Tel: 800.888.9953
Richardson
I. E. Tel: 972.783.0800
Rio Grande Valley
A. E. Tel: 210.412.2047
Stafford
I. E. Tel: 281.277.8200

Utah

Centerville
B. M. Tel: 801.295.3900
Murray
I. E. Tel: 801.288.9001
Salt Lake City
A. E. Tel: 801.365.3800
W. E. Tel: 800.477.9953

Vermont

A. E. Tel: 800.272.9255
W. E. Tel: 716.334.5970

Virginia

A. E. Tel: 800.638.5988
W. E. Tel: 301.604.8488

Washington

Kirkland
I. E. Tel: 425.820.8100
Seattle
A. E. Tel: 425.882.7000
W. E. Tel: 800.248.9953

West Virginia

A. E. Tel: 800.638.5988

Wisconsin

Milwaukee
A. E. Tel: 414.513.1500
W. E. Tel: 800.867.9953
Wauwatosa
I. E. Tel: 414.258.5338

Wyoming

A. E. Tel: 800.332.9326
W. E. Tel: 801.974.9953

Direct Sales Representatives by State (Component and Boards)

E. A. Earle Associates
E. L. Electrodyne - UT
GRP Group 2000
I. S. Infinity Sales, Inc.
ION ION Associates, Inc.
R. A. Rathsburg Associates, Inc.
SGY Synergy Associates, Inc.

Arizona

Tempe
E. A. Tel: 480.921.3305

California

Calabasas
I. S. Tel: 818.880.6480
Irvine
I. S. Tel: 714.833.0300
San Diego
E. A. Tel: 619.278.5441

Illinois

Elmhurst
R. A. Tel: 630.516.8400

Indiana

Cicero
R. A. Tel: 317.984.8608
Ligonier
R. A. Tel: 219.894.3184
Plainfield
R. A. Tel: 317.838.0360

Massachusetts

Burlington
SGY Tel: 781.238.0870

Michigan

Byron Center
R. A. Tel: 616.554.1460
Good Rich
R. A. Tel: 810.636.6060
Novi
R. A. Tel: 810.615.4000

North Carolina

Cary
GRP Tel: 919.481.1530

Ohio

Columbus
R. A. Tel: 614.457.2242
Dayton
R. A. Tel: 513.291.4001
Independence
R. A. Tel: 216.447.8825

Pennsylvania

Somerset
R. A. Tel: 814.445.6976

Texas

Austin
ION Tel: 512.794.9006
Arlington
ION Tel: 817.695.8000
Houston
ION Tel: 281.376.2000

Utah

Salt Lake City
E. L. Tel: 801.264.8050

Wisconsin

Muskego
R. A. Tel: 414.679.8250
Saukville
R. A. Tel: 414.268.1152

Sales Offices and Design Resource Centers

LSI Logic Corporation
Corporate Headquarters
Tel: 408.433.8000
Fax: 408.433.8989

NORTH AMERICA

California
Costa Mesa - Mint Technology
Tel: 949.752.6468
Fax: 949.752.6868

Irvine
◆ Tel: 949.809.4600
Fax: 949.809.4444

Pleasanton Design Center
Tel: 925.730.8800
Fax: 925.730.8700

San Diego
Tel: 858.467.6981
Fax: 858.496.0548

Silicon Valley
◆ Tel: 408.433.8000
Fax: 408.954.3353

Wireless Design Center
Tel: 858.350.5560
Fax: 858.350.0171

Colorado
Boulder
◆ Tel: 303.447.3800
Fax: 303.541.0641

Colorado Springs
Tel: 719.533.7000
Fax: 719.533.7020

Fort Collins
Tel: 970.223.5100
Fax: 970.206.5549

Florida
Boca Raton
Tel: 561.989.3236
Fax: 561.989.3237

Georgia
Alpharetta
Tel: 770.753.6146
Fax: 770.753.6147

Illinois
Oakbrook Terrace
Tel: 630.954.2234
Fax: 630.954.2235

Kentucky
Bowling Green
Tel: 270.793.0010
Fax: 270.793.0040

Maryland
Bethesda
Tel: 301.897.5800
Fax: 301.897.8389

Massachusetts
Waltham
◆ Tel: 781.890.0180
Fax: 781.890.6158

Burlington - Mint Technology
Tel: 781.685.3800
Fax: 781.685.3801

Minnesota
Minneapolis
◆ Tel: 612.921.8300
Fax: 612.921.8399

New Jersey
Red Bank
Tel: 732.933.2656
Fax: 732.933.2643

Cherry Hill - Mint Technology
Tel: 609.489.5530
Fax: 609.489.5531

New York
Fairport
Tel: 716.218.0020
Fax: 716.218.9010

North Carolina
Raleigh
Tel: 919.785.4520
Fax: 919.783.8909

Oregon
Beaverton
Tel: 503.645.0589
Fax: 503.645.6612

Texas
Austin
Tel: 512.388.7294
Fax: 512.388.4171

Plano
◆ Tel: 972.244.5000
Fax: 972.244.5001

Houston
Tel: 281.379.7800
Fax: 281.379.7818

Canada
Ontario
Ottawa
◆ Tel: 613.592.1263
Fax: 613.592.3253

INTERNATIONAL

France
Paris
◆ **LSI Logic S.A.**
Immeuble Europa
Tel: 33.1.34.63.13.13
Fax: 33.1.34.63.13.19

Germany
Munich
◆ **LSI Logic GmbH**
Tel: 49.89.4.58.33.0
Fax: 49.89.4.58.33.108

Stuttgart
Tel: 49.711.13.96.90
Fax: 49.711.86.61.428

Italy
Milano
◆ **LSI Logic S.P.A.**
Tel: 39.039.687371
Fax: 39.039.6057867

Japan
Tokyo
◆ **LSI Logic K.K.**
Tel: 81.3.5463.7821
Fax: 81.3.5463.7820

Osaka
◆ Tel: 81.6.947.5281
Fax: 81.6.947.5287

Korea
Seoul
◆ **LSI Logic Corporation of Korea Ltd**
Tel: 82.2.528.3400
Fax: 82.2.528.2250

The Netherlands
Eindhoven
◆ **LSI Logic Europe Ltd**
Tel: 31.40.265.3580
Fax: 31.40.296.2109

Singapore
Singapore
◆ **LSI Logic Pte Ltd**
Tel: 65.334.9061
Fax: 65.334.4749

Tel: 65.835.5040
Fax: 65.732.5047

Sweden
Stockholm
◆ **LSI Logic AB**
Tel: 46.8.444.15.00
Fax: 46.8.750.66.47

Taiwan
Taipei
◆ **LSI Logic Asia, Inc.**
Taiwan Branch
Tel: 886.2.2718.7828
Fax: 886.2.2718.8869

United Kingdom
Bracknell
◆ **LSI Logic Europe Ltd**
Tel: 44.1344.426544
Fax: 44.1344.481039

◆ Sales Offices with
Design Resource Centers

International Distributors

Australia

New South Wales

◆ Reptechnic Pty Ltd

Tel: 612.9953.9844

Fax: 612.9953.9683

Belgium

Acal nv/sa

Tel: 32.2.7205983

Fax: 32.2.7251014

China

Beijing

LSI Logic International Services Inc.

Tel: 86.10.6804.2534

Fax: 86.10.6804.2521

France

Rungis Cedex

Azzurri Technology France

Tel: 33.1.41806310

Fax: 33.1.41730340

Germany

Haar

EBV Elektronik

Tel: 49.89.4600980

Fax: 49.89.46009840

Munich

Avnet Emg GmbH

Tel: 49.89.45110102

Fax: 49.89.42.27.75

Wuennenberg-Haaren

Peacock AG

Tel: 49.2957.79.1692

Fax: 49.2957.79.9341

Hong Kong

Hong Kong

AVT Industrial Ltd

Tel: 852.2428.0008

Fax: 852.2401.2105

EastEle

Tel: 852.2798.8860

Fax: 852.2305.0640

India

Bangalore

Spike Technologies India Private Ltd

◆ Tel: 91.80.664.5530

Fax: 91.80.664.9748

Israel

Tel Aviv

Eastronics Ltd

Tel: 972.3.6458777

Fax: 972.3.6458666

Japan

Tokyo

Global Electronics Corporation

Tel: 81.3.3260.1411

Fax: 81.3.3260.7100

Technical Center

Tel: 81.471.43.8200

Yokohama-City

Macnica Corporation

Tel: 81.45.939.6140

Fax: 81.45.939.6141

The Netherlands

Eindhoven

Acal Nederland b.v.

Tel: 31.40.2.502602

Fax: 31.40.2.510255

Switzerland

Brugg

LSI Logic Sulzer AG

Tel: 41.32.3743232

Fax: 41.32.3743233

Taiwan

Taipei

Avnet-Mercuries Corporation, Ltd

Tel: 886.2.2516.7303

Fax: 886.2.2505.7391

Lumax International Corporation, Ltd

Tel: 886.2.2788.3656

Fax: 886.2.2788.3568

Prospect Technology Corporation, Ltd

Tel: 886.2.2721.9533

Fax: 886.2.2773.3756

Serial Semiconductor Corporation, Ltd

Tel: 886.2.2579.5858

Fax: 886.2.2570.3123

United Kingdom

Maidenhead

Azzurri Technology Ltd

Tel: 44.1628.826826

Fax: 44.1628.829730

Swindon

EBV Elektronik

Tel: 44.1793.849933

Fax: 44.1793.859555

◆ Sales Offices with
Design Resource Centers

