Technical Manual

LSIFC919 Single Channel Fibre Channel I/O Processor

Revision 2.0

October 2001

LSI LOGIC®

DB15-000151-01

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This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

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Preface

This book is the primary reference and technical manual for the LSIFC919 Fibre Channel I/O Processor. It contains a complete functional description for the LSIFC919 and includes complete physical and electrical specifications for the product.

Audience

This document was prepared for logic designers and applications engineers and is intended to provide an overview of the LSI Logic LSIFC919 and to explain how to use the LSIFC919 in the initial stages of system design.

This document assumes that you have some familiarity with microprocessors and related support devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the LSIFC919 for possible use in a system
- Engineers who are designing the LSIFC919 into a system

Organization

This document has the following chapters and appendixes:

- Chapter 1, **Introduction**, provides a general description of the LSIFC919.
- Chapter 2, **Fibre Channel Overview**, briefly describes some key elements of Fibre Channel, including Layers, Topologies, and Classes of Service.

- Chapter 3, **LSIFC919 Overview**, provides an introduction to the basic features of the LSIFC919, including the host interface, protocol assist engines, and support components.
- Chapter 4, **Signal Descriptions**, lists and describes the signals on the LSIFC919.
- Chapter 5, **Register Descriptions**, briefly describes the PCI address space, the Configuration Registers, and the Host Interface Registers.
- Chapter 6, **Specifications**, describes the electrical specifications of the LSIFC919, and provides pinout information and packaging dimensions.
- Appendix A, **Register Summary**, is a register summary.
- Appendix B, **Reference Specifications**, lists several specifications and applicable World Wide Web URLs that may be of benefit to the reader.
- Appendix C, **Glossary of Terms and Abbreviations**, is a glossary of terms and abbreviations.

Related Publications

Fusion-MPT™ Message Passing Interface Specification, Number DB14-000174-00

Conventions Used in This Manual

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive. Signals that are active LOW end in an "/."

Hexadecimal numbers are indicated by the prefix "0x" —for example, 0x32CF. Binary numbers are indicated by the prefix "0b" —for example, 0b0011.0010.1100.1111.

Revision Record

Revision	Date	Remarks
0.3	04/2000	First Advance Information printing.
2.0	09/2001	Release of Final Manual. Changes: Deleted Section 1.7. Table 4.2 - RTRIM description changed. Table 4.2 - RXLOS description changed. Table 4.4 - Test Modes removed from MODE[7:0] description. Section 5.3.2 - Note reworded. Page 5-14, Register 0x00C - Cache Line Size description modified. Page 5-31, Register 0x040 - Changed this register from Read/Write to Write Only. Table 6.1 - Changed ESD maximum spec to 1.5 kV. Tables 6.4 through 6.10 - Added signal names to appropriate DC tables. Section 6.2.2 - Referred user to the Fibre Channel Physical Interfaces specification (FC-PI, Rev. 11) for Fibre Channel Interface Timings. Figure 4.1 and Tables 4.1 and 4.2 have been moved to the end of Chapter 6, making the layout of this Manual consistent with our current guidelines. They are now Figure 6.16 and Tables 6.16 and 6.17 Table 4.1 - new signals are added to the device, incorporating hot swap capabilities. They are also added to Figure 6.16 and Tables 6.16 and 6.17. Appendix B, Table 6.8 - Updated the list of Reference Specifications.

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Chapter 1
Introduction

This chapter provides general overview information on the LSIFC919 Single Channel Fibre Channel I/O Processor chip. The chapter contains the following sections:

- Section 1.1, “Overview”
- Section 1.2, “General Description”
- Section 1.3, “Hardware Overview”
- Section 1.4, “Initiator Operations”
- Section 1.5, “Target Operations”
- Section 1.6, “Diagnostics”

1.1 Overview

The LSIFC919 is a high-performance, cost effective Single Channel Fibre Channel (FC) I/O Processor. It represents the very latest system level integration technology in intelligent I/O processors from LSI Logic. The Storage Area Network (SAN) environment is fully supported with both Fibre Channel Protocol for SCSI (FCP) and LAN/IP.

1.1.1 Hardware Features

The LSIFC919 supports these hardware features:

- Highly integrated full duplex Single Channel Fibre Channel I/O Processor
- Integrated 2 Gbit/s Single Channel FC serial link
- 64-bit/66 MHz host PCI bus (backward compatible with 32-bit/33 MHz)

- Integrated BER link testing
- 32-bit ARM RISC processor
- Intelligent high-performance context management
- Synchronous SRAM external memory interface
- Full simultaneous target and initiator operations
- Implements common Message Passing Interface (MPI)
- Load Balancing
- Up to 2000 concurrent host commands
- PC01 compliant
- PCI 2.2 compliant
- JTAG debug interface
- 329-pin BGA

1.1.2 FC Features

The LSIFC919 supports these Fibre Channel features:

- Class 2 support and Class 3 support (with optional confirmed delivery)
- BB credit of 3, alternate login of 1
- FC-PH compliance
- FC-AL 7.0 compliance
- FC-FCP, FC-PLDA compliance
- FC-FLA compliance
- FCA-IP, IETF-IPFC compliance
- NL_Port (NL_Port Attach)
- FL_Port (Public Loop Attach)
- F_Port (Fabric Attach)
- N-Port (Point-to-Point)
- Autonegotiate between 1 Gbit/s and 2 Gbit/s link speeds under firmware control for easy updating

1.1.3 Software Features

The LSIFC919 supports these software features:

- Fusion-MPT™ drivers
- Optimum server I/O profile with low CPU utilization
- Optimum workstation I/O profile with maximum I/O performance
- Remote diagnostic capability
- OS drivers support fail over and load balancing
- SAN storage management

1.1.4 OS Support

The LSIFC919 supports these operating systems:

- Windows 2000
- Windows NT 4.0 SP4 and NT 5.0
- Windows XP
- NetWare 4.11 and 5.0
- UnixWare 2.12 and Gemini
- Solaris 2.6, 2.7 – X86
- Linux

1.1.5 Targeted Applications

The LSIFC919 supports specific applications:

- SANs
- Server clustering environments
- Embedded RAID
- Low cost PCI/FC host adapters
- Host main boards
- Routers and bridges

1.2 General Description

The LSI Logic LSIFC919 Single Channel Fibre Channel I/O Processor is a high-performance, Intelligent I/O Processor (IOP) designed to simultaneously support mass storage and IP protocols on a full duplex 2 GBaud FC Link. The sophisticated design and local memory architecture work together to reduce the host CPU and PCI bandwidth required to support FC I/O operations.

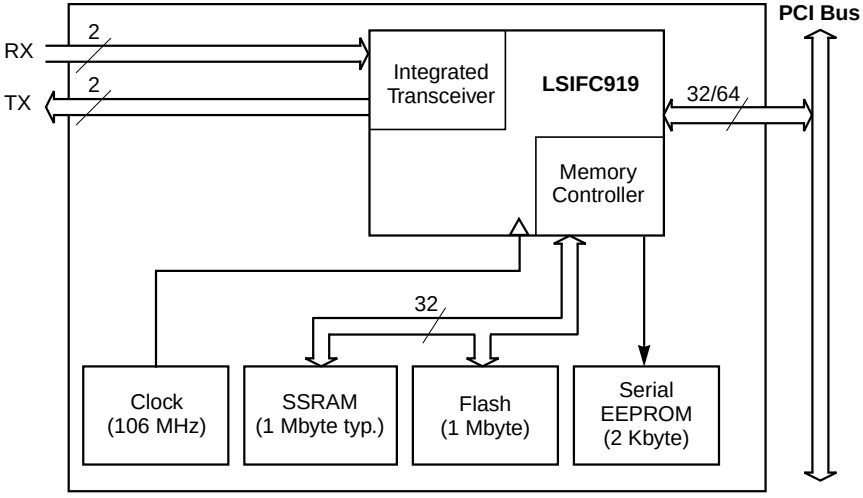
From the host CPU perspective, the LSIFC919 manages the FC Link at the exchange level for mass storage (FCP) protocols. The LSIFC919 supports multiple I/O requests per host interrupt in most applications.

From the FC Link perspective, the LSIFC919 is a highly efficient NL_Port supporting point-to-point, and public and private loop topologies, as well as the FC switch/attach topology defined under the ANSI X3T11 FC-PH standard. The LSIFC919 contains sufficient hardware support to perform both Class 3 and Class 2 levels of service. The LSIFC919 is uniquely designed to support FC environments where independent, full duplex transmission is required for maximum FC Link efficiency. Special attention has been given to the design to accelerate context switching and Link utilization.

The LSIFC919 includes a 64-bit, 66 MHz PCI interface to the host environment. The host interface is designed to minimize the amount of time spent on the PCI bus for nondata moving activities such as initialization, command and error recovery. In addition, the host interface has inherent flexibility to support the OEM's implementation trade-offs between CPU, PCI, and I/O bandwidth.

The high level of integration in the LSIFC919 controller enables low cost FC implementations. Figure 1.1 shows a typical configuration incorporating the LSIFC919 controller to implement a FC NL_Port.

Figure 1.1 LSIFC919 Typical Implementation



1.2.1 Multifunction PCI

The LSIFC919 provides multifunction capability on the PCI bus. This capability allows the host to see two distinct logical devices. Each function can be programmed to be a different I/O protocol. For example, Function[0] can be designated as the storage controller running the FCP protocol and Function[1] could be designated as the network controller running the IP protocol.

1.2.2 Simple Autospeed Negotiation Algorithm

Backward compatibility with 1 Gbit/s FC devices are maintained through the use of the “Simple Autospeed Negotiation Algorithm.” After a power-on, loss of signal, or loss of word synchronization for longer than the R_T_TOV timeout, the LSIFC919 will perform this operation to determine whether a point-to-point device or all of the devices on a loop are either 1 Gbit/s or 2 Gbit/s devices.

1.3 Hardware Overview

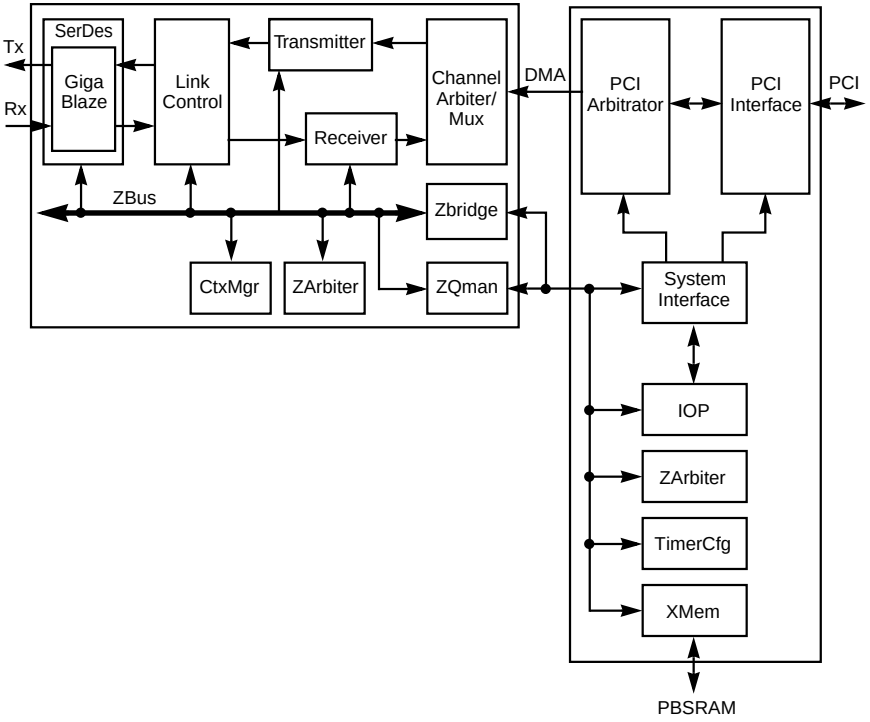
With today's fast growing RAID server environments along with workstation marketplaces, higher levels of performance, scalability and reliability are required to stay competitive in the SAN market.

The LSIFC919 provides the performance and flexibility to meet tomorrow's FC connectivity requirements.

The LSIFC919 and the LSI Logic software drivers provide superior performance and lower host CPU overhead than other competitive solutions. Due to its high level of integration and streamlined architecture, the LSIFC919 provides the highest level of performance in a more cost effective FC solution.

Figure 1.2 illustrates the functional block diagram for the LSIFC919. The architecture maximizes performance and flexibility by deploying fixed gates in critical performance areas and utilizing multiple ARM RISC processors. One processor is for context management and the additional one is for the I/O Processor. Each of the major blocks is briefly described below.

Figure 1.2 LSIFC919 Block Diagram



1.3.1 PCI Interface

The LSIFC919 uses a 64-bit (33 MHz or 64 MHz) PCI interface or a 32-bit (33 MHz or 64 MHz) PCI interface. In addition, support is provided for Dual Address Cycle (DAC), PCI power management, Subsystem Vendor ID and Vendor Product Data (VPD). Extended access cycles (MRL, MRM, MWI) are also supported.

1.3.2 32-Bit Memory Controller

The memory controller provides access to Flash ROM and 32-bit synchronous SRAM. It supports both interleaved and noninterleaved configurations up to a maximum of 4 Mbytes of synchronous SRAM. A general purpose memory expansion bus supports up to 1 Mbyte of Flash ROM.

1.3.3 I/O Processor

The LSIFC919 uses a 32-bit ARM RISC processor to control all system interface and message transport functionality. This frees the host CPU for other processing activity and improves overall I/O performance. The RISC processor and associated firmware have the ability to manage an I/O from start to finish without host intervention. The RISC processor also manages the message passing interface.

1.3.4 System Interface

The system interface efficiently passes messages between the LSIFC919 and other I/O agents. It consists of four hardware FIFOs for the message queuing lists: Request Free, Request Post, Reply Free, and Reply Post. The LSIFC919 system interface provides control logic for the FIFOs with messages stored in external memory.

1.3.5 Integrated 2 Gbit/s Transceivers

The LSIFC919 implements LSI Logic's GigaBlaze® 2 Gbit/s integrated transceivers. GigaBlaze is backward compatible with 1 Gbit/s systems, using a firmware-implemented "Simple Autospeed Negotiation Algorithm" for easy updates. The integrated 2 Gbit/s transceivers provide an FC compliant physical interface for cost conscience and real estate limited applications.

1.3.6 Link Controllers

The integrated link controller is FC-AL-2 (Rev. 7.0) compatible and performs all link operations. The controller monitors the Link State and strictly adheres to the Loop Port State Machine ensuring maximum system interoperability. The link control interfaces to the integrated transceiver.

1.3.7 Transmitter

The transmitter builds sequences based on context information and transmits resulting frames to the FC link using the Link Controller. The transmitter includes two 2 Kbyte buffers to support frame payloads.

1.3.8 Receiver

The receiver accepts frame data from the Link Controller and DMAs the encapsulated information to local or system memory. The receiver contains three 2 Kbyte buffers which support a BB-Credit of up to three or an Alternate Login BB-Credit of 1.

1.3.9 Context Managers

The LSIFC919 uses an ARM RISC processor to support I/O context swap to external memory and FCP management for both Initiator and Target applications. Context operations include support for transmit and resource queue management as well as scatter/gather list management.

1.4 Initiator Operations

The LSIFC919 autonomously handles FCP exchanges upon request from the host. The LSIFC919 generates appropriated sequences and frames necessary to complete the request and provides feedback to the host on the status of the request.

1.5 Target Operations

The LSIFC919 provides for general purpose target functions such as those required for front-end RAID applications.

1.6 Diagnostics

The LSIFC919 provides the capabilities to do a simplified “Link Check” Bit Error Rate (BER) test on the link for diagnostic purposes. In a special test mode, the controller can transmit and verify a programmed data pattern for link evaluation.

Chapter 2
Fibre Channel Overview

This chapter provides general overview information on Fibre Channel (FC). The chapter contains the following sections:

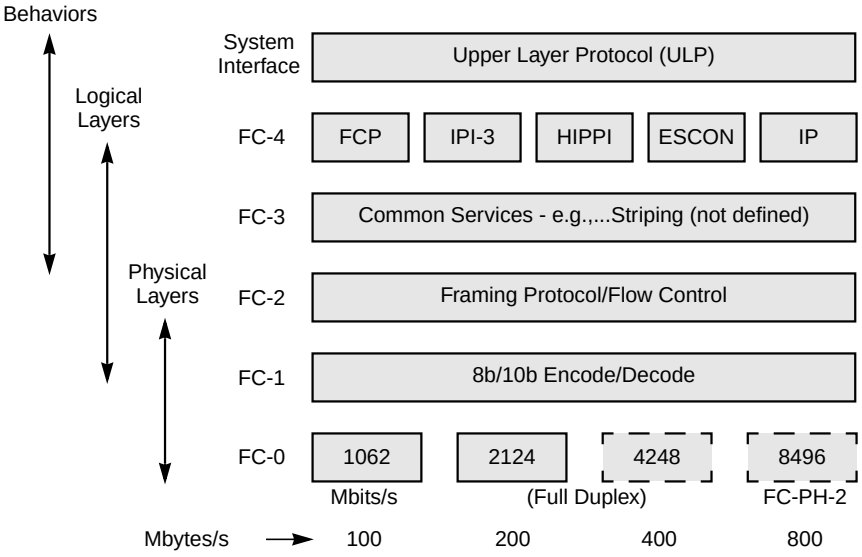
- Section 2.1, “Introduction”
- Section 2.2, “FC Layers”
- Section 2.3, “Frames”
- Section 2.4, “Exchanges”
- Section 2.5, “FC Ports”
- Section 2.6, “FC Topologies”
- Section 2.7, “Classes of Service”

2.1 Introduction

FC is a high-performance, hybrid interface. It is both a channel and a network interface that contains network features to provide the required connectivity, distance, and protocol multiplexing. It also provides traditional channel features to retain the required simplicity, repeatable performance, and guaranteed delivery. Popular industry standard networking protocols such as Internet Protocol (IP) and channel protocols such as Small Computer System Interface (SCSI) have been mapped to the FC standard.

Five functional layers define the FC structure. Figure 2.1 shows these layers, which define the physical media and transmission rates, encoding scheme, framing protocol and flow control, common services, and the Upper Level Protocol (ULP) interfaces.

Figure 2.1 FC Layers



2.2 FC Layers

The lowest layer, FC-0, is the media interface layer. It defines the physical characteristics of the interface. It includes transceivers, copper-to-optical transducers, connectors, and any other associated circuitry necessary to transmit or receive at 1062 or greater Mbit/s rates over copper or optical cable.

The FC-1 layer defines the 8b/10b encoding/decoding scheme, the transmission protocol necessary to integrate the data and transmit clock, and the receive clock recovery. Implementation of this layer is usually divided between the hardware implementing the FC-0 layer in a transceiver, and the protocol device which implements the FC-2 layer. Specifically, the FC-0 transceivers can include the clock recovery circuitry while the 8b/10b encoding/decoding is provided in the protocol device.

The FC-2 layer defines the rules for the signaling protocol and describes transfer of the Frames, Sequences, and Exchanges. The meaning of the data being transmitted or received is transparent to the FC-2 layer. However, the context between any given set of frames is maintained at

the FC-2 layer through the Sequence and Exchange constructs. The framing protocol creates the constructs necessary to form frames with the data being packetized within each frame's payload.

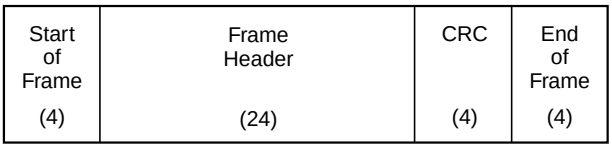
The FC-3 layer provides common services that span multiple N_Ports (see Section 2.5, "FC Ports," page 2-7). Some of these services include Striping, Hunt Groups, and Multicasting. All of these services allow a single port or fabric to communicate to several N_Ports at one time.

The FC-4 layer provides a seamless integration of existing standards. It specifies the mapping of Upper Layer Protocols (ULPs) to the layers below. Some of these ULPs include SCSI and IP. Each of these ULPs is defined in its own ANSI document.

2.3 Frames

Two types of frames are used in FC: Link Control frames and Data frames. Link Control frames contain no payload and are flow control responses to Data frames. An example of a Link Control frame is the ACK frame.

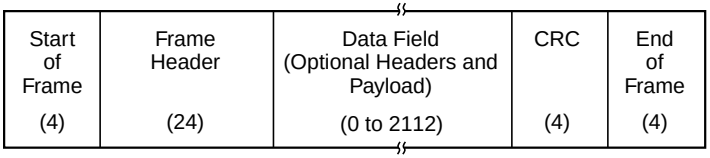
Figure 2.2 Link Control Frame



( ) = Number of Bytes

A Data frame is any frame which contains data in the payload field. An example of a Data frame is the LOGIN frame.

Figure 2.3 Data Frame



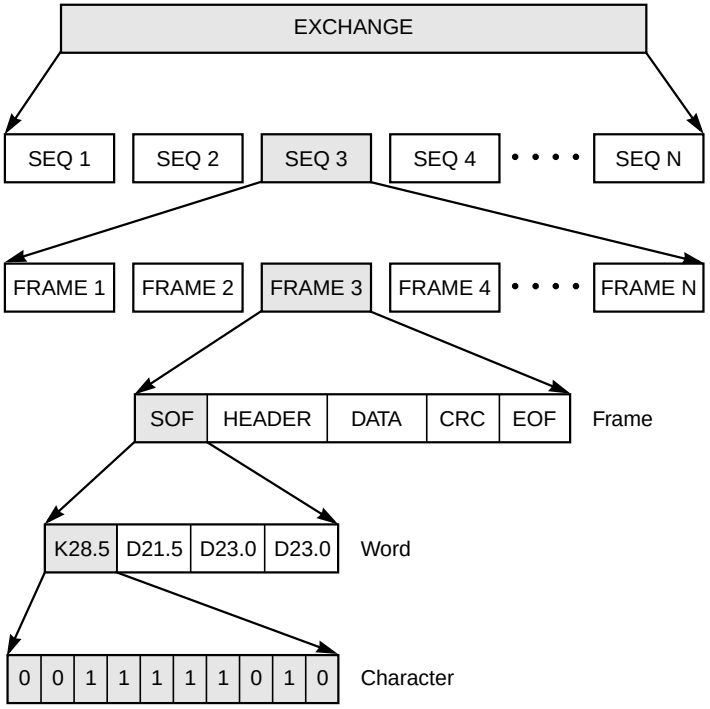
( ) = Number of Bytes

In FC, an Ordered Set is a group of four 10-bit characters that provide low level Link functions, such as frame demarcation and signaling between two ends of a Link. All frames start with a Start-of-Frame (SOF) and end with an End-of-Frame (EOF) Ordered Set. Each frame contains at least a 24-byte header defining such things as Destination and Source ID, Class of Service and type of frame (e.g., FCP or FC-LE). The biggest field within a frame can be the payload field. If the frame is a Link Control frame, then there is no payload. If it is a Data frame, then the frame will contain a Payload field of up to 2112 bytes. Finally, the frame includes a Cyclic Redundancy Check (CRC) field used for detection of transmission errors, followed by the EOF Ordered Set.

2.4 Exchanges

Figure 2.4 illustrates the FC hierarchical data structures. At the most elemental level, four 8b/10b encoded characters make up an FC Word. An FC Frame is a collection of FC words. An FC Sequence is made up of one or more frames, and an FC Exchange is made up of one or more sequences.

Figure 2.4 Exchange to Character



The following discussion illustrates an Exchange by considering a typical parallel SCSI I/O. In parallel SCSI, there are several phases that make up the I/O. These phases include Command, Data, Message, and Status phases.

Using the FCP for the SCSI ULP, these phases can be mapped into the other lower FC layers. Figure 2.5 shows the components that make up the FCP exchange.

Figure 2.5 FCP Exchange

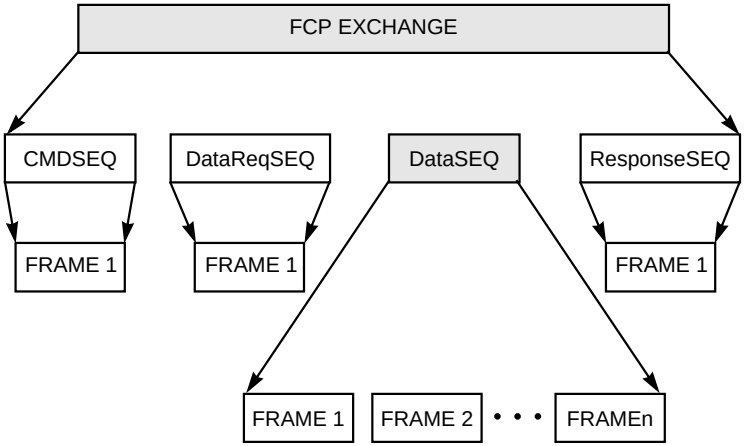
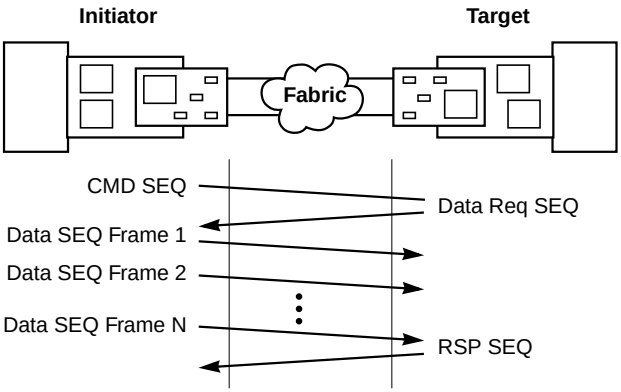


Figure 2.6 illustrates how the Exchange flows between the Initiator and Target. The Initiator starts the FCP Exchange by sending a Command Sequence containing one frame to the Target. The Frame's payload contains the Command Descriptor Block (CDB). The Target responds with a Data Delivery Request Sequence containing one Frame. The payload of this Frame contains a XFER_RDY response. Once the Initiator receives the Target's response, it will begin sending the Data Sequence(s), which may contain one or more Frames. This is analogous to parallel SCSI's DATA_OUT phase. When the Target has received the last Frame of the Data Sequence(s), it will send a Response Sequence containing one Frame to the Initiator, thus concluding the FCP Exchange.

Figure 2.6 Write Event Trellis



2.5 FC Ports

FC devices are called nodes. Each node has at least one port to provide access to other ports in other nodes. The “port” is the hardware entity within a node that performs data communications over the FC Link.

The FC standard defines various types of ports, based on the location of the port and the topology associated with it. The most commonly used ports are N_Ports, NL_Ports, F_Ports, and FL_Ports. These types of ports appear in Figure 2.7, Figure 2.8, and Figure 2.9.

2.6 FC Topologies

The capability and the presence or absence of Fabric between the N_Ports defines all FC topologies. A discussion follows about these FC topologies:

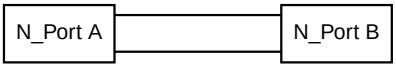
- Point-to-Point topology
- Fabric topology
- Arbitrated Loop topology

FC-PH protocols are topology independent. Attributes of a Fabric may restrict operation to certain communication models.

2.6.1 Point-to-Point Topology

Figure 2.7 illustrates how the point-to-point topology communication occurs between N_Ports without the use of Fabric.

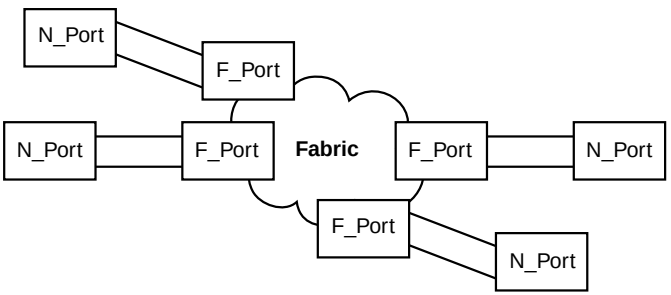
Figure 2.7 Point-to-Point Topology



2.6.2 Fabric Topology

Figure 2.8 illustrates multiple N_Ports interconnected by a Fabric. This topology uses the Destination_Identifier (D_ID) embedded in the Frame Header to route the Frame through a Fabric to the desired Destination N_Port.

Figure 2.8 Fabric Topology

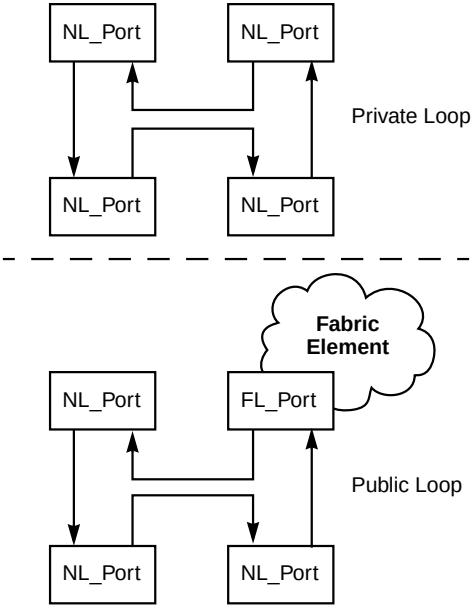


2.6.3 Arbitrated Loop Topology

The Arbitrated Loop topology permits 2 to 127 L_Ports to communicate without the use of a Fabric, as in Fabric topology. The arbitrated loop supports a maximum of one point-to-point circuit at a time. When two L_Ports are communicating, the arbitrated loop topology supports simultaneous, symmetrical bidirectional flow.

Figure 2.9 illustrates two independent arbitrated loop configurations, each with multiple L_Ports attached. Each line in the figure between L_Ports represents a single fibre. The lower configuration shows an Arbitrated Loop composed of three NL_Ports and one FL_Port (a Public Loop).

Figure 2.9 Arbitrated Loop Topology



2.7 Classes of Service

FC provides several classes of service. The different classes are distinguished from each other in three ways: by the level of guarantee for data being delivered, the order in which data is delivered, and how data flow control is maintained.

Class 1 is a dedicated connection between two N_Ports. The data delivered is guaranteed with a required acknowledgement frame (ACK), which a Class 1 device uses for flow control. All frames are received in order.

Class 2 is a connectionless class. The data delivered is guaranteed with an ACK frame. The frames can be received out of order. Class 2 uses both ACK frames and the R_RDY Ordered Set for flow control.

Class 3 is also a connectionless class (the data being delivered is not guaranteed). The frames can be received out of order. Class 3 uses only the R_RDY Ordered Set for flow control.

Intermix is an enhancement of Class 1 service. A dedicated Class 1 connection may waste fabric bandwidth while frames are not being transmitted or received between two N_Ports. In order to recover some of this bandwidth, Intermix allows Class 2 and Class 3 frames to be transmitted/received between Class 1 frames. N_Ports advertising Intermix capability must be capable of receiving Class 2 and Class 3 frames from other N_Ports while maintaining the original Class 1 Link.

Chapter 3
LSIFC919 Overview

This chapter provides a general description of the LSIFC919 Fibre Channel PCI Protocol Controller firmware. The chapter contains the following sections:

- Section 3.1, “Introduction”
- Section 3.2, “Message Interface”
- Section 3.3, “SCSI Message Class”
- Section 3.4, “LAN Message Class”
- Section 3.5, “Target Message Class”
- Section 3.6, “Support Components”

3.1 Introduction

The LSI Logic LSIFC919 connects a host to a high speed Fibre Channel (FC) Link. The FCP ANSI standard, FC Private Loop Direct Attach, and Fabric Loop Attach profiles are supported with the use of a sophisticated firmware implementation. Refer to Appendix B, “Reference Specifications” for profiles, specifications, and interoperability lists maintained by the LSIFC919.

Although optimized for a 64-bit PCI interface to communicate with the system CPU(s) and memory, the LSIFC919 also supports a 32-bit PCI environment. The system interface to the LSIFC919 is designed to minimize the amount of PCI bandwidth required to support I/O requests. A packetized message passing interface reduces the number of single cycle PCI bus cycles. All FC Data traffic on the PCI bus occurs with zero wait state bursts across the PCI bus.

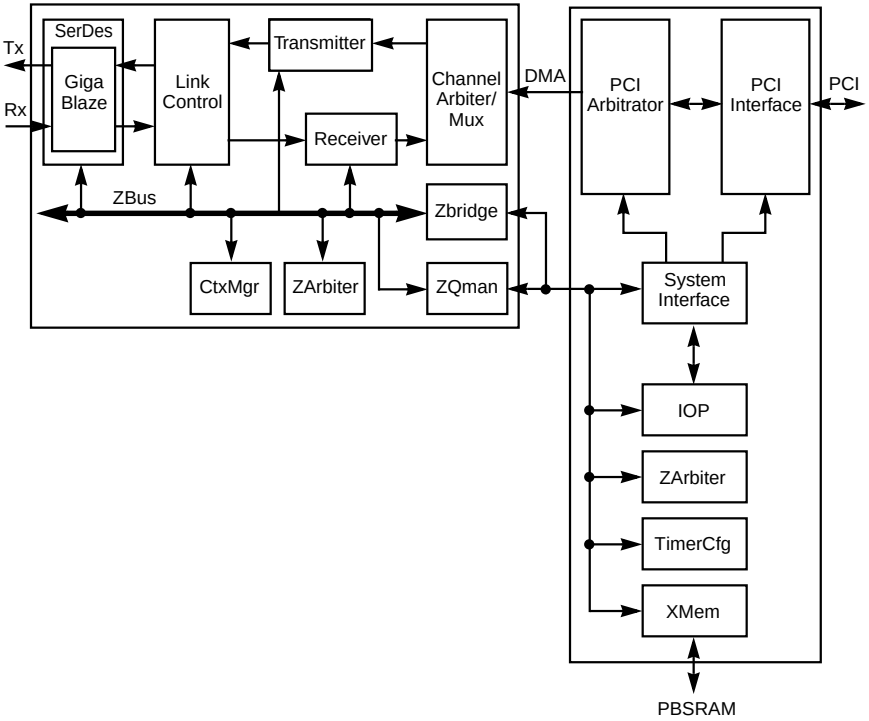
The intelligent LSIFC919 architecture allows the system to specify I/Os at the command level. The LSIFC919 manages I/Os at the Frame,

Sequence, and Exchange levels. The LSIFC919 also handles error detections and I/O retries, which allow the system to offload part of the exception handling work from the system driver.

3.1.1 Data Flows

The LSIFC919 uses a 64-bit (33 MHz or 66 MHz) PCI interface to pass control and data information between the system and the protocol controller. Figure 3.1 illustrates how the PCI Interface block manages this interface. It is backward compatible with 32-bit/33 or 66 MHz buses.

Figure 3.1 LSIFC919 Block Diagram



For incoming serial data, the physical Link transfers the data to Link Control using the GigaBlaze Integrated Transceiver. The Link Controller analyzes the received frame and if appropriate, it passes the frame to the Receiver. The Receiver strips off the frame header and places it in a separate header buffer while the data in the frame payload is placed in a data buffer. The Frame Receiver uses the Receive Context Manager to manage the received frame's order and priority. The data contained in

the Receiver buffers are associated with a specific scatter/gather entry and passed on to the PCI Interface and it requests the PCI bus and bursts the data into system memory.

The I/O Processor, with its firmware, provides the translation from FC specific protocols to the high level Block Storage, SCSI, and LAN message interface. This translation allows the LSIFC919 to be integrated into the system as if it were a native Parallel SCSI or LAN device, hiding all FC unique characteristics. Internal communication between the I/O Processor and the Context manager occurs over an internal bus, which is also connected to an External Memory Controller. The I/O Processor uses the External Memory Controller to access local memory. This memory contains the firmware, as well as the dynamic data structures used by the firmware.

3.2 Message Interface

The LSIFC919 system interface is a high-performance, packetized, mailbox architecture that leverages the intelligence in the LSIFC919 to minimize traffic on the PCI bus.

The Message Interface provides two basic constructs. The Message is the first construct, which communicates between the system and the LSIFC919. Messages are moved between the system(s) and the LSIFC919 using the second construct, a Transport mechanism.

3.2.1 Messages

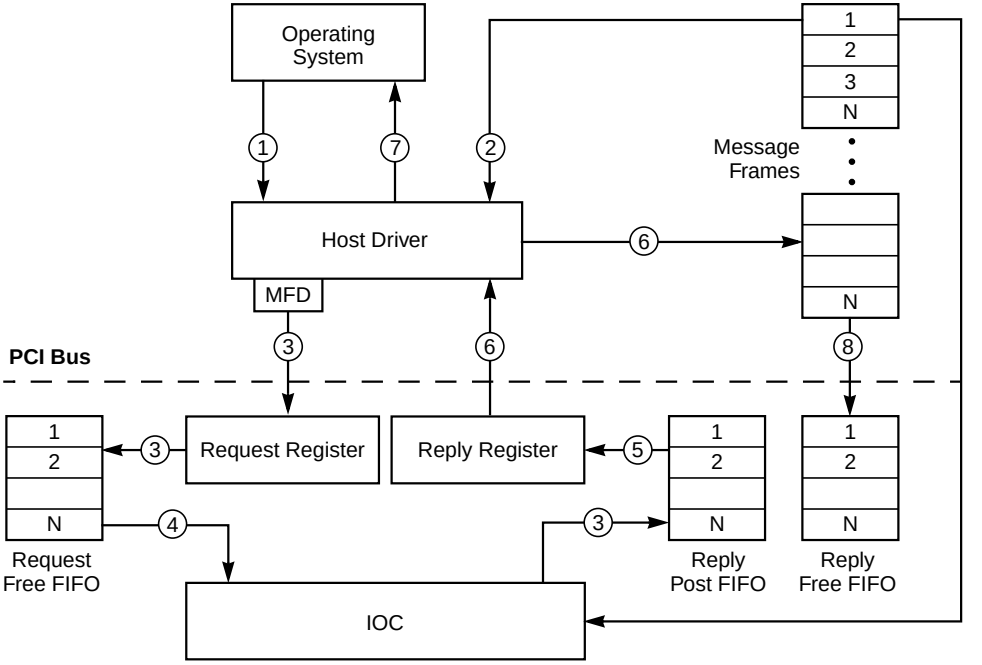
The LSIFC919 uses Request and Reply messages to communicate with the system. The system initiates all request messages, which ask for a specific action by the LSIFC919. To send status information back to the system, the LSIFC919 uses reply messages. Request message data structures are up to 128 bytes in length. The message includes a message header and a payload. The header includes information to uniquely identify the message. The payload is specific to the request itself, and is unique for Block Storage, SCSI, LAN, and Target messages. For more information regarding the details of the message format, refer to the LSIFC919 Programming Model.

3.2.2 Message Flow

Before posting requests to the LSIFC919, the system must allocate and initialize a pool of message frames, and provide a mechanism to assign individual message frames on a per-request basis. The host must also provide one message frame per target LUN and prime the Reply Free FIFOs for each function with the physical address of these message frames. Once allocation has been completed, requests will flow from the host to the LSIFC919. Figure 3.2 illustrates how a message flow occurs in a system.

1. The host driver receives an I/O request from the operating system.
2. The host driver allocates a system message frame and builds an I/O request message within the SMF. The allocation method is the responsibility of the host driver.
3. The host driver creates the Message Frame Descriptor (MFD) and writes the MFD to the Request Post FIFO.
4. The IOC reads the MFD from the Request Post FIFO and DMAs the request to a local message frame.
5. The IOC sends the appropriate Fibre Channel request, and subsequently receives the reply from the target.
   - If the I/O status was successful, the IOC writes the MessageContext value, plus turbo reply bits, to the Reply Post FIFO, which automatically generates a system interrupt.
   - If the I/O status was not successful, the IOC pops a reply message frame from the Reply Free FIFO, and generates a reply message in the reply message frame. The IOC then writes the system physical address of the reply message frame to the Reply Post FIFO, which generates a system interrupt.
6. The host driver receives an interrupt and reads the Reply Register. If no posted messages exists, the system reads the value 0xFFFFFFFF.
7. The host driver responds to the Operating System appropriately.
8. The host driver returns it to the Reply Free FIFO if the I/O status was not successful.

Figure 3.2 LSIFC919 Message Flow



3.3 SCSI Message Class

The SCSI message interface provides the most direct interface for block-oriented storage media. This includes disk drives and tape devices.

The SCSI I/O path translates a SCSI CDB into an FCP exchange. The LSIFC919 completely manages all FC device and target discovery operations. The LSIFC919 assigns a logical (bus, target ID) identifier to FC target devices, and the system accesses these devices as if they were parallel SCSI devices. The system is responsible for scanning the target devices, and identifying LUNs on the target devices.

In general, the system is responsible for retrying operations at an I/O request level. The LSIFC919 is responsible for responding to bus protocol-specific errors and exceptions and retrying bus sequences within the scope of an I/O operation. The system is also responsible for maintaining a timer for SCSI I/O operations if this is required by the host system. The host driver may use the provided SCSI Task Management functions to terminate one or more I/O operations when a timeout occurs.

For more information regarding the SCSI Message Class, refer to the LSIFC919 Programming Model.

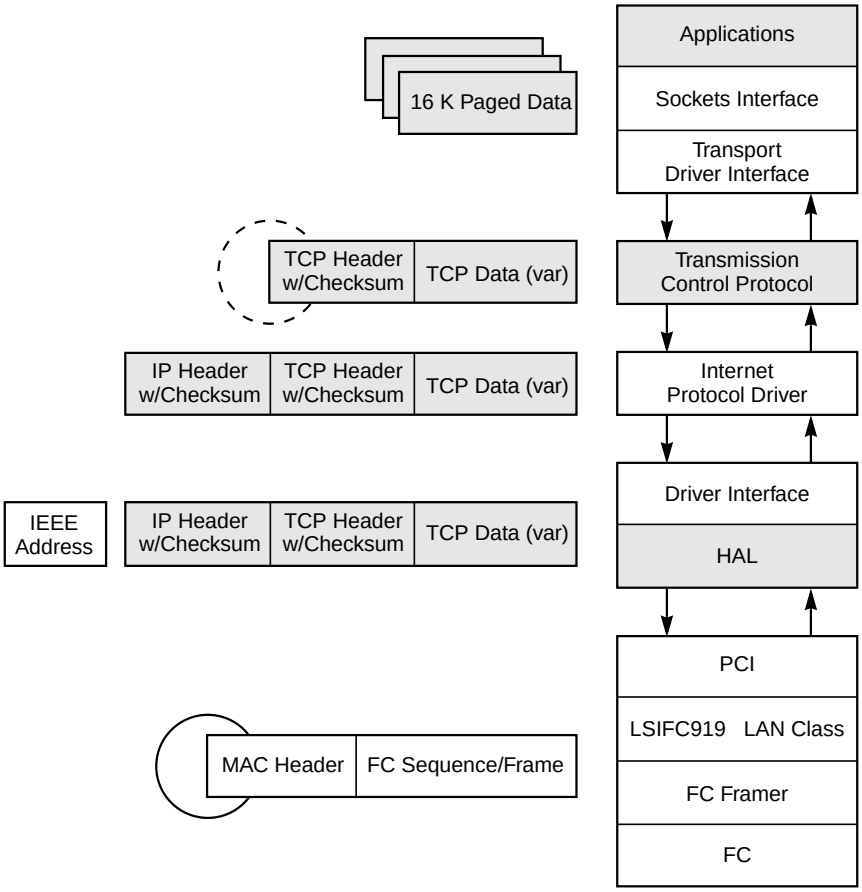
3.4 LAN Message Class

The LSIFC919 provides a LAN message interface that supports the system TCP or UDP network driver stack, providing MAC level communication between FC ports.

The typical network driver stack in the system consists of a Socket Driver with a Transport Driver Interface, supported by TCP or UDP and IP drivers, and a Hardware Abstraction layer interface to the LSIFC919. The TCP driver provides data buffer segmentation. The IP driver provides MTU segmentation, adds a header and checksum to the TCP data, and maps each Fibre Channel MAC port address to an IEEE standard address. The TCP driver requires ACKs to ensure all segments of the data block are transmitted/received.

The LAN message interface may also be used by proprietary protocol stacks in the host. Figure 3.3 provides an example of a LAN Protocol Stack. In this environment, the LSIFC919 transmits and receives data between FC nodes, without regard to data content. For more information regarding the LAN Message Class, refer to the LSIFC919 Programming Model.

Figure 3.3 LAN Protocol Stack



3.5 Target Message Class

The Target interface allows the LSIFC919 to be used as the system interface for FC bridge controllers. The LSIFC919 provides an FCP exchange level message interface that routes commands to the system. The system identifies the appropriate data, and passes a Scatter Gather List (SGL) to the LSIFC919 describing the data to transfer. A single Target message directs the LSIFC919 to send a Xfer_Rdy, as needed, and to transfer data and FCP response. The system manages Target

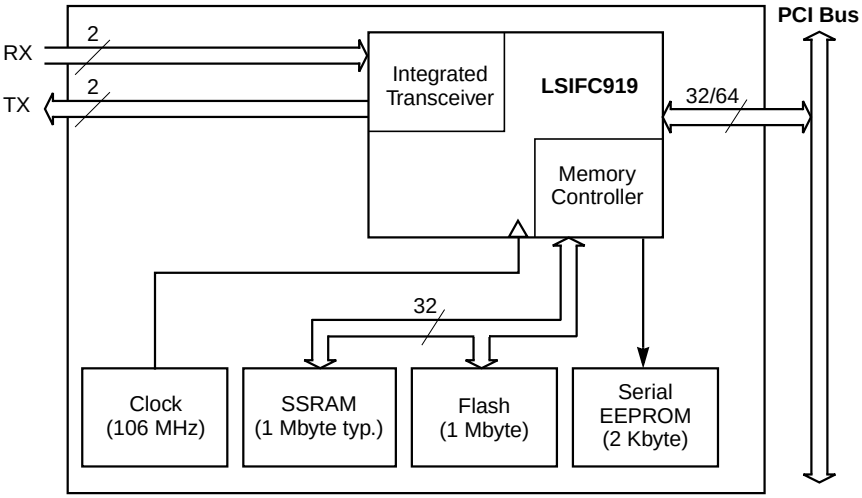
specific Process Login/Logout actions. For more information regarding the Target Message Class, refer to the LSIFC919 Programming Model.

3.6 Support Components

The memory controller block within the LSIFC919 provides access to external local memory resources required to manage FCP.

The following sections provide guidance in choosing the support components necessary for a fully functional implementation using the LSIFC919. Figure 3.4 illustrates a diagram that shows a typical implementation of the LSIFC919.

Figure 3.4 LSIFC919 Typical Implementation



3.6.1 SSRAM Memory

The primary function of this memory is to store data structures used by the LSIFC919 to manage exchanges and transmit and receive queues. The SSRAM memory also stores part of the run time image of the LSIFC919 firmware, such as initialization and error recovery code. The mainline code is stored within the internal LRAM for performance reasons.

The LSIFC919 uses a 32-bit nonmultiplexed memory bus to access the SSRAM. This memory bus has the capability to address up to 4 Mbytes of SSRAM.

The LSIFC919 firmware also supports optional byte wide parity error detection. This option is configurable and is specified as a serial EEPROM parameter.

The amount of SSRAM (1 Mbyte) determines the maximum number of outstanding Request Messages (1024). This roughly equates to the maximum number of outstanding I/O requests pending in the LSIFC919.

3.6.2 Flash ROM

The memory controller in the LSIFC919 also manages an optional Flash ROM. If present, the Flash ROM will store the firmware for the LSIFC919 I/O Processor, and if desired, the INT13h boot software.

If the Flash ROM is not used, then the host platform is responsible for downloading the I/O Processor firmware to the LSIFC919 through the PCI interface. The LSIFC919 supports a diagnostic interface, enabled through a sequence of commands issued to the PCI configuration space. Firmware may be directly written to the LSIFC919 internal memory and external SSRAM through the diagnostic interface. Details of this implementation are available in the LSI Logic LSIFC919 Programming Model. Flash ROM is needed for firmware storage if INT13h boot software is used.

The Flash ROM is accessed using the upper eight bits of the Memory Interface. If a Flash ROM is to be used, then it should have a capacity of 1 Mbyte with a maximum access time of 150 ns. Refer to the LSI Logic LSIFC919 Programming Model for more information regarding the programming of the Flash ROM.

3.6.3 Serial EEPROM

The serial EEPROM stores the World Wide Name, VPD, and other vendor specific information. The Programming Model describes how the serial EEPROM is programmed using the host interface of the LSIFC919. The required size of the EEPROM is 2 Kbytes.

Chapter 4
Signal Descriptions

This chapter contains signal descriptions for the LSIFC919. A slash (/) indicates an active low signal, I/O = bidirectional signal, I = input signal, O = output signal, T/S = 3-state, and S/T/S = sustained 3-state. Figure 4.1 on page 4-2 is a functional signal grouping for the chip.

Figure 4.1 LSIFC919 Functional Signal Grouping

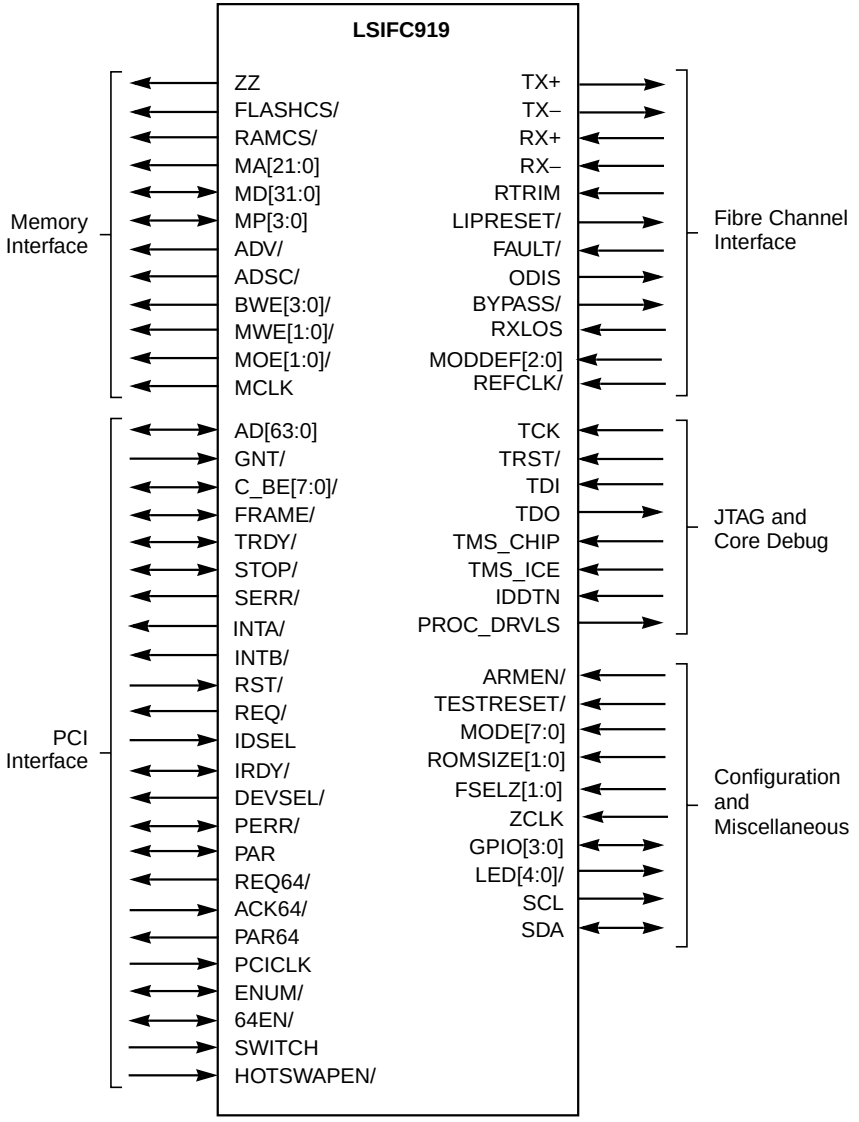


Table 4.1 PCI Interface

Signal	I/O	BGA Pad Number	Pad Type	Description
PCICLK	I	AA13	5 V Tol In	**Clock** provides timing for all transactions on the PCI bus and is an input to every PCI device. All other PCI signals are sampled on the rising edge of PCICLK, and other timing parameters are defined with respect to this edge.
RST/	I	T3	5 V Tol In	**Reset** forces the PCI sequencer of the device to a known state. All 3-state and sustained 3-state signals are forced to a high impedance state, and all internal logic is reset. The RST/ input is synchronized internally to the rising edge of PCICLK. The PCICLK input must be active while RST/ is asserted to properly reset the device.
GNT/	I	V1	5 V Tol BiDir PCI	**Grant** indicates to the agent that access to the PCI bus has been granted. This is a point-to-point signal. Every master has its own GNT/.
REQ/	O	V2	5 V Tol BiDir PCI	**Request** indicates to the system arbiter that this agent desires use of the PCI bus. This is a point-to-point signal. Every master has its own REQ/.
REQ64/	O	AA15	5 V Tol BiDir PCI	**Request64** indicates that the current bus master desires to transfer data using 64 bits. REQ64/ is sampled at the end of reset to indicate the presence of a 64-bit bus.
ACK64/	S/T/S	Y15	5 V Tol BiDir PCI	**Acknowledge64** is an input from the Target that decodes the address, and indicates that the Target is willing to complete a 64-bit transfer. No slaves on the LSIFC919 assert this pin (i.e., all slaves are 32-bit slaves). The LSIFC919 will not assert this pin when accessed as a Target, but will monitor this pin when initiating transfers (i.e., the LSIFC919 presents itself as a 32-bit slave device, but operates as a 64-bit bus master).

Table 4.1 PCI Interface (Cont.)

Signal	I/O	BGA Pad Number	Pad Type	Description
AD[63:0]	T/S	AC18, AB18, AA18, AC19 AB19, AA19, AC20, AB20 AC21, AA20, AC22, AB21 AC23, AB22, AA22, AB23 AA23, Y22, Y23, W21 W22, W23, V21, V22 V23, U22, U23, T21 T20, T22, T23, R21 V3, W1, W2, W3 Y1, Y2, AA1, AB1 AB2, AB3, AC2, AA4 AC3, AB4, AC4, AA5 AC8, AA9, AB9, AC9 AA10, Y11, AB10, AC10 AC11, AB11, AC12, AB14 Y13, AA14, AC15, AB15	5 V Tol BiDir PCI	The physical longword **Address and Data** are multiplexed on the same PCI pins. During the first clock of a transaction, AD[63:0] contains a physical byte address. During subsequent clocks, AD[63:0] contains data. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. AD[7:0] define the least significant byte, and AD[63:56] define the most significant byte.
C_BE[7:0]/	T/S	AC16, AB16, AC17, AB17, AA2, AB5, AB8, AA11	5 V Tol BiDir PCI	Bus **Command and Byte Enables** are multiplexed on the same PCI pins. During the address phase of a transaction, C_BE[3:0]/ define the bus command. During the data phase, C_BE[7:0]/ are used as byte enables. The byte enables determine which byte lanes carry meaningful data. C_BE[0]/ applies to the least significant byte, and C_BE[7]/ applies to the most significant byte. Byte enables are active low.

Table 4.1 PCI Interface (Cont.)

Signal	I/O	BGA Pad Number	Pad Type	Description
IDSEL	I	AC1	5 V Tol BiDir PCI	**Initialization Device Select** is used as a chip select in place of the upper 24 address lines during configuration read and write transactions.
FRAME/	S/T/S	AC5	5 V Tol BiDir PCI	**Cycle Frame** is driven by the current master to indicate the beginning and duration of an access. FRAME/ is asserted to indicate a bus transaction is beginning. While FRAME/ is deasserted, the transaction is in the final data phase or the bus is idle.
IRDY/	S/T/S	AA6	5 V Tol BiDir PCI	**Initiator Ready** indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY/ is used with TRDY/. A data phase is completed on any clock when both IRDY/ and TRDY/ are sampled asserted. During a write, IRDY/ indicates that valid data is present on AD[63:0]. During a read, it indicates that the master is prepared to accept data. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together.
TRDY/	S/T/S	AB6	5 V Tol BiDir PCI	**Target Ready** indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY/ is used with IRDY/. A data phase is completed on any clock when used with IRDY/. A data phase is completed on any clock when both TRDY/ and IRDY/ are sampled asserted. During a read, TRDY/ indicates that valid data is present on AD[63:0]. During a write, it indicates that the target is prepared to accept data. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together.
DEVSEL/	S/T/S	AC6	5 V Tol BiDir PCI	**Device Select** indicates that the driving device has decoded its address as the target of the current access. As an input, it indicates to a master whether any device on the bus has been selected.
STOP/	S/T/S	AA7	5 V Tol BiDir PCI	**Stop** indicates that the selected target is requesting the master to stop the current transaction.

Table 4.1 PCI Interface (Cont.)

Signal	I/O	BGA Pad Number	Pad Type	Description
PERR/	S/T/S	AB7	5 V Tol BiDir PCI	**Parity Error** may be pulsed active by an agent that detects a parity error. PERR/ can be used by any agent to signal data corruption. However, on detection of a PERR/ pulse, the central resource may generate a nonmaskable interrupt to the host CPU, which often implies the system will be unable to continue operation once error processing is complete.
SERR/	O	AC7	5 V Tol BiDir PCI	**System Error** is an open drain output used to report address parity errors and data parity errors on the Special Cycle command.
PAR	T/S	AA8	5 V Tol BiDir PCI	**Parity** is the even parity bit that protects the AD[31:0] and C_BE[3:0]/ lines. During the address phase, both the address and command bits are covered. During the data phase, both data and byte enables are covered.
PAR64	T/S	AA17	5 V Tol BiDir PCI	**Parity64** is the even parity bit that protects the AD[63:32] and C_BE[7:4]/ lines. During the address phase, both the address and command bits are covered. During the data phase, both data and byte enables are covered.
INTA/	O	U2	5 V Tol BiDir PCI	**Interrupt A**. This open-drain signal, when asserted low, indicates that PCI Function[0] is requesting service from its Host device driver. If the chip is configured as a single-function device, only INTA/ is used.
INTB/	O	U1	5 V Tol BiDir PCI	**Interrupt B**. This open-drain signal, when asserted low, indicates that PCI Function[1] is requesting service from its Host device driver. If the chip is configured as a single-function device, only INTA/ is used.

Table 4.1 PCI Interface (Cont.)

Signal	I/O	BGA Pad Number	Pad Type	Description
ENUM/	B	AC13	5 V Tol BiDir PCI	**ENUM/**. This signal must be asserted by a hot swap capable card immediately after insertion and during removal. This signal notifies the system host either that a board has been freshly inserted or that one is about to be extracted, and informs the system host that the configuration of the system has changed. The system host then can perform any necessary maintenance such as installing a device driver upon board insertion, or quiescing a device driver and the board, prior to the board's extraction.
64EN/	B	AC14	5 V Tol BiDir PCI	**PCI Bus Width Enable**. This signal indicates the width of the bus when hot swap capability is enabled.
SWITCH	I	A1	5 V Tol In	**Insertion/deassertion indicator**. This signal is an input to the LSIFC929 to signal the insertion or impending extraction of a board. This signal causes the assertion of ENUM/. The operator normally activates the switch (actuator), waits for the illumination of the LED, and then extracts the board.
HOTSWAPEN/	I	M3	5 V Tol In	**Hot Swap Enable**. When this signal is low, the LSIFC929 is configured to comform to hot swap protocol. This includes changing the bus width detection method, the addition of configuration registers, and support for the ENUM/, BLUELED/ and SWITCH pins.
GPIO[2] (BLUELED/)	B	C5	3.3 V BiDir 8 mA w/pullup	**GPIO[2] (BLUELED/)**. This signal will drive a blue LED that is mounted on the front of hot swap capable host adapters. This signal indicates that the system software has been placed in a state for orderly extraction of the board. See also the description of the GPIO[2] pin in Table 4.5, page 4-14, for additional information regarding other operational capabilities of this signal.

Table 4.2 Fibre Channel Interface

Signal	I/O	BGA Pad Number	Pad Type	Description
TX+	O	N2	Diff Tx	Transmit differential data.
TX-	O	N1	Diff Tx	Transmit differential data.
RX+	I	L2	Diff Rx	Receive differential data.
RX-	I	L1	Diff Rx	Receive differential data.
RTRIM	I	L4		This pin is the analog current reference for the integrated transceiver core. A 2.74 kΩ ± 1% resistor should be tied from the RTRIM pad to the RXVDD pin.
LIPRESET/	O	R1	3.3 V BiDir 4 mA	This pin is asserted low when a selective reset is received that is targeted to one of this device's aliases. This pin is asserted for 1–2 ms after the last LIPr is received.
FAULT/	I	R2	3.3 V TTL Input w/pullup	This active-low pin indicates that an electrical fault has been detected by the PHY device/module and, if the module has a laser, the laser has been turned off. This pin causes no interrupt or other reaction. It is assumed that a LinkFailure will occur and the register bit reporting this pin's value will be used to diagnose the problem.
ODIS	O	R3	3.3 V BiDir 4 mA	**Output Disable.** This output when asserted disables an external GBIC or MIA transmitter. This output is also used to clear a module fault.
BYPASS/	O	T1	3.3 V BiDir 4 mA	This line is driven LOW when the LSIFC919 Link Controller block has determined that the device is operating in a loop environment and the device has entered a bypassed mode. This may be caused by an internal request or a loop primitive generated by another node.

Table 4.2 Fibre Channel Interface

Signal	I/O	BGA Pad Number	Pad Type	Description
RXLOS	I	P3	3.3 V 4 mA BiDir w/pulldown	This line is driven HIGH, disabling the on-chip receiver, when the GBIC of the LSIFC919 has detected a loss of signal. If enabled through the Link Control Register, this signal becomes an output test strobe.
MODDEF[2:0]	I	A9, C10, D11	3.3 V BiDir 8 mA w/pullup	GBIC and pluggable SFF optical module identifiers.
REFCLK	I	E2	3.3 V Schmitt Input	FC reference clock (106.25 MHz ± 100 ppm).

Table 4.3 Memory Interface

Signal	I/O	BGA Pad Number	Pad Type	Description
MD[31:0] *MD[31:24]*	I/O	H22, H20, H21, G23 G22, G21, F23, F22 E21, E23, E22, F21 D23, D22, C23, D21 B18, A18, C17, B17 A17, C16, B16, A16 C15, B15, A15, C14 D13, B14, A14, C13	3.3 V BiDir 4 mA	**SSRAM Read/Write Data**. *MD[31:24] are used for the FLASH ROM Read/Write Data.*
MP[3:0]	I/O	H23, B23, D18, A13	3.3 V 4 mA BiDir w/pullup	**Memory Parity**. Byte lane parity as follows: MP [0]: Parity for MD[7: 0] MP [1]: Parity for MD[15: 8] MP [2]: Parity for MD[23:16] MP [3]: Parity for MD[31:24] Memory Parity may be optionally even, odd, or none (not used) as defined in the LSIFC919 Programming Model.
MA[21:0]	O	R20, P21, R23, R22 N20, P23, P22, N21 N23, N22, M23, M21 M22, L22, L21, L23, K23 K22, J23, K21, J22, J21	3.3 V BiDir 4 mA	**SSRAM/FLASH ROM Address**.
MOE[1:0]/	O	B19, A19	3.3 V BiDir 8 mA	**Memory Output Enable**. When asserted low, the selected SRAM or FLASH *(MOE[1]/)* device may drive data. This signal is typically an asynchronous input to SRAM and/or FLASH devices. The two output enables allow for interleaving configurations, with MOE[0]/ being the only output enable used for a noninterleaved implementation.

Table 4.3 Memory Interface (Cont.)

Signal	I/O	BGA Pad Number	Pad Type	Description
MWE[1:0]/	O	B20, A20	3.3 V BiDir 4 mA	**Memory Write Enables**. These active low bank write enables are required for interleaving configurations. MWE[0]/ is the only write enable used for a noninterleaved implementation.
FLASHCS/	O	C18	3.3 V BiDir 4 mA	**FLASH Chip Select**. This active-low chip select allows connection of a single 8-bit FLASH ROM device.
MCLK	O	A23	3.3 V 8 mA T/S Output	**Memory Clock**. All synchronous RAM control/data signals are referenced to the rising edge of this clock. Exceptions are MOE/ and ZZ which are typically asynchronous inputs to SRAM and/or FLASH devices.
ADSC/	O	C22	3.3 V 4 mA T/S Output	**Address-Strobe-Controller**. Initiates READ, WRITE, or chip deselect cycle. When this signal is asserted, it also latches the memory address signals.
ADV/	O	B22	3.3 V 4 mA T/S Output	**Advance**. When asserted low, the ADV/ input causes a selected synchronous SRAM to increment its burst address counter.
BWE[3:0]/	O	B21, A22, C20, A21	3.3 V BiDir 4 mA	**Memory Byte Write Enables**. These active-low, byte lane write enables allow writing of partial words to memory.
RAMCS/	O	C19	3.3 V BiDir 4 mA	**RAM Chip Select**. This pin is an active-low synchronous chip select for all SSRAMS (up to four SSRAMS for interleaved and depth expanded configuration without additional decode logic).
ZZ	O	D19	3.3 V BiDir 4 mA	**Snooze Control**. Asserting this output high will cause a synchronous SRAM to enter its lowest power state (not all RAMs support this function).

Table 4.4 Configuration Signals

Signal	I/O	BGA Pad Number	Pad Type	Description
ROMSIZE [1:0]	I	C12, A12	3.3 V TTL Input w/pullup	This field identifies the size of the ROM that is connected to the device. The value of this bus should be established at chip reset and should remain unchanged until another chip reset. The encoding of this field is: **Bits [1:0] ROM Size** 00 256 Kbytes 01 512 Kbytes 10 1024 Kbytes 11 No external memory present
TESTRESET/	I	A11	3.3 V Schmitt Input w/pullup	**Test Reset.** This pin forces the chip into the Power-On-Reset state or Soft-Reset state, depending on the state of the Mode pins.
ARMEN/	I	B13	3.3 V TTL Input w/pullup	When this pin is asserted low, the ARM RISC processor core (IOP) is enabled and will boot from the FLASH ROM following a chip reset. If this configuration pin is held high, the IOP core will be held reset until the DisARM bit in the Diagnostic register is cleared by the Host CPU.
FSELZ[1:0]	I	A3, B4	3.3 V TTL Input w/pullup	**Frequency Select.** These pins indicate how the RefClk input (106.25 MHz) is internally divided to generate the internal ZClk source. When FSELZ[1] is high, the internal ZClk tree is sourced directly from the ZCLK input signal. **FSELZ[1:0] Internal ZClk** 00 REFCLK/2 01 REFCLK * 2/3 10 External ZCLK 11 External ZCLK

Table 4.4 Configuration Signals (Cont.)

Signal	I/O	BGA Pad Number	Pad Type	Description
MODE[7:0]	I	A5, C6, D6, B6, A6, C7, B7, A7	3.3 V TTL Input w/pullup	**Mode Select.** This 8-bit bus defines operational and test modes for the chip. Valid Mode encodings are given below. Mode[7:0] = 001xxxxx == Interleaved BSRAM Mode[7:0] = 000xxxxx == Noninterleaved BSRAM Mode[7:0] = 00xx1xxx == Link Reset Mode Mode[7:0] = 00xxx1xx == Soft Reset Mode Mode[7:0] = 00xxxx11 == Normal SEPROM Auto Load Mode[7:0] = 00xxxx10 == Fast SEPROM Auto Load Mode[7:0] = 00xxxx01 == Firmware PCI Config Mode **(ARMEN/ must also be low)** Mode[7:0] = 00xxxx00 == PCI Config use default values

Table 4.5 Miscellaneous Signals

Signal	I/O	BGA Pad Number	Pad Type	Description
GPIO[3:0]	I/O	A4, C5, D5, B5	3.3 V BiDir 8 mA w/pullup	**General purpose I/O pins.** These pins default to input mode on reset. Firmware controls and observes these signals, which may be configured as inputs or outputs. GPIO[3] may be optionally enabled as an external interrupt source to the ARM RISC Processor core.See also the description of the GPIO[2] pin in Table 4.1, page 4-3, for additional information regarding other operational capabilities of this signal.
LED[4:0]/	O	C8, B8, A8, C9, B9	3.3 V BiDir 8 mA	These output signals may be controlled by firmware or driven by chip activity. When configured as activity driven, the LED[n] outputs have the following meaning when asserted low: LED[4]: Reserved LED[3]: Reserved LED[2]: Channel Fault LED[1]: Channel Active LED[0]: Firmware controlled (Heartbeat)
SCL	O	B11	3.3 V 4 mA BiDir w/pullup	**Serial EEPROM clock.**
SDA	I/O	B12	3.3 V 4 mA BiDir w/pullup	**Serial EEPROM data.**
ZCLK	I	B3	3.3 V Schmitt Input	**External ZBus reference clock.** Based on the table below, this input pin provides the reference timing for the internal ZBus, IOP and CtxMgr processors, and memory interface. When FSELZ[1] is high, the internal ZClk tree is sourced directly from the ZCLK input signal. **FSELZ[1:0] Internal ZClk** 00 REFCLK/2 01 REFCLK * 2/3 10 External ZCLK 11 External ZCLK

Table 4.6 JTAG Test and I/O Processor Debug

Signal	I/O	BGA Pad Number	Pad Type	Description
TCK	I	D3	3.3 V Schmitt w/pullup	JTAG/CtxMgr Debug Test Clock.
TRST/	I	C1	3.3 V Schmitt w/pullup	JTAG/Debug Test Reset. Asynchronous active-low.
TDI	I	D1	3.3 V Schmitt w/pullup	JTAG/CtxMgr Debug Test Data In.
TDO	O	E3	3.3 V 4mA T/S Output w/pullup	JTAG/CtxMgr Debug Test Data Out.
TMS_CHIP	I	B1	3.3 V Schmitt w/pullup	JTAG Test Mode Select.
TMS_ICE	I	D2	3.3 V Schmitt w/pullup	CtxMgr Debug Test Mode Select.
IDDTN	I	B2	Input w/"large" pulldown	QIDD Test Enable.
PROC_DRVLS	O	C2		Process Monitor Test Output Driver.

Table 4.7 Power and Ground Pins

Signal	BGA Pad Number	Description	Voltage
VDDIO	D10, D14, D17, D7 G20, G4, K20, K4 P20, P4, U20, U4 Y10, Y14, Y17, Y7	I/O power.	3.3 V
VSSIO	AA21, AA3, C21, C3 D12, D20, D4, K10 K11, K12, K13, K14 L10, L11, L12, L13 L14, M10, M11, M12 M13, M14, M20, M4 N10, N11, N12, N13 N14, P10, P11, P12 P13, P14, Y12, Y20, Y4	I/O ground.	0 V
VDDC	D9, D15, F1, F20, F4, H3, H4, J4, L20 N4, V20, V4, Y16, Y8	Core power.	2.5 V
VSSC	D16, D8, E20, E4, F2, G3, J2, J3, J20 R4, W20, W4, Y18, Y6	Core ground.	0 V
PCI5VREF	AA12, AA16, U21, U3, Y19, Y21, Y3, Y5, Y9	PCI 5 V reference power supply.	5 V
PLLZVDD	C4	Analog power for PCI FSN cell.	2.5 V
PLLZVSS	A2	Analog ground for PCI FSN cell.	0 V
RXBVDD	M1	Analog power for integrated transceiver core.	2.5 V
RXBVSS	L3	Analog ground for integrated transceiver core.	0 V
RXVDD	K1	Analog power for integrated transceiver core.	2.5 V
RXVSS	K2	Analog ground for integrated transceiver core.	0 V
TXBVDD	M2	Analog power for integrated transceiver core.	2.5 V
TXBVSS	N3	Analog ground for integrated transceiver core.	0 V
TXVDD	P1	Analog power for integrated transceiver core.	2.5 V
TXVSS	P2	Analog ground for integrated transceiver core.	0 V

Chapter 5
Registers

This chapter provides a description of the registers in the LSIFC919 Fibre Channel PCI Protocol Controller chip. The chapter contains the following sections:

- Section 5.1, “PCI Addressing”
- Section 5.2, “PCI Bus Commands Supported”
- Section 5.3, “PCI Cache Mode”
- Section 5.4, “Unsupported PCI Commands”
- Section 5.5, “Programming Model”
- Section 5.6, “PCI/Multifunction PCI Configuration Registers”
- Section 5.7, “Host Interface Registers”
- Section 5.8, “Shared Memory”

5.1 PCI Addressing

The three types of PCI-defined address space are:

- Configuration space
- Memory space
- I/O space

Configuration space is a contiguous 256 x 8-bit set of addresses dedicated to each “slot” or “stub” on the bus. Decoding C_BE[7:0]/ determines if a PCI cycle is intended to access configuration register space. The IDSEL bus signal is a “chip select” that allows access to the configuration register space only. A configuration read/write cycle without IDSEL is ignored. The eight lower order addresses are used to select a specific 8-bit register. AD[10:8] are decoded as well, but they must be

"000" (for PCI Function 0) or "001" (for PCI Function 1), or the LSIFC919 will not respond. According to the PCI specification, AD[10:8] are used for multifunction devices. The host processor uses the PCI configuration space to initialize the LSIFC919.

At initialization time, each PCI device is assigned a base address for memory accesses and I/O accesses. On every access, the LSIFC919 compares its assigned base addresses with the value on the Address/Data bus during the PCI address phase. A decode of C_BE[7:0]/ determines which registers and what type of access is to be performed.

5.2 PCI Bus Commands Supported

Bus commands indicate to the target the type of transaction the master is requesting. Bus commands are encoded on the C_BE[3:0]/ lines during the address phase. Table 5.1 lists the PCI bus commands and encoding types.

The Memory Read, Memory Read Multiple, and Memory Read Line commands are used to read data from an agent mapped in memory address space. All 64 address bits are decoded (DAC).

The Memory Write, and Memory Write and Invalidate commands are used to write data to an agent when mapped in memory address space. All 64 address bits are decoded (DAC).

Table 5.1 PCI Bus Commands and Encoding Types

C_BE[3:0]/	Command Type	Supported as Master	Supported as Slave
0000	Special Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read Cycle	Yes	Yes
0011	I/O Write Cycle	Yes	Yes
0100	Reserved	N/A	N/A
0101	Reserved	N/A	N/A
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	N/A	N/A
1001	Reserved	N/A	N/A
1010	Configuration Read	N/A	Yes
1011	Configuration Write	N/A	Yes
1100	Memory Read Multiple	Yes	Yes
1101	Dual Address Cycle	Yes	Yes
1110	Memory Read Line	Yes	Yes
1111	Memory Write and Invalidate	Yes	Yes

5.3 PCI Cache Mode

The LSIFC919 supports the PCI specification for an 8-bit Cache Line Size register located in PCI configuration space. The Cache Line Size register provides the ability to sense and react to nonaligned addresses corresponding to cache line boundaries. Memory Write and Invalidate is enabled using bit 4 of the Command Register in PCI configuration space. Cache Read commands cannot be disabled. Slaves, however, can alias the Memory Read Line and Memory Read Multiple commands to the Memory Read command.

5.3.1 Support for PCI Cache Line Size Register

The LSIFC919 supports the PCI specification for an 8-bit Cache Line Size register in PCI configuration space. It can sense and react to nonaligned addresses corresponding to cache line boundaries.

5.3.2 Selection of Cache Line Size

The cache logic selects a cache line size based on the value specified in the Cache Line Size register.

Note: If a value of 1 is specified in the PCI Cache Line size register, caching is disabled. Otherwise, the LSIFC919 uses whatever legal value is specified (2, 4, 8, 16, 32, 64, or 128) for all aligned burst data transfers.

5.3.3 Memory Write and Invalidate Command

The Memory Write and Invalidate command is identical to the Memory Write command, except that it additionally guarantees a minimum transfer of one complete cache line. This means the master intends to write all bytes within the addressed cache line in a single PCI transaction, unless interrupted by the target. This command requires implementation of the PCI Cache Line Size register at address 0x00C in PCI configuration space.

5.3.3.1 Alignment

The LSIFC919 uses the calculated line size value to monitor the current address for alignment to the cache line size. When it is not aligned, the chip attempts to align to the cache boundary by using a noncache command.

For nonaligned initial addresses, the chip executes a burst to bring the address counter to an aligned value. Once a cache line boundary is reached, the chip uses the cache line size as the burst size from then on, except in the case of Multiple Cache Line Transfers. The alignment process is finished at this point. Memory Write and Invalidate commands are issued when the following conditions are met:

1. The PCI configuration Command register, bit 4 must be set.
2. The Cache Line Size register must contain a legal burst size (2, 4, 8, 16, 32, 64, or 128) value.
3. The chip must have enough bytes in the DMA FIFO to complete at least one full cache line burst.
4. The chip must be aligned to a cache line boundary.

When these conditions have been met, the LSIFC919 issues a Memory Write and Invalidate command instead of a Memory Write command during all PCI write cycles.

5.3.3.2 Multiple Cache Line Transfers

The Memory Write and Invalidate command can write multiple cache lines of data in a single bus ownership. The chip issues a burst transfer as soon as it reaches a cache line boundary. The size of the transfer will not automatically be the cache line size, but rather a multiple of the cache line size as allowed for in the *PCI Local Bus Specification, Revision 2.2.* The logic selects the largest multiple of the cache line size based on the amount of data to transfer.

When the DMA buffer contains less data than the value specified in the Cache Line Size register, the LSIFC919 throttles back to a Memory Write command on the next cache line boundary.

5.3.3.3 Latency

In accordance with the PCI specification, the chip's latency timer is ignored when issuing a Memory Write and Invalidate command. When a latency time-out has occurred and GNT/ is deasserted, the LSIFC919 continues to transfer up until a cache line boundary. At that point, the chip relinquishes the bus, and finishes the transfer at a later time using another bus ownership. In accordance with the *PCI Local Bus Specification, Revision 2.2,* the latency timer is completely ignored as long as GNT/ is asserted to the LSIFC919.

5.3.3.4 PCI Target Retry

During a Memory Write and Invalidate transfer, if the target device issues a retry (STOP with no TRDY, indicating that no data was transferred), the LSIFC919 relinquishes the bus and immediately tries to finish the

transfer on another bus ownership. The chip issues another Memory Write and Invalidate command on the next ownership, in accordance with the *PCI Local Bus Specification, Revision 2.2.*

5.3.3.5 PCI Target Disconnect

During a Write and Invalidate transfer, if the target device issues a disconnect the LSIFC919 relinquishes the bus and immediately tries to finish the transfer on another bus ownership. The chip will not issue another Memory Write and Invalidate command on the next ownership unless the address is aligned.

5.3.4 Read Commands

Memory Read Line and Memory Read Multiple commands are issued with burst transfers where the memory system and the requesting master may gain some performance advantage by prefetching read data. The remainder of this section describes Cache command usage.

5.3.4.1 Memory Read Line

The Memory Read Line command is issued on any burst read of two or more dwords in which a cache line boundary is not crossed. The starting address of the burst need not be aligned to a cache line boundary. This command allows a capable bridge to prefetch and burst up to an entire cache line of data, as opposed to disconnecting after every data phase.

5.3.4.2 Memory Read Multiple

The Memory Read Multiple command is issued on any burst read that crosses a cache line boundary. The starting address of the burst need not be aligned to a cache line boundary. This command allows a capable bridge to prefetch multiple cache lines of data, maximizing read burst potential.

5.3.4.3 Memory Read

The Memory Read command is used for single dword (nonburst) transfers.

5.4 Unsupported PCI Commands

The LSIFC919 does not respond to reserved commands, special cycle, or interrupt acknowledge commands as a slave. It never generates these commands as a master.

5.5 Programming Model

The LSIFC919 Host Programming model includes all necessary hardware registers, shared memory and associated memory addresses from the Host (using System Addresses) viewpoint. The Host Programming Model consists of PCI/Multifunction PCI Configuration Registers, Host Interface Registers, and a Shared Memory region.

5.6 PCI/Multifunction PCI Configuration Registers

The Configuration registers are accessible only by the system BIOS during PCI configuration cycles. These registers are not available to the user at any time. No other cycles can access these registers.

Note: The configuration register descriptions provide general information only, to indicate which PCI configuration addresses are supported in the LSIFC919. Table 5.2 shows the PCI configuration registers implemented by the LSIFC919. Addresses 0x048 through 0x07F are not defined.

All PCI-compliant devices, such as the LSIFC919, must support the Vendor ID, Device ID, Command, and Status Registers. Support of other PCI-compliant registers is optional. In the LSIFC919, registers that are not supported are not writable and return all zeroes when read. Only those registers and bits that are currently supported by the LSIFC919 are described in this chapter. For more detailed information on PCI registers, refer to the *PCI Local Bus Specification, Revision 2.2*.

PCI configuration space provides identification, configuration, initialization, and error management functions for PCI devices. Table 5.2 defines the configuration registers for the LSIFC919 device.

5.6.1 Multifunction PCI

The LSIFC919 supports multifunction capability on the PCI bus. Both Function[0] and Function[1] have identical looking configuration space memory maps, and most of the data reported in these registers by the LSIFC919 are also the same. The only exceptions are the Device ID, Class Code, Subsystem ID, and Subsystem Vendor ID. Each of these values can be set separately for each function within the serial EEPROM, which is downloaded into these registers before any configuration cycles are completed. While the Class Code, Subsystem ID, and the Subsystem Vendor ID can all be set to any value, the Device ID is more restrictive. The upper 15 bits are hardcoded to a value of 0x0624, but the least significant bit (bit 16) can be programmed to either a 0 or a 1 to provide two possible Device ID values of 0x0624 or 0x0625.

Table 5.2 LSIFC919 PCI Configuration Register Map

31 16	15 0	Address
Device ID = 0x06nn	Vendor ID = 0x1000	0x000
Status	Command	0x004
Class Code	Revision ID	0x008
BIST / Header Type	Latency Timer / Cache Line Size	0x00C
I/O Base Address		0x010
Mem0 Base Address Low		0x014
Mem0 Base Address High		0x018
Mem1 Base Address Low		0x01C
Mem1 Base Address High		0x020
Reserved		0x024
Reserved		0x028
Subsystem ID	Subsystem Vendor ID	0x02C
Expansion ROM Base Address		0x030
Reserved	CapPtr	0x034
Reserved		0x038
Max Latency / Min Grant	Interrupt Pin / Interrupt Line	0x03C
Power Management Capabilities	Next Item Ptr / Capability ID	0x040
PM Data / PMCSR-BSE	Power Management Control/Status	0x044
Reserved		0x048–0x07F

Resources assigned to each function by the PCI BIOS are maintained separately. However, in most cases they will still access the same memory locations in the LSIFC919. The shared memory locations within Mem0 and all of the memory accessed through Mem1 and the expansion ROM are all aliased to the same spaces between the two functions. Within the host registers located in I/O space and Mem0, some of the registers are also aliased and some are unique to the different functions.

The multifunction feature of the LSIFC919 can be disabled by setting bit 0 in the Hardware Configuration entry in the serial EEPROM. This clears the multifunction bit in the PCI configuration space, and the LSIFC919 will only respond to Function[0].

Register: 0x000
Device ID/Vendor ID
Read Only

31															16
DevID (Most Significant)															
0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	1

15															0
VenID (Least Significant)															
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

DevID **Device ID (Read Only)** **[31:16]**
The most significant half of this register identifies the particular device. The upper 15 bits are hardcoded to a value of 0x0624, but the least significant bit (bit 16) can be programmed to either a 0 or 1 to provide two possible LSIFC919 Device ID values of 0x0624 or 0x0625. The 0x06nn indicates a FC device. The 0xnn24 (or 0xnn25) indicates a specific device and PCI Function; in this case, the LSIFC919, Function 0 (or Function 1).

VenID **Vendor ID (Read Only)** **[15:0]**
The least significant half of this register identifies the manufacturer of the device. The LSI Logic Vendor ID is 0x1000.

Register: 0x004
Status/Command
Read/Write

31	30	29	28	27	26	25	24	23							16
DPE	SSE	MA	RTA	R	DevSEL/Tim		DPR	R							
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

15							9	8	7	6	5	4	3	2	1	0
R								SERR	R	EPER	R	WIM	R	EBM	EMS	EIOS
0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

The most significant half of the Status/Command Register is used to record status information for PCI bus-related events.

Reads to the upper half of this register (status) behave normally. Writes are slightly different in that bits can be cleared, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a one. For instance, to clear bit 31 and not affect any other bits, write the value 0x8000 to the register.

The least significant half of the Status/Command Register provides coarse control over a device's ability to generate and respond to PCI cycles. When a zero is written to this register, the LSIFC919 is logically disconnected from the PCI bus for all accesses except configuration accesses.

DPE **Detected Parity Error (Read/Write)** **31**
The LSIFC919 sets this bit whenever it detects a data parity error, even if parity error handling is disabled.

SSE **Signaled System Error (Read/Write)** **30**
This bit is set whenever a device asserts the SERR/ signal.

MA **Master Abort (Read/Write)** **29**
A master device should set this bit whenever its transaction (except for Special Cycle) is terminated with master abort. All master devices should implement this bit.

RTA **Received Target Abort (Read/Write)** **28**
A master device should set this bit whenever its transaction is terminated with a target abort. All master devices should implement this bit.

R **Reserved** **27**
Reserved for future use.

DevSEL/Tim **DevSEL/Timing (Read/Write)** **[26:25]**
These bits encode the timing of DEVSEL/. These are encoded as:

0b00	fast
0b01	medium
0b10	slow
0b11	reserved

These bits are read only and should indicate the slowest time that a device asserts DEVSEL/ for any bus command except Configuration Read and Configuration Write. In the LSIFC919, medium (0b01) is supported.

DPR **Data Parity Reported (Read/Write)** **24**
This bit is set when the following three conditions are met:

1) The bus agent asserted PERR/ itself or observed PERR/ asserted;

2) The agent setting this bit acted as the bus master for the operation in which the error occurred;

3) The Parity Error Response bit in the Command register is set.

R **Reserved** **[23:9]**
Reserved for future use.

SERR **SERR/Enable (Read/Write)** **8**
This bit enables the SERR/ driver. SERR/ is disabled when this bit is cleared. The default value of this bit is zero. This bit and bit 6 must be set to report address parity errors.

R **Reserved** **7**
Reserved for future use.

EPER **Enable Parity Error Response (Read/Write)** **6**
This bit allows the LSIFC919 to detect parity errors on the PCI bus and report these errors to the system. Only data parity checking is enabled. The LSIFC919 always generates parity for the PCI bus.

R **Reserved** **5**
Reserved for future use.

WIM **Write and Invalidate Mode (Read/Write)** **4**
When set, this bit causes Memory Write and Invalidate cycles to be issued on the PCI bus after certain conditions have been met. For more information on these conditions, refer to Section 5.3.3, “Memory Write and Invalidate Command”.

R **Reserved** **3**
Reserved for future use.

EBM **Enable Bus Mastering (Read/Write)** **2**
This bit controls the ability of the LSIFC919 to act as a master on the PCI bus. A value of zero disables the device from generating PCI bus master accesses. A value of one allows the LSIFC919 to behave as a bus master.

EMS **Enable Memory Space (Read/Write)** **1**
This bit controls the response of the LSIFC919 to Memory Space accesses. A value of zero disables the device response. A value of one allows the LSIFC919 to respond to Memory Space accesses at the address specified by the Memory Base Address registers in the PCI configuration space.

EIOS **Enable I/O Space (Read/Write)** **0**
This bit controls the response of the LSIFC919 to I/O space accesses. A value of zero disables the response. A value of one allows the LSIFC919 to respond to I/O space accesses at the address specified in I/O Base Address register in the PCI configuration space.

Register: 0x008
Class Code/Revision ID
Read/Write

31							24	23							16
ClCode (Most Significant)								ClCode (Middle)							
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

15							8	7							0
ClCode (Least Significant)								RevID							
0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x

ClCode **Class Code (Read Only)** **[31:8]**
This register identifies the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register level programming interface.

The value defaults to 0x010000 unless firmware programs it to a different value prior to PCI configuration, or it is changed using serial EEPROM.

RevID **Revision ID (Read Only)** **[7:0]**
This register specifies device and revision identifiers. In the LSIFC919, the upper nibble is 0b0000. The lower nibble reflects the current revision level of the device.

Register: 0x00C
BIST/Header/Latency/Cache Line
Read/Write

31							24	23							16
BIST								HdTyp							
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

15							8	7							0
LatTim								Cache							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIST **Built-In Self Test (Read Only)** **[31:24]**

HdTyp **Header Type (Read Only)** **[23:16]**
This register identifies the layout of bytes 0x10 through 0x3F in configuration space and also whether or not the device contains multiple functions. The value of this register is 0x80, indicating the LSIFC919 is a multifunction controller.

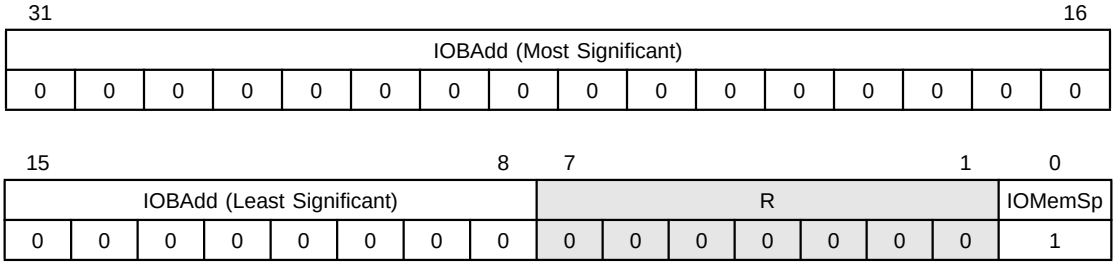
LatTim **Latency Timer (Read/Write)** **[15:8]**
The Latency Timer register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. The LSIFC919 supports this timer. All eight bits are writable, allowing latency values of 0–255 PCI clocks. Use the following equation to calculate an optimum latency value for the LSIFC919:

Latency = 2 + (Burst Size * (typical wait states + 1)).

Values other than optimum are also acceptable.

Cache **Cache Line Size (Read/Write)** **[7:0]**
This register specifies the system cache line size in units of 32-bit words. For more information on this register, see Section 5.3.1, “Support for PCI Cache Line Size Register”.

Register: 0x010
I/O Base Address
Read/Write



Note that this register is only 32 bits, because I/O must be mapped into the lower 4 Gbytes of address space.

IOBAdd **I/O Base Address (Read/Write)** **[31:8]**
Indicates location of I/O space required by the device and is fixed at a size of 256 bytes.

R **Reserved** **[7:1]**
Reserved for future use.

IOMemSp **I/O or Memory Space Indicator (Read Only)** **0**
This bit is set to “1” to indicate I/O space mapping.

Register: 0x014
Mem0 Base Address Low
Read/Write

31															16
Mem0BAddL (Most Significant)															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15											4	3	2	1	0
Mem0BAddL (Least Significant)												Prefetch	Type		IOMemSp
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Mem0BAddL **Mem0 Base Address Low (Read/Write)** **[31:4]**
Indicates lower 32 bits of the 64-bit memory address width, and the location of memory required by the device. Its size is programmable from 16 Kbytes (2^{14}) through 512 Kbytes (2^{19}) in steps of powers of 2 (based on bits [27:24] of the PCI Config0 register). The default value indicated is 64 Kbytes, unless firmware programs a different value prior to PCI configuration, or if programmed with the serial EEPROM.

Prefetch **Prefetchable Memory Block** **3**
With this bit set, there are no side effects to prefetching. For reads, all bytes can be sent regardless of the state of the byte enables. For writes, sequential writes can be combined into a burst.

Type **Location of Memory** **[2:1]**
With bit 2 = 1 and bit 1 = 0, the user can map this device anywhere in the 64-bit space.

IOMemSp **I/O or Memory Space Indicator (Read Only)** **0**
This bit is set to “0” to indicate Memory Space mapping.

Register: 0x018

Mem0 Base Address High

Read/Write

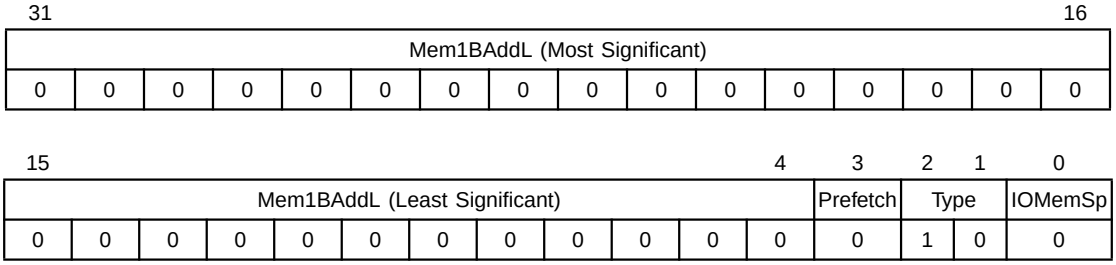
31															16
Mem0BAddH (Most Significant)															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15															0
Mem0BAddH (Least Significant)															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mem0BAddH Mem0 Base Address High (Read/Write) [31:0]

Indicates upper 32 bits of the 64-bit memory address width, and the location of memory required by the device. This allows the LSIFC919 to be mapped above the 4 Gbyte boundary.

Register: 0x01C
Mem1 Base Address Low
Read/Write



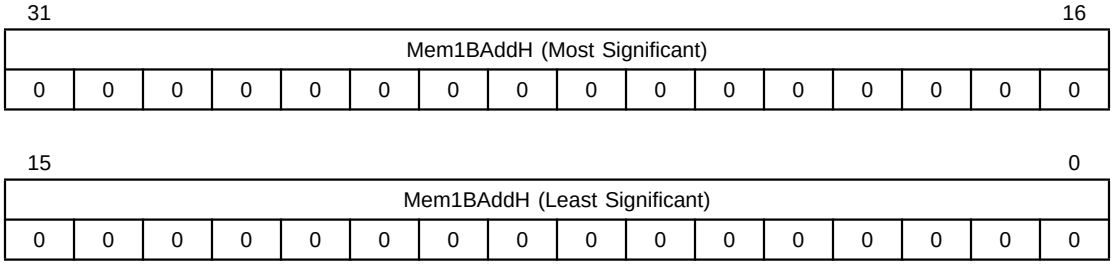
Mem1BAddL **Mem0 Base Address Low (Read/Write)** **[31:4]**
Indicates lower 32 bits of the 64-bit memory address width, and the location of memory required by the device. Its size is programmable from 16 Kbytes (2^{14}) through 512 Kbytes (2^{19}) in steps of powers of 2 (based on bits [27:24] of the PCI Config0 register). The default value indicated is 64 Kbytes, unless firmware programs a different value prior to PCI configuration, or if programmed with the serial EPROM.

Prefetch **Prefetchable Memory Block** **3**
With this bit set, there are no side effects to prefetching. For reads, all bytes can be sent regardless of the state of the byte enables. For writes, sequential writes can be combined into a burst.

Type **Location of Memory** **[2:1]**
With bit 2 = 1 and bit 1 = 0, the user can map this device anywhere in the 64-bit space.

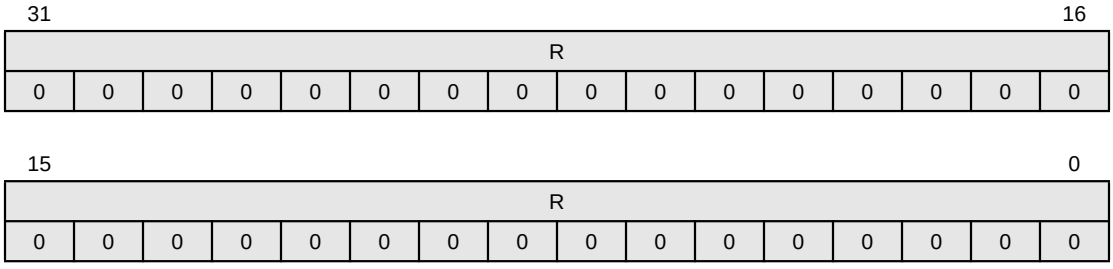
IOMemSp **I/O or Memory Space Indicator (Read Only)** **0**
This bit is set to “0” to indicate Memory Space mapping.

Register: 0x020
Mem1 Base Address High
Read/Write

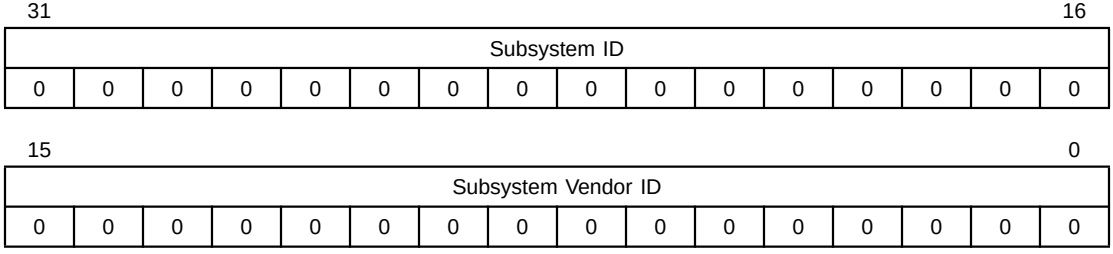


Mem1BAddH Mem0 Base Address High (Read/Write) [31:0]
Indicates upper 32 bits of the 64-bit memory address width, and the location of memory required by the device. This allows the LSIFC919 to be mapped above the 4 Gbyte boundary.

Register: 0x024–0x028
Reserved



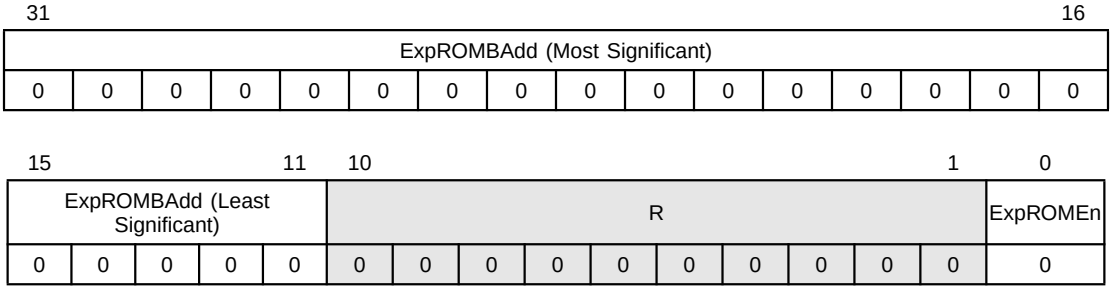
Register: 0x02C
Subsystem ID/Vendor ID
Read Only



SID **Subsystem ID** **[31:16]**
These bits uniquely identify the add-in board or subsystem where this PCI device resides.

SVID **Subsystem Vendor ID** **[15:0]**
These bits uniquely identify the vendor manufacturing the add-in board or subsystem where this PCI device resides.

Register: 0x030
Expansion ROM Base Address
Read/Write



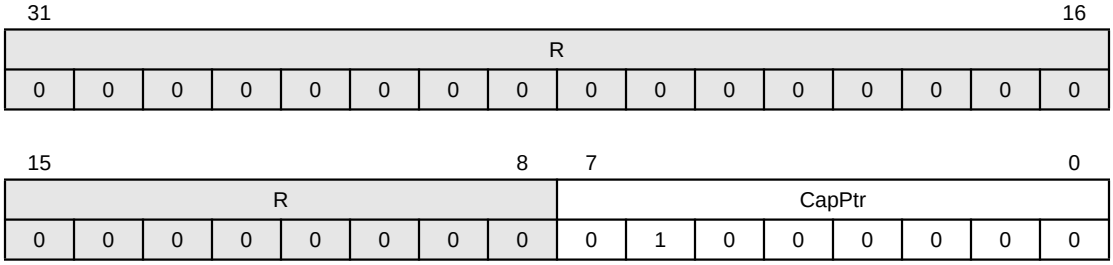
See also Section 3.6.2, “Flash ROM” of this manual for more details regarding the Expansion ROM.

ExpROMBAdd **Expansion ROM Base Address (Read/Write)** **[31:11]**
Indicates location of the Expansion ROM device and is programmable from 256 Kbytes (2^{18}) through 1 Mbytes (2^{20}) in steps of powers of 2 (using the ROMSIZE[1:0] input bus).

R **Reserved** **[10:1]**

ExpROMEn **Expansion ROM Enable (Read/Write)** **0**
When set, this bit enables access to an expansion ROM, providing memory access has been enabled using the EMS (Enable Memory Space) bit in the Command register. **Note:** If ROMSIZE[1:0] = 11, then there is no Expansion ROM.

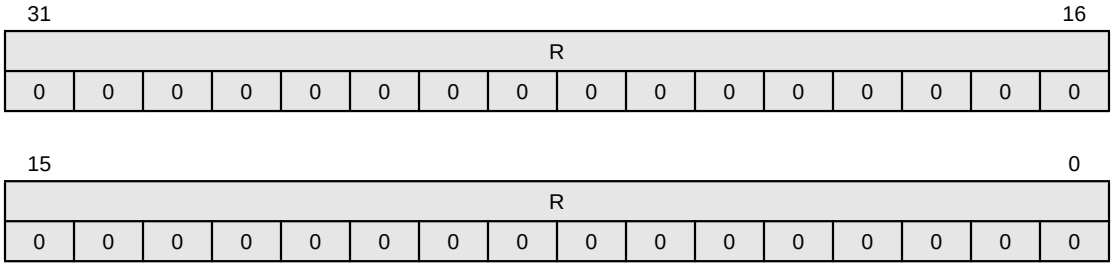
Register: 0x034
Capabilities Pointer
Read/Write



R **Reserved** **[31:8]**
Reserved for future use.

CapPtr **Capabilities Pointer (Read Only)** **[7:0]**
These bits indicate the location of the first extended capability register in the PCI configuration space.

Register: 0x038
Reserved



Register: 0x03C/0x13C

Latency/Interrupt
Read/Write

31							24	23							16
MaxLat								MinGnt							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15							8	7							0
IntPin								IntLin							
0	0	0	0	0	0	X	X	0	0	0	0	0	0	0	0

MaxLat **Maximum Latency (Read Only)** **[31:24]**
This value has been set to a small number (0x08) to request small latencies for PCI arbitration.

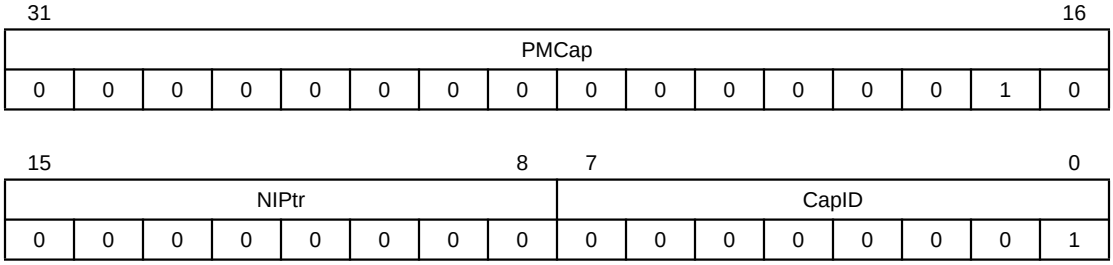
MinGnt **Minimum Grant (Read Only)** **[23:16]**
This value has been set to a large number (0x1E) to indicate that the LSIFC919 is capable of large burst transfers.

IntPin **Interrupt Pin (Read Only)** **[15:8]**
This register tells which interrupt pin the device uses. Its value is set at power-up to 0x01 for the INTA/ signal (Function[0]), or 0x02 for the INTB/ signal (Function[1]).

IntLin **Interrupt Line (Read/Write)** **[7:0]**
This register communicates interrupt line routing information. POST software will write the routing information into this register as it initiates and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin has been connected to. System architecture will specify the values in this register.

Register: 0x040

Power Management Configuration
Read Only



PMCap **Power Management Capabilities (Read Only) [31:16]**
These bits indicate the power management states supported by the LSIFC919, and to which version of the PCI Power Management Interface Specification the LSIFC919 complies. For more information, refer to the *PCI Local Bus Specification, Revision 2.2.*

NIPtr **Next Item Pointer (Read Only) [15:8]**
These bits contain the offset location of the next item in the function's capabilities list. For more information, refer to the *PCI Local Bus Specification, Revision 2.2*.

CapID **Capability ID (Read/Write) [7:0]**
These bits indicate the type of data structure currently being used. For more information, refer to the *PCI Local Bus Specification, Revision 2.2.*

Register: 0x044
Power Management Control/Status
Read/Write

31							24	23							16
PMData								PMCSR-BSE							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15															0
PMCtrl/St															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PMData **Power Management Data (Read Only) [31:16]**
These bits provide an optimal mechanism for the function to report state-dependent operating data. For more information, refer to the *PCI Local Bus Specification, Revision 2.2.*

PMCSR-BSE **Bridge Support Extensions (Read Only) [15:8]**
These bits indicate PCI Bridge-specific functionality. For more information, refer to the *PCI Local Bus Specification, Revision 2.2.*

PMCtrl/St **Power Management Control/Status (Read/Write) [7:0]**
These bits indicate various control/status information specific to the LSIFC919. For more information, refer to the *PCI Local Bus Specification, Revision 2.2.*

Register: 0x048–0x07F
Reserved

31															16
R															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15															0
R															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.7 Host Interface Registers

The first 128 bytes of PCI Memory 0 address space contain the Host Interface Register set as specified in Table 5.3. Both 32 and 64-bit accesses are allowed to the Host Register set. The LSIFC919 design supports only nonburst accesses to the Host Interface Register Set and will *Disconnect-with-data* (TRDY/ and STOP/ both asserted) after the first transfer of any burst attempt.

The LSIFC919 also specifies an I/O space requirement of 128 bytes of I/O mapped space which the system is required to assign during PCI configuration. The 128 bytes of I/O space are mapped onto the first 128 bytes of Memory 0 space; they provide an alternate access path to the Host Interface register set.

Table 5.3 PCI Memory 0 Address Map

31 16 15 0	
System Doorbell Register	0x000
Write Sequence Register	0x004
Host Diagnostic Register	0x008
Test Base Address Register	0x00C
Reserved	0x010–0x02F
Host Interrupt Status Register	0x030
Host Interrupt Mask Register	0x034
Reserved	0x038–0x03F
Request FIFO	0x040
Reply FIFO	0x044
Reserved	0x048–0x04F
Host Index Register	0x050
Reserved	0x054–0x07F
SHARED MEMORY	0x080– 0x(Sizeof(Mem0)–1)

The following Host Registers/Bits are shared (aliased) between Function[0] and Function[1]:

1. Write Sequence Register
2. Diagnostic Register (except ResetHistory bit)

3. Test Base Address Register
4. Request FIFO

The following Host Registers/Bits are unique and operate independently with respect to Function[0] and Function[1]:

1. System Doorbell Register
2. Diagnostic Register (ResetHistory bit)
3. Host Interrupt Status Register
4. Host Interrupt Mask Register
5. Reply FIFO
6. Host Index Register

The Request FIFOs are internally combined between the two functions due to the fact that both FIFOs are managed by the single IOP microprocessor internal to the LSIFC919. A small piece of hardware logic places a stamp onto Message Frame Address (MFA) bit 2 indicating from which function the request originated. Unlike the Request FIFOs, the Reply FIFOs are managed independently by the drivers associated with each function. Therefore, separate hardware FIFOs are needed to support each.

Register: 0x000

System Doorbell Register

Read/Write

31															16
HDV (Most Significant)															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15															0
HDV (Least Significant)															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

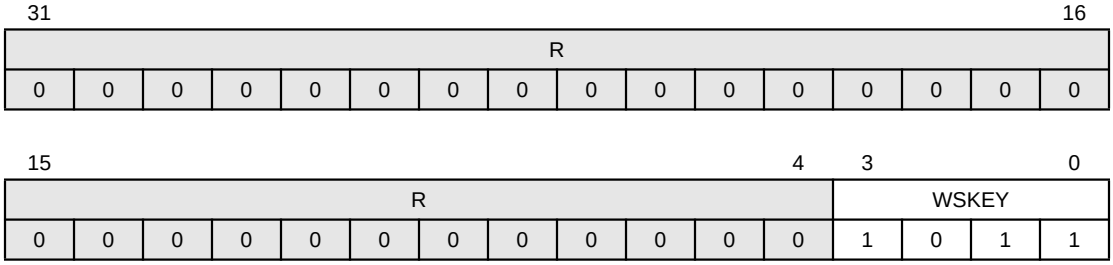
The System Doorbell Register is a simple message passing mechanism to allow the system to pass single word messages to the embedded IOP processor and vice versa. When a PCI master writes to the *HostRegs: Doorbell* register, a maskable interrupt is generated to the IOP processor. The value written by the system master is available for the IOP processor to read in the *SysIfRegs: Doorbell* register. The interrupt status is cleared when the IOP writes any value to the *SysIfRegs: DoorbellClear* register. Conversely, when the IOP processor writes to the *SysIfRegs: Doorbell* register, a maskable interrupt is generated to the PCI system using the INTA/ signal pin. The value written by the IOP is available to the system for reading from the *HostRegs: Doorbell* register. The interrupt status/pin is cleared when the System writes any value to the *HostRegs: IntStatus* register.

HDV **Host Doorbell Value (Read/Write)** **[31:0]**

Write: Doorbell value passed to IOP processor.

Read: Doorbell value received from IOP processor.

Register: 0x004
Write Sequence Register
Read/Write



The Write Sequence Register provides a protection mechanism against inadvertent writes to the Host Diagnostic Register. A sequence of five data specific writes must be written into the Write Sequence KEY field in order to enable writes to the Host Diagnostic Register. Any data value written incorrectly causes the Write Sequence Register to restart by looking for the first sequence value. The required data sequence is:

0x4, 0xB, 0x2, 0x7, 0xD

After the last value (0xD) is written, the Host Diagnostic Register may be written to until another write occurs to the Write Sequence Register (of any value). A bit is provided in the Host Diagnostic Register that indicates if write access has been enabled for the Host Diagnostic Register (e.g., to verify that the Write Sequence data sequence was correct or to verify that writes to the Host Diagnostic Register have been disabled).

R **Reserved** **[31:4]**
Reserved for future use.

WSKEY **Write Sequence KEY (Read/Write)** **[3:0]**
KEY field for Write Sequence as described above.

Register: 0x008
Host Diagnostic Register
Read/Write

31															16
R															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15							8	7	6	5	4	3	2	1	0
R								DWE	FBS	RH	R	TTLI	RA	DisARM	DME
0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	0

The Host Diagnostic Register contains low level diagnostic controls and status information.

R **Reserved** **[31:8]**
Reserved for future use.

DWE **Diagnostic Write Enable (Read Only)** **7**
When set to “1”, this bit indicates that write access to the Host Diagnostic Register may occur. This bit is set as a result of writing the correct key sequence into the Write Sequence Register.

FBS **Flash Bad Signature (Read Only)** **6**
When set to “1”, this bit indicates that the IOP ARM processor has attempted to boot from Flash ROM but encountered a bad Flash signature. When this occurs, the DisARM bit in this register is set to “1” (holding the IOP ARM reset) until both the FlashBadSignature and DisARM conditions are cleared by the Host.

RH **Reset History** **5**
When set to “1”, this bit indicates that physical reset (POR, PCI, or Test Reset/) has occurred within the LSIFC919 device. This bit may be written to zero by a Host driver to help coordinate error/reset recovery between multiple driver instances in a multifunction PCI implementation.

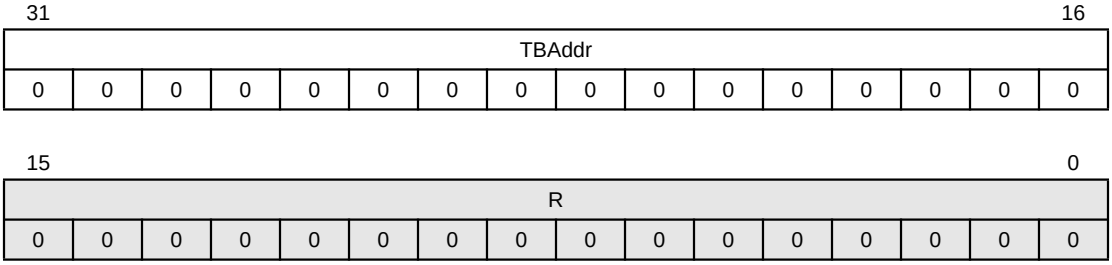
R **Reserved** **4**
Reserved for future use.

TTLI	**TTL Interrupt (Read/Write)** This bit configures the PCI INTA/ pin as either open drain or TTL. This bit defaults to “0” (open drain) on reset and should only be set to “1” when the device is being tested on a tester.	**3**
RA	**Reset Adapter (Write Only)** When set to “1”, this bit will cause a Soft Reset condition within the LSIFC919 design. The bit is self-cleared after eight PCI clock periods. After this bit is deasserted, the IOP ARM will be executing from its default Reset Vector.	**2**
DisARM	**Disable ARM (Read/Write)** When set to “1”, this bit causes the IOP ARM to be held reset. This bit primarily enables downloading of code/data by a Host resident utility.	**1**
DME	**Diagnostic Memory Enable (Read/Write)** When set to “1”, this bit enables Diagnostic Memory accesses using PCI Memory 1 address space. If writes/reads to Memory 1 space are attempted with this bit cleared to “0”, they are properly terminated on the PCI bus, but are not NOP’d by the chip.	**0**

Register: 0x00C

Test Base Address Register

Read/Write



The Test Base Address Register specifies the base address for Diagnostic Memory (Memory 1) access.

TBAddr **Test Base Address (Read/Write)** **[31:16]**
These are significant bits that are determined by the size of Diagnostic Memory (programmed using serial EEPROM).

R **Reserved** **[15:0]**
Reserved for future use.

Register: 0x030
Host Interrupt Status Register
Read Only

31	30														16
IOPDS	R														
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15											4	3	2	1	0
R												RI	R		DI
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Host Interrupt Status Register provides read only interrupt status information to the PCI Host. A write of any value to this register clears the interrupt associated with the System Doorbell.

IOPDS — **IOP Doorbell Status (Read Only)** — **31**
When set to “1”, this bit indicates that the IOP has received a *System: IOP Doorbell* message but has not yet processed it (has not cleared the corresponding SysReq interrupt).

R — **Reserved** — **[30:4]**
Reserved for future use.

RI — **Reply Interrupt (Read Only)** — **3**
Reply Interrupt – set to “1” when:

1. Std reply option – whenever the ReplyPostFIFO is not empty.
2. Alt reply option – whenever the Host Index Register is not equal to the ReplyPostWrPtr register.

If this bit is set to “1” and the corresponding mask bit in the Host Interrupt Mask Register is cleared to “0”, a PCI INTA/ interrupt will be generated.

R — **Reserved** — **[2:1]**
Reserved for future use.

DI — **Doorbell Interrupt (Read Only)** — **0**
This bit is the System Doorbell Interrupt. It is set to “1” when the IOP writes a value to the System Doorbell. It is cleared by a write of any value to this register. If this bit is set to “1” and the corresponding mask bit in the Host Interrupt Mask Register is cleared to “0”, a PCI INTA/ interrupt is generated.

Register: 0x034

Host Interrupt Mask Register
Read/Write

31															16
R															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15											4	3	2	1	0
R												RIM	R		DIM
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

The Host Interrupt Mask Register masks the interrupt conditions reported in the Host Interrupt Status Register.

R — **Reserved** — **[31:4]**
Reserved for future use.

RIM — **Reply Interrupt Mask (Read/Write)** — **3**
When set to “1”, this bit masks the Reply Interrupt condition (prevents the assertion of PCI INTA/).

R — **Reserved** — **[2:1]**
Reserved for future use.

DIM — **Doorbell Interrupt Mask (Read/Write)** — **0**
When set to “1”, this bit masks the System Doorbell Interrupt condition (prevents the assertion of PCI INTA/).

Register: 0x040
Request FIFO
Write Only

31															16
ReqMFA (Most Significant)															
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

15															0
ReqMFA (Least Significant)															
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The Request FIFO is used to accept Request Post MFAs from the Host on writes.

ReqMFA **Request MFA (Write)** **[31:0]**
Writes: Request Post MFA.

Register: 0x044
Reply FIFO
Read/Write

31															16
RepMFA (Most Significant)															
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

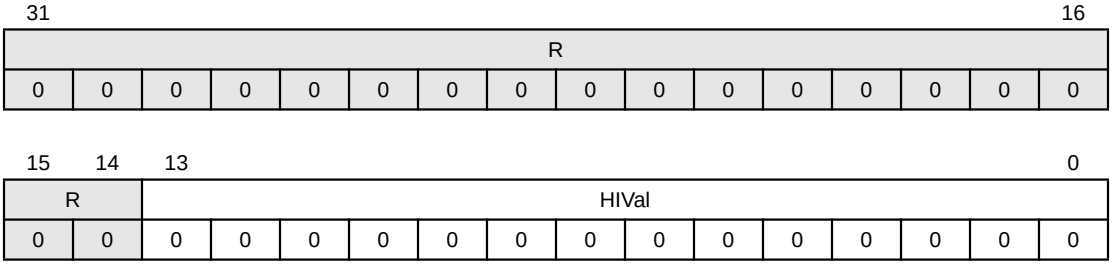
15															0
RepMFA (Least Significant)															
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The Reply FIFO provides Reply Post MFAs to the Host on reads and to accept Reply Free MFAs from the Host on writes.

RepMFA **Reply MFA (Read/Write)** **[31:0]**
Reads: Reply Post MFA (0xFFFFFFFF = EMPTY).

Writes: Reply Free MFA.

Register: 0x050
Host Index Register
Read/Write



The Host Index Register is used with the Outbound Reply Option (AltReplyPost method) to enable Host resident reply post queues. The Host Index provides an indication of which Reply Post MFA's the Host has processed and is used to generate Reply Interrupts when the AltReplyPost option is enabled.

R	**Reserved** *Reserved for future use.*	**[31:14]**
HIVal	**Host Index Value (Read/Write)**	**[13:0]**

5.8 Shared Memory

A region of Shared Memory (LSIFC919 local memory mapped to System Addresses) is provided to allow the Host to write Request Message Frames into it. This is the default method (PUSH model) for Request Message Frame transport, where the Host itself copies the Request Message Frame into the LSIFC919 local memory. The total size of Shared Memory is configured by the I/O Processor on reset. Supported values are 32 Kbytes, 64 Kbytes, 128 Kbytes (default), 256 Kbytes, and 512 Kbytes. Shared memory is accessible only through Mem0 space starting at address 0x080.

Chapter 6
Specifications

This chapter provides a description of the DC and AC Electrical Characteristics of the LSIFC919 Single Channel Fibre Channel I/O Processor chip, and the available packaging. The chapter contains the following sections:

- Section 6.1, “Electrical Requirements”
- Section 6.2, “AC Timing”
- Section 6.3, “Packaging”
- Section 6.4, “Mechanical Drawing”
- Section 6.5, “Package Thermal Considerations”

6.1 Electrical Requirements

Table 6.1 provides absolute maximum stress ratings for the LSIFC919, while Table 6.2 specifies the normal operating conditions. Table 6.4 through Table 6.9 specify the input and output electrical characteristics.

Table 6.1 Absolute Maximum Stress Ratings[1]

Symbol	Parameter	Min	Max	Unit	Test Conditions
T_{STG}	Storage temperature	– 55	150	C	–
V_{DD}	Supply voltage	– 0.5	4.5	V	–
V_{IN}	Input Voltage	V_{SS} – 0.3	V_{DD} + 0.3	V	–
I_{LP}[2]	Latch-up current	± 150	–	mA	–
ESD	Electrostatic discharge	–	1.5 k	V	MIL-STD 883C, Method 3015.7

1. Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions section of the manual is not implied.
2. – 3 V < V_{PIN} < 6.6 V.

Table 6.2 Operating Conditions[1]

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{DDC}	Core supply voltage	2.37	2.63	V	–
V_{DDIO}	I/O supply voltage	3.13	3.47	V	–
PCI5VREF	PCI 5 V reference voltage	4.75	5.25	V	5 V PCI System
		–	VDDIO	V	3.3 V PCI System
T_A	Operating free air	0	70	C	–
θ_{JA}[2]	Thermal resistance (junction to ambient air)	–	20	C/W	–

1. Conditions that exceed the operating limits may cause the device to function incorrectly.
2. θ_{JAmax} assumes a 4-layer package substrate, a 329-pad PBGA, and a 4-layer PCB design (10–12 watt/meter °K).

Table 6.3 Capacitance

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input capacitance of input pads	–	7	pF	–
C_{IO}	Input capacitance of I/O pads	–	10	pF	–

Table 6.4 Input Signals (FAULT, ROMSIZE[1:0], ARMEN/, FSELZ[1:0], MODE[7:0], SWITCH, HOTSWAPEN/)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	0.7 V_{DD}	V_{DD} + 0.3	V	–
V_{IL}	Input low voltage	V_{SS} – 0.3	0.2 V_{DD}	V	–
I_{IN}	Input leakage	10	10	µA	–

Table 6.5 Schmitt Input Signals (REFCLK, TESTRESET/, ZCLK, TCK, TDI, TRST/, TMS_CHIP, TMS_ICE)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.3	V	–
V_{IL}	Input low voltage	V_{SS} – 0.3	0.8	V	–
I_{IN}	Input leakage	10	10	µA	–

Table 6.6 4 mA Bidirectional Signals (LIPRESET/, ODIS, BYPASS/, MD[31:0], MA[21:0], MWE[1:0]/, FLASHCS/, BWE[3:0]/, RAMCS/, ZZ, MP[3:0], SCL, SDA, RXLOS, ADSC/, ADV/, TDO)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	0.7 V_{DD}	V_{DD} + 0.3	V	–
V_{IL}	Input low voltage	V_{SS} – 0.3	0.2 V_{DD}	V	–
V_{OH}	Output high voltage	2.4	V_{DD}	V	– 4 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	4 mA
I_{OZ}	3-state leakage	– 10	10	µA	–

Table 6.7 8 mA Bidirectional Signals (MODDEF[2:0], GPIO[3:0], MOE[1:0]/, LED[4:0]/, MCLK)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	0.7 V_{DD}	V_{DD} + 0.3	V	–
V_{IL}	Input low voltage	V_{SS} – 0.3	0.2 V_{DD}	V	–
V_{OH}	Output high voltage	2.4	V_{DD}	V	– 8 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	8 mA
I_{OZ}	3-state leakage	– 10	10	µA	–

Table 6.8 PCI Input Signals (PCICLK, GNT/, IDSEL, RST/)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	5 V PCI System
		0.5 V_{DD}	5.5	V	3.3 V PCI System
V_{IL}	Input low voltage	– 0.5	0.8	V	5 V PCI System
		– 0.5	0.3 V_{DD}		3.3 V PCI System

Table 6.9 PCI Bidirectional Signals (AD[63:0], C_BE[7:0]/, FRAME/, IRDY/, TRDY/, STOP/, PERR/, PAR, ACK64/, ENUM/, 64EN/)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	5 V PCI System
		0.5 V_{DD}	5.5	V	3.3 V PCI System
V_{IL}	Input low voltage	– 0.5	0.8	V	5 V PCI System
		– 0.5	0.3 V_{DD}		3.3 V PCI System
V_{OH}	Output high voltage	0.9V_{DD}	V_{DD}	V	– 0.5 mA (3.3 V PCI)
V_{OH}	Output high voltage	2.4	–	V	– 2 mA (5 V PCI)
V_{OL}	Output low voltage	V_{SS}	0.1V_{DD}	V	1.5 mA (3.3 V PCI)
V_{OL}	Output low voltage	–	0.55	V	3 mA, 6 mA (5 V PCI)[1]
I_{OZ}	3-state leakage	– 10	10	µA	–

1. Signals without pull-up resistors meet a 3 mA output current load. Signals requiring pull-ups meet a 6 mA output current load. The latter include, **FRAME/**, **TRDY/**, **IRDY/**, **STOP/**, **PERR/**, and, when used, **AD[63:32]**, **C_BE[7:4]**, and **ACK64/**.

Table 6.10 PCI Output Signals (PAR64, REQ/, REQ64/, DEVSEL/, SERR/, INTA/, INTB/)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	0.9V_{DD}	V_{DD}	V	– 0.5 mA (3.3 V PCI)
V_{OH}	Output high voltage	2.4	–	V	– 2 mA (5 V PCI)
V_{OL}	Output low voltage	V_{SS}	0.1V_{DD}	V	1.5 mA (3.3 V PCI)
V_{OL}	Output low voltage	–	0.55	V	3 mA, 6 mA (5 V PCI)[1]
I_{OZ}	3-state leakage	– 10	10	µA	–

1. Signals without pull-up resistors meet a 3 mA output current load. Signals requiring pull-ups meet a 6 mA output current load. The latter include, **DEVSEL/**, **SERR/**, **INTA/**, **INTB/**, and, when used, **PAR64**, and **REQ64/**.

6.2 AC Timing

The AC characteristics described in this section apply over the entire range of operating conditions. Chip timings are based on simulation at worst case voltage, temperature, and processing. Timings were developed with a load capacitance of 50 pF.

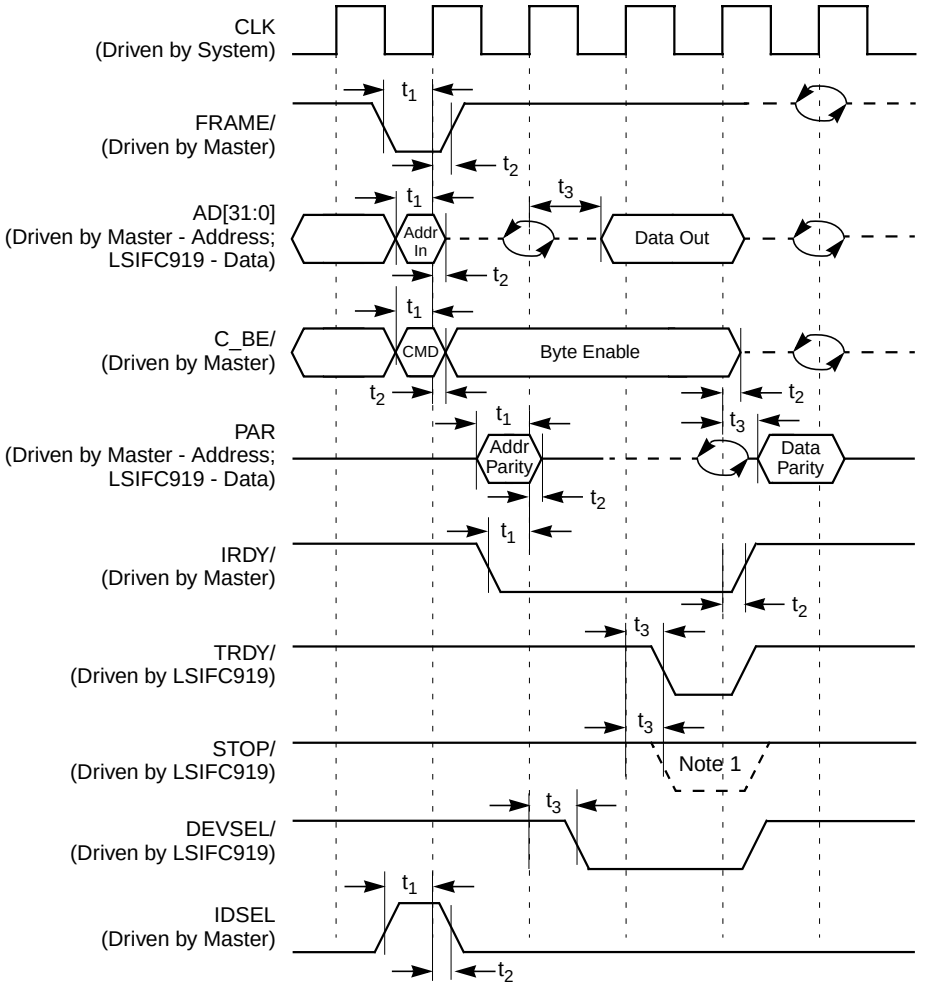
6.2.1 PCI Interface Timing Diagrams

Figure 6.1 through Figure 6.10 represent signal activity when the LSIFC919 accesses the PCI bus. The timings for the PCI bus are listed on page 6-17. The LSIFC919 conforms to the *PCI Local Bus Specification, Revision 2.2.* The timing specifications are provided here for ease of reference only.

Timing diagrams included in this section:

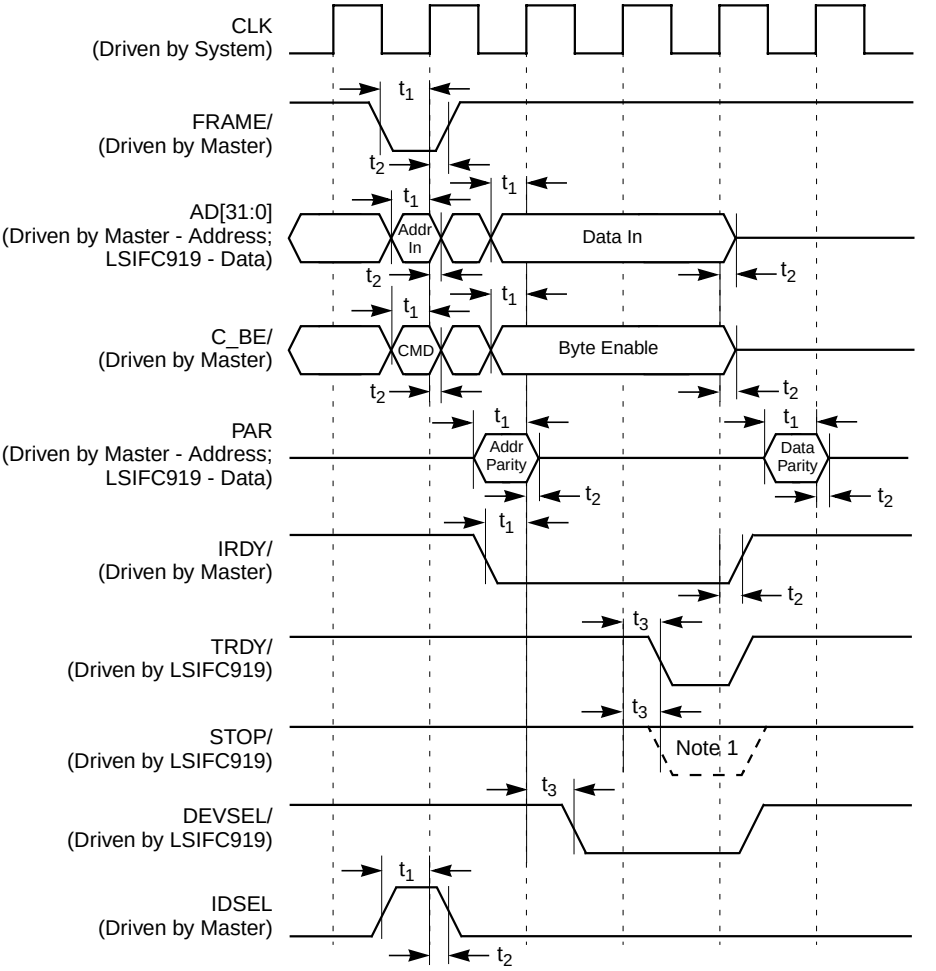
- Configuration Register Read
- Configuration Register Write
- Operating Register Read
- Operating Register Write
- Back-to-Back Read
- Back-to-Back Write
- Burst Read
- Burst Write
- Read With 64-Bit Initiator and 64-Bit Target
- 64-Bit Dual-Address Cycle

Figure 6.1 Configuration Register Read



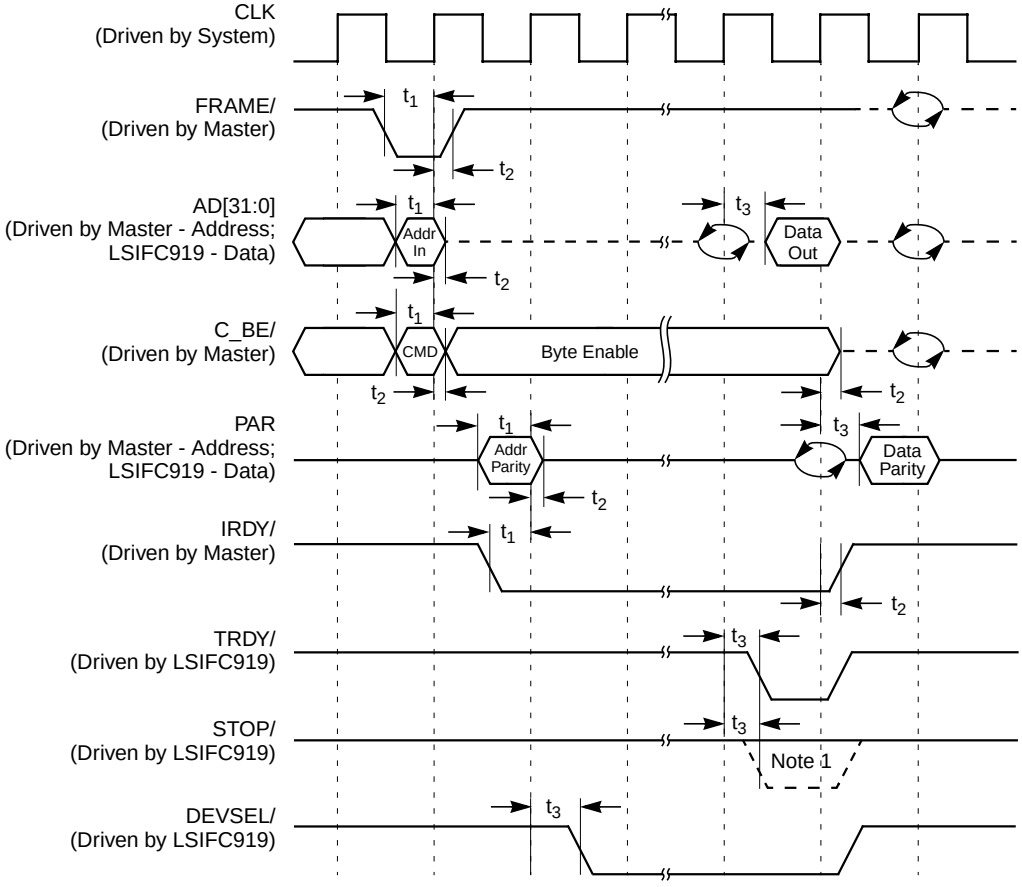
Note: STOP/ is only asserted low if the Master attempts a burst (i.e., FRAME/ is still asserted low) or if the LSIFC919 issues a retry.

Figure 6.2 Configuration Register Write



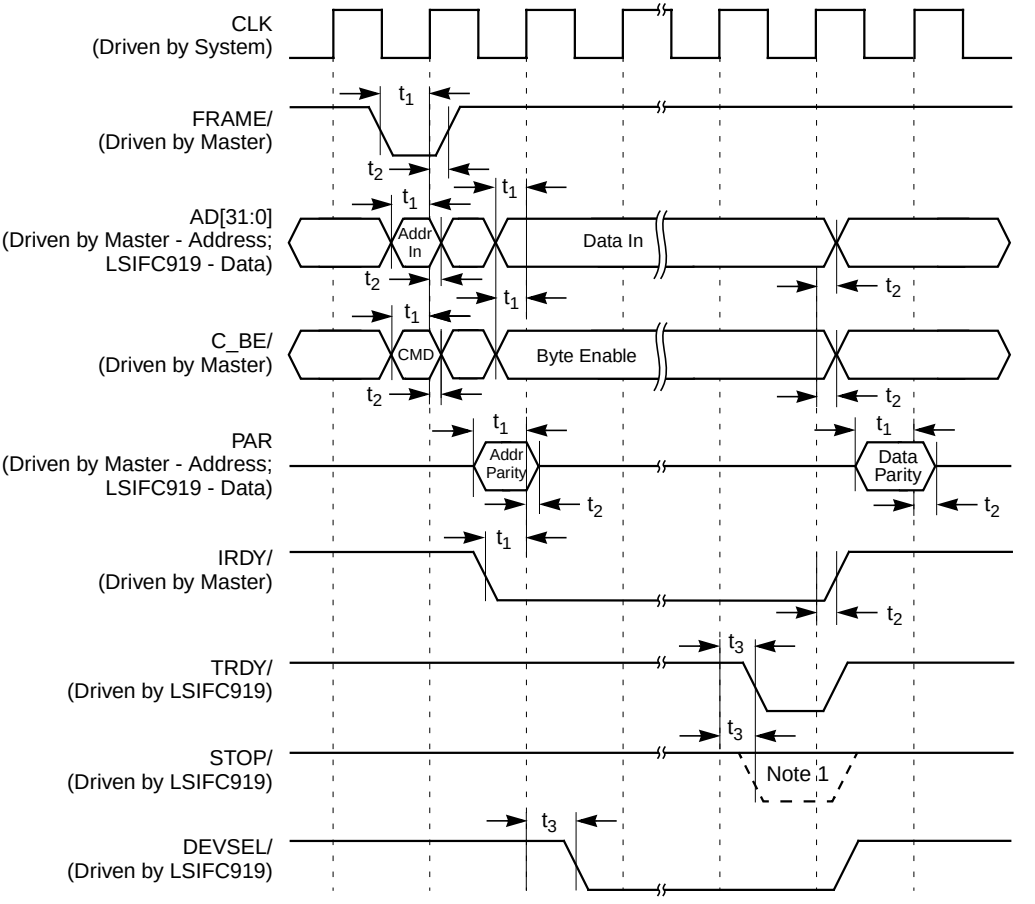
Note: STOP/ is only asserted low if the Master attempts a burst (i.e., FRAME/ is still asserted low.)

Figure 6.3 Operating Register Read



Note: STOP/ is only asserted low if the Master attempts a burst (i.e., FRAME/ is still asserted low).

Figure 6.4 Operating Register Write



Note: STOP/ is only asserted low if the Master attempts a burst (i.e., FRAME/ is still asserted low) or if the LSIFC919 issues a retry.

Figure 6.5 Back-to-Back Read

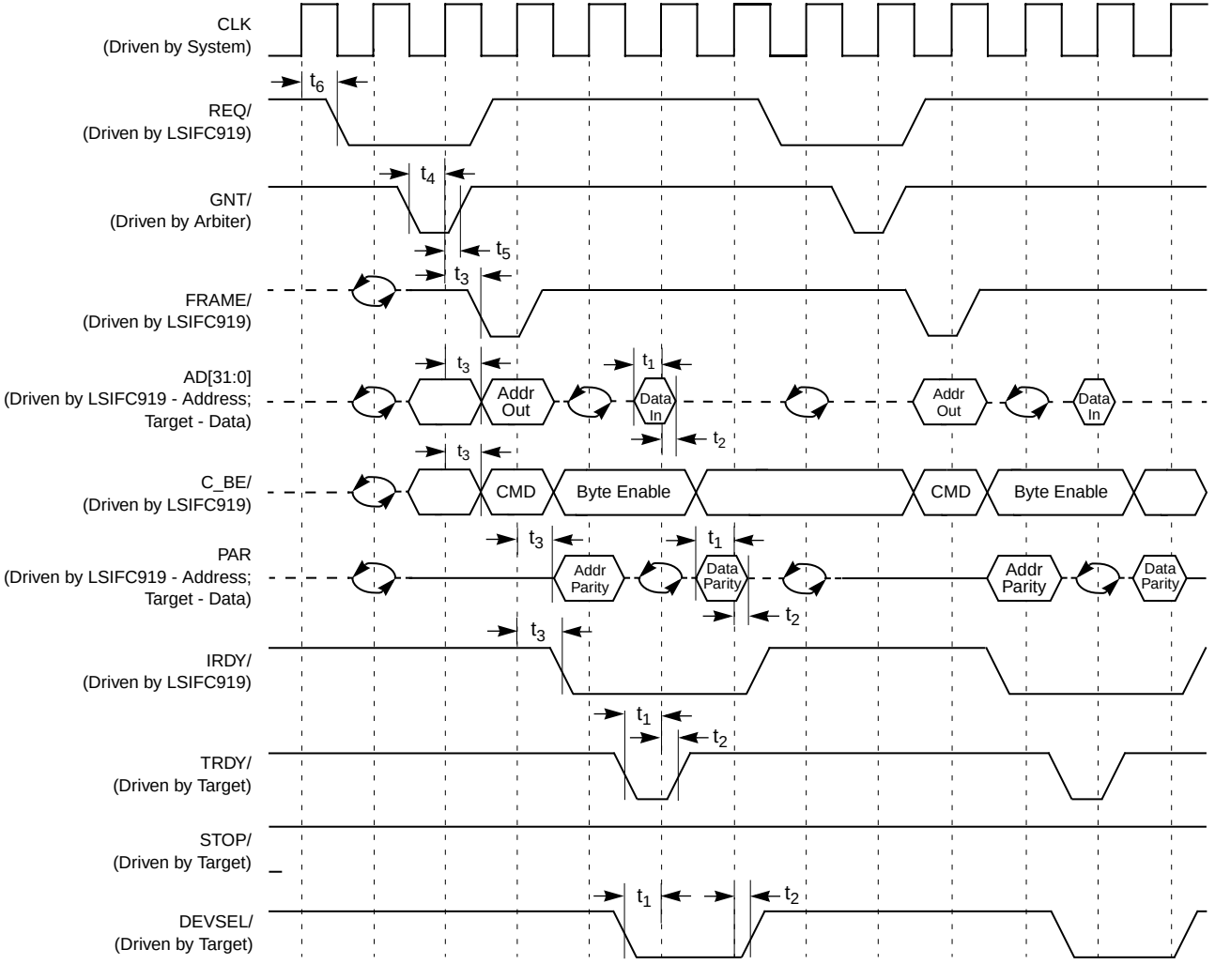


Figure 6.6 Back-to-Back Write

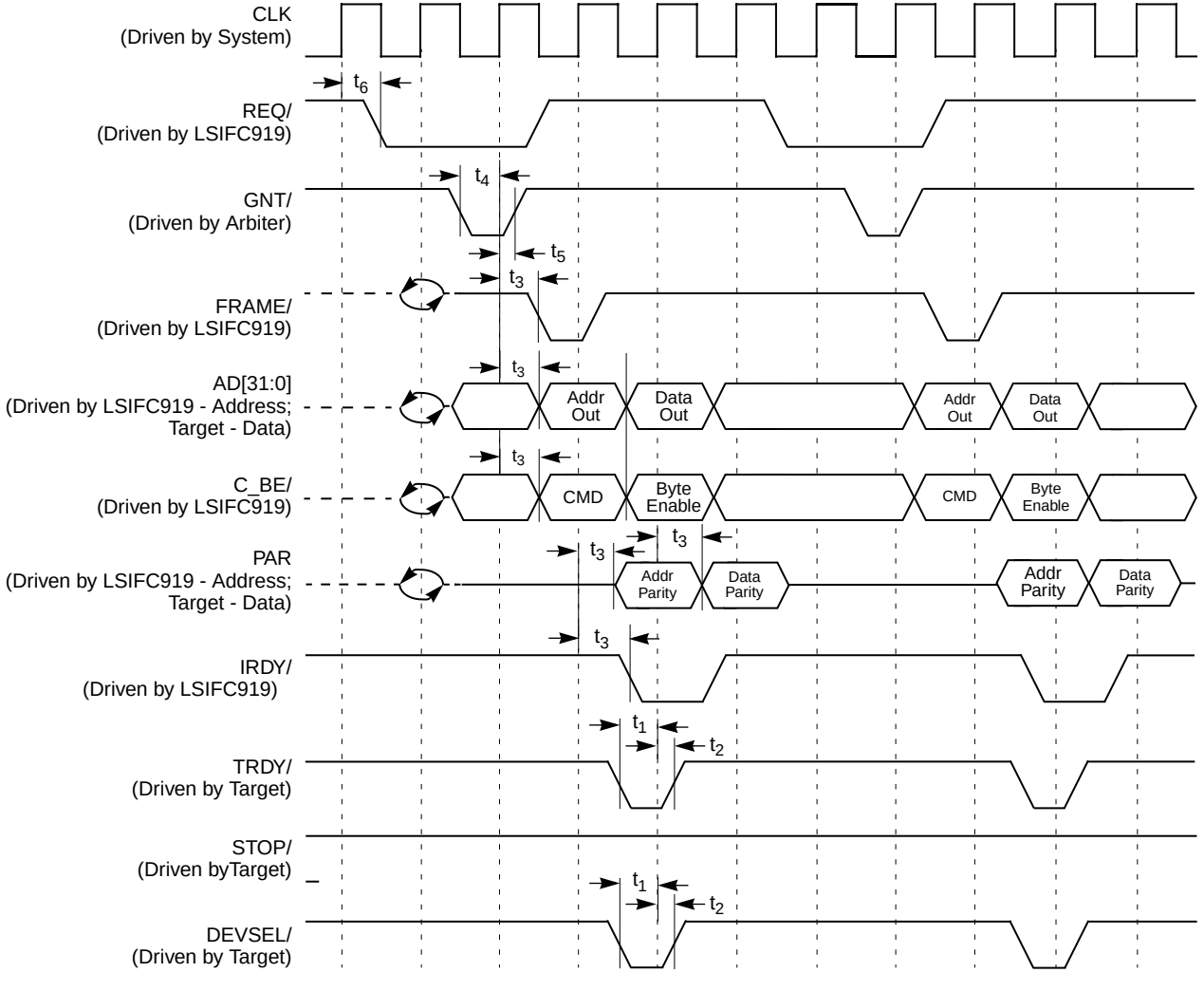


Figure 6.7 Burst Read

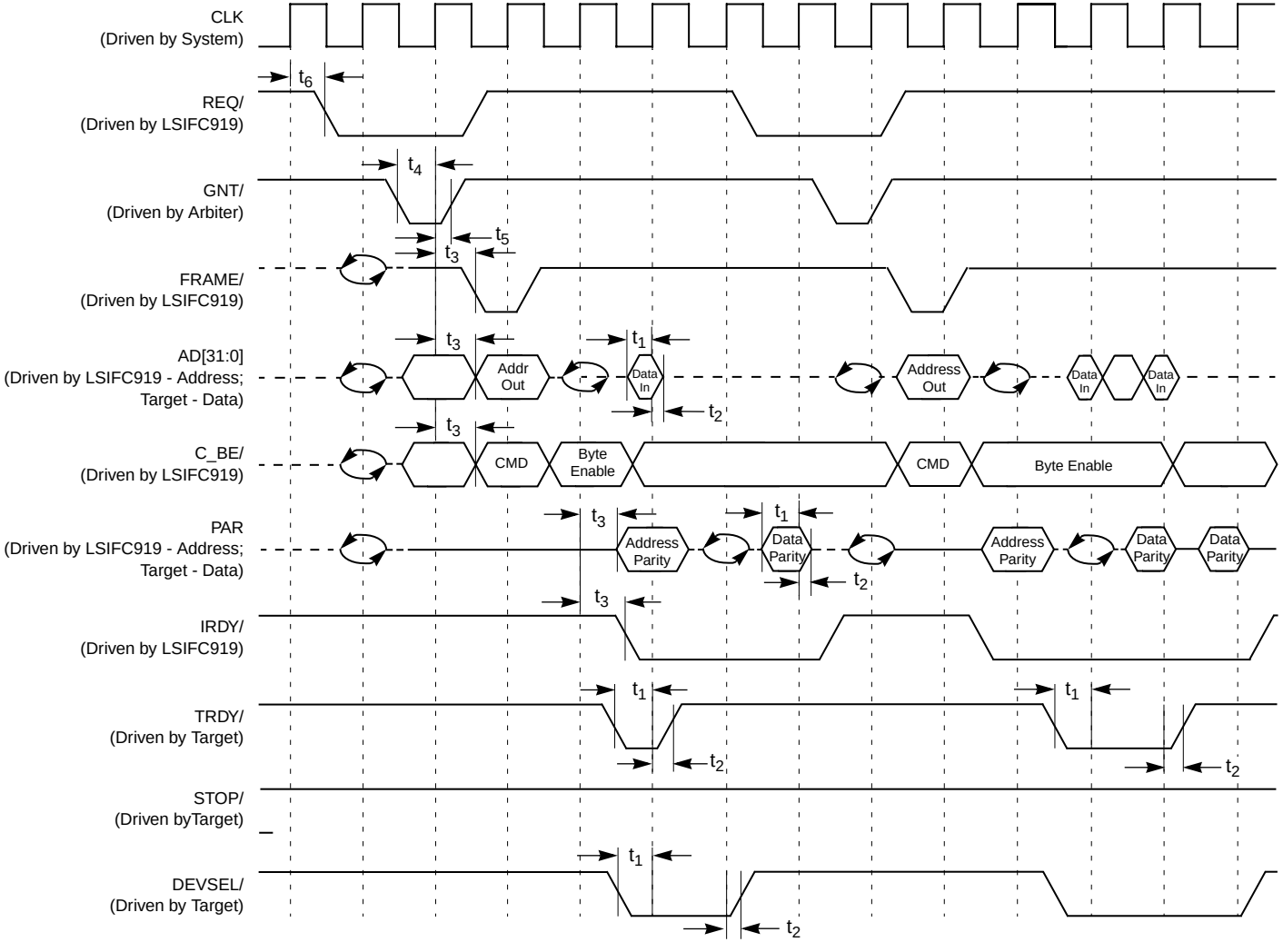


Figure 6.8 Burst Write

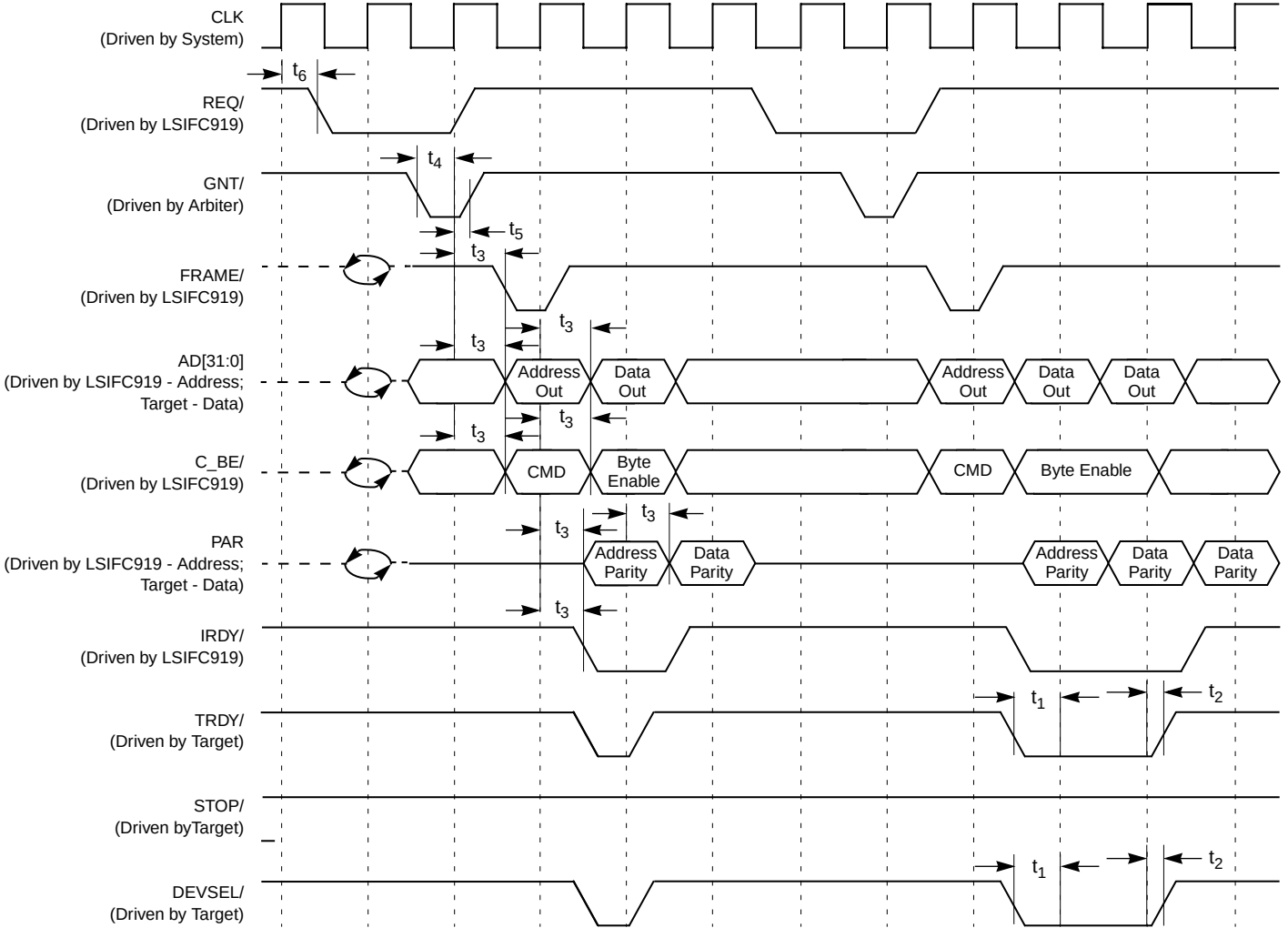


Figure 6.9 Read With 64-Bit Initiator and 64-Bit Target

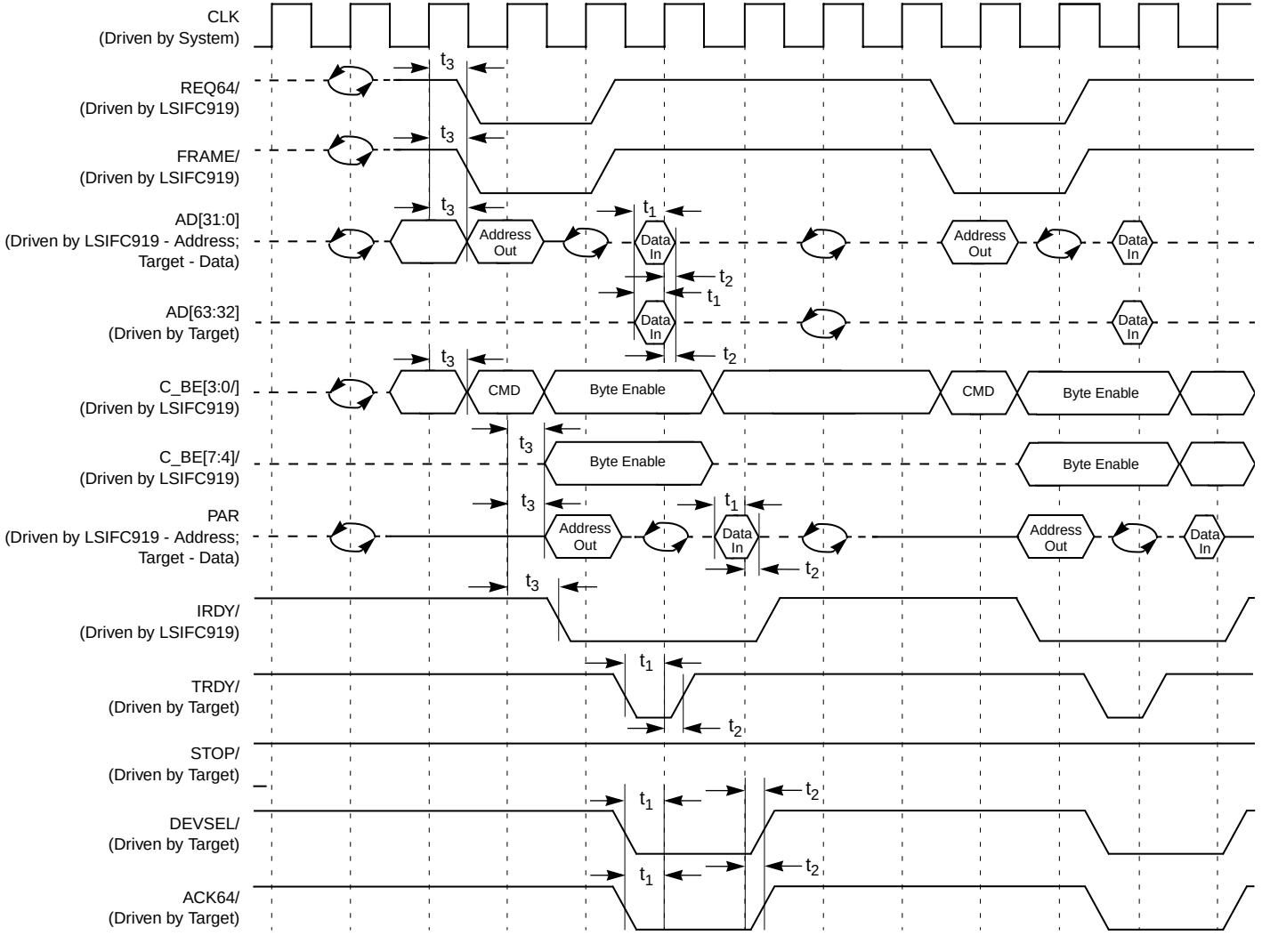
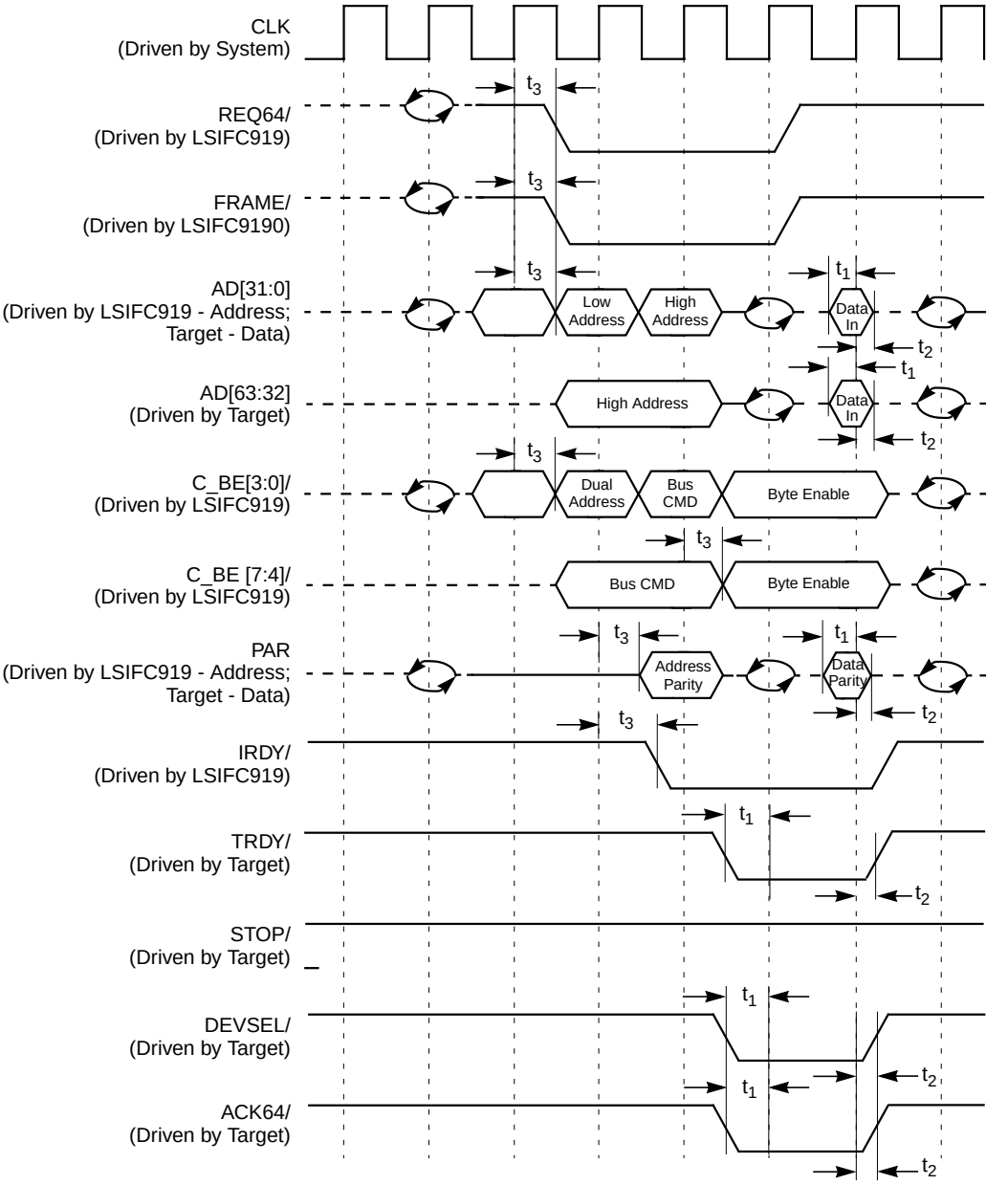


Figure 6.10 64-Bit Dual-Address Cycle



6.2.1.1 PCI Interface Timings

Table 6.11 PCI Interface Timings

Symbol	Parameter	33 MHz		66 MHz		Unit
		Min	Max	Min	Max	
t_1	Shared signal input setup time	7	–	3	–	ns
t_2	Shared signal input hold time	0	–	0	–	ns
t_3	CLK to shared signal output valid	2	11	2	6	ns
t_4	Side signal input setup time	10	–	5	–	ns
t_5	Side signal input hold time	0	–	0	–	ns
t_6	CLK to side signal output valid	2	12	2	6	ns

6.2.2 Fibre Channel Interface Timings

The LSIFC919 receiver and transmitter serial differential signal pairs conform to the electrical and timing standards as shown in the Fibre Channel Physical Interface specification (FC-PI, Rev. 11). All hardware validation testing performed by LSI Logic guarantees that the LSIFC919 meets or exceeds the specifications contained in that document.

6.2.3 Memory Interface Timings

6.2.3.1 SSRAM Timings

Figure 6.11 SSRAM Read/Write/Read Timing Waveforms

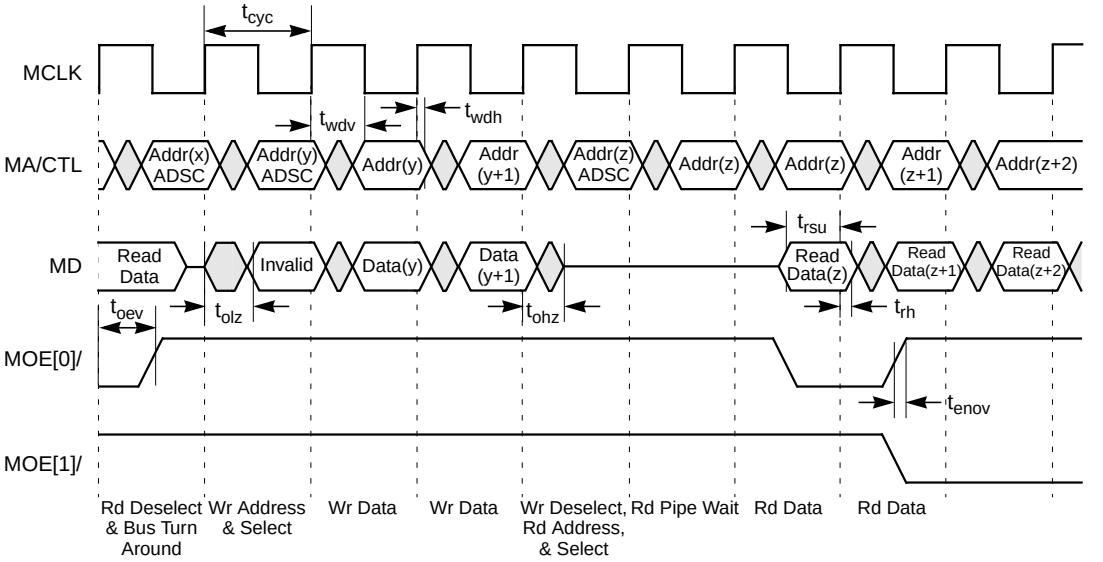


Table 6.12 SSRAM Read/Write/Read Timings

Symbol	Parameter	Min	Max	Unit
t_{cyc}	MCLK cycle time	14.115 [1]	14.119 [1]	ns
t_{rsu}	Read setup time	7	–	ns
t_{rh}	Read hold time	0	–	ns
t_{wdv}	Write valid time	–	10	ns
t_{wdh}	Write hold time	2	–	ns
t_{oev}	Output enable valid	–	8	ns
t_{olz}	Data low impedance	2.5	12	ns
t_{ohz}	Data high impedance	2	12	ns
t_{enov}	Output enable non-overlap	0	–	ns

1. The settings of FSELZ[1:0] determine the minimum and maximum MCLK cycle time. The values shown above are for FSELZ[1:0] = 01 (MCLK = 70.833 MHz).

6.2.3.2 Flash Timings

Figure 6.12 Flash ROM Read Timing Waveforms

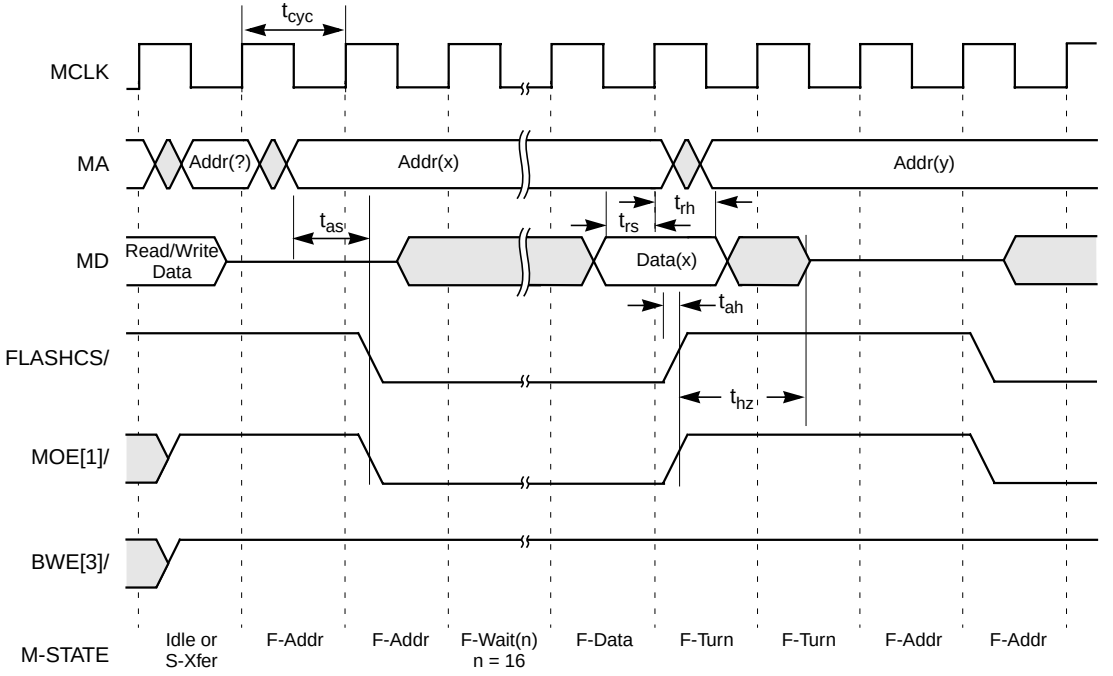


Table 6.13 Flash ROM Read Timings

Symbol	Parameter	Min	Max	Unit
t_{cyc}	MCLK cycle time	14.115 [1]	14.119 [1]	ns
t_{as}	Address setup time	– 5.0 [2]	1 – MCLK [2]	ns
t_{ah}	Address hold time	0	–	ns
t_{rs}	Read setup time	7	–	ns
t_{rh}	Read hold time	0	–	ns
t_{hz}	Data high impedance	0	32	ns

1. The settings of FSELZ[1:0] determine the minimum and maximum MCLK cycle time. The values shown above are for FSELZ[1:0] = 01 (MCLK = 70.833MHz).
2. Address setup time defaults to one (1) MCLK but may be programmed to zero (0) MCLKs using the serial EEPROM.

Figure 6.13 FLASH ROM Write Timing Waveforms

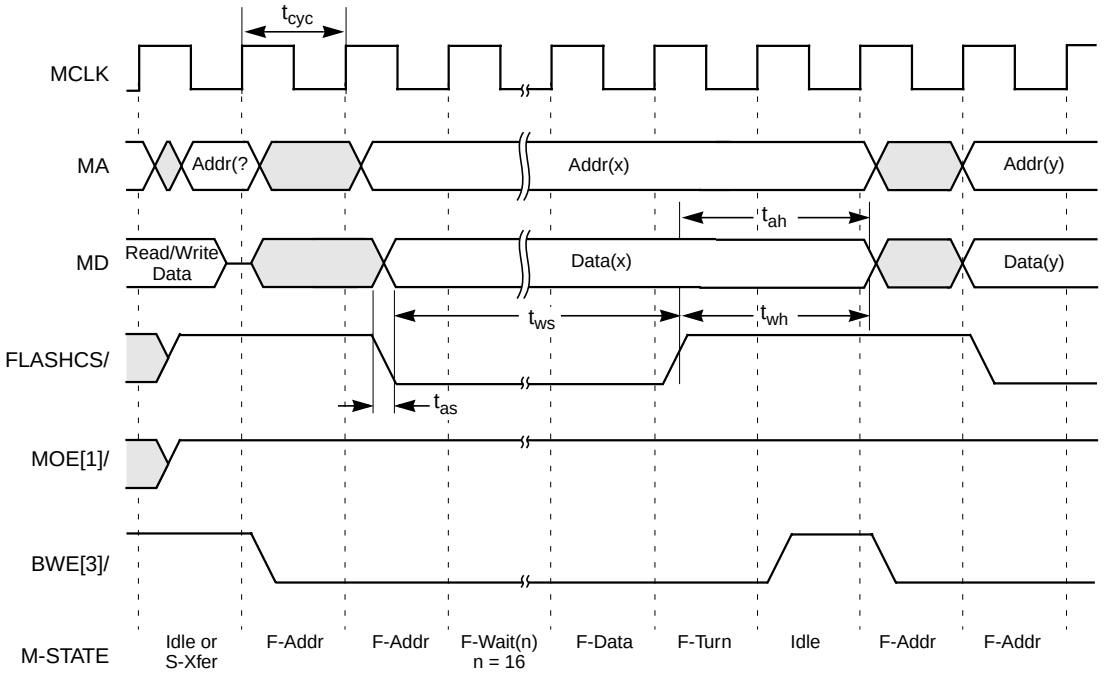


Table 6.14 FLASH ROM Write Timings

Symbol	Parameter	Min	Max	Unit
t_{cyc}	MCLK cycle time	14.115 [1]	14.119 [1]	ns
t_{as}	Address setup time	– 5.0[2]	1 – MCLK[2]	ns
t_{ah}	Address hold time	1 MCLK	–	ns
t_{ws}	Write setup time	3[3]	11[3]	MCLK
t_{wh}	Write hold time	1 – MCLK	–	ns

1. The settings of FSELZ[1:0] determine the minimum and maximum MCLK cycle time. The values shown above are for FSELZ[1:0] = 01 (MCLK = 70.833 MHz).
2. Address setup time defaults to one (1) MCLK but may be programmed to zero (0) MCLKs using the serial EEPROM.
3. Programmed using the serial EEPROM.

6.3 Packaging

The signal locations for the 329 Ball Grid Array (BGA) are illlustrated in Figure 6.14. Table 6.14 lists the LSIFC919 signals in alphanumeric order by BGA position. Table 6.15 lists the LSIFC919 signals alphanumerically by signal name.

Figure 6.14 LSIFC919 Pinout (329-Pin BGA) Top View

	1	2	3	4	5	6	7	8	9	10	11	12
A	SWITCH	PLLZVSS	FSELZ[1]	GPIO[3]	MODE[7]	MODE[3]	MODE[0]	LED[2]/	MOD DEF[2]	NC	TEST RESET/	ROMSIZE[0]
B	TMS_CHIP	IDDTN	ZCLK	FSELZ[0]	GPIO[0]	MODE[4]	MODE[1]	LED[3]/	LED[0]/	NC	NC	SDA
C	TRST/	PROC_ DRVLS	VSSIO	PLLZVDD	GPIO[2] (BLUELED/)	MODE[6]	MODE[2]	LED[4]/	LED[1]/	MOD DEF[1]	NC	ROMSIZE[1]
D	TDI	TMS_ICE	TCK	VSSIO	GPIO[1]	MODE[5]	VDDIO	VSSC	VDDC	VDDIO	MOD DEF[0]	VSSIO
E	NC	REFCLK	TDO	VSSC								
F	VDDC	VSSC	NC	VDDC								
G	NC	NC	VSSC	VDDIO								
H	NC	NC	VDDC	VDDC								
J	NC	VSSC	VSSC	VDDC								
K	RXVDD	RXVDD	NC	VDDIO						VSSIO	VSSIO	VSSIO
L	RX-	RX+	RXBVSS	RTRIM						VSSIO	VSSIO	VSSIO
M	RXBVDD	TXBVDD	HOTSWAPEN/	VSSIO						VSSIO	VSSIO	VSSIO
N	TX-	TX+	TXBVSS	VDDC						VSSIO	VSSIO	VSSIO
P	TXVDD	TXVSS	RXLOS	VDDIO						VSSIO	VSSIO	VSSIO
R	LIPRESET/	FAULT/	ODIS	VSSC								
T	BYPASS/	NC	RST/	NC								
U	INTB/	INTA/	PCI5VREF	VDDIO								
V	GNT/	REQ/	AD[31]	VDDC								
W	AD[30]	AD[29]	AD[28]	VSSC								
Y	AD[27]	AD[26]	PCI5VREF	VSSIO	PCI5VREF	VSSC	VDDIO	VDDC	PCI5VREF	VDDIO	AD[10]	VSSIO
AA	AD[25]	C_BE[3]/	VSSIO	AD[20]	AD[16]	IRDY/	STOP/	PAR	AD[14]	AD[11]	C_BE[0]/	PCI5VREF
AB	AD[24]	AD[23]	AD[22]	AD[18]	C_BE[2]/	TRDY/	PERR/	C_BE[1]/	AD[13]	AD[09]	AD[06]	NC
AC	IDSEL	AD[21]	AD[19]	AD[17]	FRAME/	DEVSEL/	SERR/	AD[15]	AD[12]	AD[08]	AD[07]	AD[05]
	1	2	3	4	5	6	7	8	9	10	11	12

Figure 6.14 LSIFC919 Pinout (329-Pin BGA) Top View (Cont.)

13	14	15	16	17	18	19	20	21	22	23	
MP[0]	MD[01]	MD[05]	MD[08]	MD[11]	MD[14]	MOE[0]/	MWE[0]/	BWE[0]/	BWE[2]/	MCLK	A
ARMEN/	MD[02]	MD[06]	MD[09]	MD[12]	MD[15]	MOE[1]/	MWE[1]/	BWE[3]/	ADV/	MP[2]	B
MD[00]	MD[04]	MD[07]	MD[10]	MD[13]	FLASHCS/	RAMCS/	BWE[1]/	VSSIO	ADSC/	MD[17]	C
MD[03]	VDDIO	VDDC	VSSC	VDDIO	MP[1]	ZZ	VSSIO	MD[16]	MD[18]	MD[19]	D
							VSSC	MD[20]	MD[21]	MD[22]	E
							VDDC	MD[23]	MD[24]	MD[25]	F
							VDDIO	MD[26]	MD[27]	MD[28]	G
							MD[30]	MD[29]	MD[31]	MP[3]	H
							VSSC	MA[00]	MA[01]	MA[03]	J
VSSIO	VSSIO						VDDIO	MA[02]	MA[04]	MA[05]	K
VSSIO	VSSIO						VDDC	MA[07]	MA[08]	MA[06]	L
VSSIO	VSSIO						VSSIO	MA[10]	MA[09]	MA[11]	M
VSSIO	VSSIO						MA[17]	MA[14]	MA[12]	MA[13]	N
VSSIO	VSSIO						VDDIO	MA[20]	MA[15]	MA[16]	P
							MA[21]	AD[32]	MA[18]	MA[19]	R
							AD[35]	AD[36]	AD[34]	AD[33]	T
							VDDIO	PCI5VREF	AD[38]	AD[37]	U
							VDDC	AD[41]	AD[40]	AD[39]	V
							VSSC	AD[44]	AD[43]	AD[42]	W
AD[03]	VDDIO	ACK64/	VDDC	VDDIO	VSSC	PCI5VREF	VSSIO	PCI5VREF	AD[46]	AD[45]	Y
PCICLK	AD[02]	REQ64/	PCI5VREF	PAR64	AD[61]	AD[58]	AD[54]	VSSIO	AD[49]	AD[47]	AA
NC	AD[04]	AD[00]	C_BE[6]/	C_BE[4]/	AD[62]	AD[59]	AD[56]	AD[52]	AD[50]	AD[48]	AB
ENUM/	64EN/	AD[01]	C_BE[7]/	C_BE[5]/	AD[63]	AD[60]	AD[57]	AD[55]	AD[53]	AD[51]	AC
13	14	15	16	17	18	19	20	21	22	23	

Table 6.15 Alphanumeric Pad Listing by BGA Position

BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name
A1	SWITCH	C22	ADSC/	K3	NC	R20	MA[21]	AA9	AD[14]
A2	PLLZVSS	C23	MD[17]	K4	VDDIO	R21	AD[32]	AA10	AD[11]
A3	FSELZ[1]	D1	TDI	K10	VSSIO	R22	MA[18]	AA11	C_BE[0]/
A4	GPIO[3]	D2	TMS_ICE	K11	VSSIO	R23	MA[19]	AA12	PCI5VREF
A5	MODE[7]	D3	TCK	K12	VSSIO	T1	BYPASS/	AA13	PCICLK
A6	MODE[3]	D4	VSSIO	K13	VSSIO	T2	NC	AA14	AD[02]
A7	MODE[0]	D5	GPIO[1]	K14	VSSIO	T3	RST/	AA15	REQ64/
A8	LED[2]/	D6	MODE[5]	K20	VDDIO	T4	NC	AA16	PCI5VREF
A9	MODDEF[2]	D7	VDDIO	K21	MA[02]	T20	AD[35]	AA17	PAR64
A10	NC	D8	VSSC	K22	MA[04]	T21	AD[36]	AA18	AD[61]
A11	TESTRESET/	D9	VDDC	K23	MA[05]	T22	AD[34]	AA19	AD[58]
A12	ROMSIZE[0]	D10	VDDIO	L1	RX-	T23	AD[33]	AA20	AD[54]
A13	MP[0]	D11	MODDEF[0]	L2	RX+	U1	INTB/	AA21	VSSIO
A14	MD[01]	D12	VSSIO	L3	RXBVSS	U2	INTA/	AA22	AD[49]
A15	MD[05]	D13	MD[03]	L4	RTRIM	U3	PCI5VREF	AA23	AD[47]
A16	MD[08]	D14	VDDIO	L10	VSSIO	U4	VDDIO	AB1	AD[24]
A17	MD[11]	D15	VDDC	L11	VSSIO	U20	VDDIO	AB2	AD[23]
A18	MD[14]	D16	VSSC	L12	VSSIO	U21	PCI5VREF	AB3	AD[22]
A19	MOE[0]/	D17	VDDIO	L13	VSSIO	U22	AD[38]	AB4	AD[18]
A20	MWE[0]/	D18	MP[1]	L14	VSSIO	U23	AD[37]	AB5	C_BE[2]/
A21	BWE[0]/	D19	ZZ	L20	VDDC	V1	GNT/	AB6	TRDY/
A22	BWE[2]/	D20	VSSIO	L21	MA[07]	V2	REQ/	AB7	PERR/
A23	MCLK	D21	MD[16]	L22	MA[08]	V3	AD[31]	AB8	C_BE[1]/
B1	TMS_CHIP	D22	MD[18]	L23	MA[06]	V4	VDDC	AB9	AD[13]
B2	IDDTN	D23	MD[19]	M1	RXBVDD	V20	VDDC	AB10	AD[09]
B3	ZCLK	E1	NC	M2	TXBVDD	V21	AD[41]	AB11	AD[06]
B4	FSELZ[0]	E2	REFCLK	M3	HOTSWAPEN/	V22	AD[40]	AB12	NC
B5	GPIO[0]	E3	TDO	M4	VSSIO	V23	AD[39]	AB13	NC
B6	MODE[4]	E4	VSSC	M10	VSSIO	W1	AD[30]	AB14	AD[04]
B7	MODE[1]	E20	VSSC	M11	VSSIO	W2	AD[29]	AB15	AD[00]
B8	LED[3]/	E21	MD[20]	M12	VSSIO	W3	AD[28]	AB16	C_BE[6]/
B9	LED[0]/	E22	MD[21]	M13	VSSIO	W4	VSSC	AB17	C_BE[4]/
B10	NC	E23	MD[22]	M14	VSSIO	W20	VSSC	AB18	AD[62]
B11	SCL	F1	VDDC	M20	VSSIO	W21	AD[44]	AB19	AD[59]
B12	SDA	F2	VSSC	M21	MA[10]	W22	AD[43]	AB20	AD[56]
B13	ARMEN/	F3	NC	M22	MA[09]	W23	AD[42]	AB21	AD[52]
B14	MD[02]	F4	VDDC	M23	MA[11]	Y1	AD[27]	AB22	AD[50]
B15	MD[06]	F20	VDDC	N1	TX-	Y2	AD[26]	AB23	AD[48]
B16	MD[09]	F21	MD[23]	N2	TX+	Y3	PCI5VREF	AC1	IDSEL
B17	MD[12]	F22	MD[24]	N3	TXBVSS	Y4	VSSIO	AC2	AD[21]
B18	MD[15]	F23	MD[25]	N4	VDDC	Y5	PCI5VREF	AC3	AD[19]
B19	MOE[1]/	G1	NC	N10	VSSIO	Y6	VSSC	AC4	AD[17]
B20	MWE[1]/	G2	NC	N11	VSSIO	Y7	VDDIO	AC5	FRAME/
B21	BWE[3]/	G3	VSSC	N12	VSSIO	Y8	VDDC	AC6	DEVSEL/
B22	ADV/	G4	VDDIO	N13	VSSIO	Y9	PCI5VREF	AC7	SERR/
B23	MP[2]	G20	VDDIO	N14	VSSIO	Y10	VDDIO	AC8	AD[15]
C1	TRST/	G21	MD[26]	N20	MA[17]	Y11	AD[10]	AC9	AD[12]
C2	PROC_DRVLS	G22	MD[27]	N21	MA[14]	Y12	VSSIO	AC10	AD[08]
C3	VSSIO	G23	MD[28]	N22	MA[12]	Y13	AD[03]	AC11	AD[07]
C4	PLLZVDD	H1	NC	N23	MA[13]	Y14	VDDIO	AC12	AD[05]
C5	GPIO[2](BLUELED/)	H2	NC	P1	TXVDD	Y15	ACK64/	AC13	ENUM/
C6	MODE[6]	H3	VDDC	P2	TXVSS	Y16	VDDC	AC14	64EN/
C7	MODE[2]	H4	VDDC	P3	RXLOS	Y17	VDDIO	AC15	AD[01]
C8	LED[4]/	H20	MD[30]	P4	VDDIO	Y18	VSSC	AC16	C_BE[7]/
C9	LED[1]/	H21	MD[29]	P10	VSSIO	Y19	PCI5VREF	AC17	C_BE[5]/
C10	MODDEF[1]	H22	MD[31]	P11	VSSIO	Y20	VSSIO	AC18	AD[63]
C11	NC	H23	MP[3]	P12	VSSIO	Y21	PCI5VREF	AC19	AD[60]
C12	ROMSIZE[1]	J1	NC	P13	VSSIO	Y22	AD[46]	AC20	AD[57]
C13	MD[00]	J2	VSSC	P14	VSSIO	Y23	AD[45]	AC21	AD[55]
C14	MD[04]	J3	VSSC	P20	VDDIO	AA1	AD[25]	AC22	AD[53]
C15	MD[07]	J4	VDDC	P21	MA[20]	AA2	C_BE[3]/	AC23	AD[51]
C16	MD[10]	J20	VSSC	P22	MA[15]	AA3	VSSIO		
C17	MD[13]	J21	MA[00]	P23	MA[16]	AA4	AD[20]		
C18	FLASHCS/	J22	MA[01]	R1	LIPRESET/	AA5	AD[16]		
C19	RAMCS/	J23	MA[03]	R2	FAULT/	AA6	IRDY/		
C20	BWE[1]/	K1	RXVDD	R3	ODIS	AA7	STOP/		
C21	VSSIO	K2	RXVDD	R4	VSSC	AA8	PAR		

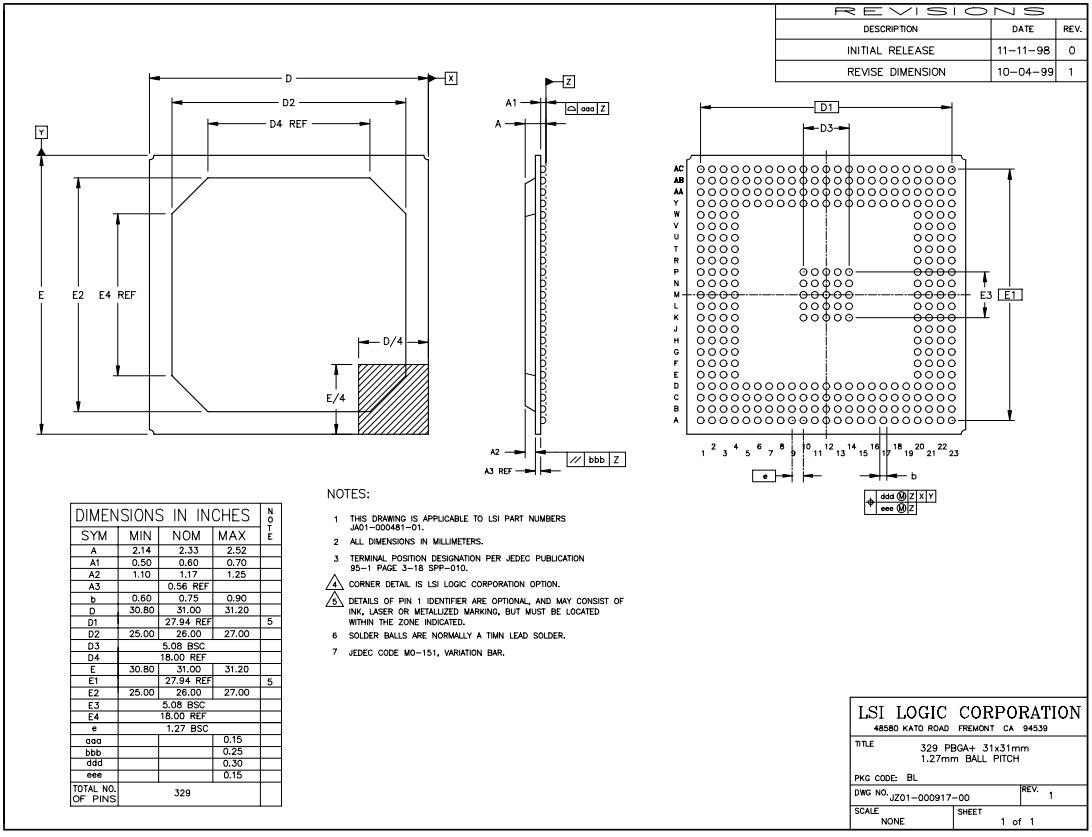
Table 6.16 Alphanumeric Pad Listing by Signal Name

Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos	Signal Name	BGA Pos
64EN/	AC14	ADV/	B22	MD[04]	C14	PCI5VREF	AA16	VDDIO	G4
ACK64/	Y15	ARMEN/	B13	MD[05]	A15	PCI5VREF	U21	VDDIO	K20
AD[00]	AB15	BWE[0]/	A21	MD[06]	B15	PCI5VREF	U3	VDDIO	K4
AD[01]	AC15	BWE[1]/	C20	MD[07]	C15	PCI5VREF	Y19	VDDIO	P20
AD[02]	AA14	BWE[2]/	A22	MD[08]	A16	PCI5VREF	Y21	VDDIO	P4
AD[03]	Y13	BWE[3]/	B21	MD[09]	B16	PCI5VREF	Y3	VDDIO	U20
AD[04]	AB14	BYPASS/	T1	MD[10]	C16	PCI5VREF	Y5	VDDIO	U4
AD[05]	AC12	C_BE[0]/	AA11	MD[11]	A17	PCI5VREF	Y9	VDDIO	Y10
AD[06]	AB11	C_BE[1]/	AB8	MD[12]	B17	PCICLK	AA13	VDDIO	Y14
AD[07]	AC11	C_BE[2]/	AB5	MD[13]	C17	PERR/	AB7	VDDIO	Y17
AD[08]	AC10	C_BE[3]/	AA2	MD[14]	A18	PLLZVDD	C4	VDDIO	Y7
AD[09]	AB10	C_BE[4]/	AB17	MD[15]	B18	PLLZVSS	A2	VSSC	D16
AD[10]	Y11	C_BE[5]/	AC17	MD[16]	D21	PROC_DRVLS	C2	VSSC	D8
AD[11]	AA10	C_BE[6]/	AB16	MD[17]	C23	RAMCS/	C19	VSSC	E20
AD[12]	AC9	C_BE[7]/	AC16	MD[18]	D22	REFCLK	E2	VSSC	E4
AD[13]	AB9	DEVSEL/	AC6	MD[19]	D23	REQ/	V2	VSSC	F2
AD[14]	AA9	ENUM/	AC13	MD[20]	E21	REQ64/	AA15	VSSC	G3
AD[15]	AC8	FAULT/	R2	MD[21]	E22	ROMSIZE[0]	A12	VSSC	J2
AD[16]	AA5	FLASHCS/	C18	MD[22]	E23	ROMSIZE[1]	C12	VSSC	J3
AD[17]	AC4	FRAME/	AC5	MD[23]	F21	RST/	T3	VSSC	J20
AD[18]	AB4	FSELZ[0]	B4	MD[24]	F22	RTRIM	L4	VSSC	R4
AD[19]	AC3	FSELZ[1]	A3	MD[25]	F23	RXBVDD	M1	VSSC	W20
AD[20]	AA4	GNT/	V1	MD[26]	G21	RXBVSS	L3	VSSC	W4
AD[21]	AC2	GPIO[0]	B5	MD[27]	G22	RXLOS	P3	VSSC	Y18
AD[22]	AB3	GPIO[1]	D5	MD[28]	G23	RX-	L1	VSSC	Y6
AD[23]	AB2	GPIO[2](BLUELED/)	C5	MD[29]	H21	RX+	L2	VSSIO	AA21
AD[24]	AB1	GPIO[3]	A4	MD[30]	H20	RXVDD	K1	VSSIO	AA3
AD[25]	AA1	HOTSWAPEN/	M3	MD[31]	H22	RXVSS	K2	VSSIO	C21
AD[26]	Y2	IDDTN	B2	MODDEF[0]	D11	SCL	B11	VSSIO	C3
AD[27]	Y1	IDSEL	AC1	MODDEF[1]	C10	SDA	B12	VSSIO	D12
AD[28]	W3	INTA/	U2	MODDEF[2]	A9	SERR/	AC7	VSSIO	D20
AD[29]	W2	INTB/	U1	MODE[0]	A7	STOP/	AA7	VSSIO	D4
AD[30]	W1	IRDY/	AA6	MODE[1]	B7	SWITCH	A1	VSSIO	K10
AD[31]	V3	LED[0]/	B9	MODE[2]	C7	TCK	D3	VSSIO	K11
AD[32]	R21	LED[2]/	A8	MODE[3]	A6	TDI	D1	VSSIO	K12
AD[33]	T23	LED[1]/	C9	MODE[4]	B6	TDO	E3	VSSIO	K13
AD[34]	T22	LED[3]/	B8	MODE[5]	D6	TESTRESET/	A11	VSSIO	K14
AD[35]	T20	LED[4]/	C8	MODE[6]	C6	TMS_CHIP	B1	VSSIO	L10
AD[36]	T21	LIPRESET/	R1	MODE[7]	A5	TMS_ICE	D2	VSSIO	L11
AD[37]	U23	MA[00]	J21	MOE[0]/	A19	TRDY/	AB6	VSSIO	L12
AD[38]	U22	MA[01]	J22	MOE[1]/	B19	TRST/	C1	VSSIO	L13
AD[39]	V23	MA[02]	K21	MP[0]	A13	TXBVDD	M2	VSSIO	L14
AD[40]	V22	MA[03]	J23	MP[1]	D18	TXBVSS	N3	VSSIO	M10
AD[41]	V21	MA[04]	K22	MP[2]	B23	TX-	N1	VSSIO	M11
AD[42]	W23	MA[05]	K23	MP[3]	H23	TX+	N2	VSSIO	M12
AD[43]	W22	MA[06]	L23	MWE[0]/	A20	TXVDD	P1	VSSIO	M13
AD[44]	W21	MA[07]	L21	MWE[1]/	B20	TXVSS	P2	VSSIO	M14
AD[45]	Y23	MA[08]	L22	NC	A10	VDDC	D9	VSSIO	M20
AD[46]	Y22	MA[09]	M22	NC	B10	VDDC	D15	VSSIO	M4
AD[47]	AA23	MA[10]	M21	NC	C11	VDDC	F1	VSSIO	N10
AD[48]	AB23	MA[11]	M23	NC	E1	VDDC	F4	VSSIO	N11
AD[49]	AA22	MA[12]	N22	NC	F3	VDDC	F20	VSSIO	N12
AD[50]	AB22	MA[13]	N23	NC	G1	VDDC	H3	VSSIO	N13
AD[51]	AC23	MA[14]	N21	NC	G2	VDDC	H4	VSSIO	N14
AD[52]	AB21	MA[15]	P22	NC	H1	VDDC	J4	VSSIO	P10
AD[53]	AC22	MA[16]	P23	NC	H2	VDDC	L20	VSSIO	P11
AD[54]	AA20	MA[17]	N20	NC	J1	VDDC	N4	VSSIO	P12
AD[55]	AC21	MA[18]	R22	NC	K3	VDDC	V20	VSSIO	P13
AD[56]	AB20	MA[19]	R23	NC	T2	VDDC	V4	VSSIO	P14
AD[57]	AC20	MA[20]	P21	NC	T4	VDDC	Y16	VSSIO	Y12
AD[58]	AA19	MA[21]	R20	NC	AB12	VDDC	Y8	VSSIO	Y20
AD[59]	AB19	MCLK	A23	NC	AB13	VDDIO	D10	VSSIO	Y4
AD[60]	AC19	MD[00]	C13	ODIS	R3	VDDIO	D14	ZCLK	B3
AD[61]	AA18	MD[01]	A14	PAR	AA8	VDDIO	D17	ZZ	D19
AD[62]	AB18	MD[02]	B14	PAR64	AA17	VDDIO	D7		
AD[63]	AC18	MD[03]	D13	PCI5VREF	AA12	VDDIO	G20		
ADSC/	C22								

6.4 Mechanical Drawing

Figure 6.15 shows the mechanical drawing for the 329-pad BGA.

Figure 6.15 329-Pad Plastic Ball Grid Array



DIMENSIONS IN INCHES				NOTE
SYM	MIN	NOM	MAX	
A	2.14	2.33	2.52	
A1	0.50	0.60	0.70	
A2	1.10	1.17	1.25	
A3		0.56 REF		
b	0.60	0.75	0.90	
D	30.80	31.00	31.20	
D1		27.94 REF		5
D2	25.00	26.00	27.00	
D3		5.08 BSC		
D4		18.00 REF		
E	30.80	31.00	31.20	
E1		27.94 REF		5
E2	25.00	26.00	27.00	
E3		5.08 BSC		
E4		18.00 REF		
e		1.27 BSC		
aaa			0.15	
bbb			0.25	
ddd			0.30	
eee			0.15	
TOTAL NO. OF PINS		329		

Important: This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code BL.

6.5 Package Thermal Considerations

Thermal management is an important element of electronic product design. In any system environment, it is important not to exceed the maximum recommended semiconductor junction temperature. The maximum recommended junction temperature for the LSIFC919 is 115 ˚C.

To that end, LSI Logic recommends that the customer use an appropriate heat sink for the LSIFC919, and that adequate airflow exists throughout the system.

Allowing for a maximum dynamic power consumption of 4 W, Table 6.16 below shows some examples of the maximum allowable junction temperature to maintain less than a 70 ˚C ambient for the given airflow and heat sink conditions.

Table 6.17 Maximum Allowable Ambient Temperature vs. Airflow

	Airflow (cfm)	θ_{JAmax} (˚C/Watt)	Junction Temperature at 70 ˚C Ambient (˚C)	Maximum Allowable Ambient Temperature (˚C)
With Heat Sink	0	12.2	118.8	66.2
	200	8.4	103.6	81.4
	300	6.8	97.2	87.8
	600	6.0	94.0	91.0
Without Heat Sink	0	16.6	136.4	48.6
	200	14.0	126.0	59.0
	300	13.2	122.8	62.2
	600	12.4	119.6	65.4

Appendix A
Register Summary

Tables A.1 and A.2 list the register summary for the LSIFC919.

Table A.1 LSIFC919 Multifunction PCI Registers

Register Name	Address	Read/Write	Page
Device ID/Vendor ID	0x000	Read Only	5-10
Status/Command	0x004	Read/Write	5-10
Class Code/Revision ID	0x008	Read/Write	5-13
BIST/Header/Latency/Cache Line	0x00C	Read/Write	5-14
I/O Base Address	0x010	Read/Write	5-15
Mem0 Base Address Low	0x014	Read/Write	5-16
Mem0 Base Address High	0x018	Read/Write	5-17
Mem1 Base Address Low	0x01C	Read/Write	5-18
Mem1 Base Address High	0x020	Read/Write	5-19
Reserved	0x024–0x028	Read Only	5-19
Subsystem ID/Vendor ID	0x02C	Read Only	5-19
Expansion ROM Base Address	0x030	Read Only	5-20
Capabilities Pointer	0x034	Read/Write	5-21
Reserved	0x038	Read Only	5-21
Latency/Interrupt	0x03C/0x13C	Read/Write	5-22
Power Management Configuration	0x040	Read Only	5-23
Power Management Control/Status	0x044	Read/Write	5-24
Reserved	0x048–0x07F	Write Only	5-24

Table A.2 LSIFC919 Host Interface Registers

Register Name	Address	Read/Write	Page
System Doorbell Register	0x000	Read/Write	5-27
Write Sequence Register	0x004	Read/Write	5-28
Host Diagnostic Register	0x008	Read/Write	5-29
Test Base Address Register	0x00C	Read/Write	5-31
Host Interrupt Status Register	0x030	Read Only	5-32
Host Interrupt Mask Register	0x034	Read/Write	5-33
Request FIFO	0x044	Write Only	5-34
Reply FIFO	0x044	Read/Write	5-34
Host Index Register	0x050	Read/Write	5-35

Appendix B
Reference Specifications

The LSI Logic LSIFC919 is compliant with the following specifications:

Table B.1 Reference Specifications

Specification	Revision
Fibre Channel Physical Interfaces (FC-PI)	11
Fibre Channel Physical and Signaling Interface (FC-PH)	4.3
Fibre Channel Arbitrated Loop (FC-AL-2)	7.0
FC Private Loop Direct Attach (FC-PLDA)	1.5
Fibre Channel Protocol for SCSI (FCP)	12
GBIC	5.4
PCI Local Bus Specification	2.2

Appendix C
Glossary of Terms and Abbreviations

8B/10B	A data encoding scheme developed by IBM, translating byte wide data to an encoded 10-bit format.
ANSI	American National Standards Institute, the coordinating organization for voluntary standards in the United States.
Arbitrated loop topology (FC-AL)	A FC Topology that provides a low cost solution to attach multiple ports in a loop without switches.
BER	Bit Error Rate.
Bit	A binary digit. The smallest unit of information a computer uses. The value of a bit (0 or 1) represents a two-way choice, such as on or off, true or false, and so on.
Broadcast	Sending a transmission to all N_Ports on a fabric.
Bus	A collection of unbroken signal lines across which information is transmitted from one part of a computer system to another. Connections to the bus are made using taps on the lines.
Bus Mastering	A high-performance way to transfer data. The host adapter controls the transfer of data directly to and from system memory without bothering the computer's microprocessor. This is the fastest way for multitasking operating systems to transfer data.
Byte	A unit of information consisting of eight bits.
Channel	A point-to-point link, the main task of which is to transport data from one point to another.
Configuration	Refers to the way a computer is set up; the combined hardware components (computer, monitor, keyboard, and peripheral devices) that

	make up a computer system; or the software settings that allow the hardware components to communicate with each other.
CPU	Central Processing Unit. The “brain” of the computer that performs the actual computations. The term Micro Processor Unit (MPU) is also used.
Crosspoint-switched topology (FC-XS)	Highest performance FC fabric, providing a choice of multiple path routings between pairs of F_Ports.
DMA	Direct Memory Access. A method of moving data from a storage device directly to RAM, without using the CPU’s resources.
DMA Bus Master	A feature that allows a peripheral to control the flow of data to and from system memory by blocks, as opposed to PIO (Programmed I/O) where the processor is in control and the flow is by byte.
Device Driver	A program that allows a microprocessor (through the operating system) to direct the operation of a peripheral device.
EEPROM	Electronically Erasable Programmable Read Only Memory. A memory chip typically used to store configuration information.
EISA	Extended Industry Standard Architecture. An extension of the 16-bit ISA bus standard. It allows devices to perform 32-bit data transfers.
Exchange	A term that refers to one of the FC “building blocks”, composed of one or more nonconcurrent sequences for a single operation.
Fabric	FC defined interconnection methodology that handles routing in FC networks.
FC-EP	The future FC Enhanced Physical standard, which will build on and is compatible with FC-PH.
FC-PH	FC Physical standard, consisting of the three lower levels; FC-0, FC-1, and FC-2.
FC-0	Lowest level of the FC Physical standard, covering the physical characteristics of the interface and media.
FC-1	Middle level of the FC-PH standard, defining the 8B/10B encoding/decoding and transmission protocol.

FC-2	Highest level of FC-PH, defining the rules for signaling protocol and describing transfer of the frame, sequence, and exchanges.
FC-3	The hierarchical level in the FC standard that provides common services, such as striping definition.
FC-4	The hierarchical level in the FC standard that specifies the mapping of Upper Layer Protocols (ULPs) to levels below.
FCC	Federal Communications Commission.
FCP	Fibre Channel Protocol.
FDDI	Fiber Distributed Data Interface. ANSI's option for a Metropolitan Area Network (MAN); a network based on the use of optical fiber cable to transmit data at 100 Mbits/s.
Fibre Channel Service Protocol (FSP)	The common FC-4 level protocol for all services, transparent to the fabric type or topology.
File	A named collection of information stored on a disk.
Firmware	Software that is permanently stored in ROM. Therefore, it can be accessed during boot time.
F_Port	"Fabric" port, the access point of the fabric for physically connecting the user's N_Port.
FL_Port	An F_Port that contains arbitrated loop functions.
Frame	A linear set of transmitted bits that define a basic transport element.
Hard Disk	A disk made of metal and permanently sealed into a drive cartridge. A hard disk can store very large amounts of information.
HAL	Hardware Abstraction Layer.
HIPPI	High Performance Parallel Interface, an 800 Mbit/s interface to supercomputer networks (formerly known as high speed channel) developed by ANSI.
Host	The computer system in which a SCSI host adapter is installed. It uses the SCSI host adapter to transfer information to and from devices attached to the SCSI bus.

Host Adapter	A circuit board or integrated circuit that provides a SCSI bus connection to the computer system.
IP	Internet Protocol.
IPI	Intelligent Peripheral Interface.
ISA	Industry Standard Architecture. A type of computer bus used in most PC's. It allows devices to send and receive data up to 16-bits at a time.
Kbyte	Kilobyte. A measure of computer storage equal to 1024 bytes.
LCT	Logical Configuration Table.
LLC	Logical Link Control.
Local Bus	A way to connect peripherals directly to computer memory. It bypasses the slower ISA and EISA buses. PCI is a local bus standard.
L_Port	A FC port which supports the arbitrated loop topology.
Link_Control_ Facility	A termination card that handles the logical and physical control of the FC link for each mode of use.
Login server	Entity within the FC fabric that receives and responds to login requests.
LUN	Logical Unit Number. An identifier, zero to seven, for a logical unit.
Mbyte	Megabyte. A measure of computer storage equal to 1024 kilobytes.
MFA	Message Frame Address.
Multicast	Refers to delivering a single transmission to multiple destination N_Ports.
NIC	Network Interface Card.
N_Port	"Node" port, a FC defined hardware entity at the node end of a link.
NL_Port	An N_Port that contains arbitrated loop functions.
Operating System	A program that organizes the internal activities of the computer and its peripheral devices. An operating system performs basic tasks such as moving data to and from devices, and managing information in memory. It also provides the user interface.

Operation A term, defined in FC-2, that refers to one of the FC “building blocks” composed of one or more, possibly concurrent, exchanges.

Ordered Set A FC term referring to four 10-bit characters (a combination of data and special characters) that provide low level link functions, such as frame demarcation and signaling between two ends of a link. It provides for initialization of the link after power-on and for some basic recovery actions.

Originator A FC term referring to the initiating device.

Parity Checking A way to verify the accuracy of data transmitted over the SCSI bus. One bit in the transfer is used to make the sum of all the 1 bits either odd or even (for odd or even parity). If the sum is not correct, an error message appears.

PCI Peripheral Component Interconnect. A local bus specification that allows connection of peripherals directly to computer memory. It bypasses the slower ISA and EISA buses.

PDB Packet Descriptor Block

PIO Programmed Input/Output. A way the CPU can transfer data to and from memory using the computer’s I/O ports. PIO is usually faster than DMA, but requires CPU time.

Port The hardware entity within a node that performs data communications over the FC link.

Port Address Also Port Number. The address through which commands are sent to a host adapter board. This address is assigned by the PCI bus.

Port Number See Port Address.

RAM Random Access Memory. The computer’s primary working memory in which program instructions and data are stored and are accessible to the CPU. Information can be written to and read from RAM. The contents of RAM are lost when the computer is turned off.

Responder A FC term referring to the answering device.

RISC Core The LSI Logic LSIFC919 chips contain a RISC (Reduced Instruction Set Computer) processor, programmed through microcode scripts.

ROM	Read Only Memory. Memory from which information can be read but not changed. The contents of ROM are not erased when the computer is turned off.
SAN	Storage Area Network.
SCAM	SCSI Configured AutoMatically. A method to automatically allocate SCSI IDs using software when SCAM compliant SCSI devices are attached.
Scatter/Gather	A device driver feature that lets the host adapter modify a transfer data pointer so that a single host adapter transfer can access many segments of memory. This minimizes interrupts and transfer overhead.
SCB	SCSI Command Block.
SCSI	Small Computer System Interface. A specification for a high-performance peripheral bus and command set. The original standard is referred to as SCSI-1.
SCSI-2	The current SCSI specification which adds features to the original SCSI-1 standard.
SCSI ID	A way to uniquely identify each SCSI device on the SCSI bus. Each SCSI bus has eight available SCSI IDs numbered 0 through 7 (or 0 through 15 for Wide SCSI). The host adapter usually gets ID 7 giving it priority to control the bus.
Sequence	A term referring to one of the FC “building blocks”, composed of one or more related frames for a single operation.
SGL	Scatter Gather List.
SNAP	SubNetwork Access Protocol.
Synchronous Data Transfer	One of the ways data is transferred over the SCSI bus. Transfers are clocked with fixed frequency pulses. This is faster than asynchronous data transfer. Synchronous data transfers are negotiated between the SCSI host adapter and each SCSI device.
System BIOS	Controls the low level POST (Power-On Self-Test), and basic operation of the CPU and computer system.
TID	Target ID.
Topology	The logical and/or physical arrangement of stations on a network.

ULP	Upper Layer Protocol.
VCCI	Voluntary Control Council for Interference.
Virtual Memory	Space on a hard disk that can be used as if it were RAM.
VPD	Vendor Product Data.
Word	A two byte (or 16 bit) unit of information.
X3T9	A technical committee of the Accredited Standards Committee X3, titled X3T9 I/O Interfaces. It is tasked with developing standards for moving data in and out of central computers.

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