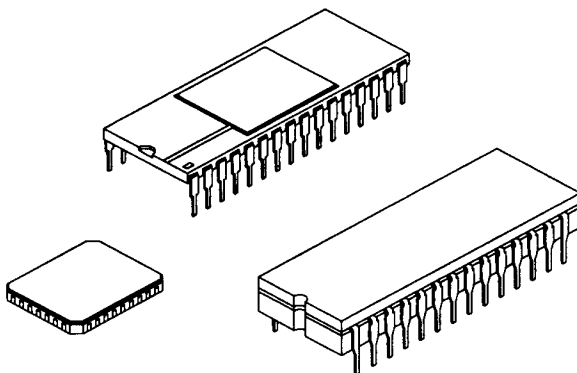


DESCRIPTION:

The DPS92256 is a 32K X 8 Static Random Access Memory (SRAM) fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5V power supply is required.

The DPS92256 is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.



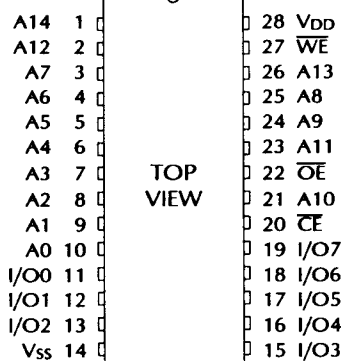
3

FEATURES:

- 32,768 Words by 8-Bits Organization
- Access Times: 85*, 100, 120, 150ns (max.)
- Low Power: 1.1mW (max.) Full Standby
- Fully Static Operation; No Clock or Refresh Required
- TTL Compatible Input and Output
- Common Data Input and Output
- Single +5V Power Supply, $\pm 10\%$ Tolerance
- Three State Output
- Standard 28-Pin DIP or 32-Pad LCC Packages

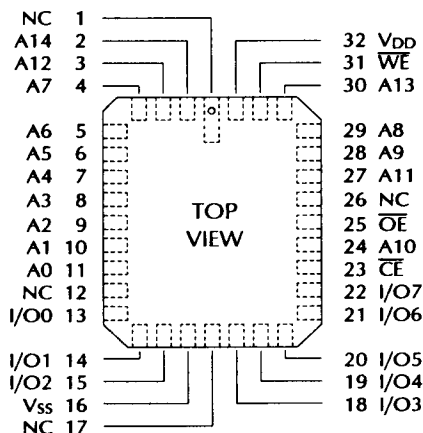
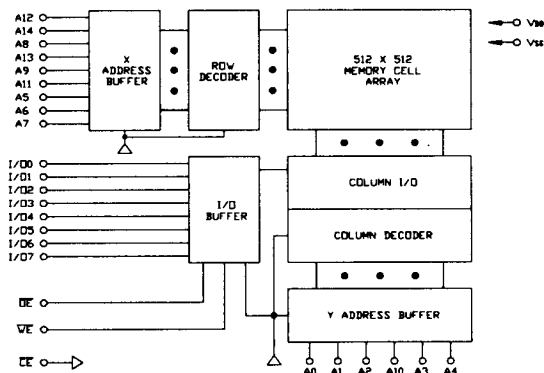
* Commercial only.

PIN-OUT DIAGRAMS



DIP

FUNCTIONAL BLOCK DIAGRAM



LCC

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
Dout Disable	L	H	H	HIGH-Z	Active
Read	L	L	H	DOUT	Active
Write	L	X	L	DIN	Active

L = LOW

H = HIGH

X = Don't Care

PIN NAMES

A0-A14	Address Inputs
I/O0 - I/O7	Data In/Out
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VDD	Power (+5V)
Vss	Ground

RECOMMENDED OPERATING RANGE¹

Symbol	Characteristic	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage	2.2		VDD+0.3	V
V _{IL}	Input LOW Voltage	-0.5 ²		0.8	V

ABSOLUTE MAXIMUM RATINGS³

Symbol	Parameter	Value	Unit
T _{STC}	Storage Temperature	-65 to + 150	°C
T _{BIAS}	Temperature Under Bias	-55 to + 125	°C
VDD	Supply Voltage ¹	-0.5 to + 7.0	V
V _{I/O}	Input/Output Voltage ¹	-0.5 to VDD+0.5	V

CAPACITANCE ⁴: T_A = 25°C, F = 1.0MHz

Symbol	Parameter	Max.	Unit	Condition
C _{CE}	Chip Enable	7	pF	V _{IN} =0V
C _{ADR}	Address Input	7		
C _{WE}	Write Enable	7		
C _{OE}	Output Enable	7		
C _{I/O}	Data Input/Output	10		

DC OPERATING CHARACTERISTICS: Over operating ranges

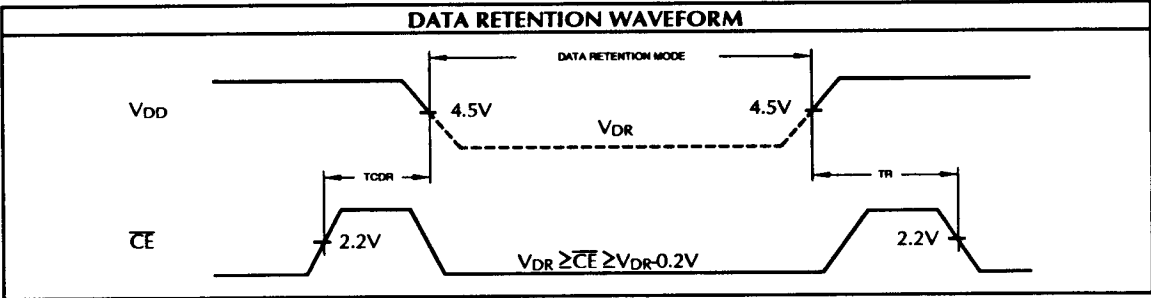
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to VDD	-2	2	-2	2	-2	2	μA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to VDD, $\overline{CE}$ or $\overline{OE}$ = V _{IH} , or $\overline{WE}$ = V _{IL}	-2	2	-2	2	-2	2	μA
I _{CC1}	Active Supply Current	$\overline{CE}$ = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA		45		45		45	mA
I _{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I _{OUT} = 0mA		60		65		70	mA
I _{SB1}	Full Standby Supply Current	$\overline{CE} \geq VDD - 0.2V$		100		200		300	μA
I _{SB2}	Standby Supply	$\overline{CE}$ = V _{IH}		2		2		2	mA
V _{OL}	Output Low Voltage	I _{OUT} = 2.1mA		0.4		0.4		0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -1.0mA	2.4		2.4		2.4		V

DATA RETENTION DC CHARACTERISTICS

Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{CCDR3}	Data Retention Supply Current	V _{DR} = 3V, $\overline{CE} \geq VDR - 0.2V$		40		50		240	μA
I _{CCDR2}	Data Retention Supply Current	V _{DR} = 2V, $\overline{CE} \geq VDR - 0.2V$		30		40		200	μA

DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V _{DR}	Data Retention Voltage	$\overline{CE} \geq VDD - 0.2V$	2.0	5.0	5.5	V
t _{CDR}	Chip Disable to Data Retention Time		0			ns
t _R	Recovery Time	t _{RC} = Read Cycle Timing	t _{RC}			ns

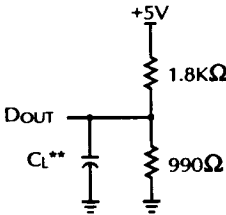


AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.

OUTPUT LOAD		
Load	CL	Parameters Measured
1	100pF	except tCLZ, tCHZ, tOHZ, tOLZ, tWLZ and tWHZ
2	5pF	tCLZ, tCHZ, tOHZ, tOLZ, tWLZ and tWHZ

Figure 1. Output Load
** Including Probe and Jig Capacitance.



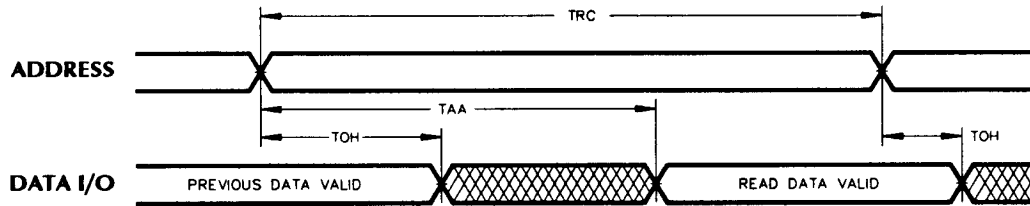
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	Symbol	Parameter	-85†		-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	tRC	Read Cycle Time	85		100		120		150		ns
2	tAA	Address Access Time		85		100		120		150	ns
3	tCO	Chip Enable to Output Valid		85		100		120		150	ns
4	tOV	Output Enable to Output Valid		60		60		60		70	ns
5	tOH	Output Hold from Address Change			10		10		10		ns
6	tCLZ	Chip Enable to Output in LOW-Z 4, 5			10		10		10		ns
7	tOLZ	Output Enable to Output in LOW-Z 4, 5			5		5		5		ns
8	tCHZ	Chip Enable to Output in HIGH-Z 4, 5				35		40		50	ns
9	tOHZ	Output Enable to Output in HIGH-Z 4, 5				35		40		50	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE ^{6,7} : Over operating ranges											
No.	Symbol	Parameter	-85†		-100		-120		-150		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	tWC	Write Cycle Time	85		100		120		150		ns
11	tAW	Address Valid to End of Write	75		90		100		120		ns
12	tCW	Chip Enable to End of Write	75		90		100		120		ns
13	tDW	Data Valid to End of Write	35		40		50		60		ns
14	tDH	Data Hold Time	0		0		0		0		ns
15	tWP	Write Pulse Width	65		75		90		110		ns
16	tAS	Address Set-up Time ***	0		0		0		0		ns
17	tAH	Address Hold Time	0		0		0		0		ns
18	tWHZ	Write Enable to Output in HIGH-Z ^{4, 5}		30		35		40		50	ns
19	tWLZ	Write Enable to Output in LOW-Z ^{4, 5}	5		5		5		5		ns

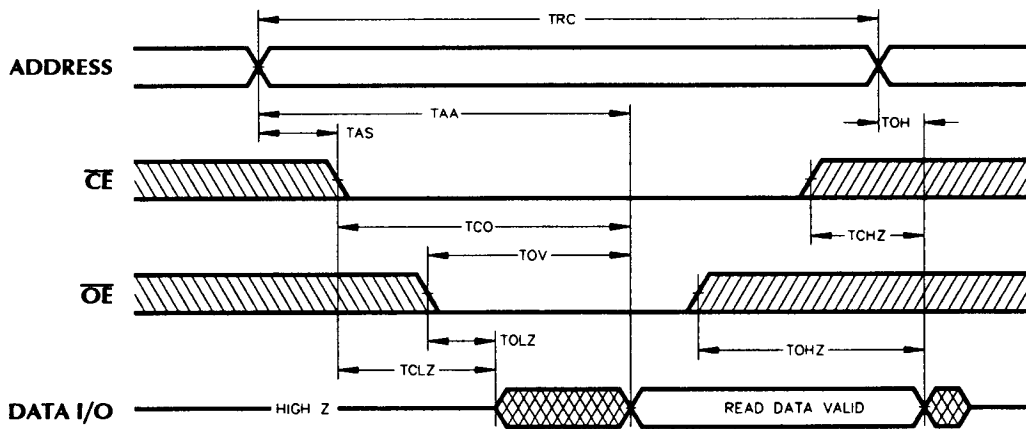
*** Valid for both Read and Write Cycles.

† Commercial only.

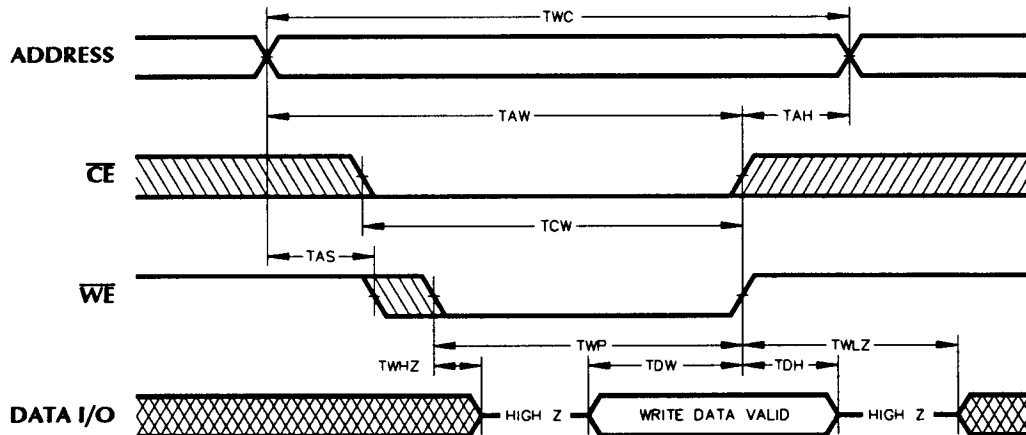
READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.

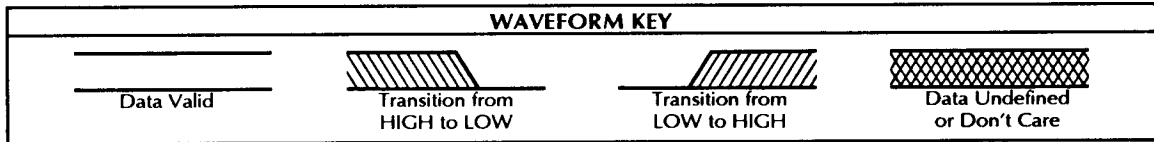
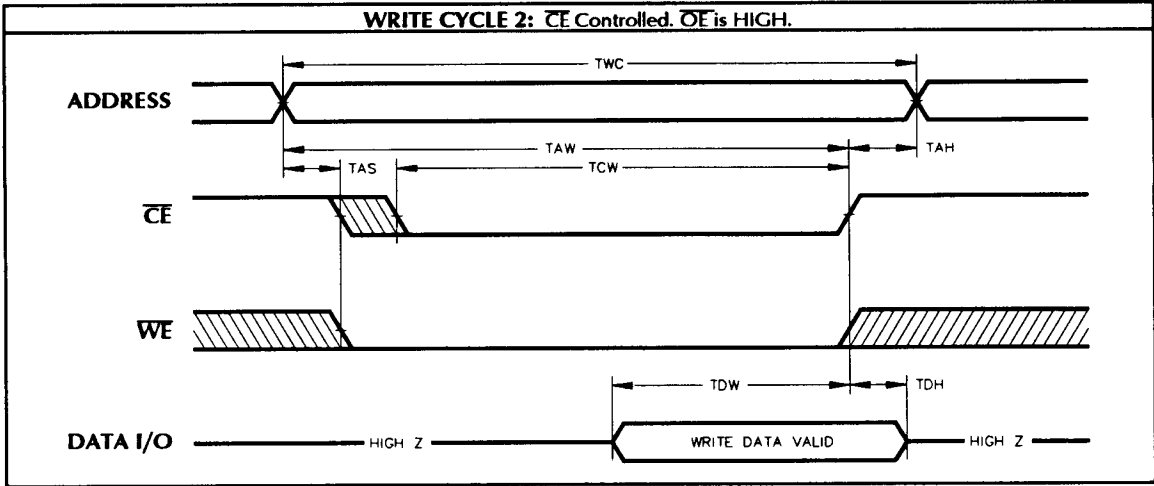


READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.

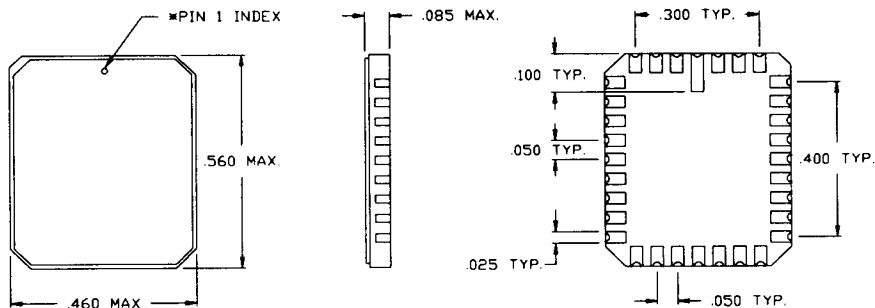




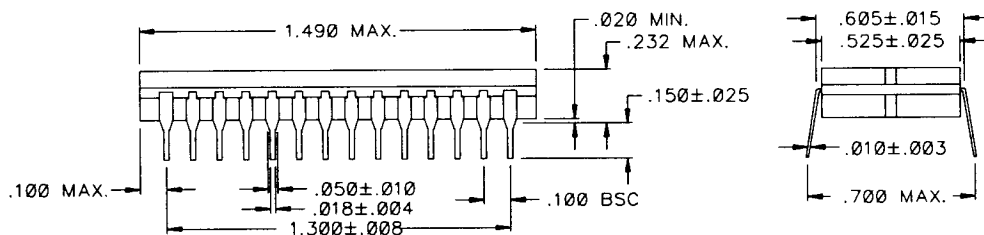
- NOTES:**
1. All voltages are with respect to V_{SS} .
 2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
 3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
 4. This parameter is guaranteed and not 100% tested.
 5. Transition is measured at the point of $\pm 500mV$ from steady state voltage.
 6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state; and, input signals of opposite phase to the outputs must not be applied.
 7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

ORDERING INFORMATION					
DP PREFIX	S92256 DEVICE TYPE	X PACKAGE	- XXX SPEED	X GRADE	
					C COMMERCIAL 0°C to +70°C
					I INDUSTRIAL -40°C to +85°C
					M MILITARY -55°C to +125°C
					B MIL-PROCESSED -55°C to +125°C
					85 85ns (COMMERCIAL ONLY)
					100 100ns
					120 120ns
					150 150ns
					G 32 PAD LCC
					N 28 LEAD SIDE BRAZED DIP
					NONE 28 LEAD CERDIP
					32K X 8 CMOS SRAM

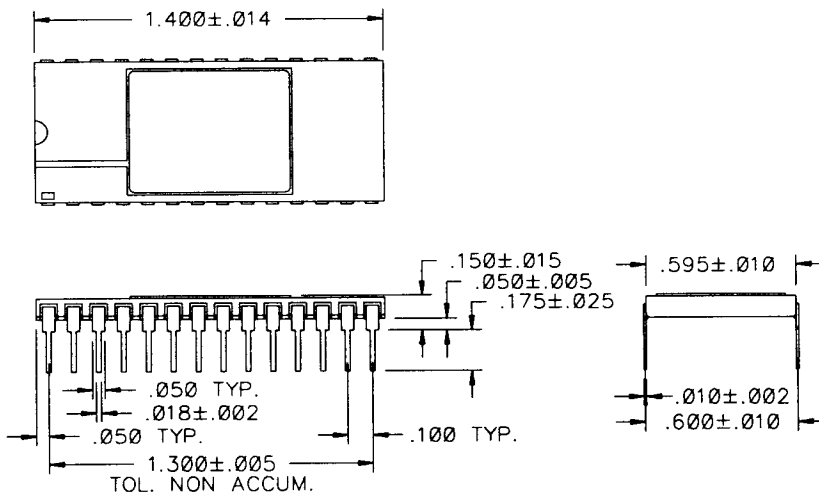
MECHANICAL DIAGRAMS



LCC



CERP



SIDE BRAZED DIP

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