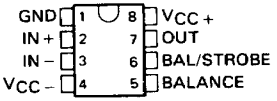
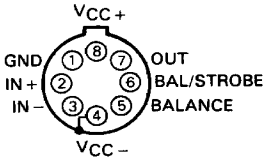
D3179, JANUARY 1989

- **Low Input Offset Voltage . . . 1.5 or 0.5 mV Max**
- **Maximum Input Bias Current . . . 50 or 25 nA**
- **Low Input Offset Current . . . 4 or 3 nA Max**
- **Output Response Time . . . 250 ns Max**
- **Voltage Gain . . . 200 V/mV Min**
- **Output Current . . . 50 mA Source or Sink**
- **Differential Input Voltage . . . ±30 V**
- **Can Operate from Single 5-V Supply**
- **Pin-Compatible with LM111 Series**
- **Designed to be Interchangeable with Linear Technology LT1011 and LT1011A**

**JG OR P PACKAGE**
**(TOP VIEW)**




**L PACKAGE**
**(TOP VIEW)**

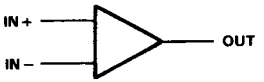



Pin 4 (L package) is in electrical contact with the case.

## description

The LT1011 and LT1011A are general-purpose comparators that are pin-compatible with the LM111. The LT1011A offers significantly better input characteristics than the LM111: four times lower bias current, six times lower offset voltage, and five times higher voltage gain. Additionally, the supply current is considerably lower than that of the LM111 with no loss in speed. The offset voltage temperature coefficient of the LT1011A is 15 µV/°C. The LT1011 and LT1011A are fully specified for dc parameters and output response time when operating from a single 5-V supply.

## symbol



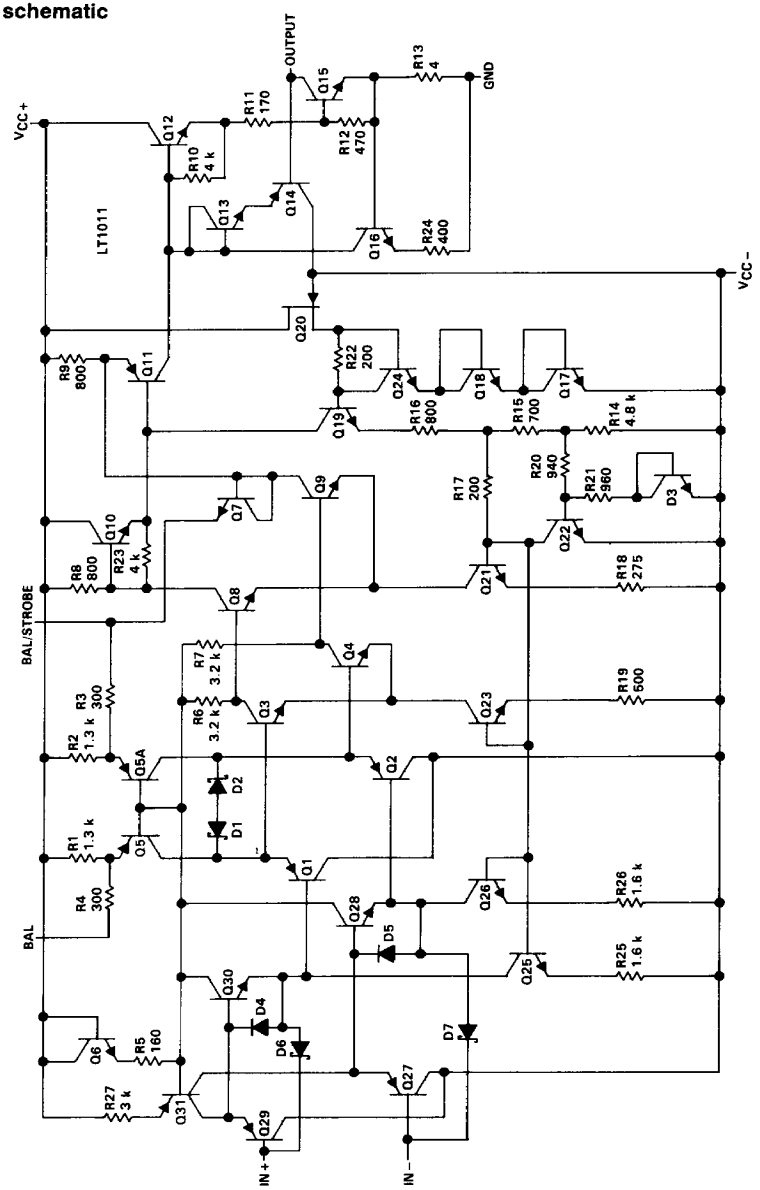

The LT1011 and LT1011A can be used in high-accuracy (≥ 12-bit) systems without trimming. The devices retain all the versatile features of the LM111 including single-supply operation (3 V to 36 V) or dual-supply operation (±1.5 V to ±18 V) and a floating transistor output with 50-mA source or sink capability. The devices can drive loads that are referenced to ground, the negative supply, or the positive supply, and are specified up to 50 V between $V_{CC-}$ and the collector output. A differential input voltage up to the full supply voltage is allowed, even with ±18-V supplies, enabling the inputs to be clamped to the supplies with simple diode clamps.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. C-suffix devices are characterized for operation from 0°C to 70°C.

**AVAILABLE OPTIONS**

| $T_A$ | $V_{IO}$ MAX at 25°C | PACKAGE | | |
|---|---|---|---|---|
| | | CERAMIC DIP (JG) | METAL CAN (L) | PLASTIC DIP (P) |
| 0°C to 70°C | 1.5 mV | LT1011CJG | LT1011CL | LT1011CP |
| | 0.5 mV | LT1011ACJG | LT1011ACL | LT1011ACP |
| −55°C to 125°C | 1.5 mV | LT1011MJG | LT1011ML | |
| | 0.5 mV | LT1011AMJG | LT1011AML | |

## schematic




Resistor values shown are nominal and in ohms.



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC+}$ . . . . . 18 V
Supply voltage, $V_{CC-}$ . . . . . −18 V
Voltage from output to $V_{CC-}$: M-suffix . . . . . 50 V
C-suffix . . . . . 40 V
Voltage from GND to $V_{CC-}$ . . . . . 30 V
Voltage from strobe to $V_{CC+}$ . . . . . 5 V
Differential input voltage (see Note 1) . . . . . ±36 V
Input voltage (either input, see Note 2) . . . . . $V_{CC\pm}$
Duration of output short circuit (see Note 3) . . . . . 10 s
Continuous power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: M-suffix . . . . . −55°C to 125°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
2. Inputs may be clamped to supplies with diodes so that the maximum input voltage actually exceeds the supply voltage by one diode drop (refer to "input protection" in the applications section).
3. The output may be shorted to ground or to either power supply.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|
| JG (M-suffix) | 1050 mW | 8.4 mW/°C | 672 mW | 210 mW |
| JG (C-suffix) | 825 mW | 6.6 mW/°C | 528 mW | N/A |
| L (M-suffix) | 825 mW | 6.6 mW/°C | 528 mW | 165 mW |
| L (C-suffix) | 650 mW | 5.2 mW/°C | 416 mW | N/A |
| P | 1000 mW | 8.0 mW/°C | 640 mW | N/A |

## recommended operating conditions

| | | M-SUFFIX | | | C-SUFFIX | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC+}$ | | | | 15 | | | 15 | V |
| Supply voltage, $V_{CC-}$ | | | | −15 | | | −15 | V |
| Input voltage, $V_I$, (see Note 4) | $V_{CC\pm}$ = ±15 V | −14.5 | | 13 | −14.5 | | 13 | V |
| | $V_{CC}$ = single 5-V | 0.5 | | 3 | 0.5 | | 3 | |
| Operating free-air temperature, $T_A$ | | −55 | | 125 | 0 | | 70 | °C |

NOTE 4: See "Input Signal Range" under "Typical Application Data."

## electrical characteristics, $V_{CC\pm}$ = ±15 V, $V_{IC}$ = 0, $R_S$ = 0, pin 1 at $V_{CC-}$, output at pin 7 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$† | LT1011 | | | LT1011A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $I_O$ = 1.5 mA, $V_O$ = 0 | 25°C | | 0.6 | 1.5 | | 0.3 | 0.5 | mV |
| | | | Full range | | | 3 | | | 1 | |
| | | $R_S$ ≤ 50 kΩ, See Note 5 | 25°C | | | 2 | | | 0.75 | |
| | | | Full range | | | 3 | | | 1.5 | |
| $\alpha_{VIO}$ | Average temperature coefficient of input offset voltage | See Note 6 | Full range | | 4 | 25 | | 4 | 15 | µV/°C |
| $I_{IO}$ | Input offset current | See Note 5 | 25°C | | 0.2 | 4 | | 0.2 | 3 | nA |
| | | | Full range | | | 6 | | | 5 | |
| $I_{IB}$ | Input bias current | $I_O$ = 1.5 mA, $V_O$ = 0 | 25°C | | −20 | ±50 | | −15 | ±25 | nA |
| | | See Note 5 | 25°C | | −25 | ±65 | | −20 | ±35 | |
| | | | Full range | | | ±80 | | | ±50 | |
| $I_{IL(S)}$ | Low-level strobe current (See Note 7) | | 25°C | | | −500 | | | −500 | µA |
| $V_{ICR}$ | Common-mode input voltage range | | Full range | −14.5 to 13 | | | −14.5 to 13 | | | V |
| $A_{VD}$ | Large-signal differential voltage amplification | $R_L$ = 1 kΩ to $V_{CC+}$, $V_O$ = −10 V to 14.5 V | 25°C | 200 | 500 | | 200 | 500 | | V/mV |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = −5 mV, $I_{OL}$ = 8 mA, Pin 1 at 0 V | Full range | | | 0.4 | | | 0.4 | V |
| | | $V_{ID}$ = −5 mV, $I_{OL}$ = 50 mA, Pin 1 at 0 V | Full range | | | 1.5 | | | 1.5 | |
| $I_{O(lkg)}$ | Output leakage current | $V_{ID}$ = 5 mV, Pin 1 at −15 V, $V_O$ = 35 V (25 V for LT1011C) | 25°C | | 0.2 | 10 | | 0.2 | 10 | nA |
| | | | Full range | | | 500 | | | 500 | |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = $V_{ICR\ min}$, $R_S$ ≤ 50 kΩ | 25°C | 90 | 115 | | 94 | 115 | | dB |
| $I_{CC+}$ | Supply current from $V_{CC+}$ | | 25°C | | 3.2 | 4 | | 3.2 | 4 | mA |
| $I_{CC-}$ | Supply current from $V_{CC-}$ | | 25°C | | −1.7 | −2.5 | | −1.7 | −2.5 | mA |
| $C_i$ | Input capacitance | | 25°C | | 6 | | | 6 | | pF |

† Full range is −55°C to 125°C for the LT1011M and LT1011AM. Full range is 0°C to 70°C for the LT1011C and LT1011AC.

NOTES: 5. These specifications apply for single supply voltages from 5 V to 30 V and dual supply voltages from ±2.5 V to ±15 V for the entire input voltage range, and for both high and low output states. The high state is $I_{OH}$ ≥ 100 µA and $V_O$ ≥ ($V_{CC+}$ − 1 V). The low state is $I_{OL}$ ≤ 8 mA and $V_O$ ≤ 0.8 V. Therefore, this specification defines a worst-case error band that includes effects due to common-mode signals, voltage gain, and output load.

6. Average temperature coefficient is calculated by dividing the offset voltage difference measured at minimum and maximum temperatures by the temperature difference.

7. This is the minimum current that must be drawn from the strobe to ensure that the output is off regardless of differential input voltage.





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## electrical characteristics, $V_{CC+}$ = 5 V, $V_{CC-}$ = 0, $V_{IC}$ = 0, $R_S$ = 0, pin 1 at 0 V, output at pin 7 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$† | LT1011 | | | LT1011A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $R_S \le 50\ k\Omega$, See Note 5 | 25°C | | | 2 | | | 0.75 | mV |
| | | | Full range | | | 3 | | | 1.5 | |
| $I_{IO}$ | Input offset current | See Note 8 | 25°C | | 0.2 | 4 | | 0.2 | 3 | nA |
| | | | Full range | | | 6 | | | 5 | |
| $I_{IB}$ | Input bias current | See Note 8 | 25°C | | 25 | 65 | | 20 | 35 | nA |
| | | | Full range | | | 80 | | | 50 | |
| $I_{IL(S)}$ | Low-level strobe current (See Note 7) | | 25°C | | | −500 | | | −500 | µA |
| $V_{ICR}$ | Common-mode input voltage range | | Full range | 0.5 to 3 | | | 0.5 to 3 | | | V |
| $A_{VD}$ | Large-signal differential voltage amplification | $R_L$ = 0.5 kΩ to $V_{CC+}$, $V_O$ = 0.5 V to 4.5 V | 25°C | 50 | 300 | | 50 | 300 | | V/mV |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = −5 mV, $I_{OL}$ = 8 mA | Full range | | | 0.4 | | | 0.4 | V |
| | | $V_{ID}$ = −5 mV, $I_{OL}$ = 50 mA | Full range | | | 1.5 | | | 1.5 | |
| $I_O$ | Output leakage current | $V_{ID}$ = 5 mV, | 25°C | | 0.2 | 10 | | 0.2 | 10 | nA |
| | | $V_O$ = 50 V (40 V for LT1011C) | Full range | | | 500 | | | 500 | |
| $I_{CC+}$ | Supply current from $V_{CC+}$ | | 25°C | | 3.2 | 4 | | 3.2 | 4 | mA |
| $I_{CC-}$ | Supply current from $V_{CC-}$ | | 25°C | | −1.7 | −2.5 | | −1.7 | −2.5 | mA |

† Full range is −55°C to 125°C for the LT1011M and LT1011AM. Full range is 0°C to 70°C for the LT1011C and LT1011AC.

NOTES: 6. Average temperature coefficient is calculated by dividing the offset voltage difference measured at minimum and maximum temperatures by the temperature difference.

7. This is the minimum current that must be drawn from the strobe to ensure that the output is off regardless of differential input voltage.

8. These specifications apply for all single-supply voltages from 5 V to 30 V for the entire input voltage range, and for both high and low output states. The high state is $I_{OH} \ge 100\ \mu A$ and $V_O \ge (V_{CC+} - 1\ V)$. The low state is $I_{OL} \le 8$ mA and $V_O \le 0.8$ V. Therefore, this specification defines a worst-case error band that includes effects due to common-mode signals, voltage gain, and output load.

## switching characteristics, $V_{CC+}$ = 5 V, $V_{CC-}$ = 0, pin 1 at 0 V, $T_A$ = 25°C

| PARAMETER | TEST CONDITIONS | LT1011 | | | LT1011A | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Output response time | $R_C$ = 500 Ω to 5 V, $C_L$ = 5 pF, See Note 9 | | 150 | 250 | | 150 | 250 | ns |

NOTE 9: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

## TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

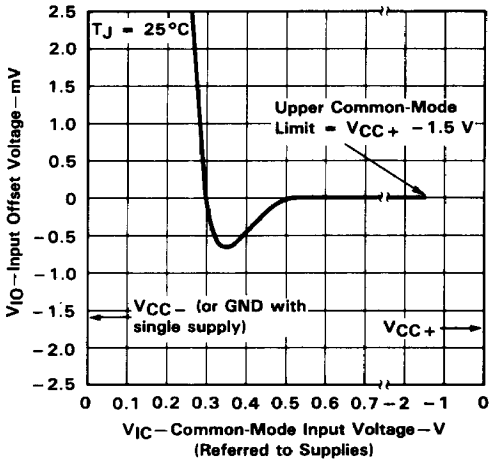


FIGURE 1

OFFSET ADJUSTMENT CHARACTERISTICS

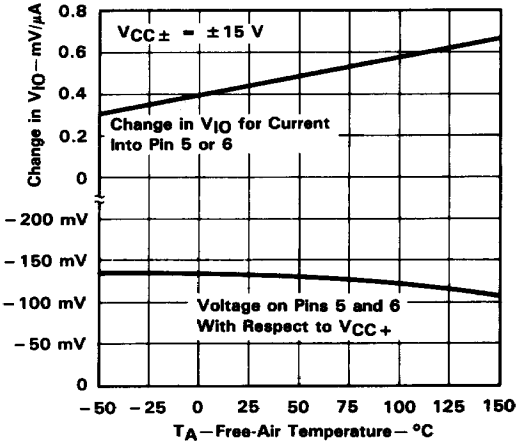


FIGURE 2

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

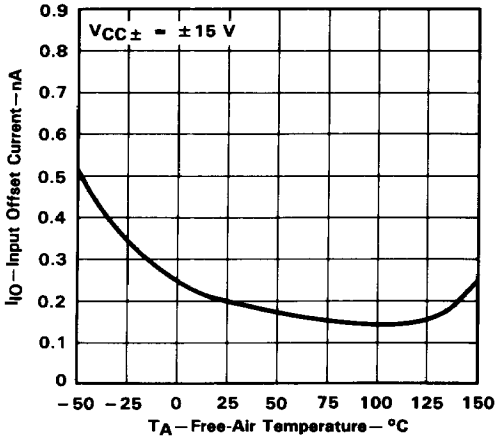


FIGURE 3

LT1011
INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

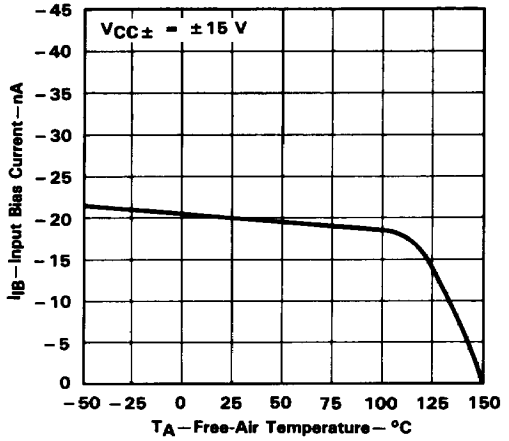


FIGURE 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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## TYPICAL CHARACTERISTICS†

INPUT VOLTAGE LIMITS
vs
FREE-AIR TEMPERATURE

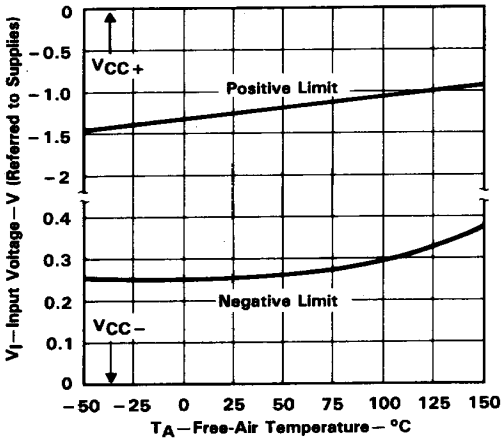


FIGURE 5

LT1011
INPUT CHARACTERISTICS
(EITHER INPUT WITH OTHER
INPUT GROUNDED)

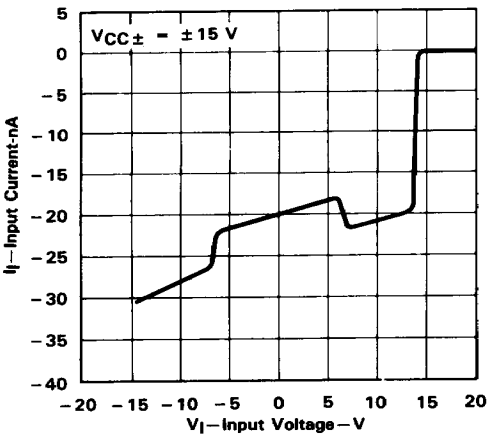


FIGURE 6

EQUIVALENT OFFSET VOLTAGE
vs
SOURCE RESISTANCE

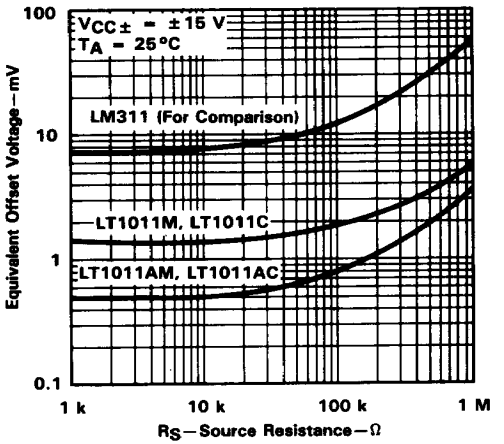


FIGURE 7

VOLTAGE TRANSFER CHARACTERISTICS

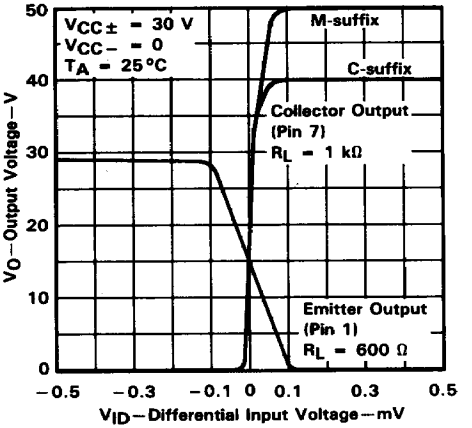


FIGURE 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
INPUT OVERDRIVE

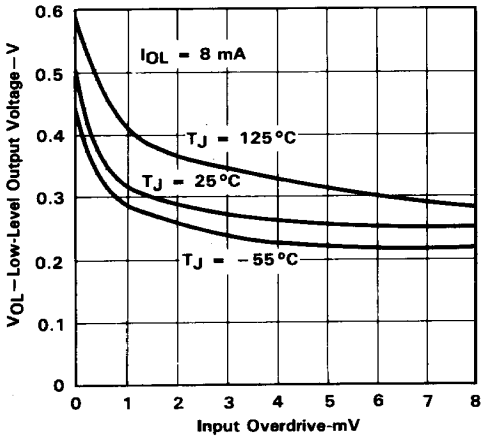


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

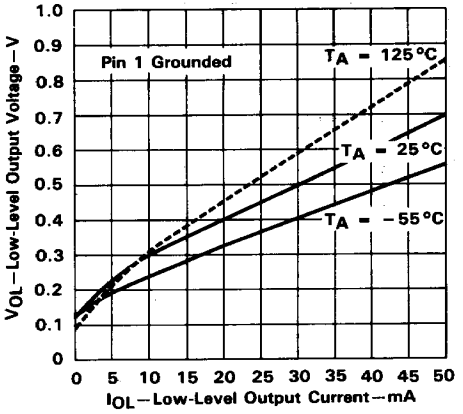


FIGURE 10

OUTPUT LEAKAGE CURRENT
vs
FREE-AIR TEMPERATURE

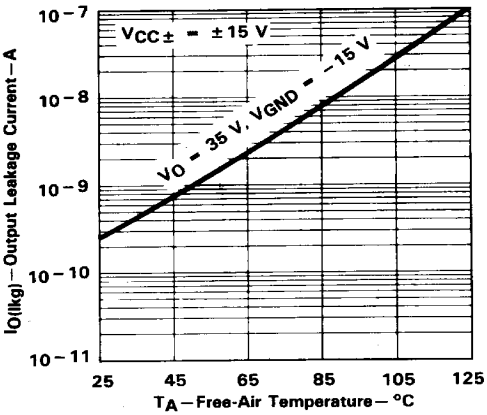


FIGURE 11

SHORT-CIRCUIT OUTPUT CURRENT
AND DISSIPATION
(3 MINUTES AFTER SHORT)
vs
OUTPUT VOLTAGE

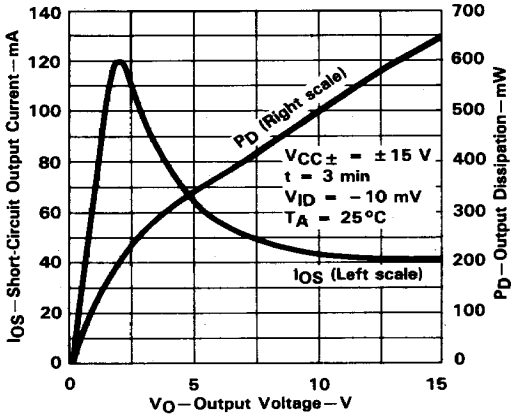


FIGURE 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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## TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

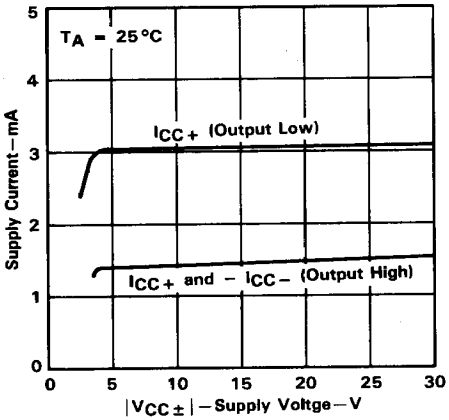


FIGURE 13

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

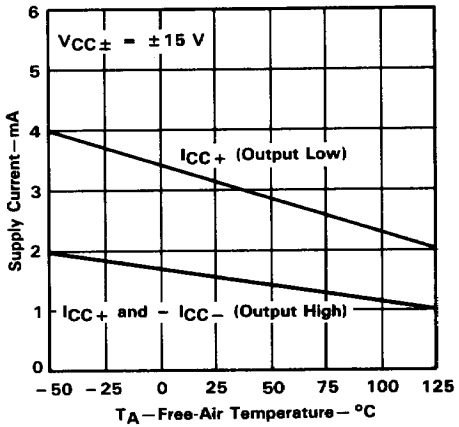


FIGURE 14

OUTPUT SATURATION VOLTAGE
(GROUND INPUT)
vs
OUTPUT CURRENT

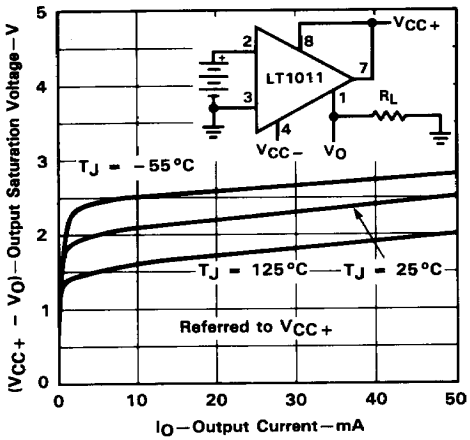


FIGURE 15

OUTPUT RESPONSE TIME
vs
INPUT STEP SIZE

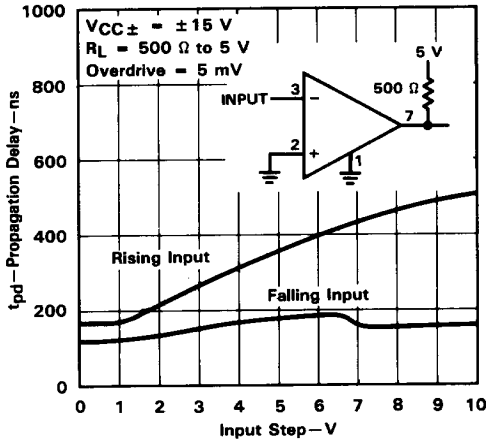


FIGURE 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS

OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

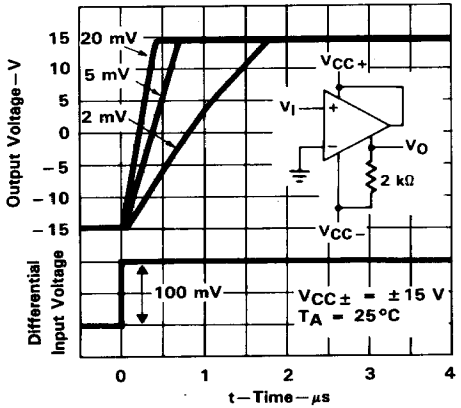


FIGURE 17

OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

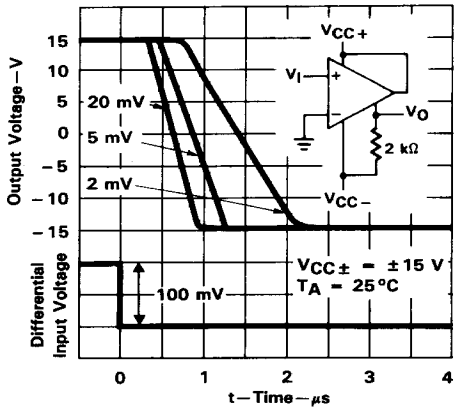


FIGURE 18

HIGH- TO LOW-LEVEL
OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

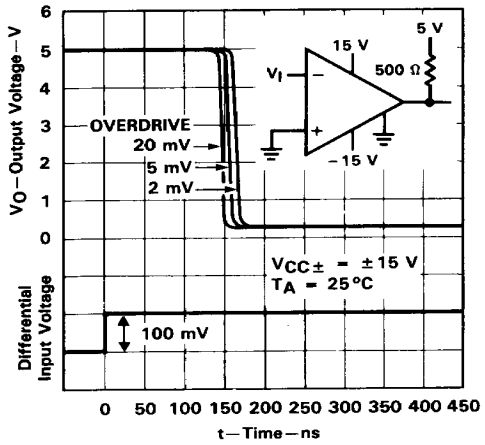


FIGURE 19

LOW- TO HIGH-LEVEL
OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

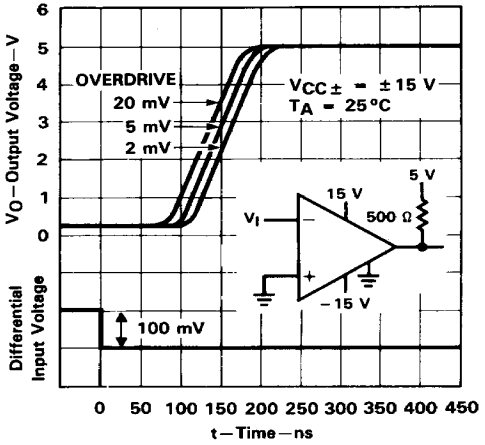


FIGURE 20



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## TYPICAL APPLICATION DATA

### preventing oscillation problems

Oscillation problems in comparators are often caused by stray capacitance between the output and inputs or between the output and other sensitive pins on the comparator. This is especially true for comparators with high gain and wide bandwidth, like the LT1011 (GBW ≥ 10 GHz), that are designed for fast switching with millivolt input signal levels. Because oscillation problems tend to occur at frequencies around 5 MHz, where the LT1011 has a gain of approximately 2 V/mV, attenuation of output signals must be at least 2000:1 at 5 MHz as measured at the inputs. If the source impedance is 1 kΩ, the effective stray capacitance between output and input must have a reactance of more than (2000)(1 kΩ) = 2 MΩ, or less than 2 pF. The actual inter-lead capacitance between input and output pins on the LT1011 is less than 0.002 pF when cut to mounting length for printed circuit boards. Additional stray capacitance due to printed circuit traces must be minimized by routing the output trace directly away from input lines and, if possible, running ground traces next to input traces to provide shielding.

Additional steps to prevent oscillation problems are:

1. Bypass the strobe/balance pins with a 0.01-μF capacitor connected from pin 5 to pin 6 to eliminate stray capacitive feedback from the output to the balance pins. The balance pins are nearly as sensitive to stray capacitive feedback as the inputs.
2. Bypass the negative supply (pin 4) with a 0.1-μF ceramic capacitor close to the comparator. A 0.1-μF capacitor can also be used for the positive supply (pin 8) if the pull-up load is tied to a separate supply. When the pull-up load is tied directly to pin 8, use a 2-μF solid tantalum bypass capacitor.
3. Bypass any slow-moving or dc input with a capacitor (≥ 0.01 μF) close to the comparator to reduce high-frequency source impedance.
4. Keep resistive source impedance as low as possible. If a resistor is added in series with one input, bypass it with a capacitor to balance source impedances for dc accuracy. The low input bias current of the LT1011 usually eliminates any need for source resistance balancing. A 5-kΩ imbalance, for example, creates only 0.25-mV offset.
5. Use hysteresis, which consists of shifting the input offset voltage of the comparator when the output changes state. Hysteresis forces the comparator to move quickly through its linear region, eliminating oscillations by "overdriving" the comparator under all input conditions. Hysteresis may be either ac or dc. An ac hysteresis technique does not shift the apparent offset voltage of the comparator but requires a minimum input signal slew rate to be effective. A dc hysteresis technique works for all input slew rates but creates a shift in offset voltage dependent on the previous condition of the input signal.

   The circuit shown in Figure 21 is an excellent compromise between ac and dc hysteresis. The 0.003-μF capacitor from pin 6 to pin 8 generates ac hysteresis by slightly shifting the voltage on the balance pins; both pins move about 4 mV depending on the state of the output. If pin 6 is bypassed, a level of ac hysteresis is created that is sufficient to switch the output at a speed near the comparator's maximum speed.

A small amount of dc hysteresis is also used to prevent problems due to low values of input slew rate. The sensitivity of the balance pins to current is about 0.5-mV input referred offset for each microampere of balance pin current. The 15-MΩ resistor tied from output to pin 5 generates 0.5-mV dc hysteresis.

The circuit is especially useful for general-purpose comparator applications because it does not force any signals directly back onto the input signal source. Instead, it takes advantage of the unique properties of the balance pins to provide extremely fast, clean output switching even with low-frequency input signals in the millivolt range. The combination of ac and dc hysteresis creates clean oscillation-free switching with very small input errors. The curve in Figure 22 plots input referred error versus switching frequency for the circuit shown in Figure 21. Note that at low frequencies, the error is simply the dc hysteresis, while at high frequencies, an additional error is created by the ac hysteresis. The high-frequency error can be reduced by reducing $C_H$, but lower values may not provide clean switching with very low slew-rate input signals.

## TYPICAL APPLICATION DATA

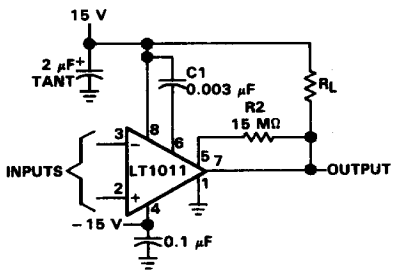



FIGURE 21. COMPARATOR WITH HYSTERESIS

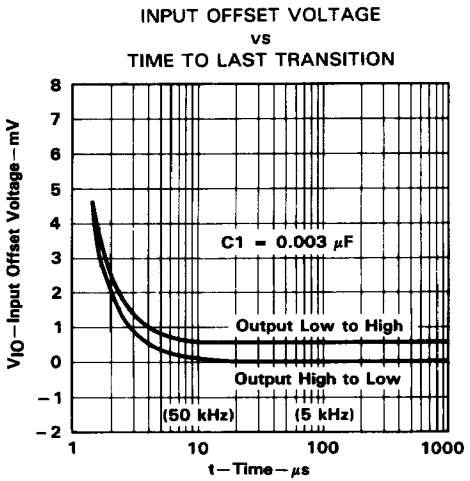
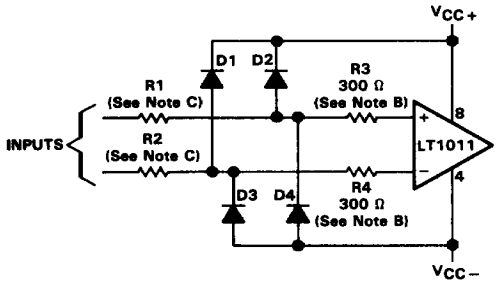



FIGURE 22

### Input protection

The inputs to the LT1011 are particularly suited to general-purpose comparator applications because large differential and/or common-mode voltages can be tolerated without damage to the comparator. Either or both inputs can be raised 40 V above the negative supply, independent of the positive supply voltage. Internal forward biased diodes conduct when the inputs are taken below the negative supply. In this condition, input current must be limited to 1 mA. If very large (fault) input voltages must be accommodated, series resistors and clamp diodes should be used, as shown in Figure 23.




NOTES: A. D1-D4 1N4148.
B. May be eliminated for fault current ≤ 1 mA.
C. Select according to allowable fault current and power dissipation.

FIGURE 23. LIMITING FAULT INPUT CURRENTS





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## TYPICAL APPLICATION DATA

The input resistors should limit fault current to a value between 0.1 mA and 20 mA. Power dissipation in the resistors must be considered for continuous faults, especially when the LT1011 supplies are off. Lightly loaded supplies may be forced to higher voltages by large fault currents flowing through D1-D4.

R3 and R4 limit input current to the LT1011 to less than 1 mA when the input signals are held below $V_{CC}-$. They may be eliminated if R1 and R2 are large enough to limit fault current to less than 1 mA.

### input slew rate limitations

In the LT1011, step size is important because the slew rate of internal nodes increases response time for input step sizes larger than 1 V. For example, at 5-V step size, response time increases from 150 ns to 360 ns (see Figure 16). If response time is critical and large input signals are expected, clamp diodes across the inputs are recommended. The slew rate limitation can also affect performance when differential input voltage is low, but both inputs must slew quickly. The maximum suggested common-mode slew rate is 10 V/μs.

### strobing

The LT1011 can be strobed by pulling current out of the strobe pin. The output transistor is forced to an off state, giving a high output at the collector (pin 7). Currents as low as −250 μA may cause strobing, but when the strobe current is low, strobe delay increases to between 200 ns and 300 ns. If strobe current is increased to −3 mA, strobe delay drops to about 60 ns. When the strobe current is 0, the voltage at the strobe pin is approximately 150 mV below $V_{CC}+$; when the strobe current is increased to −3 mA, the strobe pin voltage is approximately 2 V below $V_{CC}+$. Do not ground the strobe pin; it must be current driven.

Figure 24 shows a typical strobe circuit. Note that there is no bypass capacitor between pins 5 and 6, which maximizes strobe speed but leaves the comparator more sensitive to oscillation problems for slow, low-level inputs. A 1-pF capacitor between the output and pin 5 greatly reduces oscillation problems without reducing strobe speed.

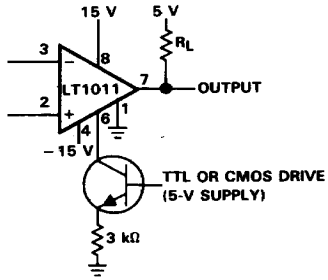


**FIGURE 24. TYPICAL STROBE CIRCUIT**

Placing a resistor from the output to pin 5 adds dc hysteresis. See step number 5 under "preventing oscillation problems."

The pin that is used for strobing (pin 6) is also one of the offset adjustment pins. Current into or out of pin 6 must be kept very low (<0.2 μA) when not strobing to prevent input offset voltage shifts.

### output transistor

When the LT1011 output transistor is in the off state, negligible current flows into or out of the collector or emitter. The equivalent circuit is shown in Figure 25.

## TYPICAL APPLICATION DATA

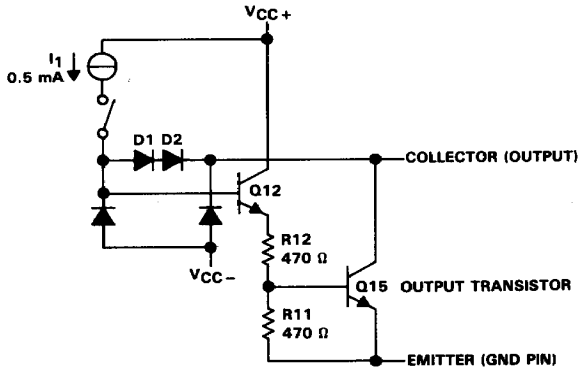


FIGURE 25. OUTPUT TRANSISTOR CIRCUITRY



### output transistor (continued)

In the off state, $I_1$ is switched off and both Q12 and Q15 turn off. The collector of Q15 can then be held above $V_{CC-}$ without conducting current. The maximum voltage above $V_{CC-}$ is 50 V for the LT1011 and 40 V for the LT1011C (these maximum voltages may exceed $V_{CC+}$). The emitter can be held at any voltage between $V_{CC-}$ and $V_{CC+}$ as long as the voltage is negative with respect to the collector.

In the on state, $I_1$ is connected, which turns on both Q12 and Q15. Diodes D1 and D2 prevent deep saturation of Q15 to improve speed and also limit the drive current of Q12. The R11/R12 divider sets the saturation voltage of Q15 and provides turn-off drive. Either the collector or emitter pin can be held at a voltage between $V_{CC-}$ and $V_{CC+}$, which allows the remaining pin to drive the load. In typical applications, the emitter is connected to $V_{CC-}$ or ground, and the collector drives a load tied to $V_{CC+}$ or a separate positive supply.

When the emitter is used as the output, the collector is typically tied to $V_{CC+}$, and the load is connected to ground or $V_{CC-}$. Note that the emitter output is phase reversed with respect to the collector output so that the "+" and "−" input designations must be reversed. When the collector is tied to $V_{CC+}$, the voltage at the emitter in the one state is about 2 V below $V_{CC+}$.

### input signal range

The input voltage range of the LT1011 is typically 300 mV above the negative supply and 1.5 V below the positive supply, independent of the actual supply voltages. This is the input voltage range over which the output will respond correctly when a voltage within the range is applied to one input and a higher or lower signal is applied to the other input. If one input is inside the range and one is outside, the output will be correct. If both inputs are outside the range, in opposite directions, the output will still be correct. If, however, both inputs are outside the range in the same direction, the output will not respond to the differential input; it will remain unconditionally off.



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## TYPICAL APPLICATIONS

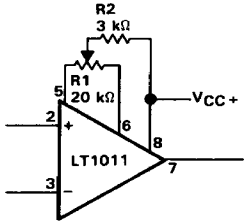
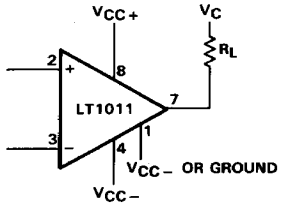
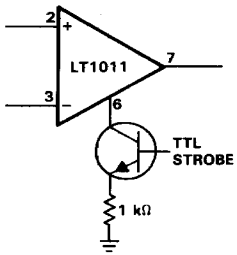



FIGURE 26. OFFSET BALANCING



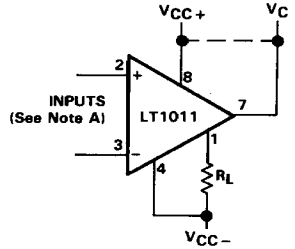

NOTE: $V_C$ can be greater or less than $V_{CC+}$.

FIGURE 28. DRIVING LOAD REFERENCED TO POSITIVE SUPPLY




NOTE: Do not ground strobe pin.

FIGURE 27. STROBING




NOTE A: Input polarity is reversed when using Pin 1 for output.

FIGURE 29. DRIVING LOAD REFERENCED TO NEGATIVE SUPPLY

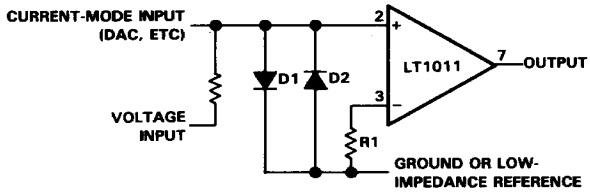
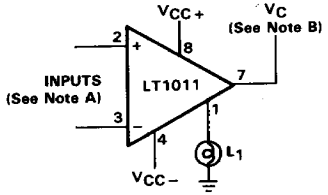


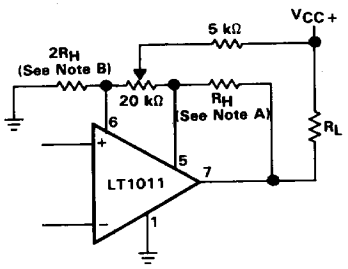

FIGURE 30. USING CLAMP DIODES TO IMPROVE FREQUENCY RESPONSE (See Figure 16)

## TYPICAL APPLICATIONS




NOTES: A. Input polarity is reversed when using Pin 1 for output.
B. $V_C$ may be any voltage above $V_{CC-}$. Pin 1 swings to within approximately 2 V of $V_{CC+}$.

**FIGURE 31. DRIVING LOAD REFERENCED TO GROUND**




NOTES: A. Hysteresis is approximately 0.45 mV/μA change in current in $R_H$.
B. This resistor causes hysteresis to be centered around $V_{IO}$.

**FIGURE 32. COMBINING OFFSET ADJUSTMENT AND HYSTERESIS**

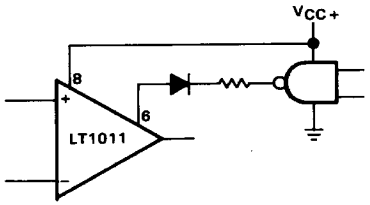



**FIGURE 33. DIRECT STROBE DRIVE WHEN CMOS LOGIC USES SAME $V_{CC+}$ SUPPLY AS LT1011 (Not applicable for TTL logic)**

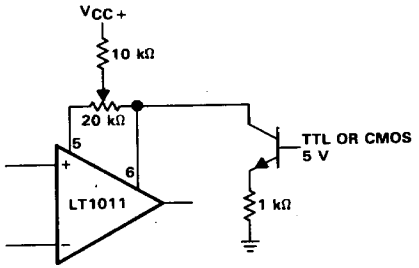



**FIGURE 34. COMBINING OFFSET ADJUSTMENT AND STROBE**





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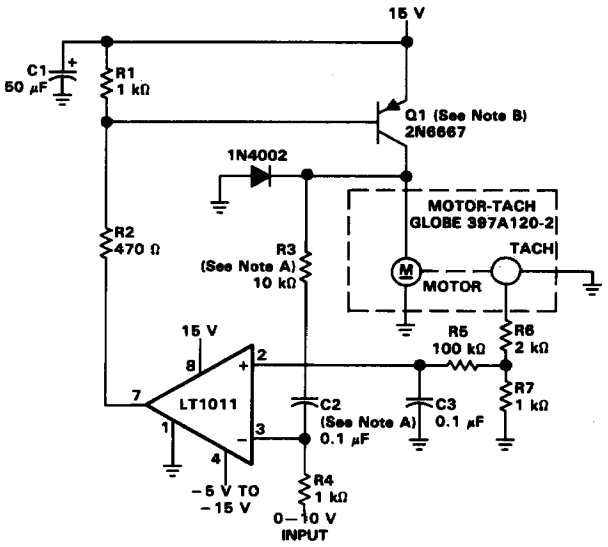
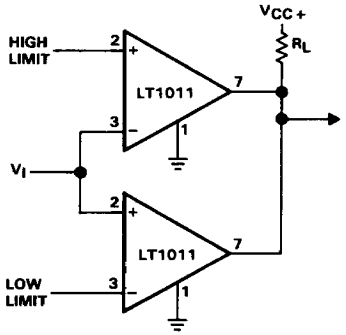
## TYPICAL APPLICATIONS




NOTES: A. R3/C2 determines oscillation frequency of controller.
B. Q1 operates in switch mode.

**FIGURE 35. HIGH-EFFICIENCY MOTOR SPEED CONTROLLER**




NOTE: Output is high inside "window" and low above high limit or below low limit.

**FIGURE 36. WINDOW DETECTOR**

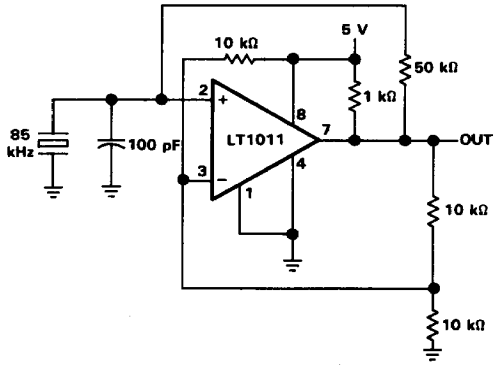
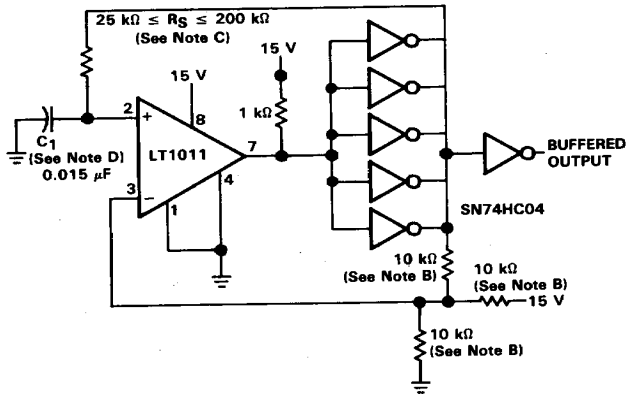


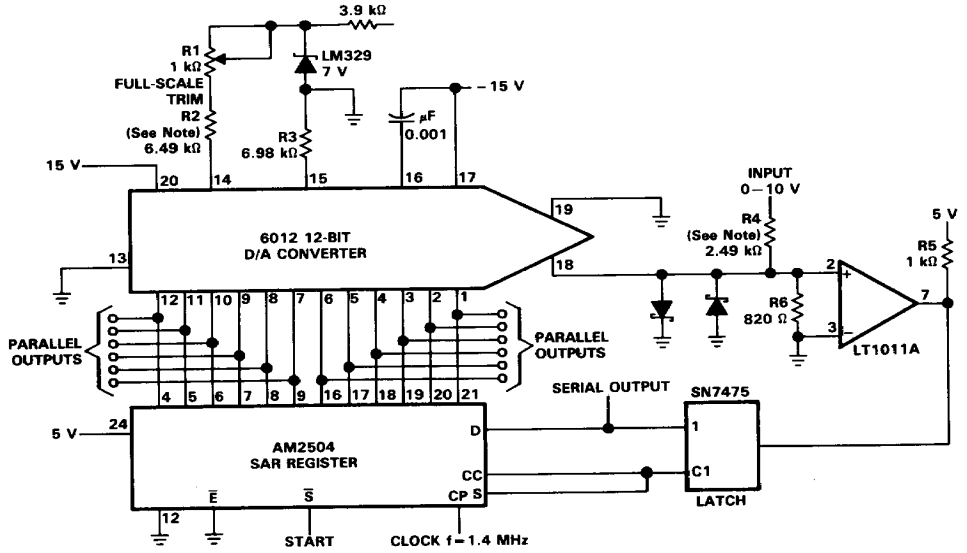

**FIGURE 37. CRYSTAL OSCILLATOR**

## TYPICAL APPLICATIONS




NOTES: A. Low drift and accurate frequency are obtained because this configuration rejects effects due to input offset voltage and input bias current of the comparator.
B. 1% metal film.
C. $R_S$ = TRW type MTR-5/ + 120 ppm/°C.
D. $C_1$ = 0.015 μF = polystyrene : 120 ppm/°C ±30 ppm WESCO type 32-P.
E. Comparator contributes ≤ 10 ppm/°C drift for frequencies below 10 kHz.

**FIGURE 38. LOW-DRIFT R/C OSCILLATOR**




NOTE: R2 and R4 should TC track.

**FIGURE 39. 10-μs 12-BIT A-D CONVERTER**





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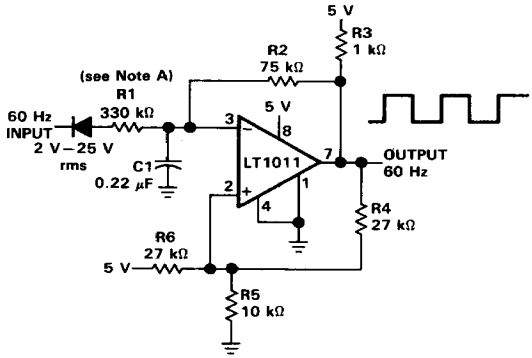
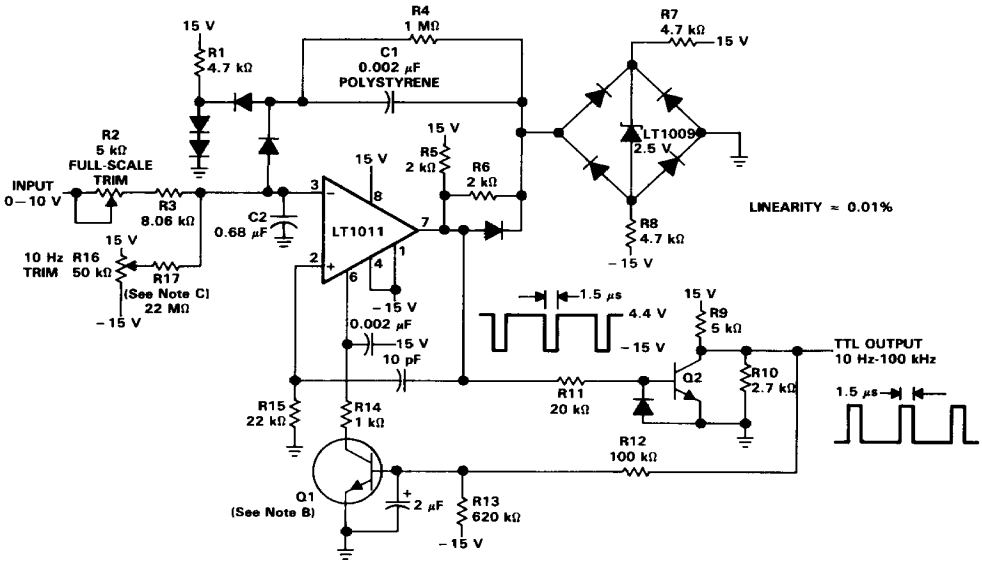
## TYPICAL APPLICATIONS




NOTES: A. Increase R1 for larger input voltages.
B. LT1011 self-oscillates at approximately 60 Hz, thereby "locking" onto incoming line signal.

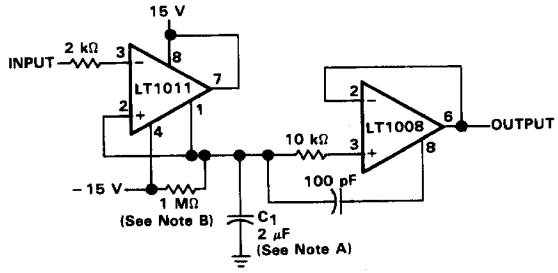
**FIGURE 40. NOISE-IMMUNE 60-Hz LINE SYNCHRONIZATION**




NOTES: A. All diodes 1N4148, transistors 2N3904.
B. Used only to guarantee start-up.
C. R17 may be increased for better 10-Hz trim resolution.

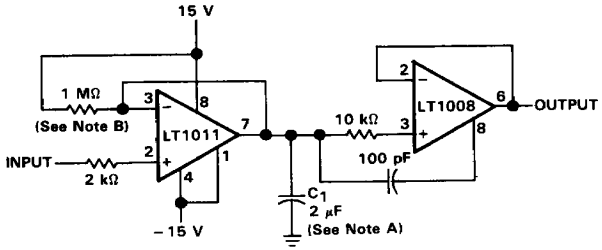
**FIGURE 41. 10-Hz TO 100-kHz VOLTAGE-TO-FREQUENCY CONVERTER**

## TYPICAL APPLICATIONS




NOTES: A. Mylar
B. Set for required reset time constant.

**FIGURE 42. POSITIVE PEAK DETECTOR**




NOTES: A. Mylar
B. Select for required reset time constant.

**FIGURE 43. NEGATIVE PEAK DETECTOR**





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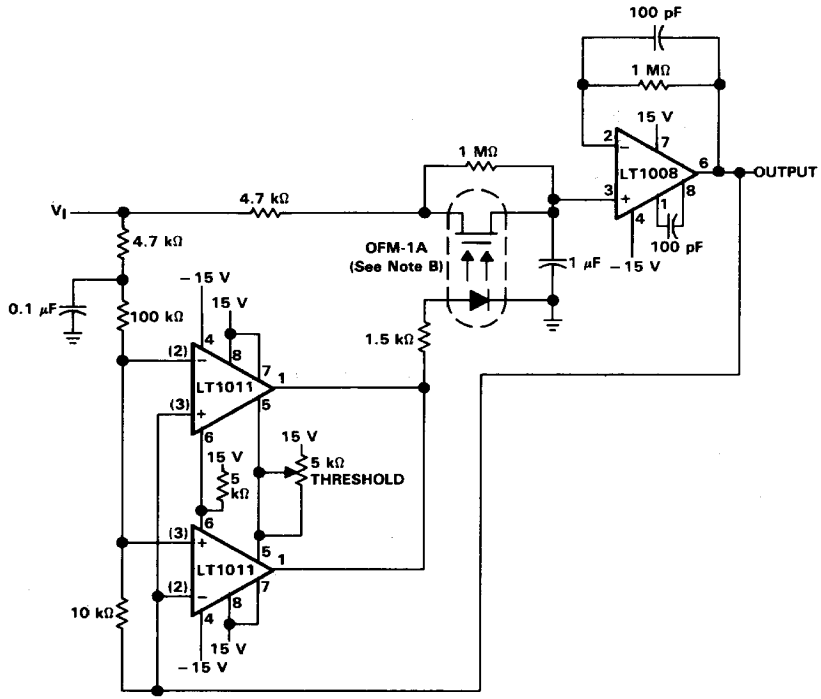
## TYPICAL APPLICATIONS




NOTES: A. The comparators drive the opto-coupled FET "on" when the difference between the output and the input exceeds threshold. When the output approaches the input, the FET turns "off" and low-pass filtering occurs.
B. From Theta-J Corporation, Woburn, Massachusetts.

**FIGURE 44. FAST-SETTLING FILTER**

## TYPICAL APPLICATIONS

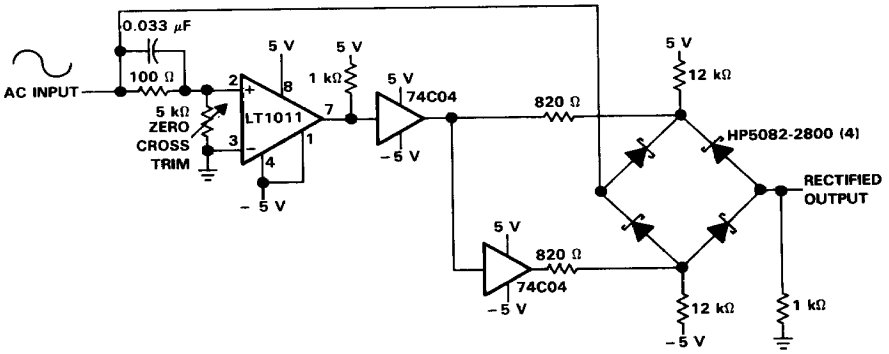
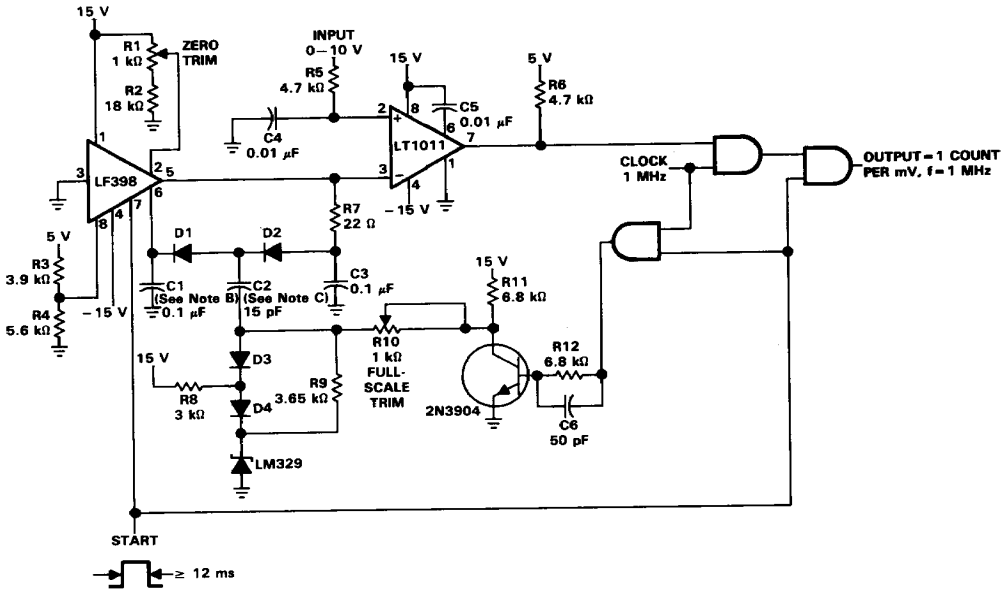



FIGURE 45. 100-kHz PRECISION RECTIFIER




NOTES: A. All diodes 1N4148
B. Polystyrene
C. NPO

FIGURE 46. 4-DIGIT (10,000-COUNT) A-D CONVERTER





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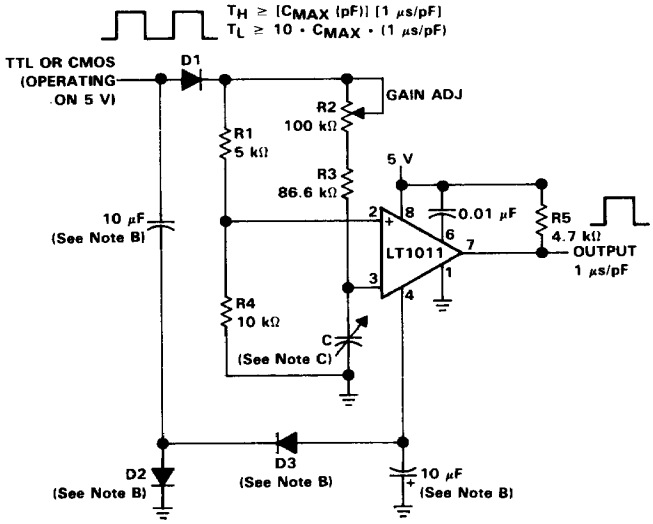
## TYPICAL APPLICATIONS




NOTES: A. PW = (R2 + R3) • (C) • [(R1 + R4)/R1]. The input capacitance of the LT1011 is approximately 6 pF. This is an offset term.
B. These components may be eliminated if negative supply is available (−1 V to −15 V).
C. Typical two sections of 365-pF variable capacitor when used as shaft-angle indication.

**FIGURE 47. CAPACITANCE-TO-PULSE-WIDTH CONVERTER**