T-58-11-31

LT1074/LT1076

Step-Down Switching Regulator

FEATURES

- 5A On-Board Switch (LT1074)
- Up to 200kHz Switching Frequency
- Greatly Improved Dynamic Behavior
- Available in Low Cost 5-Lead Packages
- Only 8.5mA Quiescent Current
- Programmable Current Limit
- Operates Up to 60V Input
- Includes Output Voltage Monitor
- Micropower Shutdown Mode

APPLICATIONS

- Buck Converter with Output Voltage Range of 2.5V to 50V
- Tapped Inductor Buck Converter with 10A Output at 5V
- Positive-to-Negative Converter
- Negative Boost Converter
- Multiple Output Buck Converter

DESCRIPTION

The LT1074 is a 5A (LT1076 is rated at 2A) monolithic bipolar switching regulator which requires only a few external parts for normal operation. The power switch, all oscillator and control circuitry, all current limit components, and an output monitor are included on the chip. The topology is a classic positive "buck" configuration but several design innovations allow this device to be used as a positive to negative converter, a negative boost converter, and as a flyback converter. The switch output is specified to swing 40V below ground, allowing the LT1074 to drive a tapped inductor in the buck mode with output currents up to 10A.

The LT1074 uses a true analog multiplier in the feedback loop. This makes the device respond nearly instantaneously to input voltage fluctuations and makes loop gain independent of input voltage. As a result, dynamic behavior of the regulator is significantly improved over previous designs.

On-chip pulse by pulse current limiting makes the LT1074 nearly bust-proof for output overloads or shorts. The input voltage range as a buck converter is 8V to 60V, but a self-boot feature allows input voltages as low as 5V in the inverting and boost configurations.

The LT1074 is available in low cost 5-lead TO-220 or TO-3 packages with frequency pre-set at 100kHz and current limit at 6.5A (LT1076 = 2.6A). An 11-pin single-in-line package (SIP) is also available which allows switching frequency to be increased to 200kHz and current limit to be adjusted down to zero. In addition, full micropower shutdown can be programmed as well as external current sensing, and soft start. An output monitor "status" pin can be used as a microprocessor reset, and a complementary output pin will allow implementation of extra-high-efficiency designs. See Application Note 44 for design details.

A fixed 5V output, 2A version is also available. See LT1076-5.

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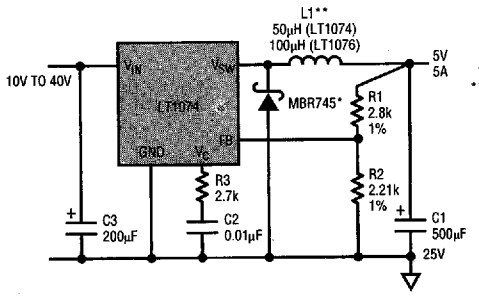
TYPICAL APPLICATION

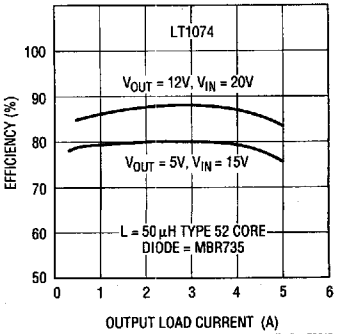
Basic Positive Buck Converter



*USE MBR340 FOR LT1076
**COILTRONICS #50-2-52 (LT1074)
#100-1-52 (LT1076)
PULSE ENGINEERING, INC.
#PE-92114 (LT1074)
#PE-92102 (LT1076)
HURRICANE #HL-AK147QQ (LT1074)
#HL-AG210LL (LT1076)

LT1074 • TA01

Buck Converter Efficiency



LT1074 • TPC27

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- LT1074/ LT1076 ..... 45V
- LT1074HV/76HV 64V

Switch Voltage with Respect to Input Voltage
- LT1074/ 76 ..... 64V
- LT1074HV/76HV 75V

Switch Voltage with Respect to Ground Pin (V_{SW} **Negative**)
- LT1074/76 (Note 6) 35V
- LT1074HV/76HV (Note 6) 45V

Feedback Pin Voltage ..... –2V, +10V

Shutdown Pin Voltage (Not to Exceed V_{IN}) 40V

Status Pin Voltage* 30V
(Current Must Be Limited to 5mA When Status Pin Switches "On")

Complementary Output Voltage* 30V
(Current Must Be Limited to 20mA When Output Switches "On")

I_{LIM} Pin Voltage (Forced) 5.5V

EXTLIM Pin Voltage* ..... V_{IN} –2V to V_{IN} +0.4V

Freq Pin Voltage* 5.5V

Maximum Operating Ambient Temperature Range
- LT1074C/76C, LT1074HVC/76HVC ..... 0°C to 70°C
- LT1074M/76M, LT1074HVM/76HVM .. –55°C to 125°C
- LT1074I/76I, LT1074HVI/76HVI ..... –40°C to 85°C

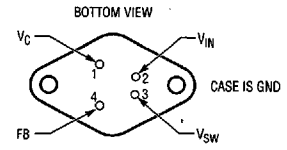
Maximum Operating Junction Temperature Range
- LT1074C/76C, LT1074HVC/76HVC ..... 0°C to 125°C
- LT1074M/76M, LT1074HVM/76HVM ... –55°C to 150°C
- LT1074I/76I, LT1074HVI/76HVI ..... –40°C to 125°C

Maximum Storage Temperature ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

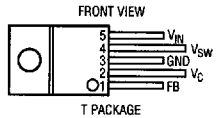
*** Refers to pins on the 11-pin package, which is not recommended for new designs.**

PACKAGE/ORDER INFORMATION



K PACKAGE
4-LEAD TO-3 METAL CAN

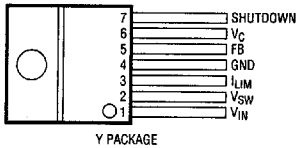
ORDER PART NUMBER: LT1074MK, LT1074CK, LT1074HVCK, LT1076MK



T PACKAGE
5-LEAD TO-220

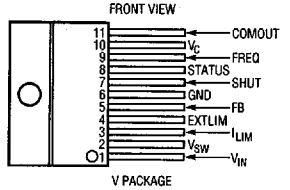
LEADS ARE FORMED STANDARD.
FOR STRAIGHT LEADS, ORDER FLOW 06.

ORDER PART NUMBER: LT1074CT, LT1074HVCT, LT1076CT, LT1076HVCT, LT1074IT, LT1074HVIT, LT1076IT, LT1076HVIT



Y PACKAGE
7-LEAD TO-220

ORDER PART NUMBER: LT1074CY



V PACKAGE
11-LEAD SIP

CASE IS CONNECTED TO GROUND.
LEADS ARE FORMED.

ORDER PART NUMBER: LT1074CV, LT1074HVCV, LT1076CV, LT1076HVCV

ELECTRICAL CHARACTERISTICS

T_j = 25°C, V_{IN} = 25V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch "On" Voltage (Note 1)	LT1074 I_{SW} = 1A, $T_j \geq 0°C$				1.85	V
	I_{SW} = 1A, $T_j < 0°C$				2.10	V
	I_{SW} = 5A, $T_j \geq 0°C$				2.30	V
	I_{SW} = 5A, $T_j < 0°C$				2.50	V
	LT1076 I_{SW} = 0.5A	●			1.2	V
	I_{SW} = 2A	●			1.7	V
Switch "Off" Leakage	LT1074 $V_{IN} \leq 25V$, V_{SW} = 0			5	300	µA
	$V_{IN} = V_{MAX}$, V_{SW} = 0 (Note 7)			10	500	µA
	LT1076 V_{IN} = 25V, V_{SW} = 0				150	µA
	$V_{IN} = V_{MAX}$, V_{SW} = 0 (Note 7)				250	µA
Supply Current (Note 2)	V_{FB} = 2.5V, $V_{IN} \leq 40V$	●		8.5	11	mA
	40V < V_{IN} < 60V	●		9	12	mA
	V_{SHUT} = 0.1V (Device Shutdown) (Note 8)	●		140	300	µA

ELECTRICAL CHARACTERISTICS

T_j = 25°C, V_{IN} = 25V, unless otherwise noted. T-58-11-31

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Supply Voltage	Normal Mode Startup Mode (Note 3)	● ●		7.3 3.5	8.0 4.8	V V
Switch Current Limit (Note 4)	LT1074 I_{LIM} Open R_{LIM} = 10k (Note 5) R_{LIM} = 7k (Note 5)	●	5.5	6.5 4.5 3	8.5	A A A
	LT1076 I_{LIM} Open R_{LIM} = 10k (Note 5) R_{LIM} = 7k (Note 5)	●	2	2.6 1.8 1.2	3.2	A A A
Maximum Duty Cycle		●	85	90		%
Switching Frequency	$T_j \leq 125°C$ $T_j > 125°C$ V_{FB} = 0V through 2kΩ (Note 4)	 ● ●	90 85 85	100 20	110 120 125	kHz kHz kHz kHz
Switching Frequency Line Regulation	$8V \leq V_{IN} \leq V_{MAX}$ (Note 7)	●		0.03	0.1	%/V
Error Amplifier Voltage Gain (Note 6)	$1V \leq V_C \leq 4V$			2000		V/V
Error Amplifier Transconductance			3700	5000	8000	µmho
Error Amplifier Source and Sink Current	Source (V_{FB} = 2V) Sink (V_{FB} = 2.5V)		100 0.7	140 1	225 1.6	µA mA
Feedback Pin Bias Current	$V_{FB} = V_{REF}$	●		0.5	2	µA
Reference Voltage	V_C = 2V	●	2.155	2.21	2.265	V
Reference Voltage Tolerance	V_{REF} (Nominal) = 2.21V All Conditions of Input Voltage, Output Voltage, Temperature and Load Current	 ●		±0.5 ±1	±1.5 ±2.5	% %
Reference Voltage Line Regulation	$8V \leq V_{IN} \leq V_{MAX}$ (Note 7)	●		0.005	0.02	%/V
V_C Voltage at 0% Duty Cycle	 Over Temperature	 ●		1.5 −4		V mV/°C
Multiplier Reference Voltage				24		V
Shutdown Pin Current	V_{SH} = 5V $V_{SH} \leq V_{THRESHOLD}$ (≅2.5V)	● ●	5	10	20 50	µA µA
Shutdown Thresholds	Switch Duty Cycle = 0 Fully Shut Down	● ●	2.2 0.1	2.45 0.3	2.7 0.5	V V
Status Window*	As a Percent of Feedback Voltage		4	±5	6	%
Status High Level*	I_{STATUS} = 10µA Sourcing	●	3.5	4.5	5.0	V
Status Low Level*	I_{STATUS} = 1.6mA Sinking	●		0.25	0.4	V
Status Delay Time*				9		µs
Status Minimum Width*				30		µs
Freq Pin Voltage*	R_{FREQ} = 15k			1.55		V
COMOUT Saturation Voltage*	I_{SINK} = 10mA	●		0.5	1	V
COMOUT Leakage*	V_{COMOUT} = 30V	●			50	µA
Thermal Resistance Junction to Case	LT1074 LT1076				2.5 4.0	°C/W °C/W

*** Refers to pins on the 11-pin package, which is not recommended for new designs.**

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: To calculate maximum switch "on" voltage at currents between low and high conditions, a linear interpolation may be used.

Note 2: A feedback pin voltage (V_{FB}) of 2.5V forces the V_C pin to its low clamp level and the switch duty cycle to zero. This approximates the zero load condition where duty cycle approaches zero.

Note 3: Total voltage from V_{IN} pin to ground pin must be ≥ 8V after startup for proper regulation. For T_A < 25°C, limit = 5V.

Note 4: Switch frequency is internally scaled down when the feedback pin voltage is less than 1.3V to avoid extremely short switch on times. During testing, V_{FB} is adjusted to give a minimum switch on time of 1µs.

Note 5: $I_{LIM} \approx \frac{R_{LIM} - 1k}{2k}$ (LT1074), $I_{LIM} \approx \frac{R_{LIM} - 1k}{5.5k}$ (LT1076).

Note 6: Switch to input voltage limitation must also be observed.

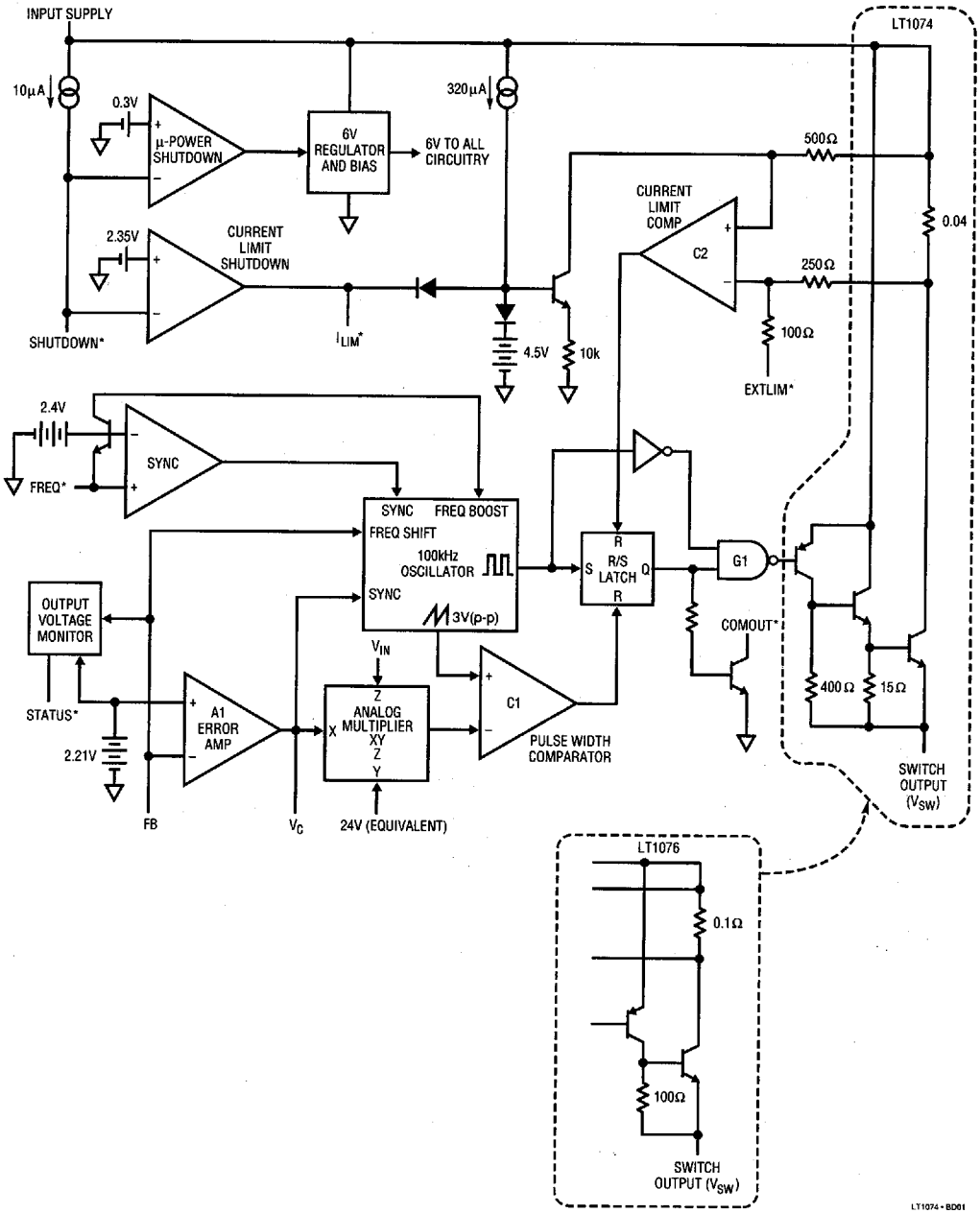
Note 7: V_{MAX} = 40V for the LT1074/76 and 60V for the LT1074HV/76HV.

Note 8: Does not include switch leakage.

4

BLOCK DIAGRAM

T-58-11-31



*Available only on the 11-pin package, which is not recommended for new designs.

BLOCK DIAGRAM DESCRIPTION

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A switch cycle in the LT1074 is initiated by the oscillator setting the R/S latch. The pulse that sets the latch also locks out the switch via gate G1. The effective width of this pulse is approximately 700ns, which sets the maximum switch duty cycle to approximately 93% at 100kHz switching frequency. The switch is turned off by comparator C1, which resets the latch. C1 has a sawtooth waveform as one input and the output of an analog multiplier as the other input. The multiplier output is the product of an internal reference voltage, and the output of the error amplifier, A1, divided by the regulator input voltage. In standard buck regulators, this means that the output voltage of A1 required to keep a constant regulated output is independent of regulator input voltage. This greatly improves line transient response, and makes loop gain independent of input voltage. The error amplifier is a transconductance type with a G_M at null of approximately 5000μmho. Slew current going positive is 140μA, while negative slew current is about 1.1mA. This asymmetry helps prevent overshoot on startup. Overall loop frequency compensation is accomplished with a series RC network from V_C to ground.

Switch current is continuously monitored by C2, which resets the R/S latch to turn the switch off if an overcurrent condition occurs. The time required for detection and switch turn off is approximately 600ns. So minimum switch "on" time in current limit is 600ns. Under dead shorted output conditions, switch duty cycle may have to be as low as 2% to maintain control of output current. This would require switch on time of 200ns at 100kHz switching frequency, so frequency is reduced at very low output voltages by feeding the FB signal into the oscillator and creating a linear frequency downshift when the FB signal drops below 1.3V. Current trip level is set by the voltage on the I_{LIM} pin which is driven by an internal 320μA current source. When this pin is left open, it self-clamps at about 4.5V and sets current limit at 6.5A for the LT1074 and 2.6A for the LT1076. An external resistor can be connected from the I_{LIM} pin to ground to set a lower current limit. A capacitor in parallel with this resistor will soft start the current limit. A slight offset in C2 guarantees that when the I_{LIM} pin is pulled to within 200mV of ground, C2 output will stay high and force switch duty cycle to zero.

An output voltage monitor is included on the chip. Its output is available only on the 11-pin* version. The monitor output* goes low when the voltage on the FB pin is more than 5% above or below the normal regulated value. This pin can be used to "hold off" load functions until the regulator output is normal or it can be used as a microprocessor reset.

The "Freq" pin* is used to raise switching frequency, and to synchronize the oscillator to an external signal. A resistor to ground will raise frequency. A 3V-5V pulse coupled through a diode will synchronize the internal oscillator from 110% to 160% of its normal frequency. The pulse should be 300ns wide. Synchronizing can also be done with the 5-lead LT1074 by pulling the V_C pin to ground for 300ns with a transistor. This has only a slight effect on regulated output voltage if the series resistor in the frequency compensation network is at least 1kΩ.

The "Shutdown" pin is used to force switch duty cycle to zero by pulling the I_{LIM} pin low, or to completely shut down the regulator. Threshold for the former is approximately 2.35V, and for complete shutdown, approximately 0.3V. Total supply current in shutdown is about 150μA. A 10μA pull-up current forces the shutdown pin high when left open. A capacitor can be used to generate delayed startup. A resistor divider will program "undervoltage lockout" if the divider voltage is set at 2.35V when the input is at the desired trip point.

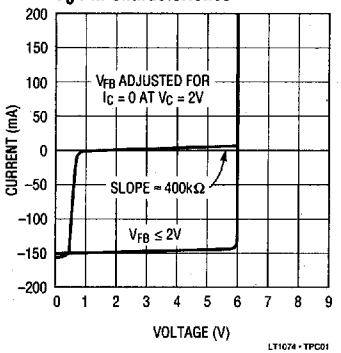
The "Comout" pin* is an open collector switch whose voltage is the complement of the switch output (V_{SW}). In addition, the edges of Comout are slightly time-shifted to avoid overlap with V_{SW}. Comout is used to drive external MOSFETs in certain mutliple-output and high efficiency applications.

The switch used in the LT1074 is a Darlington NPN (single NPN for LT1076) driven by a saturated PNP. Special patented circuitry is used to drive the PNP on and off very quickly even from the saturation state. This particular switch arrangement has no "isolation tubs" connected to the switch output, which can therefore swing to 40V below ground.

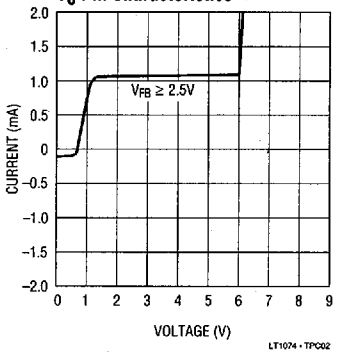
***Available only on the 11-pin package, which is not recommended for new designs.**

TYPICAL PERFORMANCE CHARACTERISTICS

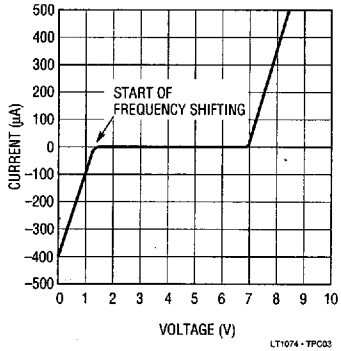
V_C Pin Characteristics



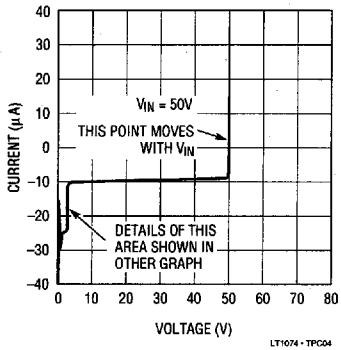
V_C Pin Characteristics



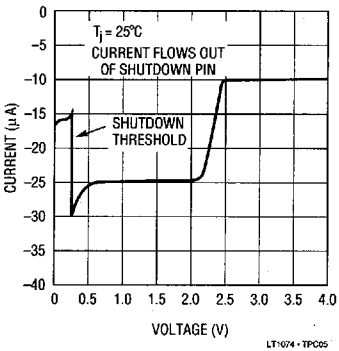
Feedback Pin Characteristics



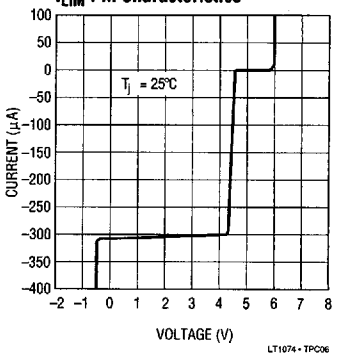
Shutdown Pin Characteristics



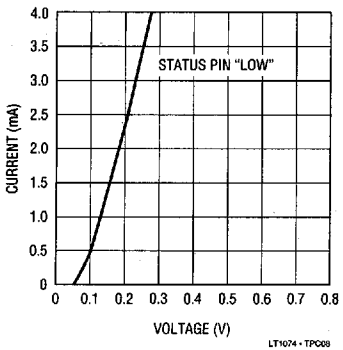
Shutdown Pin Characteristics



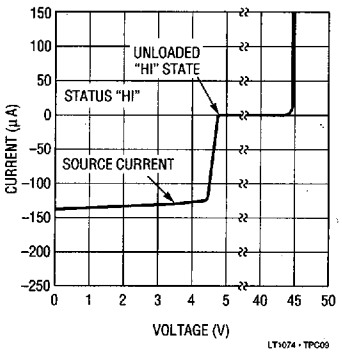
I_{LIM} Pin Characteristics



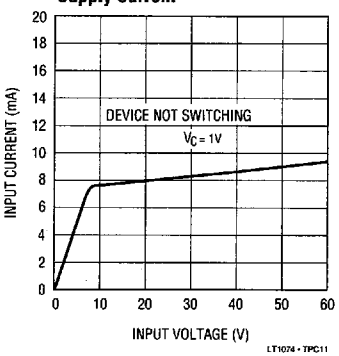
Status Pin Characteristics



Status Pin Characteristics



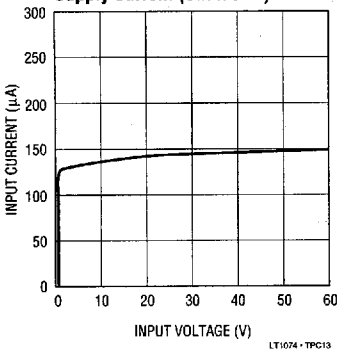
Supply Current



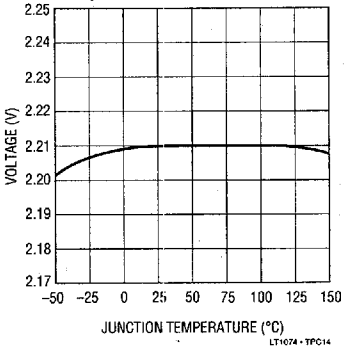
TYPICAL PERFORMANCE CHARACTERISTICS

T-58-11-31

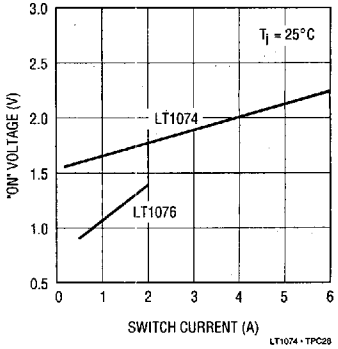
Supply Current (Shutdown)



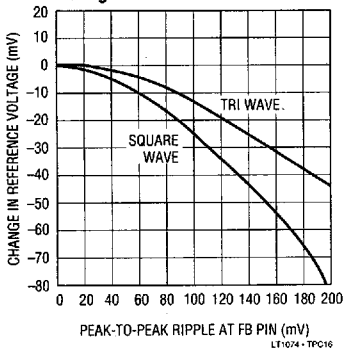
Reference Voltage vs Temperature



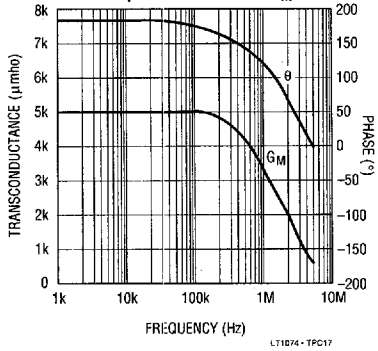
Switch "On" Voltage



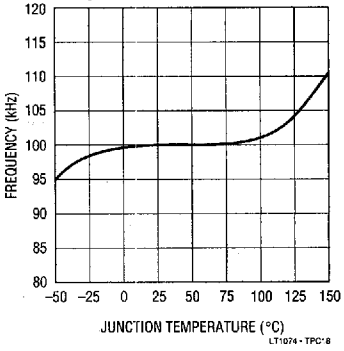
Reference Shift with Ripple Voltage



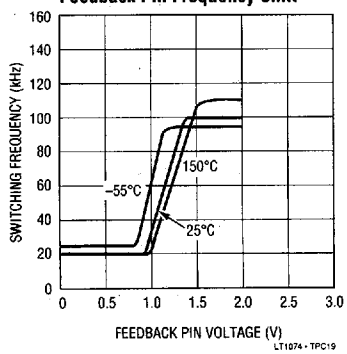
Error Amplifier Phase and G_M



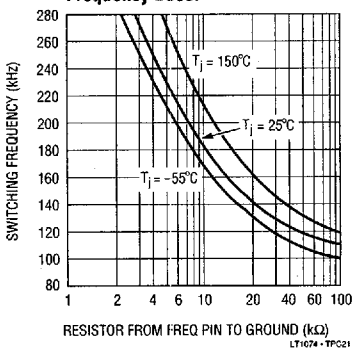
Switching Frequency vs Temperature



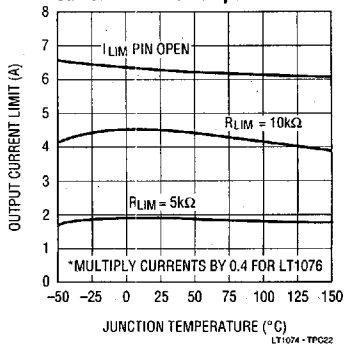
Feedback Pin Frequency Shift



Frequency Boost



Current Limit vs Temperature*



PIN DESCRIPTIONS

V_{IN} PIN

The V_{IN} pin is both the supply voltage for internal control circuitry and one end of the high current switch. It is important, *especially at low input voltages*, that this pin be bypassed with a low ESR, and low inductance capacitor to prevent transient steps or spikes from causing erratic operation. At full switch current of 5A, the switching transients at the regulator input can get very large as shown in Figure 1. Place the input capacitor very close to the regulator and connect it with wide traces to avoid extra inductance. Use radial lead capacitors.

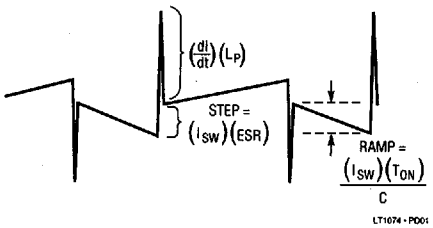


Figure 1. Input Capacitor Ripple

L_P = Total inductance in input bypass connections and capacitor.

"Spike" height $\left(\frac{dI}{dt} \bullet L_P\right)$ is approximately 2V *per inch* of lead length.

Step = 0.25V for ESR = 0.05Ω and I_{SW} = 5A is 0.25V.

Ramp = 125mV for C = 200µF, T_{ON} = 5µs, and I_{SW} = 5A is 125mV.

Input current on the V_{IN} Pin in shutdown mode is the sum of actual supply current (≈140µA, with a maximum of 300µA) and switch leakage current. Consult factory for special testing if shutdown mode input current is critical.

GROUND PIN

It might seem unusual to describe a ground pin, but in the case of regulators, the ground pin must be connected properly to ensure good load regulation. The internal reference voltage is referenced to the ground pin; so any error in ground pin voltage will be multiplied at the output;

$$\Delta V_{OUT} = \frac{(\Delta V_{GND})(V_{OUT})}{2.21}$$

To ensure good load regulation, the ground pin must be connected directly to the proper output node, so that no high currents flow in this path. The output divider resistor should also be connected to this low current connection line as shown in Figure 2.

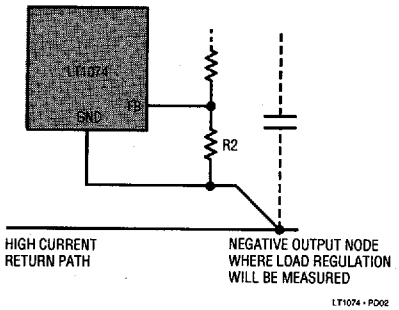


Figure 2. Proper Ground Pin Connection

FEEDBACK PIN

The feedback pin is the inverting input of an error amplifier which controls the regulator output by adjusting duty cycle. The non-inverting input is internally connected to a trimmed 2.21V reference. Input bias current is typically 0.5µA when the error amplifier is balanced (I_{OUT} = 0). The error amplifier has asymmetrical G_M for large input signals to reduce startup overshoot. This makes the amplifier more sensitive to large ripple voltages at the feedback pin. 100mVp-p ripple at the feedback pin will create a 14mV offset in the amplifier, equivalent to a 0.7% output voltage shift. To avoid output errors, output ripple (p-p) should be less than 4% of DC output voltage at the point where the output divider is connected.

See the "Error Amplifier" section for more details.

Frequency Shifting at the Feedback Pin

The error amplifier feedback pin (FB) is used to downshift the oscillator frequency when the regulator output voltage

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is low. This is done to guarantee that output short circuit current is well controlled even when switch duty cycle must be extremely low. Theoretical switch "on" time for a buck converter in continuous mode is;

$$t_{ON} = \frac{V_{OUT} + V_D}{V_{IN} \bullet f}$$

V_D = Catch diode forward voltage (≈ 0.5V)
f = Switching frequency

At f = 100kHz, t_{ON} must drop to 0.2µs when V_{IN} = 25V and the output is shorted (V_{OUT} = 0V). In current limit, the LT1074 can reduce t_{ON} to a minimum value of ≈ 0.6µs, much too long to control current correctly for V_{OUT} = 0. To correct this problem, switching frequency is lowered from 100kHz to 20kHz as the FB pin drops from 1.3V to 0.5V. This is accomplished by the circuitry shown in Figure 3.

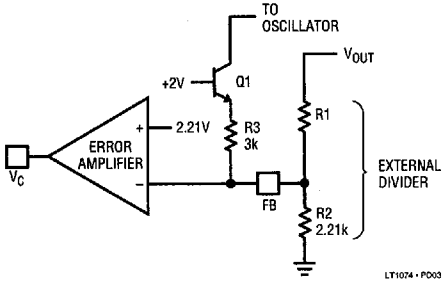

Figure 3. Frequency Shifting

Q1 is off when the output is regulating (V_{FB} = 2.21V). As the output is pulled down by an overload, V_{FB} will eventually reach 1.3V, turning on Q1. As the output continues to drop, Q1 current increases proportionately and lowers the frequency of the oscillator. Frequency shifting starts when the output is ≈ 60% of normal value, and is down to its minimum value of ≅ 20kHz when the output is ≅ 20% of normal value. The rate at which frequency is shifted is determined by both the internal 3k resistor R3 and the external divider resistors. For this reason, R2 should not be increased to more than 4kΩ, if the LT1074 will be subjected to the simultaneous conditions of high input voltage and output short circuit.

Frequency Pin*

The frequency pin can be used to raise switching frequency either by drawing a DC current to ground through a resistor or by feeding in a synchronizing pulse as shown in Figure 4. They can also be done simultaneously. The resistor pulls current through Q_A to increase oscillator ramp current. A pulse fed into the FREQ pin will toggle the sync comparator which will synchronize the oscillator. Figure 5 shows switching frequency versus temperature and resistance value.

A logic level pulse through a diode will synchronize the internal oscillator over a range equal to actual internal frequency up to 1.9 times that frequency. This does *not* mean that an unboosted LT1074 can always be synchronized at 100kHz because the actual switching frequency over temperature can range from 90kHz to 110kHz. Units above 100kHz would not synchronize at 100kHz. Designed synchronizing frequency must be higher than the *maximum* unsynchronized frequency and lower than 1.8 times the *minimum* unsynchronized frequency. For an unboosted unit, this would be 115kHz to 171kHz.

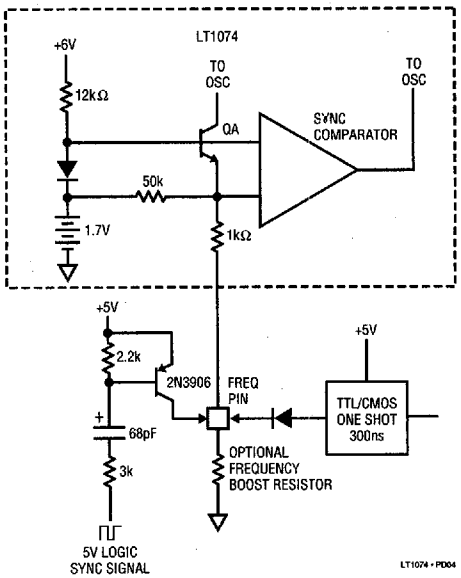

Figure 4. Frequency Pin

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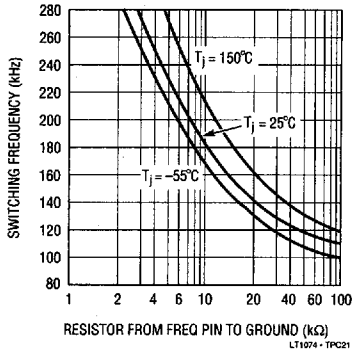

Figure 5. Frequency Boost

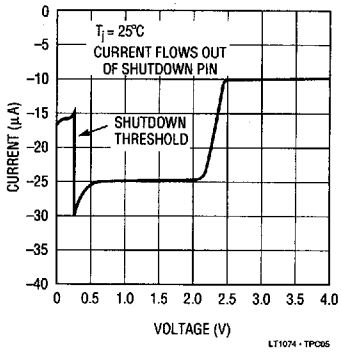

Figure 6. Shutdown Pin Characteristics

The synchronizing pulse should be ≅ 300ns wide. Figure 4 shows how this can be generated with a PNP transistor when the synchronizing signal is wider than 300ns. If a logic one-shot is used, couple it with a diode as shown in Figure 4.

SHUTDOWN PIN

The shutdown pin is used for undervoltage lockout, micropower shutdown, soft start, delayed start, or as a general purpose on/off control of the regulator output. It controls switching action by pulling the I_{LIM} pin low, which forces the switch to a continuous "off" state. Full micropower shutdown is initiated when the shutdown pin drops below 0.3V.

The V/I characteristics of the shutdown pin are shown in Figure 6. For voltages between 2.5V and ≈V_{IN}, a current of 10μA flows *out* of the shutdown pin. This current increases to ≈25μA as the shutdown pin moves through the 2.35V threshold. The current increases further to ≈ 30μA at the 0.3V threshold, then drops to ≈15μA as the shutdown voltage falls below 0.3V. The 10μA current source is included to pull the shutdown pin to its high or default state when left open. It also provides a convenient pullup for delayed start applications with a capacitor on the shutdown pin.

When activated, the typical collector current of Q1 in Figure 7, is ≈ 2mA. A soft start capacitor on the I_{LIM} pin will delay regulator shutdown in response to C1, by ≈(5V)(C_{LIM})/2mA. Soft start after full micropower shutdown is ensured by coupling C2 to Q1.

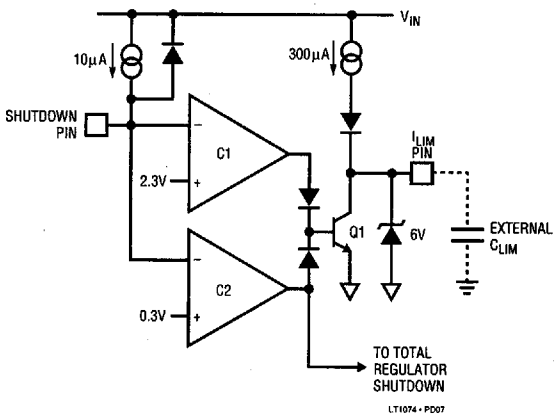

Figure 7. Shutdown Circuitry

Undervoltage Lockout

Undervoltage lockout point is set by R1 and R2 in Figure 8. To avoid errors due to the 10μA shutdown pin current, R2 is usually set at 5k, and R1 is found from:

$$R1 = R2\frac{(V_{TP} - V_{SH})}{V_{SH}}$$

V_{TP} = Desired undervoltage lockout voltage.
V_{SH} = Threshold for lockout on the shutdown pin = 2.45V.

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If quiescent supply current is critical, R2 may be increased up to 15kΩ, but the denominator in the formula for R2 should replace V_{SH} with $V_{SH} - (10\mu A)(R2)$.

Hysteresis in undervoltage lockout may be accomplished by connecting a resistor (R3) from the I_{LIM} pin to the shutdown pin as shown in Figure 9. D1 prevents the shutdown divider from altering current limit.

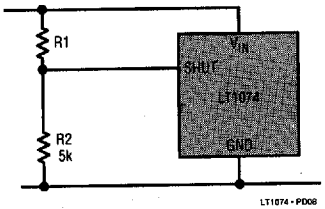

Figure 8. Undervoltage Lockout

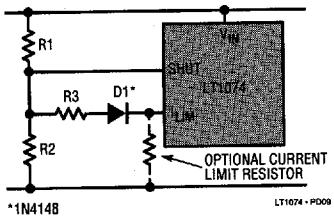

Figure 9. Adding Hysteresis

$$\text{Trip Point} = V_{TP} = 2.35V\left(1+\frac{R1}{R2}\right)$$

If R3 is added, the lower trip point (V_{IN} descending) will be the same. The upper trip point (V_{UTP}) will be;

$$V_{UTP} = V_{SH}\left(1+\frac{R1}{R2}+\frac{R1}{R3}\right) - 0.8V\left(\frac{R1}{R3}\right)$$

If R1 and R2 are chosen, R3 is given by

$$R3 = \frac{(V_{SH} - 0.8V)(R1)}{V_{UTP} - V_{SH}\left(1+\frac{R1}{R2}\right)}$$

Example: An undervoltage lockout is required such that the output will not start until V_{IN} = 20V, but will continue to operate until V_{IN} drops to 15V. Let R2 = 2.32k.

$$R1 = (2.32k)\frac{(15V - 2.35V)}{2.35V} = 12.5k$$

$$R3 = \frac{(2.35 - 0.8)(12.5)}{20 - 2.35\left(1+\frac{12.5}{2.32}\right)} = 3.9k$$

STATUS PIN*

The status pin is the output of a voltage monitor "looking" at the feedback pin. It is low for a feedback voltage which is more than 5% above or below nominal. "Nominal" in this case means the internal reference voltage, so that the ±5% window tracks the reference voltage. A time delay of ≈ 10μs prevents short spikes from tripping the status low. Once it does go low, a second timer forces it to stay low for a minimum of ≈ 30μs.

The status pin is modeled in Figure 10 with a 130μA pullup to a 4.5V clamp level. The sinking drive is a saturated NPN

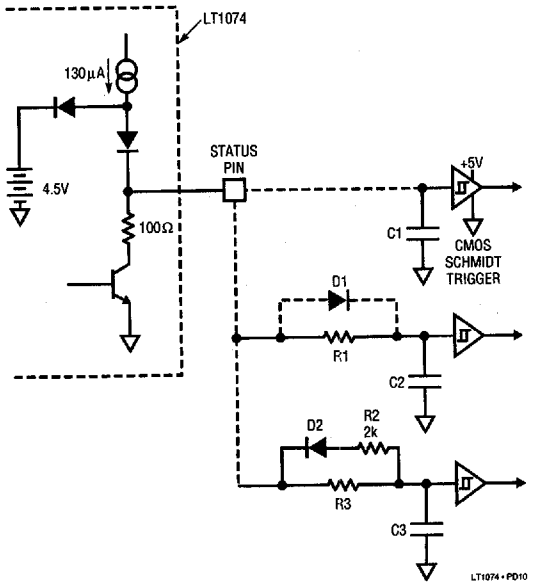

Figure 10. Adding Time Delays to Status Output

*Available only on the 11-pin package, which is not recommended for new designs.

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with ≈100Ω resistance and a maximum sink current of approximately 5mA. An external pullup resistor can be added to increase output swing up to a maximum of 20V.

When the status pin is used to indicate "output OK," it becomes important to test for conditions which might create unwanted status states. These include output overshoot, large signal transient conditions, and excessive output ripple. "False" tripping of the status pin can usually be controlled by a pulse stretcher network as shown in Figure 10. A single capacitor (C1) will suffice to delay an output "OK" (status high) signal to avoid false "true" signals during start-up, etc. Delay time for status high will be approximately (2.3×10^4) (C1), or 23ms/μF. Status low delay will be much shorter, ≈ 600μs/μF.

If false tripping of status "low" could be a problem, R1 can be added. Delay of status high remains the same if R1 ≤ 10kΩ. Status low delay is extended by R1 to approximately R1 • C2 seconds. Select C2 for high delay and R1 for low delay.

Example: Delay status high for 10ms, and status low for 3ms.

$$C2 = \frac{10ms}{23ms/\mu F} = 0.47\mu F \text{ (Use } 0.47\mu F\text{)}$$

$$R1 = \frac{3ms}{C2} = \frac{3ms}{0.47\mu F} = 6.4k\Omega$$

In this example D1 is not needed because R1 is small enough to not limit the charging of C2.

If very fast "low" tripping combined with long "high" delays is desired, use the D2, R2, R3, C3 configuration. C3 is chosen first to set "low" delay

$$C3 \approx \frac{t_{LOW}}{2k\Omega}$$

R3 is then selected for "high" delay

$$R3 \approx \frac{t_{HIGH}}{C3}$$

For t_{LOW} = 100μs and t_{HIGH} = 10ms, C3 = 0.05μF and R3 = 200kΩ.

COMOUT PIN*

The comout pin is intended to be used to drive an external low on-resistance MOSFET which parallels the catch diode. This can improve efficiency considerably for higher input voltages where the diode is "on" for most of the time. Comout is an open collector NPN with 30V maximum operating voltage and a saturation resistance of ≈ 50Ω. It has a typical sink current of 40mA with the saturation voltage guaranteed at 20mA.

EXTLIM PIN*

EXTLIM is intended as a sense pin for current limit when external power transistors are added. It can also be used to raise internal current limit by connecting an external resistor from EXTLIM to the V_{IN} pin. Current limit (minimum) can be increased from 5.5A to 6.5A with a 5.6kΩ resistor. This is allowed only for commercial parts operated at less than 40V input voltage. Capacitance between the EXTLIM pin and V_{SW} pin or ground should be minimized. Do not bypass the EXTLIM pin to V_{IN} with a capacitor; this increases internal current limit to a destructive level.

I_{LIM} PIN

The I_{LIM} pin is used to reduce current limit below the preset value of 6.5A. The equivalent circuit for this pin is shown in Figure 11.

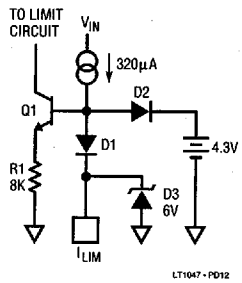

Figure 11. I_{LIM} Pin Circuit

When I_{LIM} is left open, the voltage at Q1 base clamps at 5V through D2. Internal current limit is determined by the current through Q1. If an external resistor is connected

*Available only on the 11-pin package, which is not recommended for new designs.

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between I_{LIM} and ground, the voltage at Q1 base can be reduced for lower current limit. The resistor will have a voltage across it equal to (320μA) (R), limited to ≈5V when clamped by D2. Resistance required for a given current limit is

$$R_{LIM} = I_{LIM}\,(2k\Omega) + 1k\Omega \text{ (LT1074)}$$

$$R_{LIM} = I_{LIM}\,(5.5k\Omega) + 1k\Omega \text{ (LT1076)}$$

As an example, a 3A current limit would require 3A (2k) + 1k = 7kΩ for the LT1074. The accuracy of these formulas is ±25% for $2A \le I_{LIM} \le 5A$ (LT1074) and $0.7A \le I_{LIM} \le 1.8A$ (LT1076), so I_{LIM} should be set at least 25% above the *peak* switch current required.

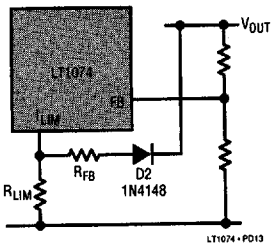

Figure 12. Foldback Current Limit

Foldback current limiting can be easily implemented by adding a resistor from the output to the I_{LIM} pin as shown in Figure 12. This allows full desired current limit (with or without R_{LIM}) when the output is regulating, but reduces current limit under short circuit conditions. A typical value for R_{FB} is 5kΩ, but this may be adjusted up or down to set the amount of foldback. D2 prevents the output voltage from forcing current back into the I_{LIM} pin. To calculate a value for R_{FB}, first calculate R_{LIM}, then R_{FB};

$$R_{FB} = \frac{(I_{SC} - 0.44^*)(R_L)}{0.5^*(R_L - 1k\Omega) - I_{SC}} \; (R_L \text{ in } k\Omega)$$

*Change 0.44 to 0.16, and 0.5 to 0.18 for LT1076.

Example: $I_{LIM} = 4A$, $I_{SC} = 1.5A$, $R_{LIM} = (4)(2k) + 1k = 9k$

$$R_{FB} = \frac{(1.5 - 0.44)(9k\Omega)}{0.5(9k - 1k) - 1.5} = 3.8k\Omega$$

ERROR AMPLIFIER

The error amplifier in Figure 13 is a single stage design with added inverters to allow the output to swing above and below the common mode input voltage. One side of the amplifier is tied to a trimmed internal reference voltage of 2.21V. The other input is brought out as the FB (feedback) pin. This amplifier has a G_M (voltage "in" to current "out") transfer function of ≈5000μmho. Voltage gain is determined by multiplying G_M times the total equivalent output loading, consisting of the output resistance of Q4 and Q6 in parallel with the series RC external frequency compensation network. At DC, the external RC is ignored, and with a parallel output impedance for Q4 and Q6 of 400kΩ, voltage gain is ≈ 2000. At frequencies above a few hertz, voltage gain is determined by the external compensation, R_C and C_C.

$$A_V = \frac{G_m}{2\pi \bullet f \bullet C_C} \text{ at midfrequencies}$$

$$A_V = G_m \bullet R_C \text{ at highfrequencies}$$

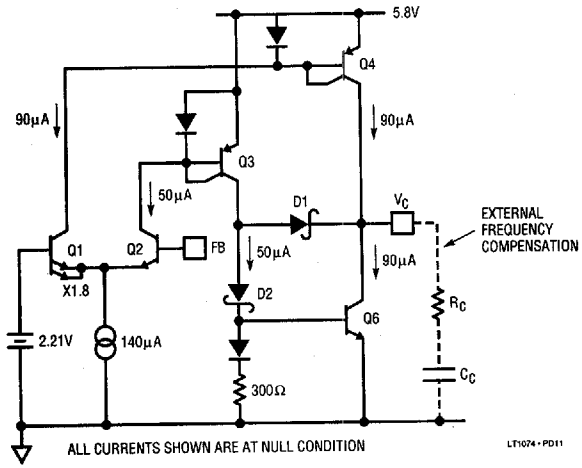

Figure 13. Error Amplifier

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Phase shift from the FB pin to the V_C pin is 90° at mid-frequencies where the external C_C is controlling gain, then drops back to 0° (actually 180° since FB is an inverting input) when the reactance of C_C is small compared to R_C. The low frequency "pole" where the reactance of C_C is equal to the output impedance of Q4 and Q6 (r_O), is

$$f_{POLE} = \frac{1}{2\pi \bullet r_O \bullet C} \quad r_O \approx 400k\Omega$$

Although f_{POLE} varies as much as 3:1 due to r_O variations, mid-frequency gain is dependent only on G_M, which is specified much tighter on the data sheet. The higher frequency "zero" is determined solely by R_C and C_C.

$$f_{ZERO} = \frac{1}{2\pi \bullet R_C \bullet C_C}$$

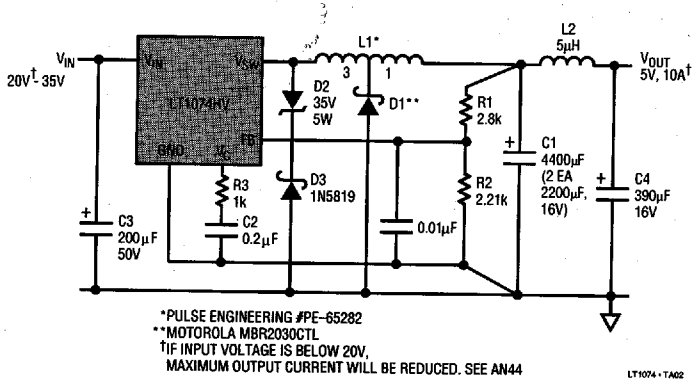
The error amplifier has *asymmetrical* peak output current. Q3 and Q4 current mirrors are unity gain, but the Q6 mirror has a gain of 1.8 at output null and a gain of 8 when the FB pin is high (Q1 current = 0). This results in a maximum positive output current of 140μA and a maximum negative (sink) output current of ≅ 1.1mA. The asymmetry is deliberate — it results in much less regulator output overshoot during rapid startup or following the release of an output overload. Amplifier offset is kept low by area scaling Q1 and Q2 at 1.8:1.

Amplifier swing is limited by the internal 5.8V supply for positive outputs and by D1 and D2 when the output goes low. Low clamp voltage is approximately one diode drop (≈ 0.7V – 2mV/°C).

Note that both the FB pin and the V_C pin have other internal connections. Refer to the frequency shifting and synchronizing discussions.

TYPICAL APPLICATIONS

Tapped Inductor Buck Converter



*PULSE ENGINEERING #PE-65282
**MOTOROLA MBR2030CTL
†IF INPUT VOLTAGE IS BELOW 20V, MAXIMUM OUTPUT CURRENT WILL BE REDUCED. SEE AN44

LT1074 • TA02

TYPICAL APPLICATIONS

Positive to Negative Converter

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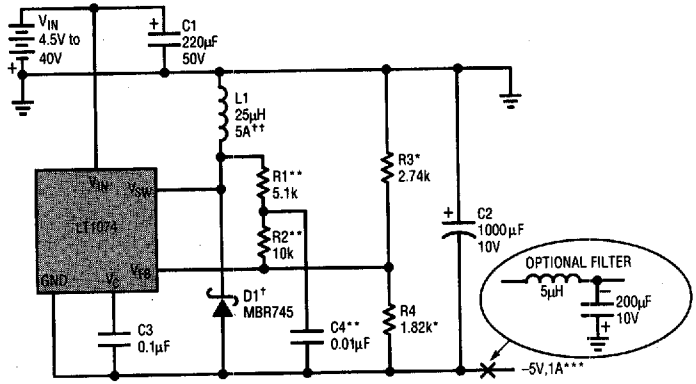

* = 1% FILM RESISTORS
D1 = MOTOROLA-MBR745
C1 = NICHICON-UPL1C221MRH6
C2 = NICHICON-UPL1A102MRH6
L1 = COILTRONICS-CTX25-5-52

† LOWER REVERSE VOLTAGE RATING MAY BE USED FOR LOWER INPUT VOLTAGES. LOWER CURRENT RATING IS ALLOWED FOR LOWER OUTPUT CURRENT. SEE AN44.

†† LOWER CURRENT RATING MAY BE USED FOR LOWER OUTPUT CURRENT. SEE AN44.

** R1, R2, AND C4 ARE USED FOR LOOP FREQUENCY COMPENSATION, BUT R1 AND R2 MUST BE INCLUDED IN THE CALCULATION FOR OUTPUT VOLTAGE DIVIDER VALUES. FOR HIGHER OUTPUT VOLTAGES, INCREASE R1, R2 AND R3 PROPORTIONATELY;
$R3 = V_{OUT} - 2.37\ (K\Omega)$
R1 = (R3) (1.86)
R2 = (R3) (3.65)

*** MAXIMUM OUTPUT CURRENT OF 1A IS DETERMINED BY MINIMUM INPUT VOLTAGE OF 4.5V. HIGHER MINIMUM INPUT VOLTAGE WILL ALLOW MUCH HIGHER OUTPUT CURRENTS. SEE AN44.

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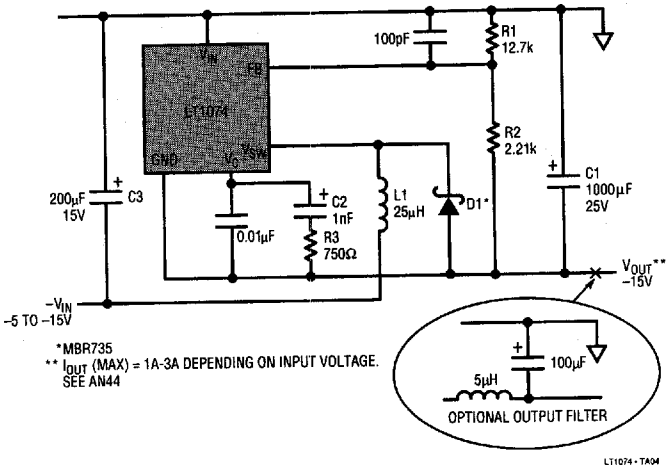
Negative Boost Converter



*MBR735
** I_{OUT} (MAX) = 1A-3A DEPENDING ON INPUT VOLTAGE. SEE AN44

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