Single/Dual 180MHz, 350V/µs Rail-to-Rail Input and Output Low Distortion Op Amps

FEATURES

- **–3dB Bandwidth: 320MHz, $A_V = 1$**
- **Gain-Bandwidth Product: 180MHz, $A_V \geq 10$**
- **Slew Rate: 350V/µs**
- **Wide Supply Range: 2.5V to 12.6V**
- **Large Output Current: 85mA**
- **Low Distortion, 5MHz: –90dBc**
- Input Common Mode Range Includes Both Rails
- Output Swings Rail-to-Rail
- Input Offset Voltage, Rail-to-Rail: 2.5mV Max
- Common Mode Rejection: 89dB Typ
- Power Supply Rejection: 87dB Typ
- Open-Loop Gain: 100V/mV Typ
- Shutdown Pin: LT1809
- Single in 8-Pin SO and 6-Pin SOT-23 Packages
- Dual in 8-Pin SO and MSOP Packages
- Operating Temperature Range: –40°C to 85°C

APPLICATIONS

- Driving A/D Converters
- Low Voltage Signal Processing
- Active Filters
- Rail-to-Rail Buffer Amplifiers
- Video Line Driver

DESCRIPTION

The LT®1809/LT1810 are single/dual low distortion rail-to-rail input and output op amps with a 350V/µs slew rate. These amplifiers have a –3dB bandwidth of 320MHz at unity-gain, a gain-bandwidth product of 180MHz ($A_V \geq 10$) and an 85mA output current to fit the needs of low voltage, high performance signal conditioning systems.

The LT1809/LT1810 have an input range that includes both supply rails and an output that swings within 20mV of either supply rail to maximize the signal dynamic range in low supply applications.

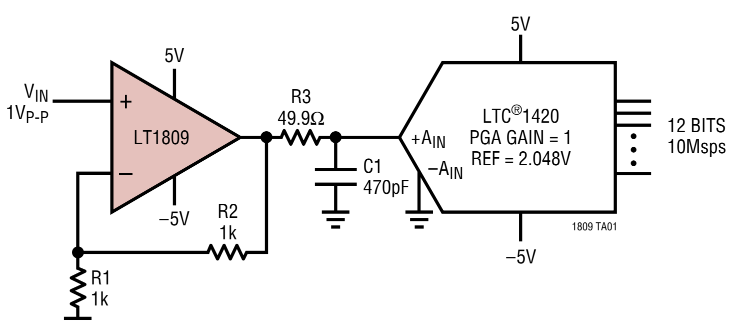
The LT1809/LT1810 have very low distortion (–90dBc) up to 5MHz that allows them to be used in high performance data acquisition systems.

The LT1809/LT1810 maintain their performance for supplies from 2.5V to 12.6V and are specified at 3V, 5V and ±5V supplies. The inputs can be driven beyond the supplies without damage or phase reversal of the output.

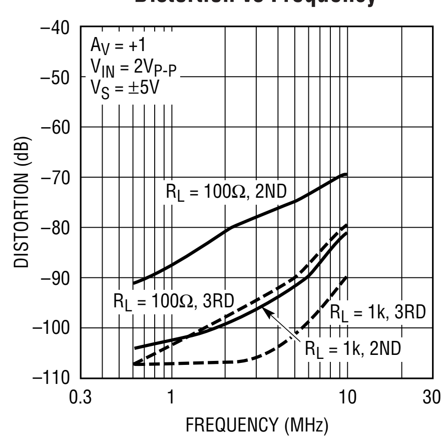
The LT1809 is available in the 8-pin SO package with the standard op amp pinout and the 6-pin SOT-23 package. The LT1810 features the standard dual op amp pinout and is available in 8-pin SO and MSOP packages. These devices can be used as a plug-in replacement for many op amps to improve input/output range and performance.

TYPICAL APPLICATION

High Speed ADC Driver



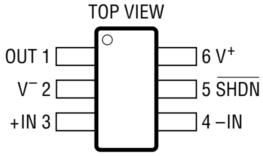
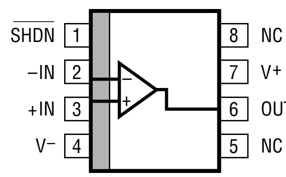
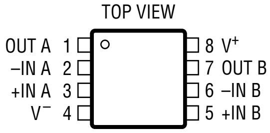
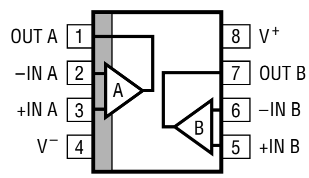
Distortion vs Frequency



ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Input Voltage (Note 2) .... $\pm V_S$
Input Current (Note 2) .... ±10mA
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range (Note 4) .. –40°C to 85°C
Specified Temperature Range (Note 5) ... –40°C to 85°C
Junction Temperature .... 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

Package	ORDER PART NUMBER	Package	ORDER PART NUMBER
TOP VIEW  S6 PACKAGE 6-LEAD PLASTIC SOT-23 T_{JMAX} = 150°C, θ_{JA} = 145°C/W (Note 9)	LT1809CS6 LT1809IS6 **S6 PART MARKING** LTKY LTUF	TOP VIEW  S8 PACKAGE 8-LEAD PLASTIC SO T_{JMAX} = 150°C, θ_{JA} = 100°C/W (Note 9)	LT1809CS8 LT1809IS8 **S8 PART MARKING** 1809 1809I
TOP VIEW  MS8 PACKAGE 8-LEAD PLASTIC MSOP T_{JMAX} = 150°C, θ_{JA} = 130°C/W (Note 9)	LT1810CMS8 LT1810IMS8 **MS8 PART MARKING** LTRF LTTQ	TOP VIEW  S8 PACKAGE 8-LEAD PLASTIC SO T_{JMAX} = 150°C, θ_{JA} = 100°C/W (Note 9)	LT1810CS8 LT1810IS8 **S8 PART MARKING** 1810 1810I

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

T_A = 25°C. V_S = 5V, 0V; V_S = 3V, 0V; $V_{\overline{SHDN}}$ = open; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ LT1809 SO-8 $V_{CM} = V^-$ LT1809 SO-8 $V_{CM} = V^+$ $V_{CM} = V^-$		0.6 0.6 0.6 0.6	2.5 2.5 3.0 3.0	mV mV mV mV
ΔV_{OS}	Input Offset Shift	$V_{CM} = V^-$ to V^+ LT1809 SO-8 $V_{CM} = V^-$ to V^+		0.3 0.3	2.0 2.5	mV mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)			0.7	6	mV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^- + 0.2V$	 –27.5	1.8 –13	8	µA µA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.2V$ to V^+		14.8	35.5	µA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^+$ $V_{CM} = V^- + 0.2V$		0.1 0.2	4 8	µA µA

ELECTRICAL CHARACTERISTICS

T_A = 25°C. V_S = 5V, 0V; V_S = 3V, 0V; $V_{\overline{SHDN}}$ = open; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^- + 0.2V$		0.05 0.2	1.2 4	µA µA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.2V$ to V^+		0.25	5.2	µA
e_n	Input Noise Voltage Density	f = 10kHz		16		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz		5		pA/√Hz
C_{IN}	Input Capacitance			2		pF
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to $V_S/2$ V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to $V_S/2$ V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k to $V_S/2$	25 4 15	80 10 42		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, $V_{CM} = V^-$ to V^+ V_S = 3V, $V_{CM} = V^-$ to V^+	66 61	82 78		dB dB
	CMRR Match (Channel-to-Channel) (Note 10)	V_S = 5V, $V_{CM} = V^-$ to V^+ V_S = 3V, $V_{CM} = V^-$ to V^+	60 55	82 78		dB dB
	Input Common Mode Range		V^-		V^+	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	71	87		dB
	PSRR Match (Channel-to-Channel) (Note 10)	V_S = 2.5V to 10V, V_{CM} = 0V	65	87		dB
	Minimum Supply Voltage (Note 6)			2.3	2.5	V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 25mA		12 50 180	50 120 375	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 25mA		20 80 330	80 180 650	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	±45 ±35	±85 ±70		mA mA
I_S	Supply Current per Amplifier			12.5	17	mA
	Supply Current, Shutdown	V_S = 5V, $V_{\overline{SHDN}}$ = 0.3V V_S = 3V, $V_{\overline{SHDN}}$ = 0.3V		0.55 0.31	1.25 0.90	mA mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	V_S = 5V, $V_{\overline{SHDN}}$ = 0.3V V_S = 3V, $V_{\overline{SHDN}}$ = 0.3V		420 220	750 500	µA µA
	Output Leakage Current, Shutdown	$V_{\overline{SHDN}}$ = 0.3V		0.1	75	µA
V_L	$\overline{SHDN}$ Pin Input Voltage Low				0.3	V
V_H	$\overline{SHDN}$ Pin Input Voltage High		V_S – 0.5			V
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100		80		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100		50		ns
GBW	Gain-Bandwidth Product	Frequency = 2MHz		160		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = $4V_{P-P}$		300		V/µs
FPBW	Full Power Bandwidth	V_S = 5V, V_{OUT} = $4V_{P-P}$		23.5		MHz
THD	Total Harmonic Distortion	V_S = 5V, A_V = 1, R_L = 1k, V_O = $2V_{P-P}$, f_C = 5MHz		–86		dB
t_S	Settling Time	0.1%, V_S = 5V, V_{STEP} = 2V, A_V = –1, R_L = 500Ω		27		ns
ΔG	Differential Gain (NTSC)	V_S = 5V, A_V = 2, R_L = 150Ω		0.015		%
$\Delta\theta$	Differential Phase (NTSC)	V_S = 5V, A_V = 2, R_L = 150Ω		0.05		Deg

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; $V_{\overline{SHDN}}$ = open; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ LT1809 SO-8 $V_{CM} = V^-$ LT1809 SO-8 $V_{CM} = V^+$ $V_{CM} = V^-$	● ● ● ●		1 1 1 1	3.0 3.0 3.5 3.5	mV mV mV mV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	$V_{CM} = V^+$ $V_{CM} = V^-$	● ●		9 9	25 25	µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+ LT1809 SO-8 $V_{CM} = V^-$ to V^+	● ●		0.5 0.5	2.5 3.0	mV mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^-$, $V_{CM} = V^+$	●		1.2	6.5	mV
I_B	Input Bias Current	$V_{CM} = V^+ - 0.2V$ $V_{CM} = V^- + 0.4V$	● ●	 −30	2 −14	10	µA µA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.4V$ to $V^+ - 0.2V$	●		16	40	µA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^+ - 0.2V$ $V_{CM} = V^- + 0.4V$	● ●		0.1 0.5	5 10	µA µA
I_{OS}	Input Offset Current	$V_{CM} = V^+ - 0.2V$ $V_{CM} = V^- + 0.4V$	● ●		0.05 0.40	1.5 4.5	µA µA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.4V$ to $V^+ - 0.2V$	●		0.45	6	µA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to $V_S/2$ V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to $V_S/2$ V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k to $V_S/2$	● ● ●	20 3.5 12	75 8.5 40		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, $V_{CM} = V^-$ to V^+ V_S = 3V, $V_{CM} = V^-$ to V^+	● ●	64 60	80 75		dB dB
	CMRR Match (Channel-to-Channel) (Note 10)	V_S = 5V, $V_{CM} = V^-$, $V_{CM} = V^+$ V_S = 3V, $V_{CM} = V^-$, $V_{CM} = V^+$	● ●	58 54	80 75		dB dB
	Input Common Mode Range		●	V^-		V^+	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	●	70	83		dB
	PSRR Match (Channel-to-Channel) (Note 10)	V_S = 2.5V to 10V, V_{CM} = 0V	●	64	83		dB
	Minimum Supply Voltage (Note 6)		●		2.3	2.5	V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 25mA	● ● ●		12 55 200	60 140 400	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 25mA	● ● ●		50 110 370	120 220 700	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	±40 ±30	±75 ±65		mA mA
I_S	Supply Current per Amplifier		●		15	20	mA
	Supply Current, Shutdown	V_S = 5V, $V_{\overline{SHDN}}$ = 0.3V V_S = 3V, $V_{\overline{SHDN}}$ = 0.3V	● ●		0.58 0.35	1.4 1.1	mA mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	V_S = 5V, $V_{\overline{SHDN}}$ = 0.3V V_S = 3V, $V_{\overline{SHDN}}$ = 0.3V	● ●		420 220	850 550	µA µA
	Output Leakage Current, Shutdown	$V_{\overline{SHDN}}$ = 0.3V	●		2		µA
V_L	$\overline{SHDN}$ Pin Input Voltage Low		●			0.3	V
V_H	$\overline{SHDN}$ Pin Input Voltage High		●	V_S – 0.5			V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; $V_{\overline{SHDN}}$ = open; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100	●		80		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100	●		50		ns
GBW	Gain-Bandwidth Product	Frequency = 2MHz	●		145		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = $4V_{P-P}$	●		250		V/µs
FPBW	Full Power Bandwidth	V_S = 5V, V_{OUT} = $4V_{P-P}$	●		20		MHz

The ● denotes the specifications which apply over the –40°C ≤ T_A ≤ 85°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; $V_{\overline{SHDN}}$ = open; V_{CM} = V_{OUT} = half supply, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+ LT1809 SO-8 V_{CM} = V^- LT1809 SO-8 V_{CM} = V^+ V_{CM} = V^-	● ● ● ●		1 1 1 1	3.5 3.5 4.0 4.0	mV mV mV mV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	V_{CM} = V^+ V_{CM} = V^-	● ●		9 9	25 25	µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = V^- to V^+ LT1809 SO-8 V_{CM} = V^-	● ●		0.5 0.5	3.0 3.5	mV mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	V_{CM} = V^+, V_{CM} = V^-	●		1.2	7	mV
I_B	Input Bias Current	V_{CM} = V^+ – 0.2V V_{CM} = V^- + 0.4V	● ●	 –35	2 –17	12	µA µA
ΔI_B	Input Bias Current Shift	V_{CM} = V^- + 0.4V to V^+ – 0.2V	●		19	47	µA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	V_{CM} = V^+ – 0.2V V_{CM} = V^- + 0.4V	● ●		0.2 0.6	6 12	µA µA
I_{OS}	Input Offset Current	V_{CM} = V^+ – 0.2V V_{CM} = V^- + 0.4V	● ●		0.08 0.5	2 6	µA µA
ΔI_{OS}	Input Offset Current Shift	V_{CM} = V^- + 0.4V to V^+ – 0.2V	●		0.58	7.5	µA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to $V_S/2$ V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to $V_S/2$ V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k to $V_S/2$	● ● ●	17 2.5 10	60 7 35		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = V^- to V^+ V_S = 3V, V_{CM} = V^- to V^+	● ●	63 58	80 75		dB dB
	CMRR Match (Channel-to-Channel) (Note 10)	V_S = 5V, V_{CM} = V^- to V^+ V_S = 3V, V_{CM} = V^- to V^+	● ●	57 52	78 72		dB dB
	Input Common Mode Range		●	V^-		V^+	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	●	69	83		dB
	PSRR Match (Channel-to-Channel) (Note 10)	V_S = 2.5V to 10V, V_{CM} = 0V	●	63	83		dB
	Minimum Supply Voltage (Note 6)		●		2.3	2.5	V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 25mA	● ● ●		18 60 210	70 150 450	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 25mA	● ● ●		55 120 375	130 240 750	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	±30 ±25	±70 ±60		mA mA
I_S	Supply Current per Amplifier		●		15	21	mA
	Supply Current, Shutdown	V_S = 5V, $V_{\overline{SHDN}}$ = 0.3V V_S = 3V, $V_{\overline{SHDN}}$ = 0.3V	● ●		0.58 0.35	1.5 1.2	mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C ≤ T_A ≤ 85°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; $V_{\overline{SHDN}}$ = open; V_{CM} = V_{OUT} = half supply, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	V_S = 5V, $V_{\overline{SHDN}}$ = 0.3V V_S = 3V, $V_{\overline{SHDN}}$ = 0.3V	● ●		420 220	900 600	µA µA
	Output Leakage Current, Shutdown	$V_{\overline{SHDN}}$ = 0.3V	●		3		µA
V_L	$\overline{SHDN}$ Pin Input Voltage Low		●			0.3	V
V_H	$\overline{SHDN}$ Pin Input Voltage High		●	V_S – 0.5			V
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100	●		80		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100	●		50		ns
GBW	Gain-Bandwidth Product	Frequency = 2MHz	●		140		MHz
SR	Slew Rate	V_S = 5V, A_V = -1, R_L = 1k, V_O = $4V_{P-P}$	●		180		V/µs
FPBW	Full Power Bandwidth	V_S = 5V, V_{OUT} = $4V_{P-P}$	●		14		MHz

T_A = 25°C. V_S = ±5V, $V_{\overline{SHDN}}$ = open, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+ LT1809 SO-8 V_{CM} = V^- LT1809 SO-8 V_{CM} = V^+ V_{CM} = V^-		0.8 0.8 0.8 0.8	3.0 3.0 3.5 3.5	mV mV mV mV
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = V^- to V^+ LT1809 SO-8 V_{CM} = V^- to V^+		0.35 0.35	2.5 3.0	mV mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	V_{CM} = V^+, V_{CM} = V^-		1	6	mV
I_B	Input Bias Current	V_{CM} = V^+ V_{CM} = V^- + 0.2V	 –30	2 –12.5	10	µA µA
ΔI_B	Input Bias Current Shift	V_{CM} = V^- + 0.2V to V^+		14.5	40	µA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	V_{CM} = V^+ V_{CM} = V^- + 0.2V		0.1 0.4	5 10	µA µA
I_{OS}	Input Offset Current	V_{CM} = V^+ V_{CM} = V^- + 0.2V		0.05 0.40	2 5	µA µA
ΔI_{OS}	Input Offset Current Shift	V_{CM} = V^- + 0.2V to V^+		0.45	7	µA
e_n	Input Noise Voltage Density	f = 10kHz		16		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz		5		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance	f = 100kHz		2		pF
A_{VOL}	Large-Signal Voltage Gain	V_O = –4V to 4V, R_L = 1k V_O = –2.5V to 2.5V, R_L = 100Ω	30 4.5	100 12		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = V^- to V^+	70	89		dB
	CMRR Match (Channel-to-Channel) (Note 10)	V_{CM} = V^- to V^+	64	89		dB
	Input Common Mode Range		V^-		V^+	V
PSRR	Power Supply Rejection Ratio	V^+ = 2.5V to 10V, V^- = 0V	71	87		dB
	PSRR Match (Channel-to-Channel) (Note 10)	V^+ = 2.5V to 10V, V^- = 0V	65	90		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 25mA		12 50 180	60 140 425	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 25mA		35 90 310	100 200 700	mV mV mV

ELECTRICAL CHARACTERISTICS

T_A = 25°C. V_S = ±5V, $V_{\overline{SHDN}}$ = open, V_{CM} = 0V, V_{OUT} = 0, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{SC}	Short-Circuit Current		±55	±85		mA
I_S	Supply Current per Amplifier			15	20	mA
	Supply Current, Shutdown	$V_{\overline{SHDN}}$ = 0.3V		0.6	1.3	mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0.3V		420	750	µA
	Output Leakage Current, Shutdown	$V_{\overline{SHDN}}$ = 0.3V		0.1	75	µA
V_L	$\overline{SHDN}$ Pin Input Voltage Low				0.3	V
V_H	$\overline{SHDN}$ Pin Input Voltage High		V^+ – 0.5			V
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100		80		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100		50		ns
GBW	Gain-Bandwidth Product	Frequency = 2MHz	110	180		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = ±4V, Measured at V_O = ±3V	175	350		V/µs
FPBW	Full Power Bandwidth	V_{OUT} = $8V_{P-P}$		14		MHz
THD	Total Harmonic Distortion	A_V = 1, R_L = 1k, V_O = $2V_{P-P}$, f_C = 5MHz		–90		dB
t_S	Settling Time	0.1%, V_{STEP} = 8V, A_V = –1, R_L = 500Ω		34		ns
ΔG	Differential Gain (NTSC)	A_V = 2, R_L = 150Ω		0.01		%
Δθ	Differential Phase (NTSC)	A_V = 2, R_L = 150Ω		0.01		Deg

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. V_S = ±5V, $V_{\overline{SHDN}}$ = open, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+ LT1809 SO-8 V_{CM} = V^- LT1809 SO-8 V_{CM} = V^+ V_{CM} = V^-	● ● ● ●		1 1 1 1	3.25 3.25 3.75 3.75	mV mV mV mV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	V_{CM} = V^+ V_{CM} = V^-	● ●		10 10	25 25	µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = V^- to V^+ LT1809 SO-8 V_{CM} = V^- to V^+	● ●		0.5 0.5	2.75 3.25	mV mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	V_{CM} = V^- to V^+	●		1.2	6.5	mV
I_B	Input Bias Current	V_{CM} = V^+ – 0.2V V_{CM} = V^- + 0.4V	● ●	 –37.5	2.5 –15	12.5	µA µA
ΔI_B	Input Bias Current Shift	V_{CM} = V^- + 0.4V to V^+ – 0.2V	●		17.5	50	µA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	V_{CM} = V^+ – 0.2V V_{CM} = V^- + 0.4V	● ●		0.1 0.5	6 12	µA µA
I_{OS}	Input Offset Current	V_{CM} = V^+ – 0.2V V_{CM} = V^- + 0.4V	● ●		0.06 0.5	2.25 6	µA µA
ΔI_{OS}	Input Offset Current Shift	V_{CM} = V^- + 0.4V to V^+ – 0.2V	●		0.56	8.25	µA
A_{VOL}	Large-Signal Voltage Gain	V_O = –4V to 4V, R_L = 1k V_O = –2.5V to 2.5V, R_L = 100Ω	● ●	27 3.5	80 10		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = V^- to V^+	●	69	86		dB
	CMRR Match (Channel-to-Channel) (Note 10)	V_{CM} = V^- to V^+	●	63	86		dB
	Input Common Mode Range		●	V^-		V^+	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. V_S = ±5V, $V_{\overline{SHDN}}$ = open, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	V^+ = 2.5V to 10V, V^- = 0V	●	70	83		dB
	PSRR Match (Channel-to-Channel) (Note 10)	V^+ = 2.5V to 10V, V^- = 0V	●	64	83		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 25mA	● ● ●		20 50 210	80 160 475	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 25mA	● ● ●		60 120 370	140 240 750	mV mV mV
I_{SC}	Short-Circuit Current		●	±45	±75		mA
I_S	Supply Current per Amplifier		●		17.5	25	mA
	Supply Current, Shutdown	$V_{\overline{SHDN}}$= 0.3V	●		0.6	1.5	mA
$I_{\overline{SHDN}}$	$\overline{\text{SHDN}}$ Pin Current	$V_{\overline{SHDN}}$ = 0.3V	●		420	850	µA
	Output Leakage Current, Shutdown	$V_{\overline{SHDN}}$ = 0.3V	●		3		µA
V_L	$\overline{\text{SHDN}}$ Pin Input Voltage Low		●			0.3	V
V_H	$\overline{\text{SHDN}}$ Pin Input Voltage High		●	V^+ – 0.5			V
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100	●		80		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100	●		50		ns
GBW	Gain-Bandwidth Product	Frequency = 2MHz	●	85	170		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = ±4V, Measured at V_O = ±3V	●	140	300		V/µs
FPBW	Full Power Bandwidth	V_{OUT} = $8V_{P-P}$	●		12		MHz

The ● denotes the specifications which apply over the –40°C ≤ T_A ≤ 85°C temperature range. V_S = ±5V, $V_{\overline{SHDN}}$ = open, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+ LT1809 SO-8 V_{CM} = V^- LT1809 SO-8 V_{CM} = V^+ V_{CM} = V^-	● ● ● ●		1 1 1 1	3.75 3.75 4.25 4.25	mV mV mV mV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	V_{CM} = V^+ V_{CM} = V^-	● ●		10 10	25 25	µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = V^- to V^+ LT1809 SO-8 V_{CM} = V^- to V^+	● ●		0.5 0.5	3.00 3.75	mV mV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	V_{CM} = V^- to V^+	●		1.2	7.5	mV
I_B	Input Bias Current	V_{CM} = V^+ – 0.2V V_{CM} = V^- + 0.4V	● ●	 –45	2.8 –17	14	µA µA
ΔI_B	Input Bias Current Shift	V_{CM} = V^- + 0.4V to V^+ – 0.2V	●		19.8	59	µA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	V_{CM} = V^+ – 0.2V V_{CM} = V^- + 0.4V	● ●		0.1 0.6	7 14	µA µA
I_{OS}	Input Offset Current	V_{CM} = V^+ – 0.2V V_{CM} = V^- + 0.4V	● ●		0.08 0.6	2.5 8	µA µA
ΔI_{OS}	Input Offset Current Shift	V_{CM} = V^- + 0.4V to V^+ – 0.2V	●		0.68	10.5	µA
A_{VOL}	Large-Signal Voltage Gain	V_O = –4V to 4V, R_L = 1k V_O = –2.5V to 2.5V, R_L = 100Ω	● ●	22 3	70 10		V/mV V/mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the $-40°C \le T_A \le 85°C$ temperature range. $V_S = \pm5V$, $V_{\overline{SHDN}}$ = open, $V_{CM} = 0V$, $V_{OUT} = 0V$, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+	●	68	86		dB
	CMRR Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^-$ to V^+	●	62	86		dB
	Input Common Mode Range		●	V^-		V^+	V
PSRR	Power Supply Rejection Ratio	$V^+ = 2.5V$ to 10V, $V^- = 0V$	●	69	83		dB
	PSRR Match (Channel-to-Channel) (Note 10)	$V^+ = 2.5V$ to 10V, $V^- = 0V$	●	63	83		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load $I_{SINK} = 5mA$ $I_{SINK} = 25mA$	● ● ●		23 60 220	100 170 525	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load $I_{SOURCE} = 5mA$ $I_{SOURCE} = 25mA$	● ● ●		75 130 375	160 260 775	mV mV mV
I_{SC}	Short-Circuit Current		●	±30	±75		mA
I_S	Supply Current per Amplifier		●		19	25	mA
	Supply Current, Shutdown	$V_{\overline{SHDN}} = 0.3V$	●		0.65	1.6	mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}} = 0.3V$	●		420	900	µA
	Output Leakage Current, Shutdown	$V_{\overline{SHDN}} = 0.3V$	●		4		µA
V_L	$\overline{SHDN}$ Pin Input Voltage Low		●			0.3	V
V_H	$\overline{SHDN}$ Pin Input Voltage High		●	$V^+ - 0.5$			V
t_{ON}	Turn-On Time	$V_{\overline{SHDN}} = 0.3V$ to 4.5V, $R_L = 100$	●		80		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}} = 4.5V$ to 0.3V, $R_L = 100$	●		50		ns
GBW	Gain-Bandwidth Product	Frequency = 2MHz	●	80	160		MHz
SR	Slew Rate	$A_V = -1$, $R_L = 1k$, $V_O = \pm4V$, Measured at $V_O = \pm3V$	●	110	220		V/µs
FPBW	Full Power Bandwidth	$V_{OUT} = 8V_{P-P}$	●		8.5		MHz

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The inputs are protected by back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT1809C/LT1809I and LT1810C/LT1810I are guaranteed functional over the operating temperature range of –40°C and 85°C.

Note 5: The LT1809C/LT1810C are guaranteed to meet specified performance from 0°C to 70°C. The LT1809C/LT1810C are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1809I/LT1810I are guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Minimum supply voltage is guaranteed by power supply rejection ratio test.

Note 7: Output voltage swings are measured between the output and power supply rails.

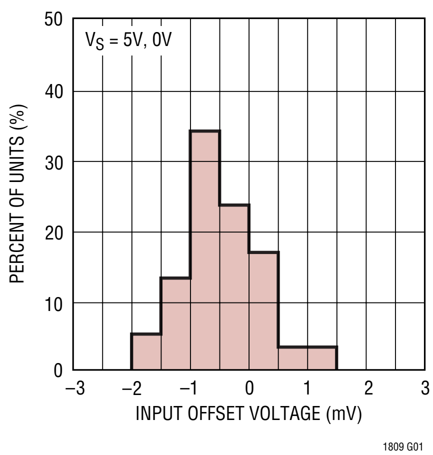
Note 8: This parameter is not 100% tested.

Note 9: Thermal resistance varies depending upon the amount of PC board metal attached to the V^- pin of the device. θ_{JA} is specified for a certain amount of 2oz of copper metal trace connecting to the V^- pin as described in the thermal resistance tables in the Applications Information section.

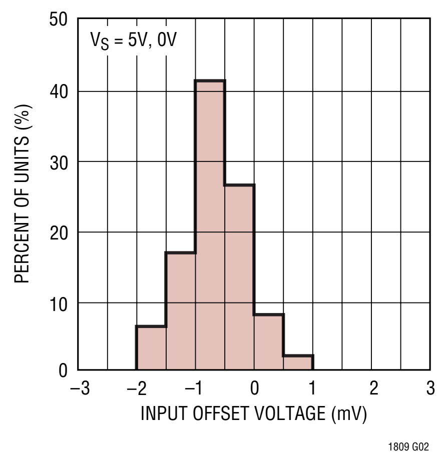
Note 10: Matching parameters are the difference between the two amplifiers of the LT1810.

TYPICAL PERFORMANCE CHARACTERISTICS

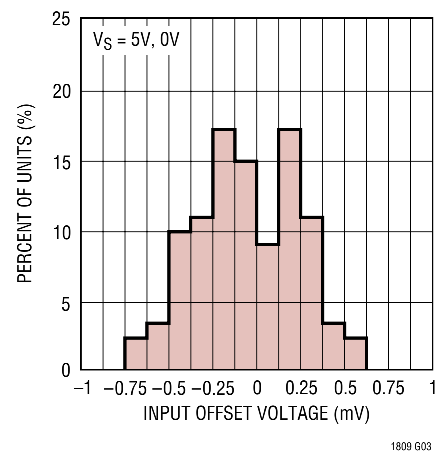
V_{OS} Distribution, V_{CM} = 0V (PNP Stage)



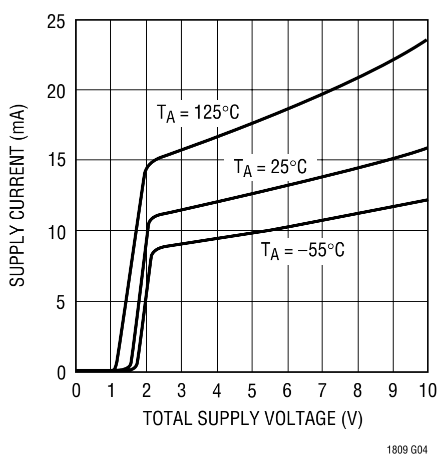
V_{OS} Distribution, V_{CM} = 5V (NPN Stage)



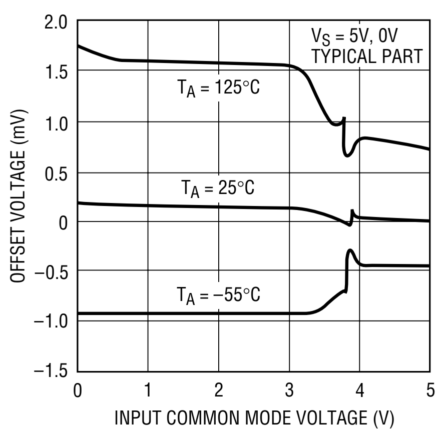
ΔV_{OS} Shift for V_{CM} = 0V to 5V



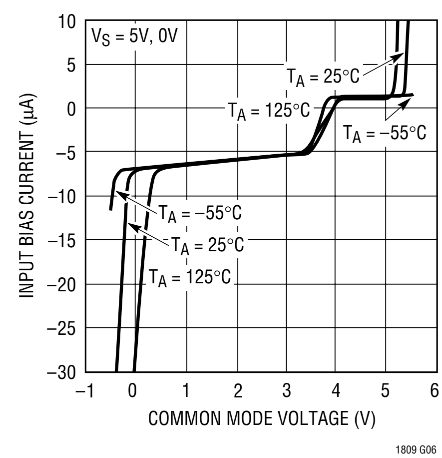
Supply Current vs Supply Voltage



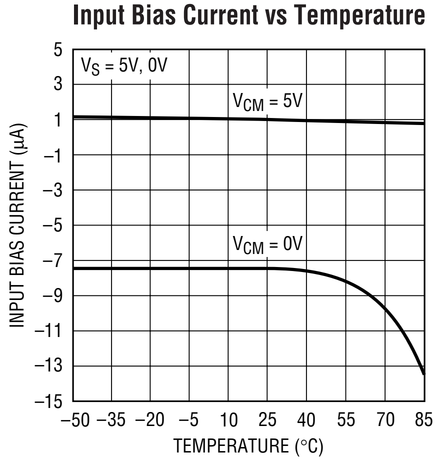
Offset Voltage vs Input Common Mode



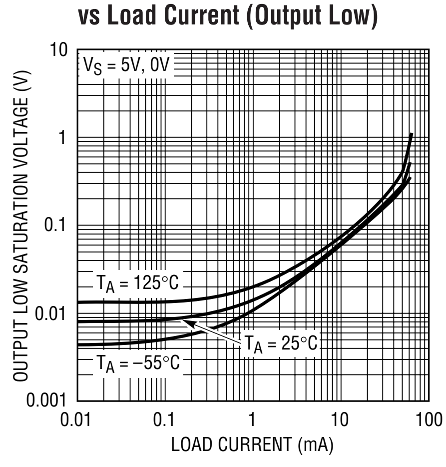
Input Bias Current vs Common Mode Voltage



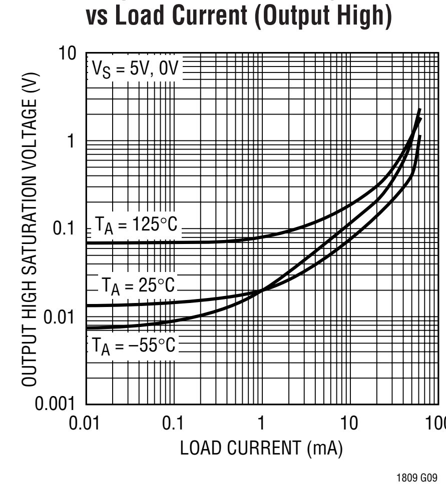
Input Bias Current vs Temperature



Output Saturation Voltage vs Load Current (Output Low)

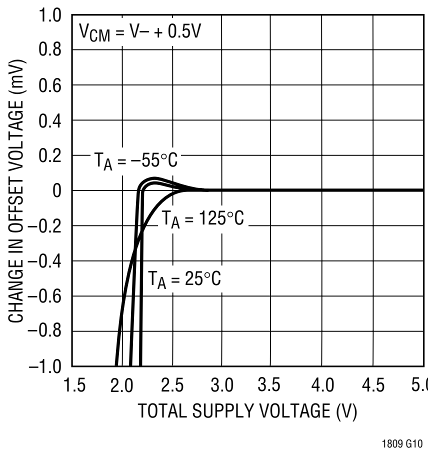


Output Saturation Voltage vs Load Current (Output High)

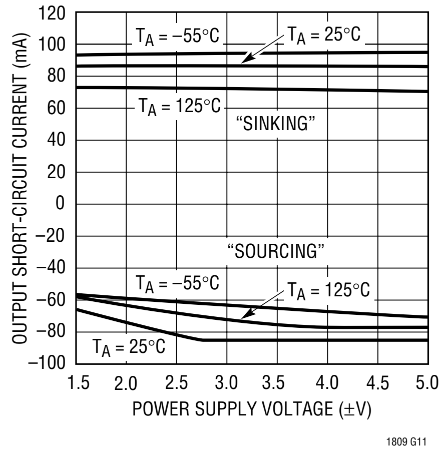


TYPICAL PERFORMANCE CHARACTERISTICS

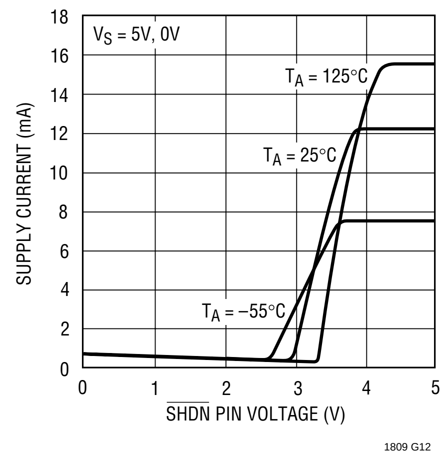
Minimum Supply Voltage



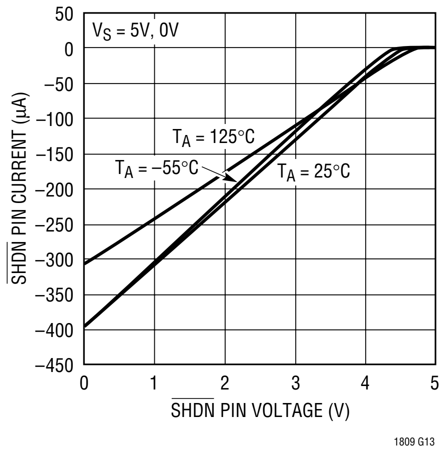
Output Short-Circuit Current vs Power Supply Voltage



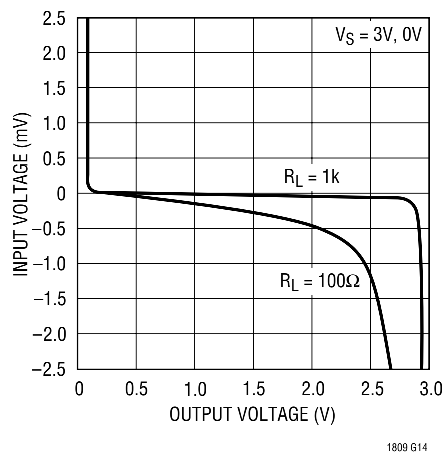
Supply Current vs $\overline{\text{SHDN}}$ Pin Voltage



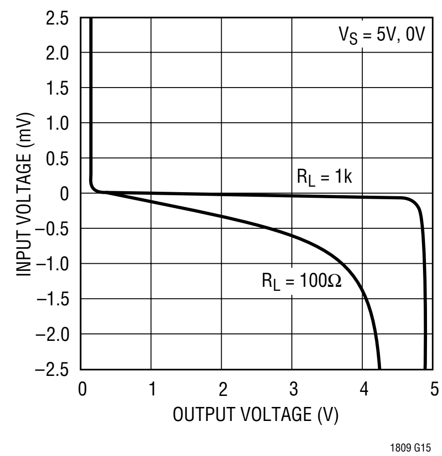
$\overline{\text{SHDN}}$ Pin Current vs $\overline{\text{SHDN}}$ Pin Voltage



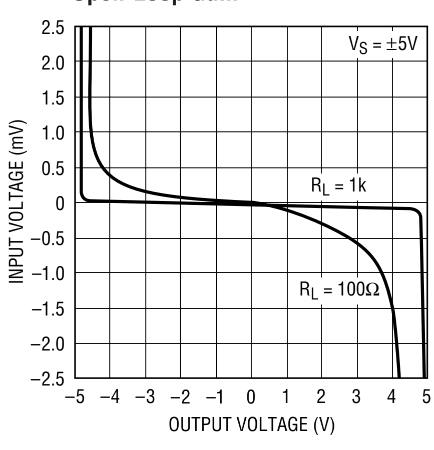
Open-Loop Gain



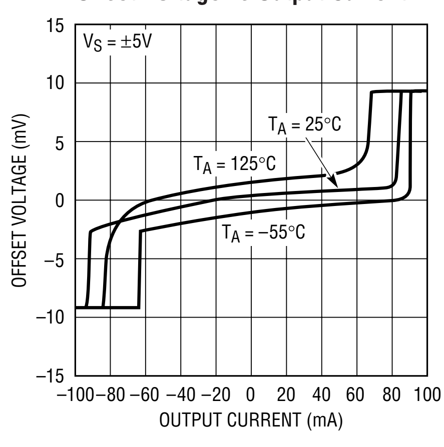
Open-Loop Gain



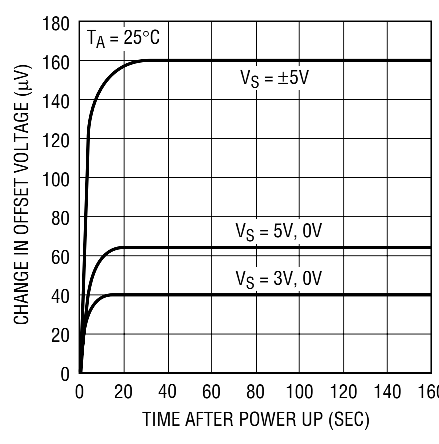
Open-Loop Gain



Offset Voltage vs Output Current

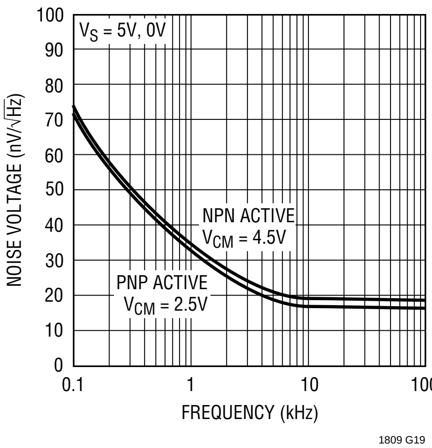


Warm-Up Drift vs Time (LT1809S8)

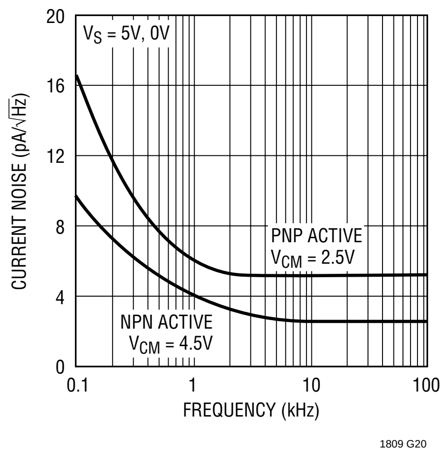


TYPICAL PERFORMANCE CHARACTERISTICS

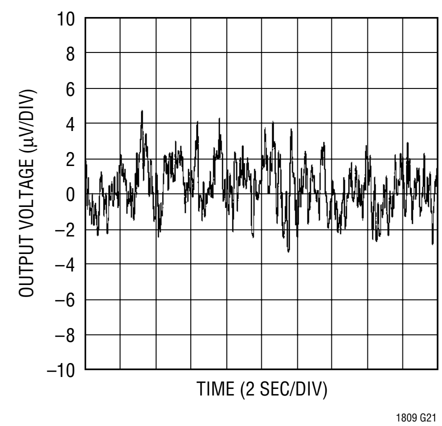
Input Noise Voltage vs Frequency



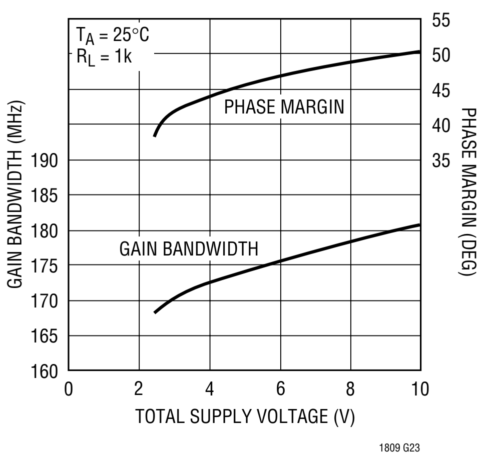
Input Noise Current vs Frequency



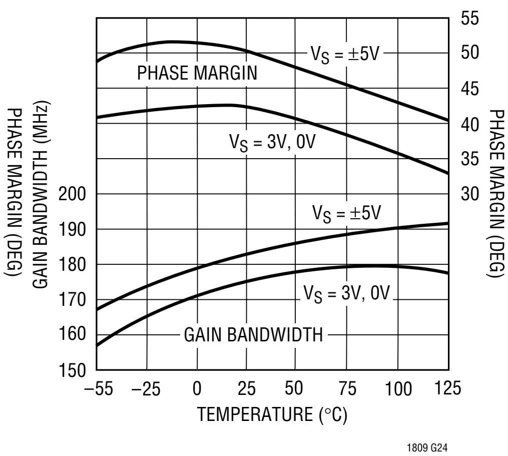
0.1Hz to 10Hz Output Voltage Noise



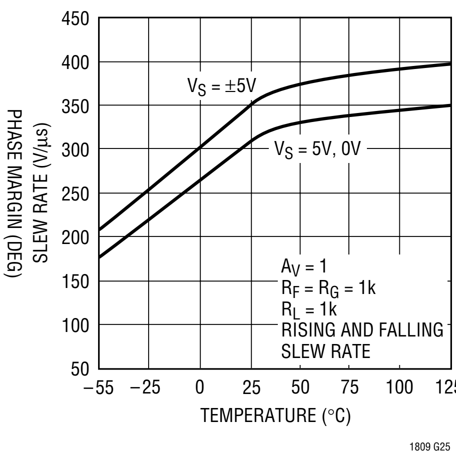
Gain Bandwidth and Phase Margin vs Supply Voltage



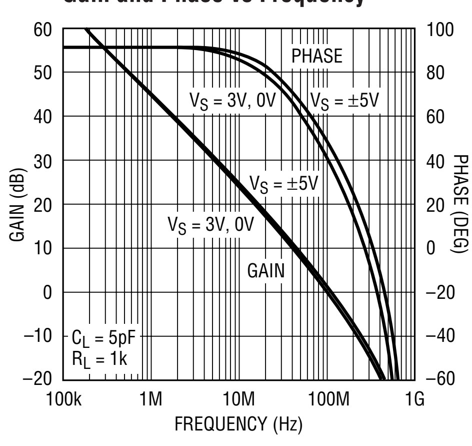
Gain Bandwidth and Phase Margin vs Temperature



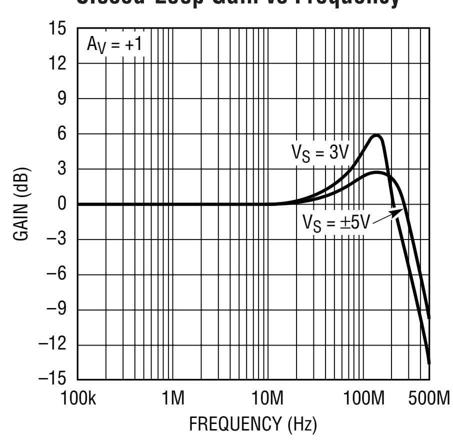
Slew Rate vs Temperature



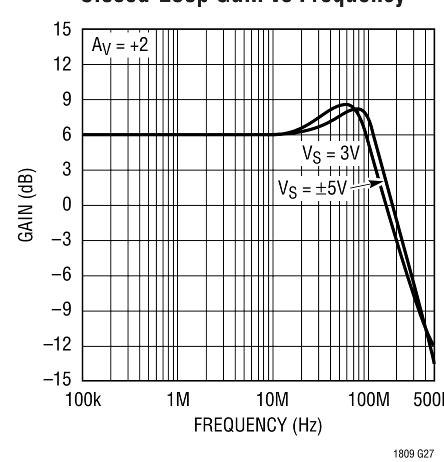
Gain and Phase vs Frequency



Closed-Loop Gain vs Frequency

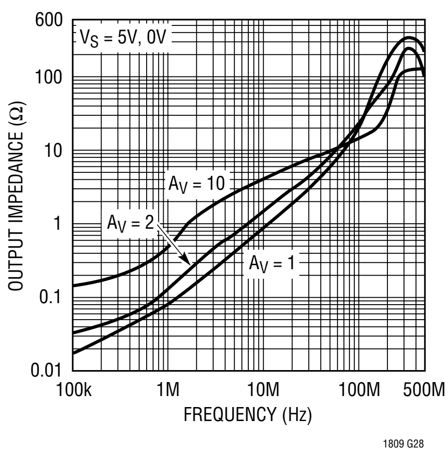


Closed-Loop Gain vs Frequency

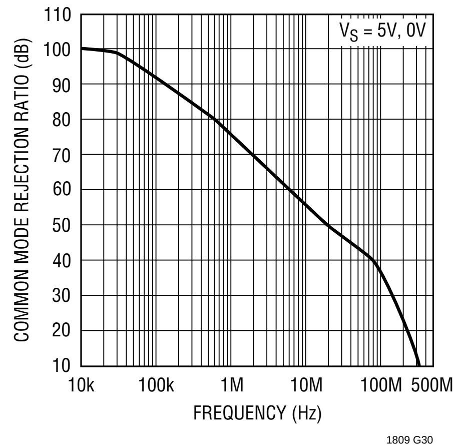


TYPICAL PERFORMANCE CHARACTERISTICS

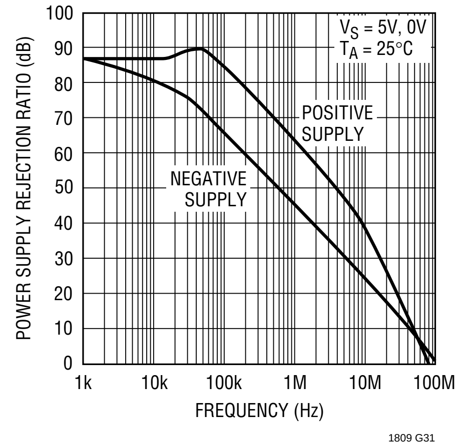
Output Impedance vs Frequency



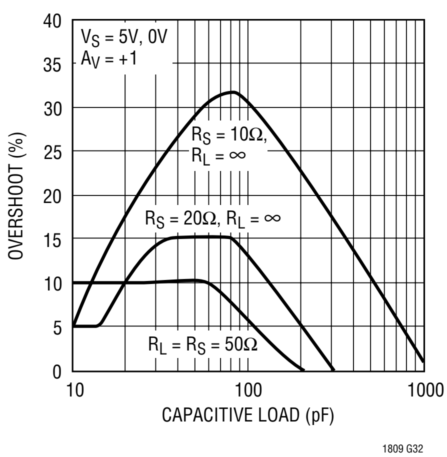
Common Mode Rejection Ratio vs Frequency



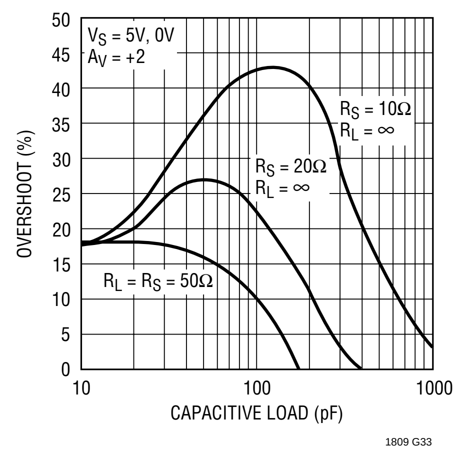
Power Supply Rejection Ratio vs Frequency



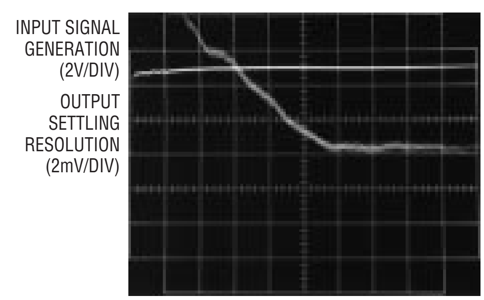
Series Output Resistor vs Capacitive Load



Series Output Resistor vs Capacitive Load

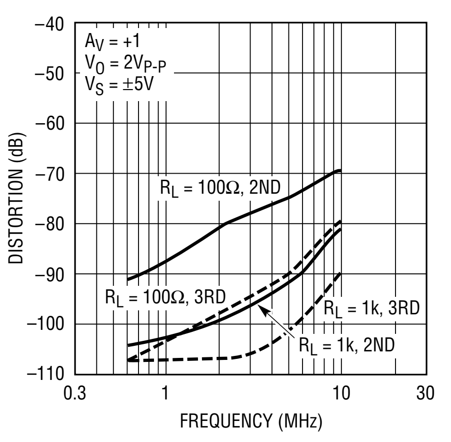


0.01% Settling Time

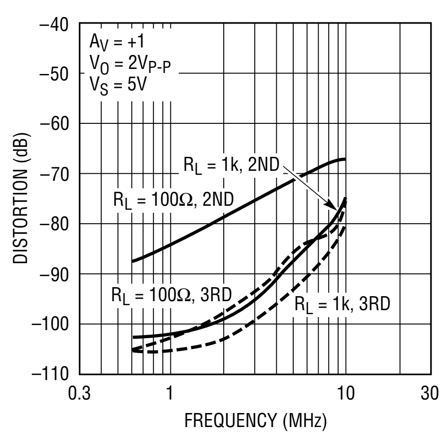


V_S = ±5V 20ns/DIV 1809 G34
V_{OUT} = ±4V
A_V = −1
R_L = 500Ω
t_S = 110ns (SETTLING TIME)

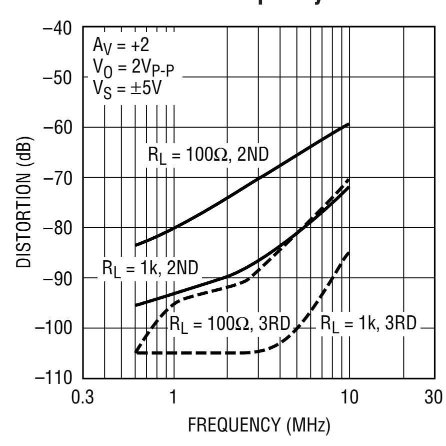
Distortion vs Frequency



Distortion vs Frequency

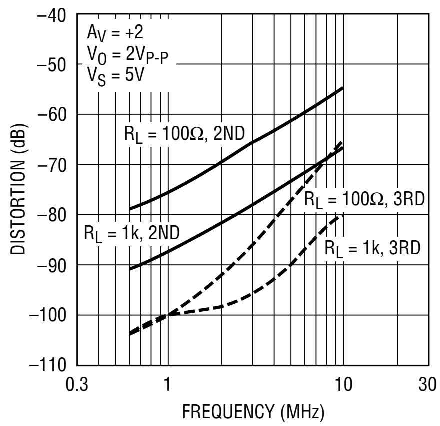


Distortion vs Frequency



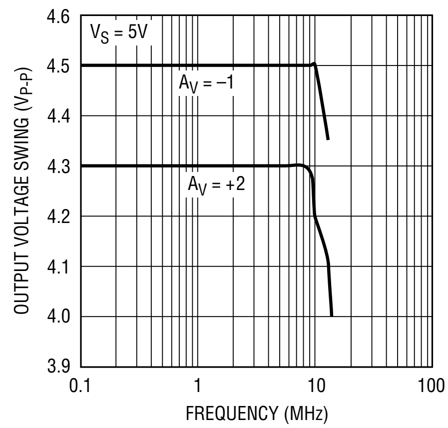
TYPICAL PERFORMANCE CHARACTERISTICS

Distortion vs Frequency



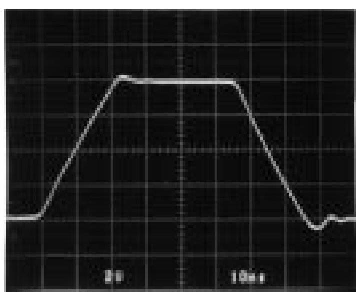
1809 G38

Maximum Undistorted Output Signal vs Frequency



1809 G39

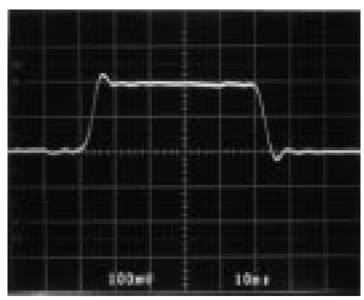
±5V Large-Signal Response



V_S = ±5V 10ns/DIV
A_V = +1
R_L = 1k

1809 G40

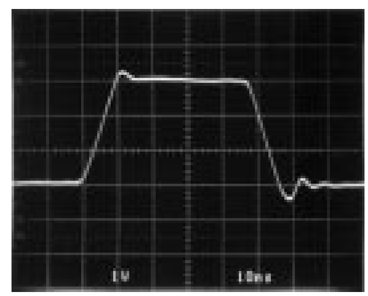
±5V Small-Signal Response



V_S = ±5V 10ns/DIV
A_V = +1
R_L = 1k

1809 G41

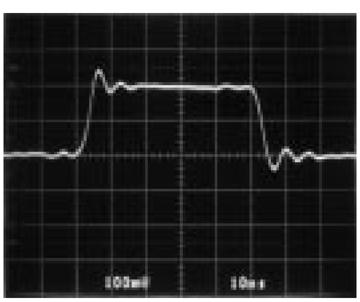
5V Large-Signal Response



V_S = 5V 10ns/DIV
A_V = +1
R_L = 1k

1809 G42

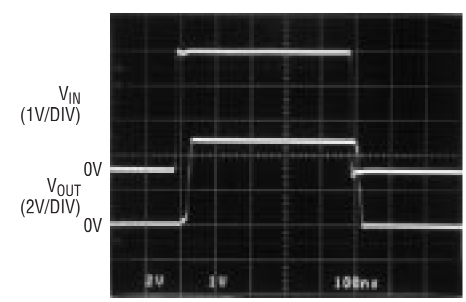
5V Small-Signal Response



V_S = 5V 10ns/DIV
A_V = +1
R_L = 1k

1809 G43

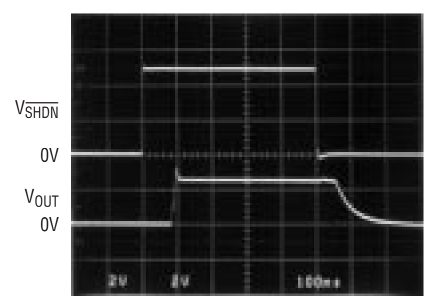
Output Overdriven Recovery



V_S = 5V, 0V 100ns/DIV
A_V = +2

1809 G44

Shutdown Response



V_S = 5V, 0V 100ns/DIV
A_V = +2
R_L = 100Ω

1809 G44

APPLICATIONS INFORMATION

Rail-to-Rail Characteristics

The LT1809/LT1810 have an input and output signal range that includes both negative and positive power supply. Figure 1 depicts a simplified schematic of the amplifier. The input stage is comprised of two differential amplifiers, a PNP stage Q1/Q2 and a NPN stage Q3/Q4 that are active over different ranges of common mode input voltage. The PNP differential pair is active for common mode voltages between the negative supply to approximately 1.5V below the positive supply. As the input voltage moves closer toward the positive supply, the transistor Q5 will steer the tail current I_1 to the current mirror Q6/Q7, activating the NPN differential pair and causing the PNP pair to become inactive for the rest of the input common mode range up to the positive supply.

A pair of complementary common emitter stages Q14/Q15 form the output stage, enabling the output to swing from rail-to-rail. The capacitors C1 and C2 form the local feedback loops that lower the output impedance at high frequency. These devices are fabricated on Linear Technology's proprietary high speed complementary bipolar process.

Power Dissipation

The LT1809/LT1810 amplifiers combine high speed with large output current in a small package, so there is a need to ensure that the die's junction temperature does not exceed 150°C. The LT1809 is housed in an SO-8 package or a 6-lead SOT-23 package and the LT1810 is in an SO-8 or 8-lead MSOP package. All packages have the V^- supply pin fused to the lead frame to enhance the thermal conductance when connecting to a ground plane or a large metal trace. Metal trace and plated through-holes can be used to spread the heat generated by the device to the backside of the PC board. For example, on a 3/32" FR-4 board with 2oz copper, a total of 660 square millimeters connected to Pin 4 of LT1810 in an SO-8 package (330 square millimeters on each side of the PC board) will bring the thermal resistance, θ_{JA}, to about 85°C/W. Without extra metal trace connected to the V^- pin to provide a heat sink, the thermal resistance will be around 105°C/W. More information on thermal resistance for all packages with various metal areas connecting to the V^- pin is provided in Tables 1, 2 and 3 for thermal consideration.

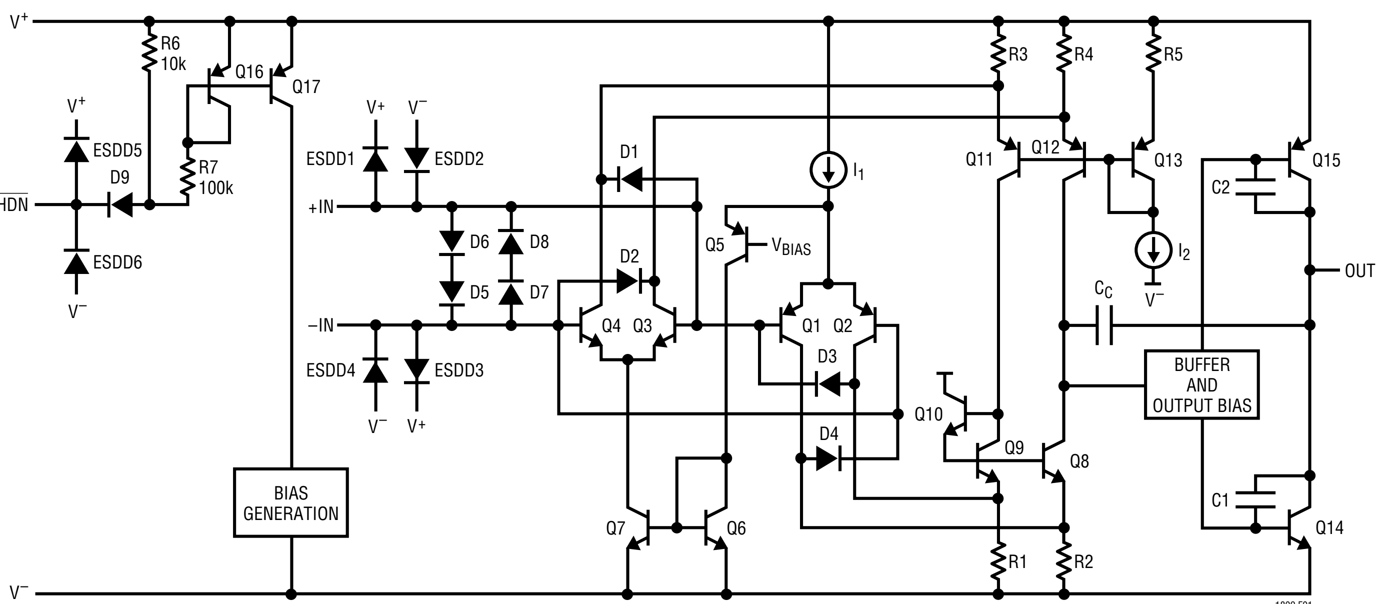


Figure 1. LT1809 Simplified Schematic Diagram

APPLICATIONS INFORMATION

Table 1. LT1809 6-Lead SOT-23 Package

COPPER AREA TOPSIDE (mm^2)	BOARD AREA (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
270	2500	135°C/W
100	2500	145°C/W
20	2500	160°C/W
0	2500	200°C/W

Device is mounted on topside.

Table 2. LT1809/LT1810 SO-8 Package

COPPER AREA		BOARD AREA (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE (mm^2)	BACKSIDE (mm^2)		
1100	1100	2500	65°C/W
330	330	2500	85°C/W
35	35	2500	95°C/W
35	0	2500	100°C/W
0	0	2500	105°C/W

Device is mounted on topside.

Table 3. LT1810 8-Lead MSOP Package

COPPER AREA		BOARD AREA (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE (mm^2)	BACKSIDE (mm^2)		
540	540	2500	110°C/W
100	100	2500	120°C/W
100	0	2500	130°C/W
30	0	2500	135°C/W
0	0	2500	140°C/W

Device is mounted on topside.

Junction temperature T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The power dissipation in the IC is the function of the supply voltage, output voltage and the load resistance. For a given supply voltage, the worst-case power dissipation $P_{D(MAX)}$ occurs at the maximum supply current with the output voltage at half of either supply voltage (or the maximum swing is less than 1/2 the supply voltage). $P_{D(MAX)}$ is given by:

$$P_{D(MAX)} = (V_S \bullet I_{S(MAX)}) + (V_S/2)^2/R_L$$

Example: An LT1810 in SO-8 mounted on a 2500mm² area of PC board without any extra heat spreading plane connected to its V⁻ pin has a thermal resistance of 105°C/W, θ_{JA}. Operating on ±5V supplies with both amplifiers simultaneously driving 50Ω loads, the worst-case power dissipation is given by:

$$P_{D(MAX)} = 2 \bullet (10 \bullet 25mA) + 2 \bullet (2.5)^2/50$$
$$= 0.5 + 0.250 = 0.750W$$

The maximum ambient temperature that the part is allowed to operate is:

$$T_A = T_J - (P_{D(MAX)} \bullet 105°C/W)$$
$$= 150°C - (0.750W \bullet 105°C/W) = 71°C$$

To operate the device at higher ambient temperature, connect more metal area to the V⁻ pin to reduce the thermal resistance of the package as indicated in Table 2.

Input Offset Voltage

The offset voltage will change depending upon which input stage is active and the maximum offset voltage is guaranteed to be less than 3mV. The change of V_{OS} over the entire input common mode range (CMRR) is less than 2.5mV on a single 5V and 3V supply.

Input Bias Current

The input bias current polarity depends upon a given input common voltage at whichever input stage is operating. When the PNP input stage is active, the input bias currents flow out of the input pins and flow into the input pins when the NPN input stage is activated. Because the input offset current is less than the input bias current, matching the source resistances at the input pin will reduce total offset error.

Output

The LT1809/LT1810 can deliver a large output current, so the short-circuit current limit is set around 90mA to prevent damage to the device. Attention must be paid to keep the junction temperature of the IC below the absolute maximum rating of 150°C (refer to the Power Dissipation section) when the output is continuously short circuited. The output of the amplifier has reverse-biased diodes connected to each supply. If the output is forced

APPLICATIONS INFORMATION

beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to several hundred milliamps, no damage to the device will occur.

Overdrive Protection

When the input voltage exceeds the power supplies, two pairs of crossing diodes, D1 to D4, will prevent the output from reversing polarity. If the input voltage exceeds either power supply by 700mV, diodes D1/D2 or D3/D4 will turn on, keeping the output at the proper polarity. For the phase reversal protection to perform properly, the input current must be limited to less than 5mA. If the amplifier is severely overdriven, an external resistor should be used to limit the overdrive current.

The LT1809/LT1810's input stages are also protected against differential input voltages of 1.4V or higher by back-to-back diodes, D5/D8, that prevent the emitter-base breakdown of the input transistors. The current in these diodes should be limited to less than 10mA when they are active. The worst-case differential input voltage usually occurs when the input is driven while the output is shorted to ground in a unity-gain configuration. In addition, the amplifier is protected against ESD strikes up to 3kV on all pins by a pair of protection diodes on each pin that are connected to the power supplies as shown in Figure 1.

Capacitive Load

The LT1809/LT1810 is optimized for high bandwidth and low distortion applications. It can drive a capacitive load about 20pF in a unity-gain configuration and more with higher gain. When driving a larger capacitive load, a resistor of 10Ω to 50Ω should be connected between the output and the capacitive load to avoid ringing or oscillation. The feedback should still be taken from the output so that the resistor will isolate the capacitive load to ensure stability. Graphs on capacitive loads indicate the transient response of the amplifier when driving capacitive load with a specified series resistor.

Feedback Components

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the feedback resistors and the total capacitance at the inverting input does not degrade stability. For instance, the LT1809 in a noninverting gain of 2, set up with two 1K resistors and a capacitance of 3pF (device plus PC board), will probably ring in transient response. The pole that is formed at 106MHz will reduce phase margin by 34 degrees when the crossover frequency of the amplifier is around 70MHz. A capacitor of 3pF or higher connected across the feedback resistor will eliminate any ringing or oscillation.

$\overline{\text{SHDN}}$ Pin

The LT1809 has a $\overline{\text{SHDN}}$ pin to reduce the supply current to less than 1.25mA. When the $\overline{\text{SHDN}}$ pin is pulled low, it will generate a signal to power down the device. If the pin is left unconnected, an internal pull-up resistor of 10k will keep the part fully operating as shown in Figure 1. The output will be high impedance during shutdown, and the turn-on and turn-off time is less than 100ns. Because the inputs are protected by a pair of back-to-back diodes, the input signal will feed through to the output during shutdown mode if the amplitude of signal between the inputs is larger than 1.4V.

TYPICAL APPLICATIONS

Driving A/D Converters

The LT1809/LT1810 have a 27ns settling time to 0.1% of a 2V step signal and 20Ω output impedance at 100MHz making it ideal for driving high speed A/D converters. With the rail-to-rail input and output and low supply voltage operation, the LT1809 is also desirable for single supply applications. As shown in Figure 2, the LT1809 drives a 10Msps, 12-bit ADC, the LTC1420. The lowpass filter, R3 and C1, reduces the noise and distortion products that might come from the input signal. High quality capacitors and resistors, an NPO chip capacitor and metal-film surface mount resistors, should be used since these components can add to distortion. The voltage glitch of the converter, due to its sampling nature, is buffered by the LT1809 and the ability of the amplifier to settle it quickly will affect the spurious-free dynamic range of the system. Figure 2 to Figure 7 depict the LT1809 driving the LTC1420 at different configurations and voltage supplies. The FFT responses show better than 90dB of SFDR for a ±5V supply, and 80dB on a 5V single supply for the 1.394MHz signal.

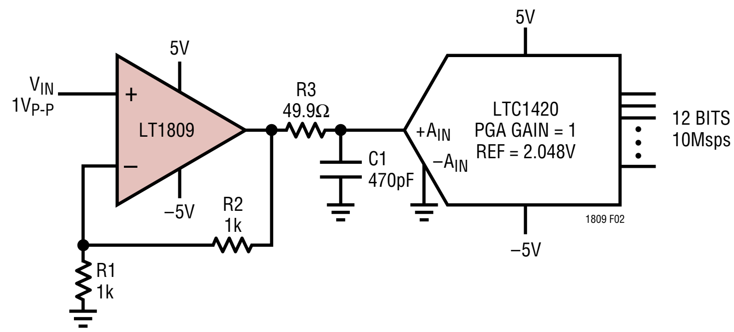


Figure 2. Noninverting A/D Driver

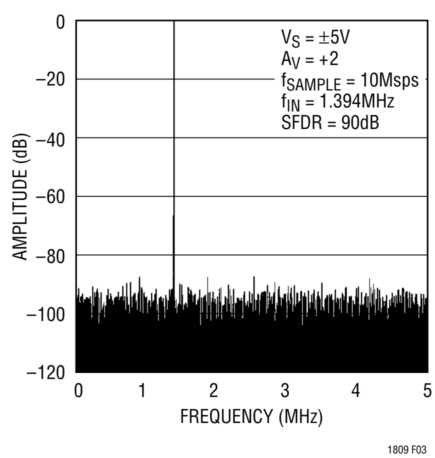


Figure 3. 4096 Point FFT Response

TYPICAL APPLICATIONS

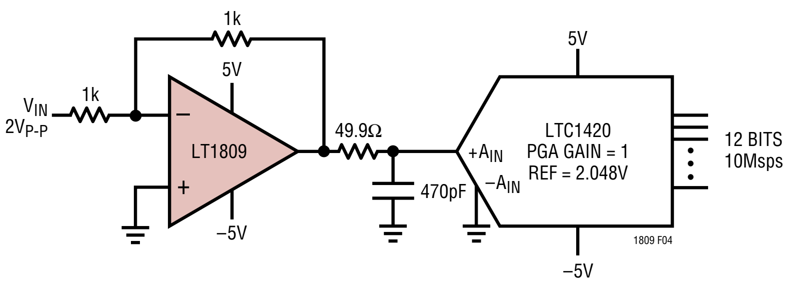


Figure 4. Inverting A/D Driver

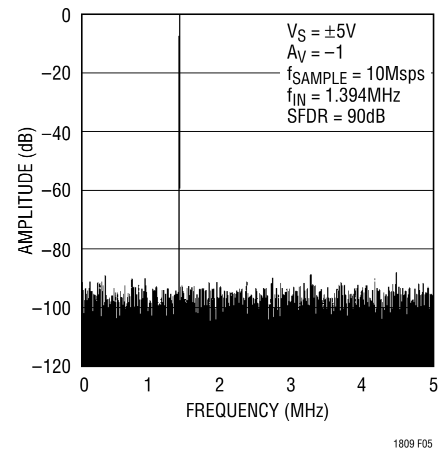


Figure 5. 4096 Point FFT Response

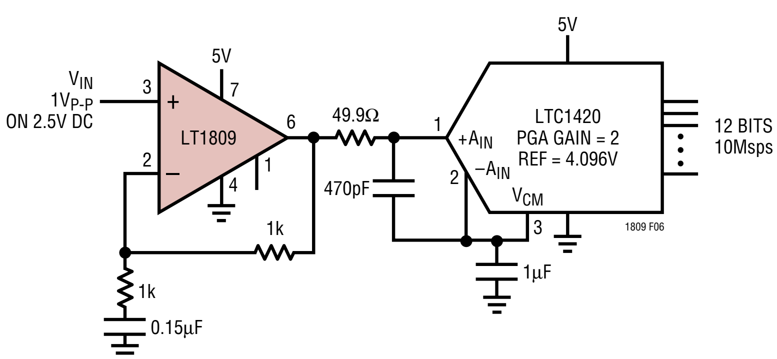


Figure 6. Single Supply A/D Driver

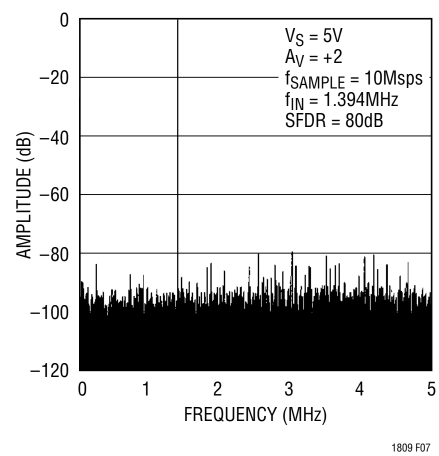


Figure 7. 4096 Point FFT Response

TYPICAL APPLICATIONS

Single Supply Video Line Driver

The LT1809 is a wideband rail-to-rail op amp with a large output current that allows it to drive video signals in low supply applications. Figure 8 depicts a single supply video line driver with AC coupling to minimize the quiescent power dissipation. Resistors R1 and R2 are used to level-shift the input and output to provide the largest signal swing. A gain of 2 is set up with R3 and R4 to restore the signal at V_{OUT}, which is attenuated by 6dB due to the matching of the 75Ω line with the back-terminated resistor, R5. The back termination will eliminate any reflection of the signal that comes from the load. The input termination resistor, R_T, is optional—it is used only if matching of the incoming line is necessary. The values of C1, C2 and C3 are selected to minimize the droop of the luminance signal. In some less stringent requirements, the value of capacitors could be reduced. The –3dB bandwidth of the driver is about 95MHz on 5V supply and the amount of peaking will vary upon the value of capacitor C4.

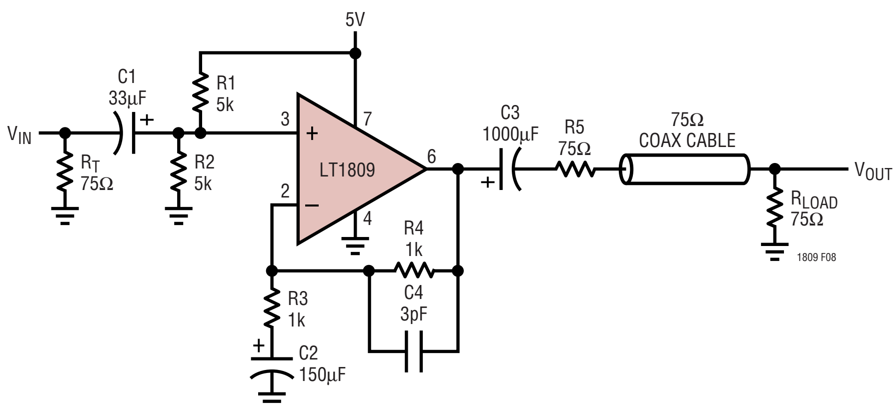


Figure 8. 5V Single Supply Video Line Driver

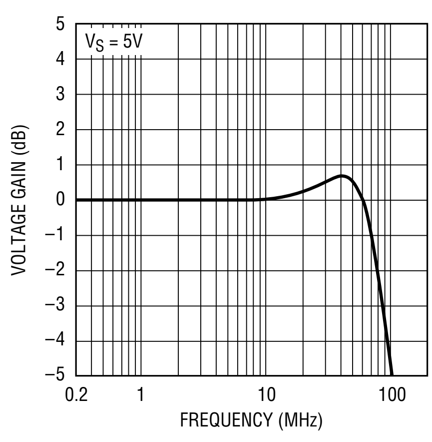
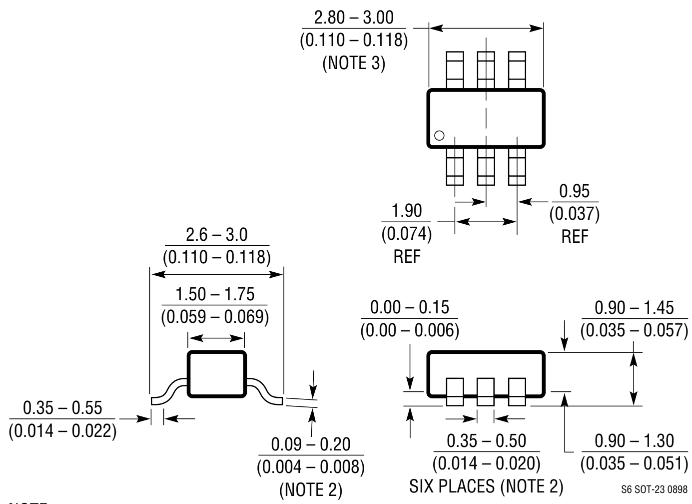


Figure 9. Video Line Driver Frequency Response

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S6 Package
6-Lead Plastic SOT-23
(LTC DWG # 05-08-1634)

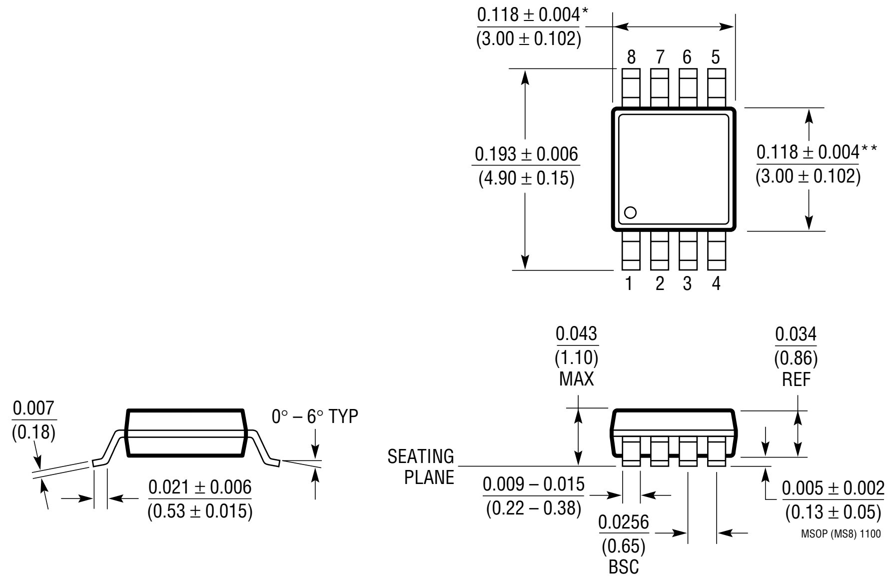


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
4. MOLD FLASH SHALL NOT EXCEED 0.254mm
5. PACKAGE EIAJ REFERENCE IS SC-74A (EIAJ)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



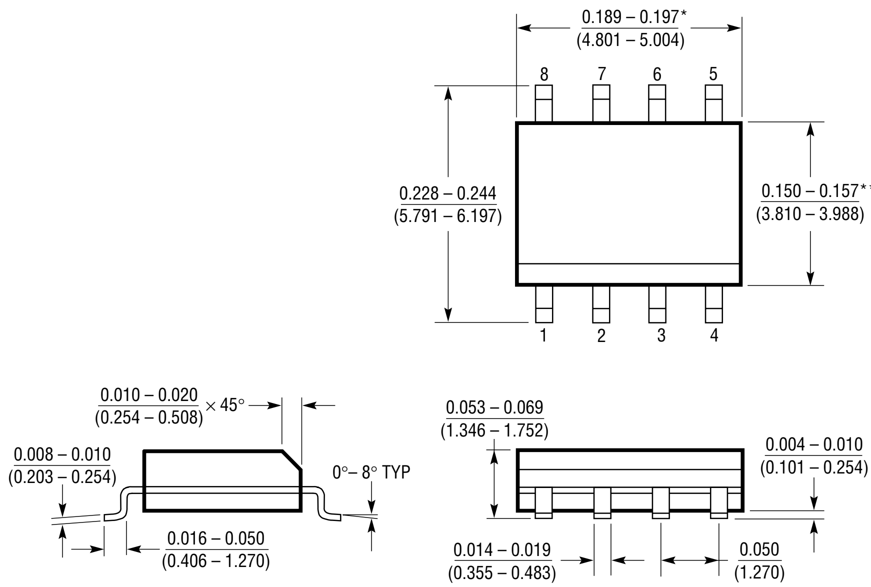
* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 1298

TYPICAL APPLICATION

Single 3V Supply, 4MHz, 4th Order Butterworth Filter

Benefiting from a low voltage supply operation, low distortion and rail-to-rail output of LT1809, a low distortion filter that is suitable for antialiasing can be built as shown Figure 10. On a 3V supply, the filter has a passband of 4MHz with $2.5V_{P-P}$ signal and a stopband that is greater than 70dB to frequency of 100MHz.

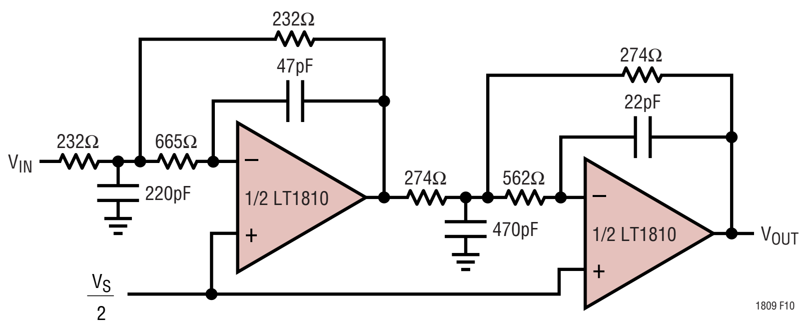


Figure 10. Single 3V Supply, 4MHz, 4th Order Butterworth Filter

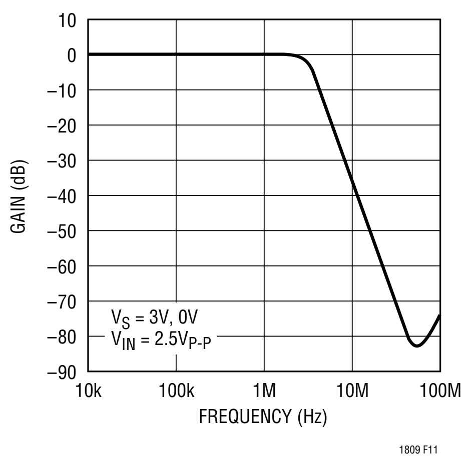


Figure 11. Filter Frequency Response

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1395	400MHz Current Feedback Amplifier	800V/µs Slew Rate, Shutdown
LT1632/LT1633	Dual/Quad 45MHz, 45V/µs Rail-to-Rail Input and Output Op Amps	High DC Accuracy, 1.35mV $V_{OS(MAX)}$, 70mA Output Current, Max Supply Current 5.2mA per Amplifier
LT1630/LT1631	Dual/Quad 30MHz, 10V/µs Rail-to-Rail Input and Output Op Amps	High DC Accuracy, 525µV $V_{OS(MAX)}$, 70mA Output Current, Max Supply Current 4.4mA per Amplifier
LT1806/LT1807	Single/Dual 325MHz, 140V/µs Rail-to-Rail Input and Output Op Amps	High DC Accuracy, 550µV $V_{OS(MAX)}$, Low Noise $3.5nV/\sqrt{Hz}$, Low Distortion –80dBc at 5MHz

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com

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