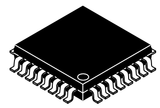


SLOS389 – NOVEMBER 2001

±3-A HIGH-EFFICIENCY PWM POWER DRIVER

FEATURES

- **±3-A Maximum Output Current**
- **Low Supply Voltage Operation: 2.8 V to 5.5 V**
- **High Efficiency Generates Less Heat**
- **Over-Current and Thermal Protection**
- **Fault Indicators for Over-Current, Thermal and Under-Voltage Conditions**
- **Two Selectable Switching Frequencies**
- **Internal or External Clock Sync**
- **PWM Scheme Optimized for EMI**
- **9×9 mm PowerPAD™ Quad Flatpack or 5×5 mm MicroStar Junior™ Packages**

APPLICATIONS

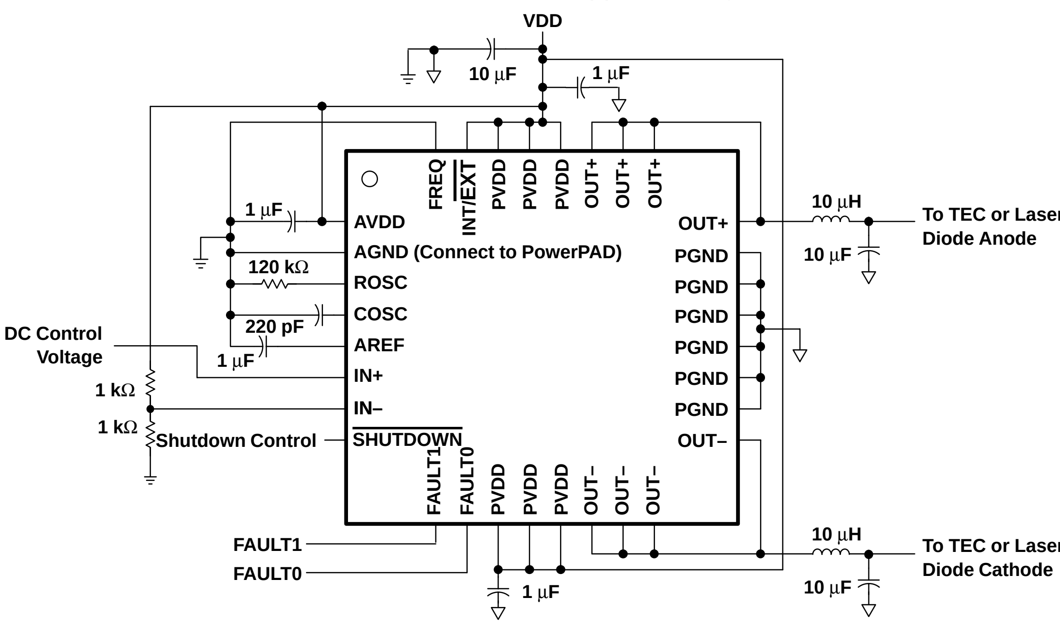
- **Thermoelectric Cooler (TEC) Driver**
- **Laser Diode Biasing**

DESCRIPTION

The DRV591 is a high-efficiency, high-current power amplifier ideal for driving a wide variety of thermo-electric cooler elements in systems powered from 2.8 V to 5.5 V. PWM operation and low output stage on-resistance significantly decrease power dissipation in the amplifier.

The DRV591 is internally protected against thermal and current overloads. Logic-level fault indicators signal when the junction temperature has reached approximately 130°C to allow for system-level shutdown before the amplifier's internal thermal shutdown circuitry activates. The fault indicators also signal when an over-current event has occurred. If the over-current circuitry is tripped, the DRV591 automatically resets (see application information section for more details).

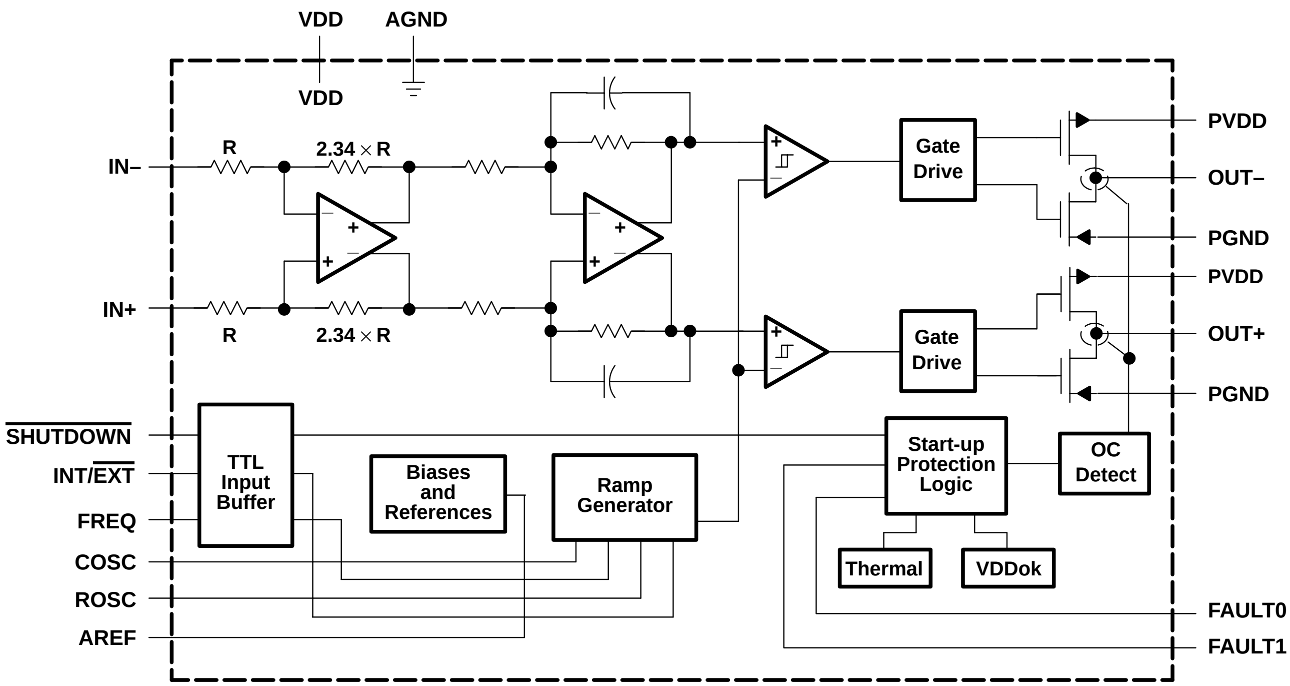
The PWM switching frequency may be set to 500 kHz or 100 kHz depending on system requirements. To eliminate external components, the gain is fixed at approximately 2.34 V/V.



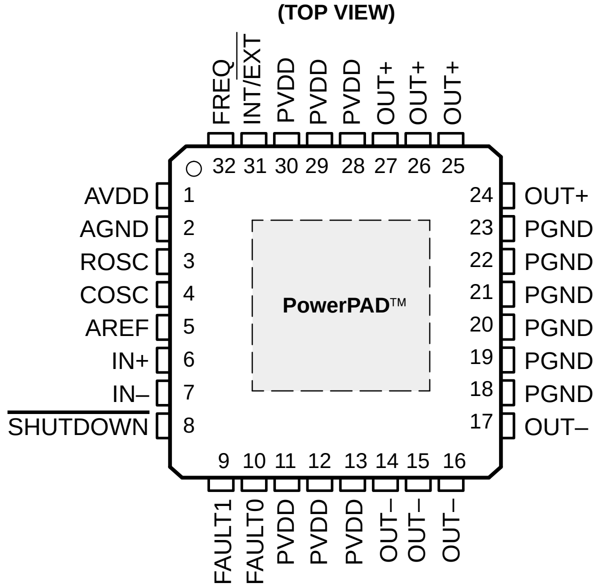
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD and MicroStar Junior are trademarks of Texas Instruments.

block diagram



VFP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	2		Analog ground
AREF	5	O	Connect 1 µF capacitor to ground for AREF voltage filtering
AVDD	1	I	Analog power supply
COSC	4	I	Connect capacitor to ground to set oscillation frequency (220 pF for 500 kHz, 1 nF for 100 kHz) when the internal oscillator is selected; connect clock signal when an external oscillator is used
FAULT0	10	O	Fault flag 0, low when active open drain output (see application information)
FAULT1	9	O	Fault flag 1, high when active open drain output (see application information)
FREQ	32	I	Selects 500 kHz switching frequency when a TTL logic low is applied to this terminal; selects 100kHz switching frequency when a TTL logic high is applied
IN–	7	I	Negative differential input
IN+	6	I	Positive differential input
INT/$\overline{\text{EXT}}$	31	I	Selects the internal oscillator when a TTL logic high is applied to this terminal; selects the use of an external oscillator when a TTL logic low is applied to this terminal
OUT–	14, 15, 16, 17	O	Negative bridge-tied load (BTL) output (4 pins)
OUT+	24, 25, 26, 27	O	Positive bridge-tied load (BTL) output (4 pins)
PGND	18, 19, 20, 21, 22, 23		High-current ground (6 pins)
PVDD	11, 12, 13, 28, 29, 30	I	High-current power supply (6 pins)
ROSC	3	I	Connect 120 kΩ resistor to AGND to set oscillation frequency (either 500 kHz or 100 kHz). Not needed if an external clock is used.
$\overline{\text{SHUTDOWN}}$	8	I	Places the amplifier in shutdown mode when a TTL logic low is applied to this terminal; places the amplifier in normal operation when a TTL logic high is applied

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, AVDD, PVDD . . . . –0.3 V to 5.5 V
Input voltage, V_I . . . . –0.3 V to V_{DD} + 0.3 V
Output current, I_O (FAULT0, FAULT1) . . . . 1 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . –65°C to 165°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA}† (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
VFP	29.4	1.2	4.1 W
GQE‡	37.8	4.56	3.3 W

† This data was taken using 2 oz trace and copper pad that is soldred directly to a JEDEC standard 4-layer 3 in × 3 in PCB.
‡ This package is in the Product Preview stage of development.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PowerPAD QUAD FLATPACK (VFP)	PLASTIC BALL GRID ARRAY MicroStar Junior (GQE) [PRODUCT PREVIEW]
–40°C to 85°C	DRV591VFP§	DRV591GQE

§ Tape and reel transport media is in the Product Preview stage of development

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, AVDD, PVDD		2.8	5.5	V
High-level input voltage, V_{IH}	FREQ, INT/$\overline{EXT}$, $\overline{SHUTDOWN}$, COSC	2		V
Low-level input voltage, V_{IL}	FREQ, INT/$\overline{EXT}$, $\overline{SHUTDOWN}$, COSC		0.8	V
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	$V_I = V_{DD}/2$, $I_O = 0$ A			14	100	mV
$\|I_{IH}\|$	High-level input current	$V_{DD} = 5.5V$, $V_I = V_{DD}$				1	µA
$\|I_{IL}\|$	Low-level input current	$V_{DD} = 5.5V$, $V_I = 0$ V				1	µA
V_n	Integrated output noise voltage	f = <1 Hz to 10 kHz			40		µV
V_{ICM}	Common-mode voltage range	$V_{DD} = 5$ V		1.2		3.8	V
V_{ICM}	Common-mode voltage range	$V_{DD} = 3.3$ V		1.2		2.1	V
A_V	Closed-loop voltage gain			2.1	2.34	2.6	V/V
	Full power bandwidth				60		kHz
V_O	Voltage output (measured differentially)	$I_O = \pm1$ A, $r_{ds(on)} = 65$ mΩ, $V_{DD} = 5$ V			4.87		V
V_O	Voltage output (measured differentially)	$I_O = \pm3$ A, $r_{ds(on)} = 65$ mΩ, $V_{DD} = 5$ V			4.61		V
$r_{DS(on)}$	Drain-source on-state resistance	$V_{DD} = 5$ V, $I_O = 4$ A, $T_A = 25°C$	High side	25	60	95	mΩ
$r_{DS(on)}$	Drain-source on-state resistance	$V_{DD} = 5$ V, $I_O = 4$ A, $T_A = 25°C$	Low side	25	65	95	mΩ
$r_{DS(on)}$	Drain-source on-state resistance	$V_{DD} = 3.3$ V, $I_O = 4$ A, $T_A = 25°C$	High side	25	80	140	mΩ
$r_{DS(on)}$	Drain-source on-state resistance	$V_{DD} = 3.3$ V, $I_O = 4$ A, $T_A = 25°C$	Low side	25	90	140	mΩ
	Maximum continuous current output				3		A
	Status flag output pins (FAULT0, FAULT1) Fault active (open drain output)	Sinking 200 µA				0.1	V
	External clock frequency range	For 500 kHz operation		225	250	275	kHz
	External clock frequency range	For 100 kHz operation		45	50	55	kHz
I_q	Quiescent current	$V_{DD} = 5$ V, No load or filter		2	6.2	12	mA
I_q	Quiescent current	$V_{DD} = 3.3$ V, No load or filter		2	4.6	8	mA
$I_{q(SD)}$	Quiescent current in shutdown mode	$V_{DD} = 5$ V, $\overline{SHUTDOWN} = 0.8$ V		0	0.1	50	µA
	Output resistance in shutdown	$\overline{SHUTDOWN} = 0.8$ V		2			kΩ
	Power-on threshold			1.7		2.8	V
	Power-off threshold			1.6		2.6	V
	Thermal trip point	FAULT0 active			130		°C
Z_I	Input impedance (IN+, IN–)				100		kΩ

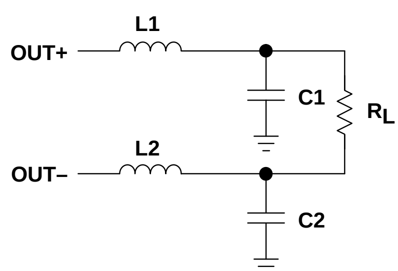
TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Efficiency	vs Load resistance	2, 3
$r_{DS(on)}$	Drain-source on-state resistance	vs Supply voltage	4
		vs Free-air temperature	5
		vs Free-air temperature	6
I_q	Supply current	vs Supply voltage	7
PSRR	Power supply rejection ratio	vs Frequency	8, 9
	Closed loop response		10, 11
I_O	Maximum output current	vs Output voltage	12
		vs Ambient temperature	13
V_{IO}	Input offset voltage	Common-mode input voltage	14, 15

test set-up for graphs

The LC output filter used in Figures 2, 3, 8, and 9 is shown below.



L1, L2 = 10 μH (part number: CDRH104R, manufacturer: Sumida)
C1, C2 = 10 μF (part number: ECJ-4YB1C106K, manufacturer: Panasonic)

Figure 1. LC Output Filter

TYPICAL CHARACTERISTICS

EFFICIENCY
vs
LOAD RESISTANCE

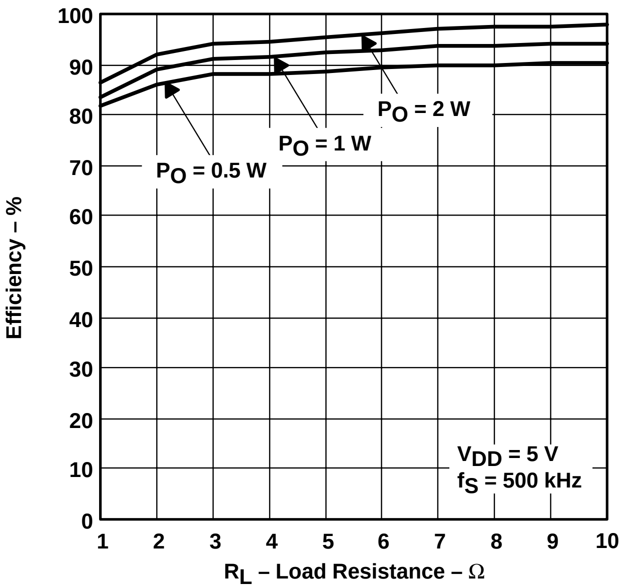


Figure 2

EFFICIENCY
vs
LOAD RESISTANCE

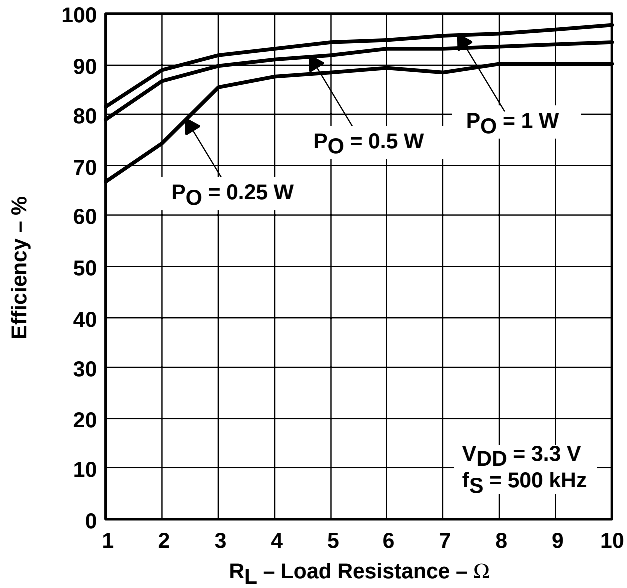


Figure 3

DRAIN-SOURCE ON-STATE RESISTANCE
vs
SUPPLY VOLTAGE

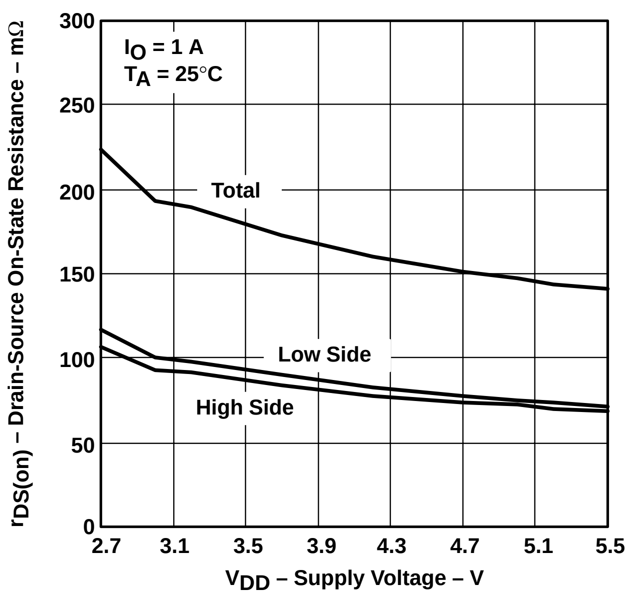


Figure 4

DRAIN-SOURCE ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

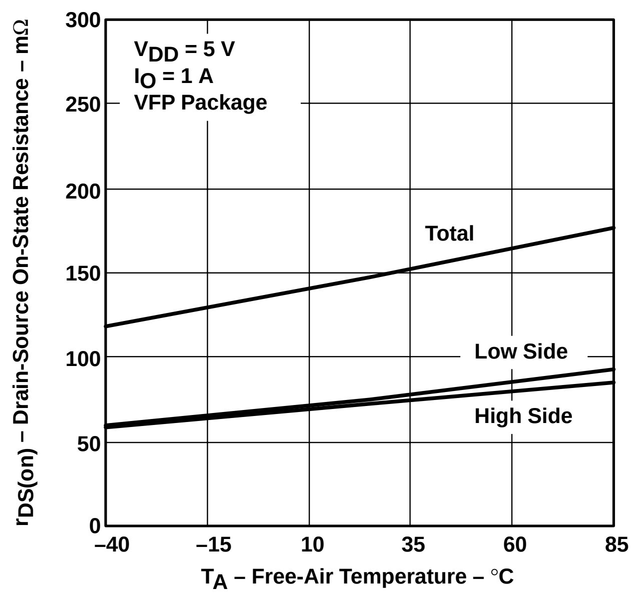


Figure 5

TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs FREE-AIR TEMPERATURE

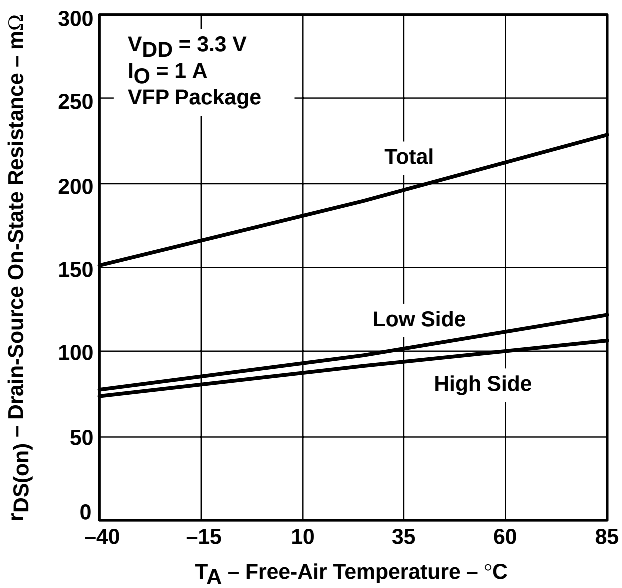


Figure 6

SUPPLY CURRENT vs SUPPLY VOLTAGE

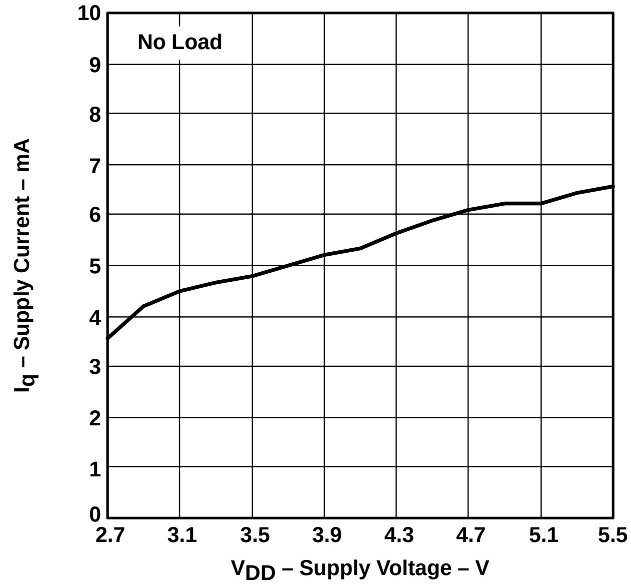


Figure 7

POWER SUPPLY REJECTION RATIO vs FREQUENCY

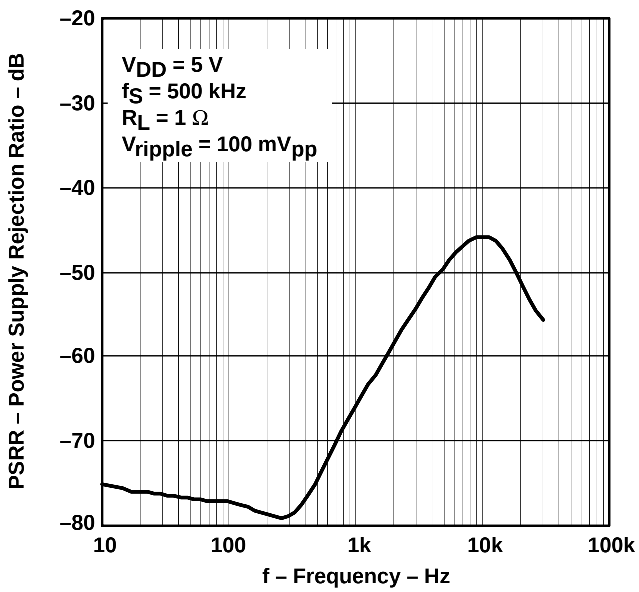


Figure 8

POWER SUPPLY REJECTION RATIO vs FREQUENCY

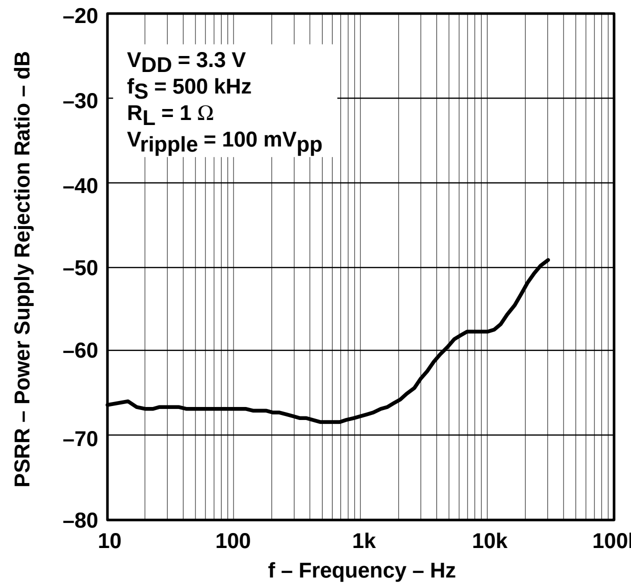


Figure 9

TYPICAL CHARACTERISTICS

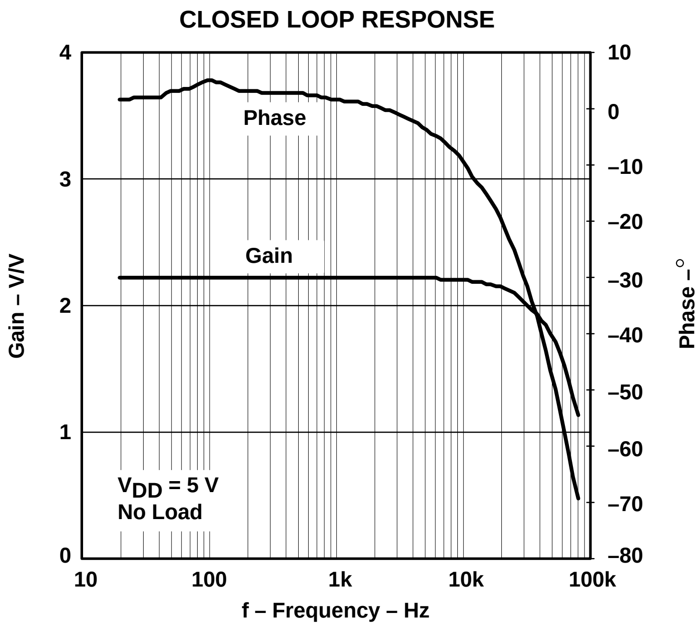


Figure 10

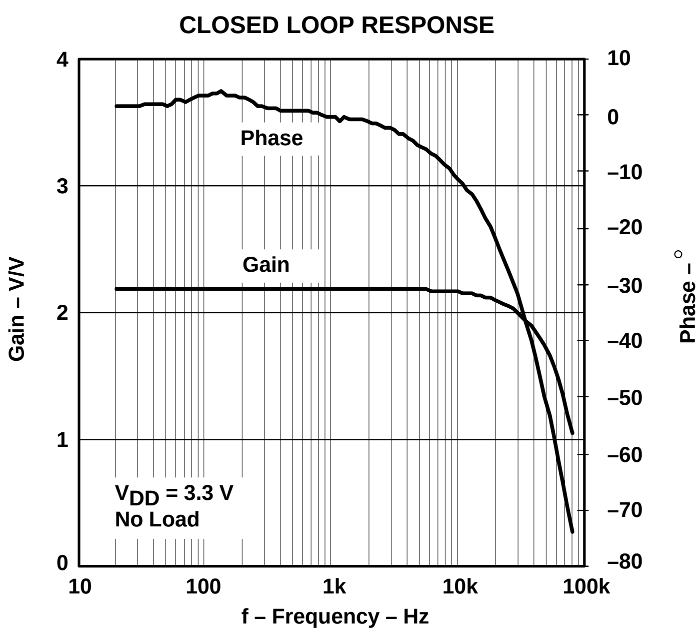


Figure 11

TYPICAL CHARACTERISTICS

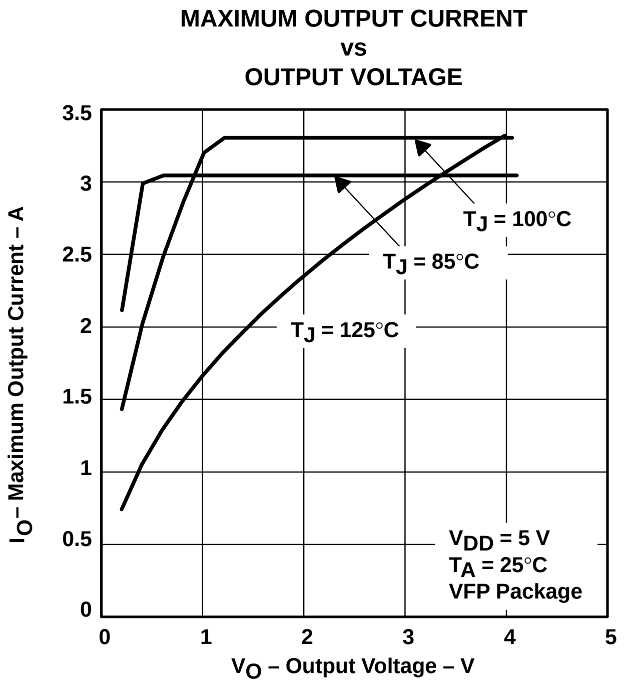


Figure 12

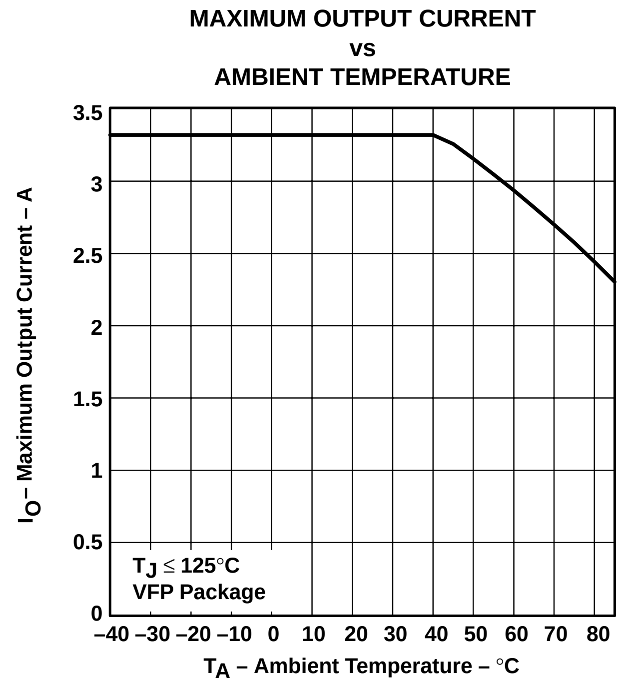


Figure 13

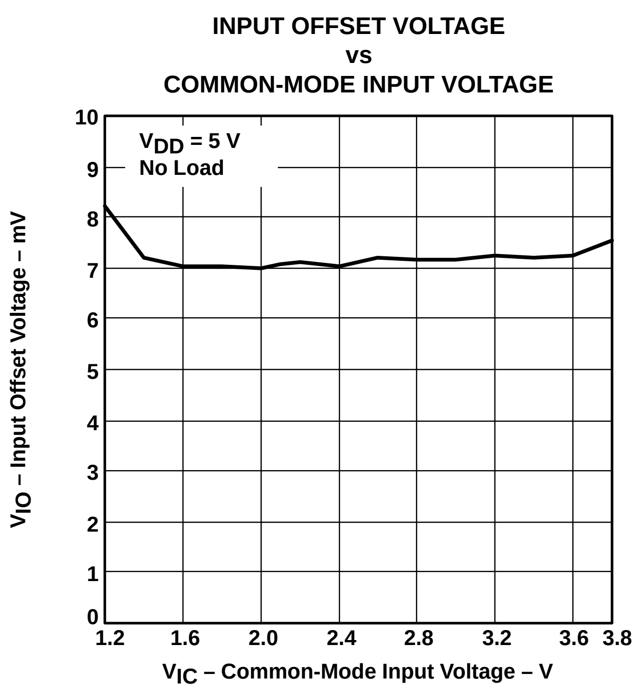


Figure 14

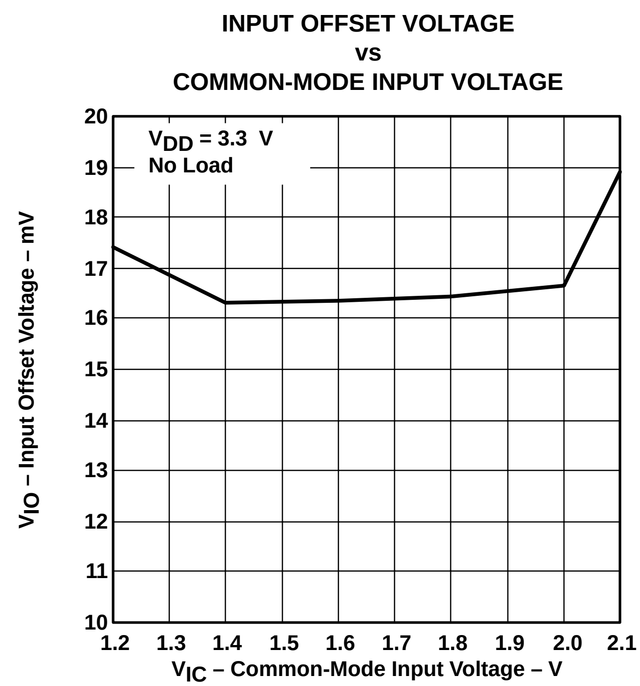


Figure 15

APPLICATION INFORMATION

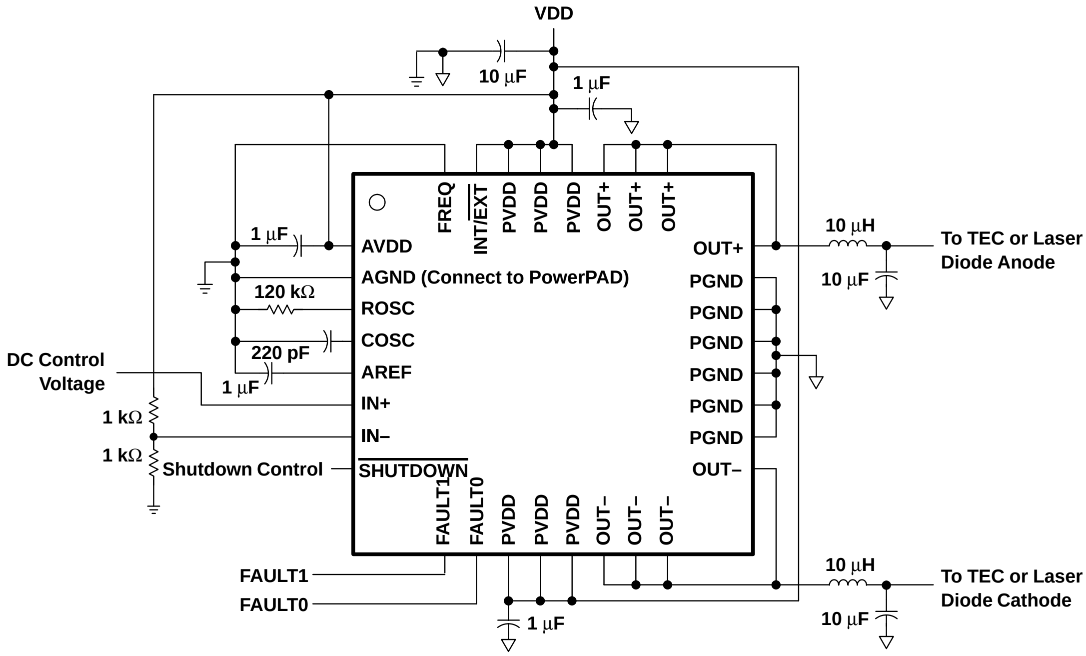


Figure 16. Typical Application Circuit

output filter considerations

TEC element manufacturers provide electrical specifications for maximum dc current and maximum output voltage for each particular element. The maximum ripple current, however, is typically only recommended to be less than 10% with no reference to the frequency components of the current. The maximum temperature differential across the element, which decreases as ripple current increases, may be calculated with the following equation:

$$\Delta T = \frac{1}{\left(1 + N^2\right)} \times \Delta T_{max} \qquad (1)$$

Where:

ΔT = actual temperature differential

ΔT_{max} = maximum temperature differential (specified by manufacturer)

N = ratio of ripple current to dc current

According to this relationship, a 10% ripple current reduces the maximum temperature differential by 1%. An LC network may be used to filter the current flowing to the TEC to reduce the amount of ripple and, more importantly, protect the rest of the system from any electromagnetic interference (EMI).

APPLICATION INFORMATION

filter component selection

The LC filter, which may be designed from two different perspectives, both described below, will help estimate the overall performance of the system. The filter should be designed for the worst-case conditions during operation, which is typically when the differential output is at 50% duty cycle. The following section serves as a starting point for the design, and any calculations should be confirmed with a prototype circuit in the lab.

Any filter should always be placed as close as possible to the DRV591 to reduce EMI.

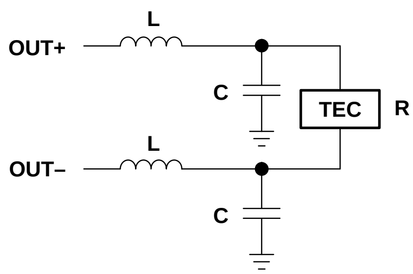


Figure 17. LC Output Filter

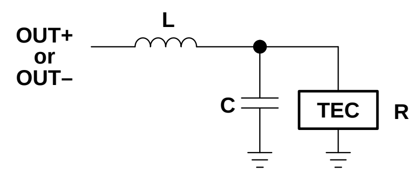


Figure 18. LC Half-Circuit Equivalent (for DRV591 Only)

LC filter in the frequency domain

The transfer function for a 2nd order low-pass filter (Figures 17 and 18) is shown in equation (2):

$$H_{LP}(j\omega) = \frac{1}{-\left(\frac{\omega}{\omega_0}\right)^2 + \frac{1}{Q}\frac{j\omega}{\omega_0} + 1} \qquad (2)$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

Q = quality factor

ω = DRV591 switching frequency

For the DRV591, the differential output switching frequency is typically selected to be 500 kHz. The resonant frequency for the filter is typically chosen to be at least one order of magnitude lower than the switching frequency. Equation (2) may then be simplified to give the following magnitude equation (3). These equations assume the use of the filter in Figure 17.

APPLICATION INFORMATION

LC filter in the frequency domain (continued)

$$\left|H_{LP}\right|_{dB} = -40\log\left(\frac{f_s}{f_o}\right) \tag{3}$$

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

$$f_s = 500\text{ kHz (DRV591 switching frequency)}$$

If L=10 μH and C=10 μF, the cutoff frequency is 15.9 kHz, which corresponds to –60 dB of attenuation at the 500 kHz switching frequency. For VDD = 5 V, the amount of ripple voltage at the TEC element is approximately 5 mV.

The average TEC element has a resistance of 1.5 Ω, so the ripple current through the TEC is approximately 3.4 mA. At the 3-A maximum output current of the DRV591, this 5.4 mA corresponds to 0.11% ripple current, causing less than 0.0001% reduction of the maximum temperature differential of the TEC element (see equation 1).

LC filter in the time domain

The ripple current of an inductor may be calculated using equation (4):

$$\Delta I_L = \frac{\left(V_O - V_{TEC}\right)DT_s}{L} \tag{4}$$

$$D = \text{duty cycle (0.5 worst case)}$$

$$T_s = 1/f_s = 1/500\text{ kHz}$$

For V_O = 5 V, V_{TEC} = 2.5 V, and L = 10 μH, the inductor ripple current is 250 mA. To calculate how much of that ripple current will flow through the TEC element, however, the properties of the filter capacitor must be considered.

For relatively small capacitors (less than 22 μF) with very low equivalent series resistance (ESR, less than 10 mΩ), such as ceramic capacitors, the following equation (5) may be used to estimate the ripple voltage on the capacitor due to the change in charge:

$$\Delta V_C = \frac{\pi^2}{2}\,(1–D)\left(\frac{f_o}{f_s}\right)^2 V_{TEC} \tag{5}$$

$$D = \text{duty cycle}$$

$$f_s = 500\text{ kHz}$$

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

APPLICATION INFORMATION

LC filter in the time domain (continued)

For L = 10 µH and C = 10 µF, the cutoff frequency, f_0, is 15.9 kHz. For worst case duty cycle of 0.5 and V_{TEC}=2.5 V, the ripple voltage on the capacitors is 6.2 mV. The ripple current may be calculated by dividing the ripple voltage by the TEC resistance of 1.5 Ω, resulting in a ripple current through the TEC element of 4.1 mA. Note that this is similar to the value calculated using the frequency domain approach.

For larger capacitors (greater than 22 µF) with relatively high ESR (greater than 100 mΩ), such as electrolytic capacitors, the ESR dominates over the charging-discharging of the capacitor. The following simple equation (6) may be used to estimate the ripple voltage:

$$\Delta V_C = \Delta I_L \times R_{ESR} \tag{6}$$

ΔI_L = inductor ripple current

R_{ESR} = filter capacitor ESR

For a 100 µF electrolytic capacitor, an ESR of 0.1 Ω is common. If the 10 µH inductor is used, delivering 250 mA of ripple current to the capacitor (as calculated above), then the ripple voltage is 25 mV. This is over ten times that of the 10 µF ceramic capacitor, as ceramic capacitors typically have negligible ESR.

For worst case conditions, the on-resistance of the output transistors has been ignored to give the maximum theoretical ripple current. In reality, the voltage drop across the output transistors decreases the maximum V_O as the output current increases. It can be shown using equation (4) that this decreases the inductor ripple current, and therefore the TEC ripple current.

switching frequency configuration: oscillator components R_{OSC} and C_{OSC} and FREQ operation

The onboard ramp generator requires an external resistor and capacitor to set the oscillation frequency. The frequency may be either 500 kHz or 100 kHz by selecting the proper capacitor value and by holding the FREQ pin either low (500 kHz) or high (100 kHz). Table 1 shows the values required and FREQ pin configuration for each switching frequency.

Table 1. Frequency Configuration Options

SWITCHING FREQUENCY	R_{OSC}	C_{OSC}	FREQ
500 kHz	120 kΩ	220 pF	LOW (GND)
100 kHz	120 kΩ	1 nF	HIGH (VDD)

For proper operation, the resistor R_{OSC} should have 1% tolerance while capacitor C_{OSC} should be a ceramic type with 10% tolerance. Both components should be grounded to AGND, which should be connected to PGND at a single point, typically where power and ground are physically connected to the printed-circuit board.

external clocking operation

To synchronize the switching to an external clock signal, pull the INT/$\overline{\text{EXT}}$ terminal low, and drive the clock signal into the COSC terminal. This clock signal must be from 10% to 90% duty cycle and meet the voltage requirements specified in the electrical specifications table. Since the DRV591 includes an internal frequency doubler, the external clock signal must be approximately 250 kHz. Deviations from the 250 kHz clock frequency are allowed and are specified in the electrical characteristic table. The resistor connected from ROSC to ground may be omitted from the circuit in this mode of operation—the source is disconnected internally.

APPLICATION INFORMATION

input configuration: differential and single-ended

If a differential input is used, it should be biased around the midrail of the DRV591 and must not exceed the common-mode input range of the input stage (see the operating characteristics at the beginning of the data sheet).

The most common configuration employs a single-ended input. The unused input should be tied to $V_{DD}/2$, which may be simply accomplished with a resistive voltage divider. For the best performance, the resistor values chosen should be at least 100 times lower than the input resistance of the DRV591. This prevents the bias voltage at the unused input from shifting when the signal input is applied. A small ceramic capacitor should also be placed from the input to ground to filter noise and keep the voltage stable. An op amp configured as a buffer may also be used to set the voltage at the unused input.

fixed internal gain

The differential output voltage may be calculated using equation (7):

$$V_O = V_{OUT+} - V_{OUT-} = A_V\left(V_{IN+} - V_{IN-}\right) \quad (7)$$

A_V is the voltage gain, which is fixed internally at 2.34 V/V. The maximum and minimum ratings are provided in the electrical specification table at the beginning of the data sheet.

power supply decoupling

To reduce the effects of high-frequency transients or spikes, a small ceramic capacitor, typically 0.1 µF to 1 µF, should be placed as close to each set of PVDD pins of the DRV591 as possible. For bulk decoupling, a 10 µF to 100 µF tantalum or aluminum electrolytic capacitor should be placed relatively close to the DRV591.

AREF capacitor

The AREF terminal is the output of an internal mid-rail voltage regulator used for the onboard oscillator and ramp generator. The regulator may not be used to provide power to any additional circuitry. A 1 µF ceramic capacitor must be connected from AREF to AGND for stability (see oscillator components above for AGND connection information).

$\overline{\text{SHUTDOWN}}$ operation

The DRV591 includes a shutdown mode that disables the outputs and places the device in a low supply current state. The $\overline{\text{SHUTDOWN}}$ pin may be controlled with a TTL logic signal. When $\overline{\text{SHUTDOWN}}$ is held high, the device operates normally. When $\overline{\text{SHUTDOWN}}$ is held low, the device is placed in shutdown. The $\overline{\text{SHUTDOWN}}$ pin must not be left floating. If the shutdown feature is unused, the pin may be connected to VDD.

APPLICATION INFORMATION

fault reporting

The DRV591 includes circuitry to sense three faults:

- Overcurrent
- Undervoltage
- Overtemperature

These three fault conditions are decoded via the FAULT1 and FAULT0 terminals. Internally, these are open-drain outputs, so an external pull-up resistor of 5 kΩ or greater is required.

Table 2. Fault Indicators

FAULT1	FAULT0	
0	0	Overcurrent
0	1	Undervoltage
1	0	Overtemperature
1	1	Normal operation

The over-current fault is reported when the output current exceeds four amps. As soon as the condition is sensed, the over-current fault is set and the outputs go into a high-impedance state for approximately 3 µs to 5 µs (500 kHz operation). After 3 µs to 5 µs, the outputs are re-enabled. If the over-current condition has ended, the fault is cleared and the device resumes normal operation. If the over-current condition still exists, the above sequence will repeat.

The under-voltage fault is reported when the operating voltage is reduced below 2.8 V. This fault is not latched, so as soon as the power-supply recovers, the fault will be cleared and normal operation will resume. During the under-voltage condition, the outputs go to 3-state to prevent over-dissipation due to increased $r_{DS(on)}$.

The over-temperature fault is reported when the junction temperature exceeds 130°C. The device continues operating normally until the junction temperature reaches 190°C, at which point the IC is disabled to prevent permanent damage from occurring. The system's controller must reduce the power demanded from the DRV591 once the over-temperature flag is set, or else the device switches off when it reaches 190°C. This fault is not latched; once the junction temperature drops below 130°C, the fault is cleared, and normal operation resumes.

power dissipation and maximum ambient temperature

Though the DRV591 is much more efficient than traditional linear solutions, the power drop across the on-resistance of the output transistors does generate some heat in the package, which may be calculated as shown in equation (8):

$$P_{DISS} = \left(I_{OUT}\right)^2 \times r_{DS(on),\ total} \tag{8}$$

For example, at the maximum output current of 3 A through a total on-resistance of 130 mΩ (at T_J = 25°C), the power dissipated in the package is 1.17 W.

Calculate the maximum ambient temperature using equation (9):

$$T_A = T_J - \left(\theta_{JA} \times P_{DISS}\right) \tag{9}$$

APPLICATION INFORMATION

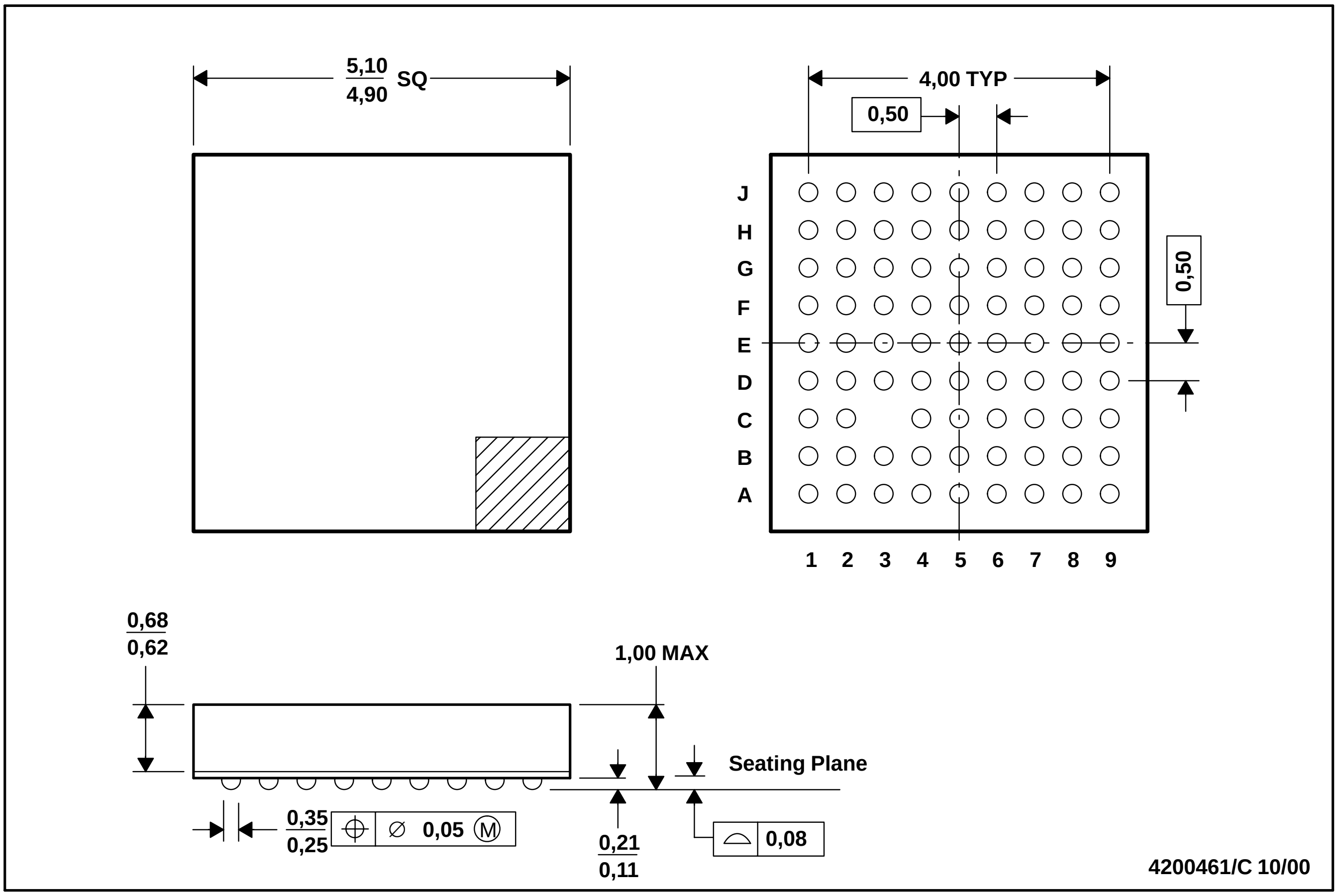
printed circuit board (PCB) layout considerations

Since the DRV591 is a high-current switching device, a few guidelines for the layout of the printed-circuit board (PCB) must be considered:

1. **Grounding.** Analog ground (AGND) and power ground (PGND) must be kept separated, ideally back to where the power supply physically connects to the PCB, minimally back to the bulk decoupling capacitor (10 μF ceramic minimum). Furthermore, the PowerPAD ground connection should be made to AGND, not PGND. Ground planes are not recommended for AGND or PGND, traces should be used to route the currents. Wide traces (100 mils) should be used for PGND while narrow traces (15 mils) should be used for AGND.
2. **Power supply decoupling.** A small 0.1 μF to 1 μF ceramic capacitor should be placed as close to each set of PVDD pins as possible, connecting from PVDD to PGND. A 0.1 μF to 1 μF ceramic capacitor should also be placed close to the AVDD pin, connecting from AVDD to AGND. A bulk decoupling capacitor of at least 10 μF, preferably ceramic, should be placed close to the DRV591, from PVDD to PGND. If power supply lines are long, additional decoupling may be required.
3. **Power and output traces.** The power and output traces should be sized to handle the desired maximum output current. The output traces should be kept as short as possible to reduce EMI, i.e., the output filter should be placed as close to the DRV591 outputs as possible.
4. **PowerPAD.** The DRV591 in the Quad Flatpack package uses TI’s PowerPAD technology to enhance the thermal performance. The PowerPAD is physically connected to the substrate of the DRV591 silicon, which is connected to AGND. The PowerPAD ground connection should therefore be kept separate from PGND as described above. The pad underneath the AGND pin may be connected underneath the device to the PowerPAD ground connection for ease of routing. For additional information on PowerPAD PCB layout, refer to the *PowerPAD Thermally Enhanced Package* application note, TI literature number SLMA002.
5. **Thermal performance.** For proper thermal performance, the PowerPAD must be soldered down to a thermal land, as described in the *PowerPAD Thermally Enhanced Package* application note, TI literature number SLMA002. In addition, at high current levels (greater than 2 A) or high ambient temperatures (greater than 25°C), an internal plane may be used for heat sinking. The vias under the PowerPAD should make a solid connection, and the plane should not be tied to ground except through the PowerPAD connection, as described above.

MECHANICAL DATA

GQE (S-PBGA-N80) **PLASTIC BALL GRID ARRAY**

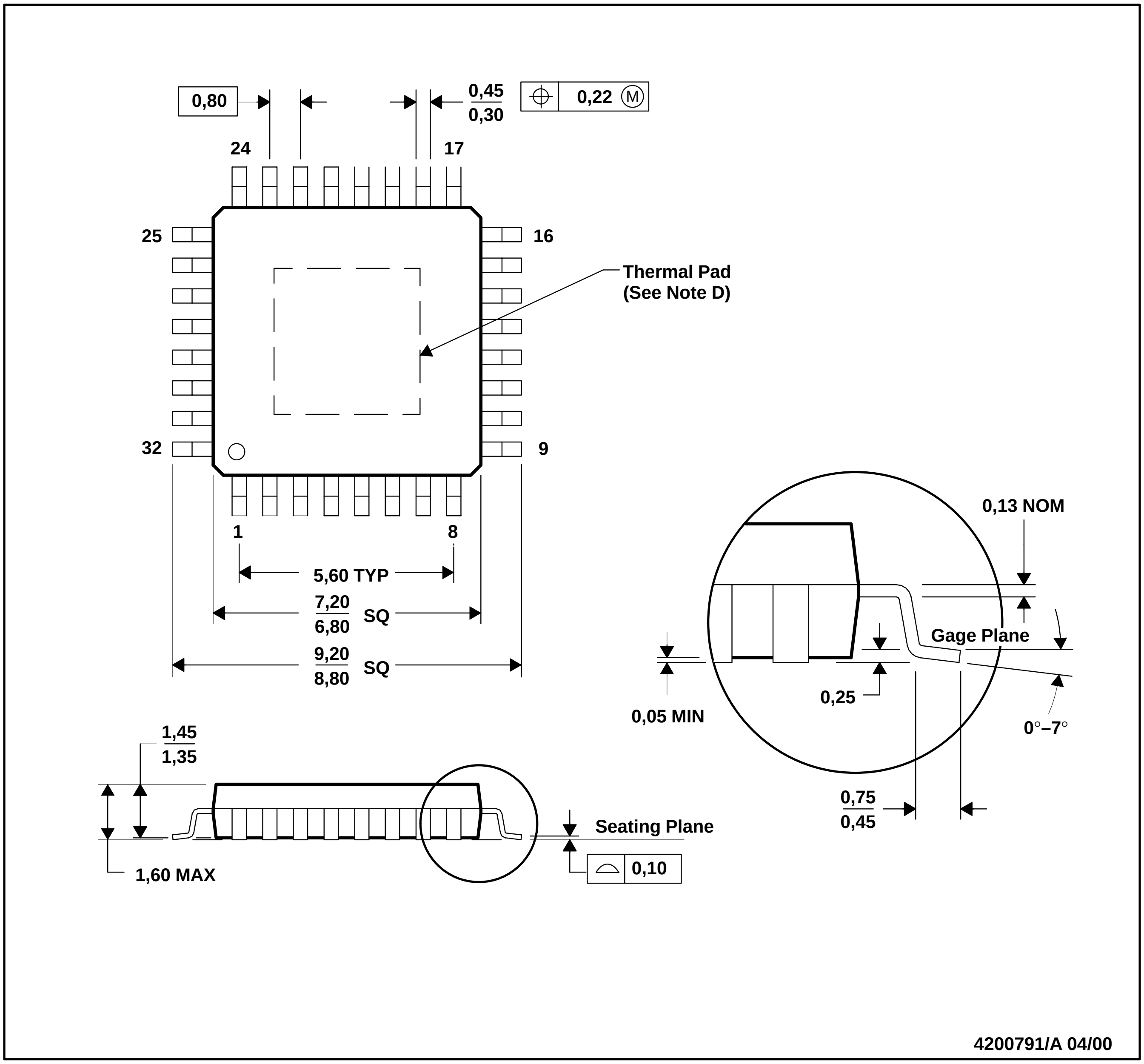


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO-225

MicroStar Junior is a trademark of Texas Instruments.

MECHANICAL DATA

VFP (S-PQFP-G32) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265