INITIAL RELEASE
Final Electrical Specifications

LTC1274/LTC1277

12-Bit, 10mW, 100ksps ADCs with 1µA Shutdown

June 1995

FEATURES

- **Low Power Dissipation: 10mW Typical**
- **Sample Rate: 100ksps**
- Samples Inputs Well Beyond Nyquist, 71dB S/(N + D) and 77dB THD Minimum at f_{IN} = 100kHz
- Single Supply 5V or ±5V Operation
- ±0.5LSB Maximum INL and ±0.75LSB Maximum DNL (A Grade)
- **Power Shutdown to 1µA in Sleep Mode**
- 160µA Nap Mode (LTC1277) with Instant Wake-Up
- 30ppm/°C (Max) Internal Reference (A Grade) Can Be Overdriven
- Internal Synchronized Clock
- 0V to 4.096V or ±2.048V Input Ranges (1mV/LSB)
- 24-Lead SO Wide Package

APPLICATIONS

- Battery-Powered Portable Systems
- High Speed Data Acquisition for PCs
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Spectrum Analysis

DESCRIPTION

The LTC®1274/LTC1277 are 8µs sampling 12-bit A/D converters which draw only 2mA (typ) from a single 5V or ±5V supplies. These easy-to-use devices come complete with a 2µs sample-and-hold, a precision reference and an internally trimmed clock. Unipolar and bipolar conversion modes add to the flexibility of the ADCs.

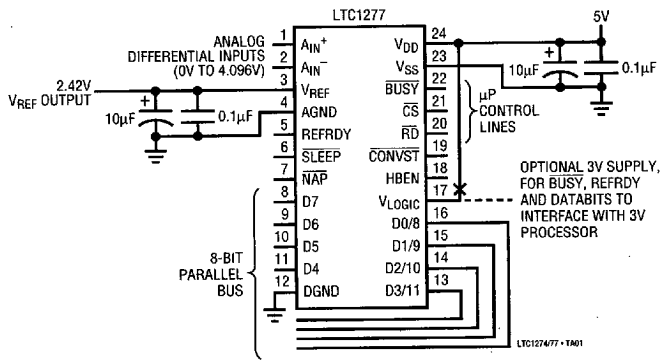
Two power-down modes are available in the LTC1277. In Nap mode, the LTC1277 draws only 160µA and the instant wake-up from Nap mode allows the LTC1277 to be powered down even during brief inactive periods. In Sleep mode only 1µA will be drawn. A REFRDY signal is used to show the ADC is ready to sample after waking up from Sleep mode. The LTC1274 also provides the Sleep mode and REFRDY signal.

The A/D converters convert 0V to 4.096V unipolar inputs from a single 5V supply or ±2.048V bipolar inputs from ±5V supplies.

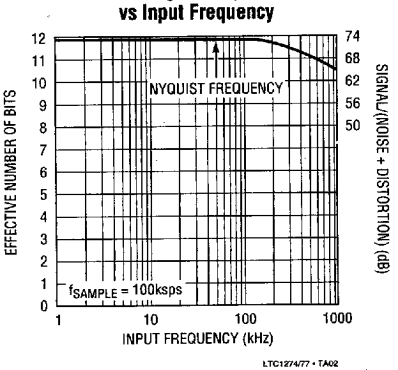
The LTC1274 has a single-ended input and a 12-bit parallel data format. The LTC1277 offers a differential input and a 2-byte read format. The bipolar mode is formatted as 2's complement for the LTC1274 and offset binary for the LTC1277.

TYPICAL APPLICATION

Single 5V Supply, 10mW, 100kHz, 12-Bit ADC



Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency

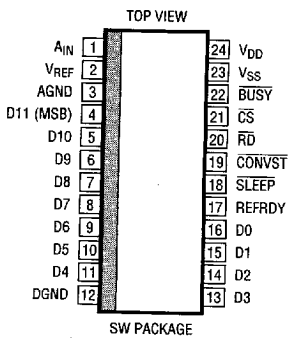


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 7V
Negative Supply Voltage (V_{SS})
  Bipolar Operation Only ..... −6V to GND
Total Supply Voltage (V_{DD} to V_{SS})
  Bipolar Operation Only 12V
Analog Input Voltage (Note 3)
  Unipolar Operation ..... − 0.3V to V_{DD} + 0.3V
  Bipolar Operation ..... V_{SS} − 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4)
  Unipolar Operation ..... − 0.3V to 12V
  Bipolar Operation ..... V_{SS} − 0.3V to 12V
Digital Output Voltage
  Unipolar Operation ..... − 0.3V to V_{DD} + 0.3V
  Bipolar Operation ..... −0.3V to V_{DD} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
  Commercial ..... 0°C to 70°C
  Industrial ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

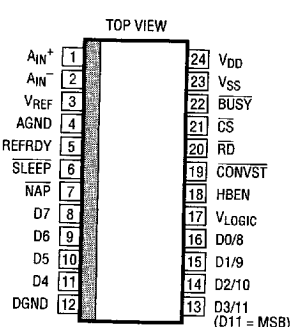
PACKAGE/ORDER INFORMATION



SW PACKAGE
24-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1274CSW
LTC1274AISW
LTC1274ISW



SW PACKAGE
24-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1277CSW
LTC1277AISW
LTC1277ISW

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		LTC1274A/LTC1277A MIN	TYP	MAX	LTC1274/LTC1277 MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 7)	●			±0.5			±1	LSB
Differential Linearity Error		●			±0.75			±1	LSB
Offset Error	(Note 8)				±4			±5	LSB
		●			±5			±7	LSB
Gain Error					±15			±20	LSB
Gain Error Tempco	$I_{OUT(REF)}$ = 0	●		±5	±30		±10	±45	ppm/°C

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ANALOG INPUT (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A LTC1274/LTC1277 MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 10)	4.75V ≤ V_{DD} ≤ 5.25V (Unipolar) 4.75V ≤ V_{DD} ≤ 5.25V, −5.25V ≤ V_{SS} ≤ −2.45V (Bipolar)	● ●		0 to 4.096 ±2.048		V V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode) During Conversions (Hold Mode)			45 5		pF pF

DYNAMIC ACCURACY (Notes 5, 9)

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A MIN	TYP	MAX	LTC1274/LTC1277 MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	50kHz Input Signal 100kHz Input Signal	 ●	 71	73 72.5		 70	73 72.5		dB dB
THD	Total Harmonic Distortion Up to 5th Harmonic	50kHz Input Signal 100kHz Input Signal	 ●		−84 −82	 −77		−84 −82	 −76	dB dB
	Peak Harmonic or Spurious Noise	50kHz Input Signal 100kHz Input Signal	 ●		−84 −82	 −77		−84 −82	 −76	dB dB
IMD	Intermodulation Distortion	f_{IN1} = 96.95kHz, f_{IN2} = 97.68kHz 2nd Order Terms 3rd Order Terms			 −78 −81			 −78 −81		 dB dB
	Full Power Bandwidth				2			2		MHz
	Full Linear Bandwidth [S/(N + D) ≥ 68dB]				400			400		kHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		LTC1274A/LTC1277A MIN	TYP	MAX	LTC1274/LTC1277 MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.400	2.420	2.440	2.400	2.420	2.440	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±5	±30		±10	±45	ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V −5.25V ≤ V_{SS} ≤ −4.75V			0.01 0.01			0.01 0.01		LSB/V LSB/V
V_{REF} Load Regulation	70µA ≥ I_{OUT} ≥ −5mA			2			2		LSB/mA

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A LTC1274/LTC1277 MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage, All Logic Outputs	V_{DD} = 4.75V I_O = −10µA I_O = −200µA	 ●	 4.0	4.7		V V

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A LTC1274/LTC1277 MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage, All Logic Outputs	V_{DD} = 4.75V I_O = 160µA I_O = 1.6mA	 ●		0.05 0.10	 0.4	V V
I_{OZ}	High-Z Output Leakage D11 to D0/8	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	High-Z Output Capacitance D11 to D0/8	$\overline{CS}$ High (Note 10)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A LTC1274/LTC1277 MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage (Notes 11, 12)	Unipolar and Bipolar Mode		4.75		5.25	V
V_{SS}	Negative Supply Voltage (Note 11)	Bipolar Mode Only		–2.45		–5.25	V
I_{DD}	Positive Supply Current	f_{SAMPLE} = 100ksps $\overline{NAP}$ = 0V (LTC1277 Only) $\overline{SLEEP}$ = 0V	● ● ●		2 160 0.3	4 320 5	mA µA µA
I_{SS}	Negative Supply Current	f_{SAMPLE} = 100ksps, Bipolar Mode Only $\overline{SLEEP}$ = 0V	● ●		40 0.3	70 5	µA µA
P_{DISS}	Power Dissipation	f_{SAMPLE} = 100ksps $\overline{NAP}$ = 0V (LTC1277 Only) $\overline{SLEEP}$ = 0V (Unipolar/Bipolar)	● ● ●		10 0.8	20 1.8 25/50	mW mW µW

TIMING CHARACTERISTICS (Note 5) See Figures 4 to 8.

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A LTC1274/LTC1277 MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency	(Note 11)	●	100			ksps
t_{CONV}	Conversion Time		●		6	8	µs
t_{ACQ}	Acquisition Time		●		0.35	2	µs
t_1	$\overline{CS}\downarrow$ to $\overline{RD}\downarrow$ Setup Time	(Note 10)	●	0			ns
t_2	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Note 10)	●	30			ns
t_3	$\overline{NAP}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time	(LTC1277 Only) (Note 11)			2		µs
t_4	$\overline{CONVST}$ Low Time	(Note 13)	●	40			ns
t_5	$\overline{CONVST}\downarrow$ to $\overline{BUSY}\downarrow$ Delay	C_L = 100pF	●		70	150	ns
t_6	Data Ready Before $\overline{BUSY}\uparrow$	C_L = 100pF	●	20	65		ns
t_7	Delay Between Conversions	(Note 11)	●		0.35	2	µs
t_8	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$	(Note 10)	●	–20			ns
t_9	Data Access Time After $\overline{RD}\downarrow$	C_L = 20pF (Note 10)	 ●		50	110 140	ns ns
		C_L = 100pF	 ●		65	125 170	ns ns
t_{10}	Bus Relinquish Time	C_L = 100pF	 ●	20 20	60	90 100	ns ns

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TIMING CHARACTERISTICS (Note 5) See Figures 4 to 8.

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A LTC1274/LTC1277 MIN	TYP	MAX	UNITS
t_{11}	$\overline{RD}$ Low Time	(Note 10)	●	t_9			ns
t_{12}	$\overline{CONVST}$ High Time	(Notes 10, 13)	●	40			ns
t_{13}	Aperture Delay of Sample-and-Hold				35		ns
t_{14}	$\overline{SLEEP}$↑ to REFRDY↑ Wake-Up Time	10µF Bypass at V_{REF} Pin			4		ms
t_{15}	HBEN↑ to High Byte Data Valid	C_L = 100pF (LTC1277 Only)	●		35	100	ns
t_{16}	HBEN↓ to Low Byte Data Valid	C_L = 100pF (LTC1277 Only)	●		45	100	ns
t_{17}	HBEN↑ to $\overline{RD}$↓ Setup Time	(Note 10) (LTC1277 Only)	●	10			ns
t_{18}	$\overline{RD}$↑ to HBEN↓ Setup Time	(Note 10) (LTC1277 Only)	●	10			ns

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} (ground for unipolar mode) or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for unipolar mode) or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below V_{SS} (ground for unipolar mode), they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for unipolar mode) without latch-up. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V (V_{SS} = −5V for bipolar mode), f_{SAMPLE} = 100ksps, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for unipolar and bipolar modes.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: For LTC1274, bipolar offset is the offset voltage measured from −0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111. For LTC1277, bipolar offset voltage is measured from −0.5LSB when the output code flickers between 0111 1111 1111 and 1000 0000 0000.

Note 9: The AC tests apply to bipolar mode only and the S/(N + D) is 71dB (typ) for unipolar mode at 100kHz input frequency.

Note 10: Guaranteed by design, not subject to test.

Note 11: Recommended operating conditions.

Note 12: A_{IN} must not exceed V_{DD} or fall below V_{SS} by more than 50mV to specified accuracy.

Note 13: The falling $\overline{CONVST}$ edge starts a conversion. If $\overline{CONVST}$ returns high at a bit decision point during the conversion it can create small errors. For best performance ensure that $\overline{CONVST}$ returns high either within 400ns after conversion start (i.e., before the first bit decision) or after $\overline{BUSY}$ rises (i.e., after bit test). See timing diagrams mode 1a and 1b (Figures 4, 5).

PIN FUNCTIONS

LTC1274

A_{IN} (Pin 1): Analog Input. 0V to 4.096V (unipolar) or ±2.048V (bipolar).

V_{REF} (Pin 2): 2.42V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic). V_{REF} can be overdriven positive with an external reference voltage.

AGND (Pin 3): Analog Ground.

D11 to D4 (Pins 4 to 11): Three-State Data Outputs. D11 is the Most Significant Bit.

DGND (Pin 12): Digital Ground.

D3 to D0 (Pins 13 to 16): Three-State Data Outputs.

REFRDY (Pin 17): Reference Ready Signal. It goes HIGH when the reference has settled after $\overline{SLEEP}$ and the ADC is ready to sample.

$\overline{SLEEP}$ (Pin 18): Sleep Mode Input. Tie this pin to LOW to put the ADC in Sleep mode and save power (REFRDY will go LOW). The device will draw 1µA in this mode.

$\overline{CONVST}$ (Pin 19): Conversion Start Signal. This active LOW signal starts a conversion on its falling edge (to recognize $\overline{CONVST}$, $\overline{CS}$ has to be LOW.)

PIN FUNCTIONS

$\overline{RD}$ (Pin 20): Read Input. This enables the output drivers when $\overline{CS}$ is LOW.

$\overline{CS}$ (Pin 21): The Chip Select input must be low for the ADC to recognize $\overline{CONVST}$ and $\overline{RD}$ inputs.

$\overline{BUSY}$ (Pin 21): The Busy output shows the converter status. It is LOW when a conversion is in progress. The rising Busy edge can be used to latch the conversion result.

V_{SS} (Pin 23): Negative 5V Supply. –5V will select bipolar operation. Bypass to AGND with 0.1µF ceramic. Tie this pin to analog ground to select unipolar operation.

V_{DD} (Pin 24): Positive 5V Supply. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

LTC1277

A_{IN}^+ (Pin 1): Positive Analog Input. ($A_{IN}^+ - A_{IN}^-$) = 0V to 4.096V (unipolar) or ±2.048V (bipolar).

A_{IN}^- (Pin 2): Negative Analog Input. This pin needs to be free of noise during conversion. For single-ended inputs tie A_{IN}^- to analog ground.

V_{REF} (Pin 3): 2.42V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic). V_{REF} can be overdriven positive with an external reference voltage.

AGND (Pin 4): Analog Ground.

REFRDY (Pin 5): Reference Ready Signal. It goes HIGH when the reference has settled after $\overline{SLEEP}$ and the ADC is ready to sample.

$\overline{SLEEP}$ (Pin 6): Sleep Mode Input. Tie this pin to LOW to put the ADC in Sleep mode and save power (REFRDY will go LOW). The device will draw 1µA in this mode.

$\overline{NAP}$ (Pin 7): Nap Mode Input. Pulling this pin LOW will shut down all currents in the ADC except the reference. In this mode the ADC draws 160µA. Wake-up from Nap mode is about 2µs.

D7 to D4* (Pins 8 to 11): Three-State Data Outputs.

DGND (Pin 12): Digital Ground.

D3/11 to D0/8* (Pins 13 to 16): Three-State Data Outputs. D11 is the Most Significant Bit.

V_{LOGIC} (Pin 17): 5V or 3V Digital Power Supply. This pin allows a 5V or 3V logic interface with the processor. All logic outputs (Data Bits, $\overline{BUSY}$ and REFRDY) will swing between 0V and V_{LOGIC}.

HBEN (Pin 18): High Byte Enable Input. The four Most Significant Bits will appear at pins 13 to 16 when this pin is HIGH. The LTC1277 uses straight binary for unipolar mode and offset binary for bipolar mode.

$\overline{CONVST}$ (Pin 19): Conversion Start Signal. This active low signal starts a conversion on its falling edge (to recognize $\overline{CONVST}$, $\overline{CS}$ has to be LOW).

$\overline{RD}$ (Pin 20): Read Input. This enables the output drivers when $\overline{CS}$ is LOW.

$\overline{CS}$ (Pin 21): The Chip Select input must be LOW for the ADC to recognize $\overline{CONVST}$ and $\overline{RD}$ inputs.

$\overline{BUSY}$ (Pin 22): The $\overline{BUSY}$ output shows the converter status. It is LOW when a conversion is in progress.

V_{SS} (Pin 23): –5V negative supply will select bipolar operation. Bypass to AGND with a 0.1µF ceramic. Tie this pin to analog ground to select unipolar operation.

V_{DD} (Pin 24): 5V Positive Supply. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

*The LTC1277 bipolar mode is in offset binary.

Table 1. LTC1277 Two-Byte Read Data Bus Status

DATA OUTPUTS	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
LOW Byte	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HIGH Byte	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

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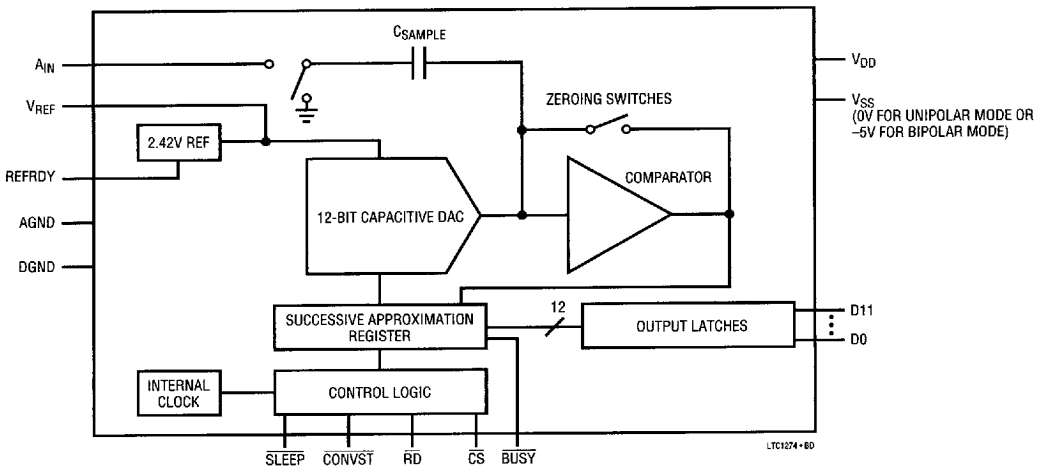
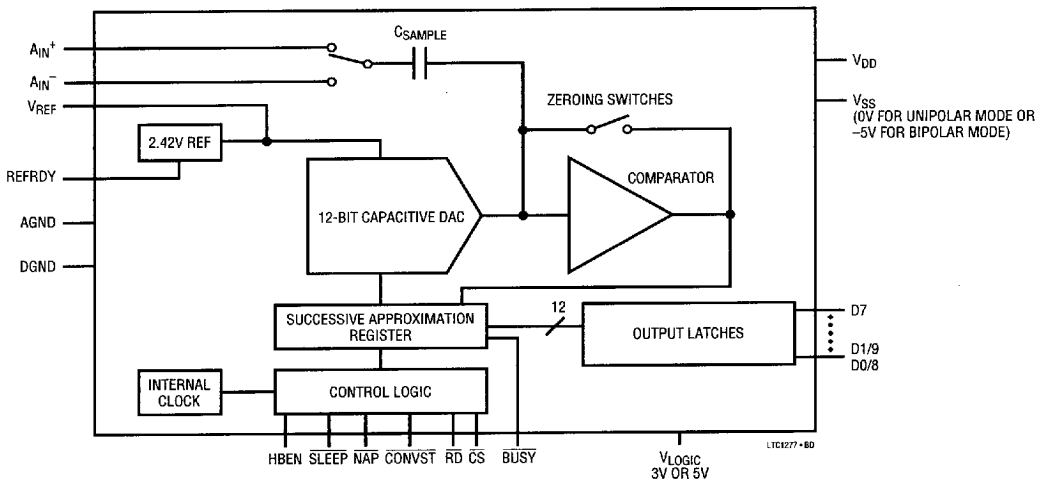
BLOCK DIAGRAMS

LTC1274

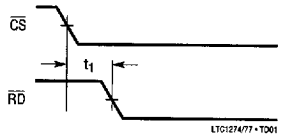


LTC1277

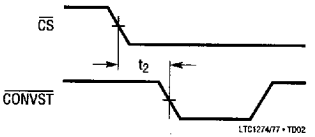


TIMING DIAGRAM

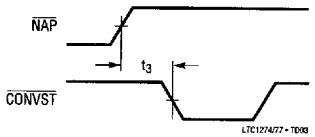
$\overline{CS}$ to $\overline{RD}$ Setup Timing



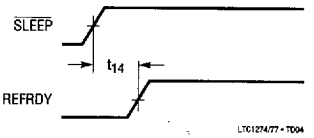
$\overline{CS}$ to $\overline{CONVST}$ Setup Timing



$\overline{NAP}$ to $\overline{CONVST}$ Setup Timing (LTC1277)



$\overline{SLEEP}$ to REFRDY Wake-Up Timing



APPLICATIONS INFORMATION

Driving the Analog Input

The analog input of the LTC1274/LTC1277 is easy to drive. It draws only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During conversion the analog input draws only a small leakage current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 2μs to small current transients will allow maximum speed operation. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADCs' A_{IN} input include the LT®1006, LT1007, LT1220, LT1223 and LT1224 op amps.

LTC1277 A_{IN}^+/A_{IN}^- Input Settling

The input capacitor for the LTC1277 is switched onto the A_{IN}^+ input during the sample phase. The voltage on the A_{IN}^+ input must settle completely within the sample period. At the end of the sample phase the input capacitor switches to the A_{IN}^- input and the conversion starts. During the conversion, the A_{IN}^+ input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. It is critical that the A_{IN}^- input voltage be free of noise and settles completely during the conversion.

Internal Reference

The ADCs have an on-chip, temperature compensated, curvature corrected, bandgap reference which is factory trimmed to 2.42V. It is internally connected to the DAC and is available at pin 2 (LTC1274) or pin 3 (LTC1277) to provide up to 1mA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10μF tantalum in parallel with a 0.1μF ceramic).

The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment. The V_{REF} pin must be driven to at least 2.45V to prevent conflict with the internal reference. The reference should be driven to no more than 3V to keep the input span within the 5V supply in unipolar mode. In bipolar mode the reference should be driven to no more than 5V, the positive supply voltage of the chip.

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APPLICATIONS INFORMATION

Figure 1 shows an LT1006 op amp driving the reference pin. In unipolar mode, the reference can be driven up to 2.95V at which point it will provide a 0V to 5V input span. For the bipolar mode, the reference can be driven up to 5V at which point it will provide a ±4.23V input span. Figure 2 shows a typical reference, the LT1019A-2.5 connected to the LTC1274. This will provide an improved drift (equal to the maximum 5ppm/°C of the LT1019A-2.5) and a ±2.115V (bipolar) or 4.231V (unipolar) full scale.

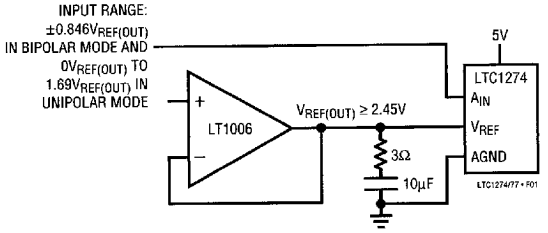

Figure 1. Driving the V_{REF} with the LT1006 Op Amp

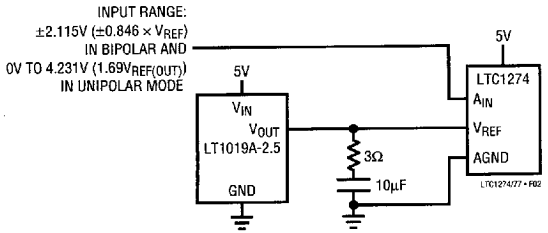

Figure 2. Supplying a 2.5V Reference Voltage to the LTC1274 with the LT1019A-2.5

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1274/LTC1277, a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD} and V_{REF} pins as shown in Figure 3. For bipolar mode, a 0.1µF ceramic provides adequate bypassing for the V_{SS} pin. The capacitors must be located as close to the pins as possible. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

Input signal leads to A_{IN} and signal return leads from AGND (pin 3 for LTC1274, pin 4 for LTC1277) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible a shielded cable between source and ADC is recommended.

Also, since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

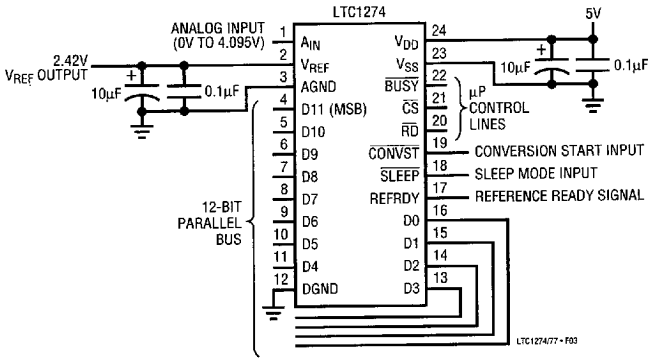

Figure 3. LTC1274 Typical Circuit

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A single point analog ground separate from the logic system ground should be established with an analog ground plane at AGND or as close as possible to the ADC. Pin 12 (DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a Wait state during conversion or by using three-state buffers to isolate the ADC data bus.

DIGITAL INTERFACE

The ADCs are designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. A separate $\overline{CONVST}$ is used to initiate a conversion. Figures 4a to 4c are the input/output characteristics of the ADCs.

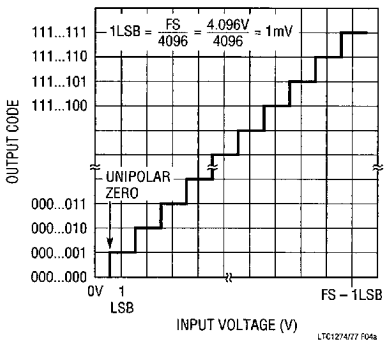

Figure 4a. LTC1274/LTC1277 Unipolar Transfer Characteristics

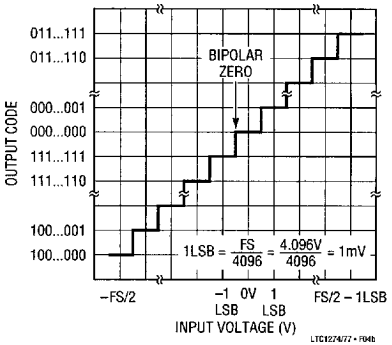

Figure 4b. LTC1274 Bipolar Transfer Characteristics (2's Complement)

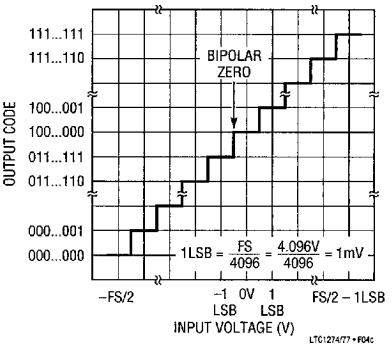

Figure 4c. LTC1277 Bipolar Transfer Characteristics (Offset Binary)

Unipolar Offset and Full-Scale Error Adjustments

In applications where absolute accuracy is important, then offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 5a shows the extra components required for full-scale error adjustment. If both offset and full-scale adjustments are needed, the circuit in Figure 5b can be used. For zero offset error apply 0.50mV (i.e., 0.5LSB) at the input and adjust the offset trim until the LTC1274/LTC1277 output code

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flickers between 0000 0000 0000 and 0000 0000 0001. For zero full-scale error apply an analog input of 4.0945V (i.e., FS – 1.5LSB or last code transition) at the input and adjust R5 until the ADC's output code flickers between 1111 1111 1110 and 1111 1111 1111.

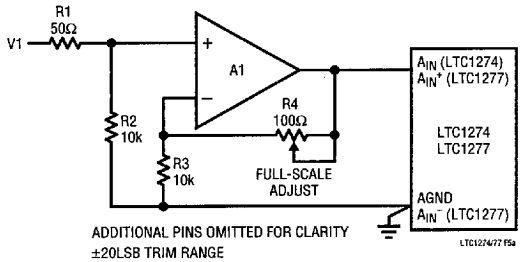

Figure 5a. Full-Scale Adjust Circuit

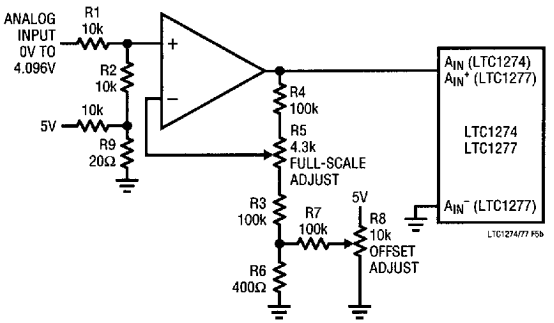

Figure 5b. LTC1274/LTC1277 Unipolar Offset and Full-Scale Adjust Circuit

LTC1274 Bipolar Offset and Full-Scale Error Adjustments

Bipolar offset and full-scale errors for LTC1274 are adjusted in a similar fashion to the unipolar case. Again, bipolar offset must be adjusted before full-scale error. Bipolar offset error adjustment is achieved by trimming the offset of the op amp driving the analog input of the

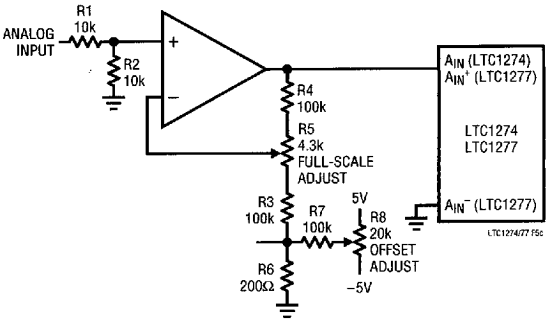

Figure 5c. LTC1274/LTC1277 Bipolar Offset and Full-Scale Adjust Circuit

LTC1274 while the input voltage is 0.5LSB below ground. This is done by applying an input voltage of –0.50mV (–0.5LSB) to the input in Figure 5c and adjusting the R8 until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, an input voltage of 2.0465V (FS – 1.5LSBs) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

LTC1277 Bipolar Offset and Full-Scale Error Adjustments

Bipolar offset and full-scale errors are adjusted in a similar fashion to the unipolar case. Again, bipolar offset must be adjusted before full-scale error. Bipolar offset error adjustment is achieved by trimming the offset of the op amp driving the analog input of the LTC1277 while the input voltage is 0.5LSB below ground. This is done by applying an input voltage of –0.50mV (–0.5LSB) to the input in Figure 5c and adjusting the R8 until the ADC output code flickers between 0111 1111 1111 and 1000 0000 0000. For full-scale adjustment, an input voltage of 2.0465V (FS – 1.5LSBs) is applied to the input and R5 is adjusted until the output code flickers between the input 1111 1111 1110 and 1111 1111 1111.

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Power Shutdown

The LTC1274/LTC1277 provide shutdown features that will save power when the ADC is in inactive periods. Both ADCs have a Sleep mode. To power down the ADCs, $\overline{SLEEP}$ (pin 18 in LTC1274 or pin 6 in LTC1277) needs to be tied low. When in Sleep mode, the LTC1274/LTC1277 will not start a conversion even though the $\overline{CONVST}$ goes low. The parts are drawing 1µA. After releasing from the Sleep mode, the ADCs need 4ms (10µF bypass capacitor on V_{REF} pin) to wake up and a REFRDY signal will go to high to indicate the ADC is ready to do conversions.

For the LTC1277, it has an additional Nap mode. When pin 7 ($\overline{NAP}$ pin the LTC1277) is tied low, all the power is off except the internal reference which is still active and provides 2.42V output voltage to the other circuitry. In this mode the ADC draws 0.8mW instead of 10mW (for minimum power, the logic inputs must be within 600mV from the supply rails). The wake-up time from the power shutdown to active state is 2µs.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs in the LTC1274: $\overline{CS}$, $\overline{CONVST}$ and $\overline{RD}$. For the LTC1277 there are four digital inputs: $\overline{CS}$, $\overline{CONVST}$, $\overline{RD}$ and HBEN. A logic "0" for $\overline{CONVST}$ will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output and this is LOW while conversion is in progress. The High Byte Enable input (HBEN) in the LTC1277 is to multiplex the 12 bits of conversion data onto the lower D7 to D0/8 outputs.

Figures 6 through 10 show several different modes of operation. In modes 1a and 1b (Figures 6 and 7) $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling edge of $\overline{CONVST}$ starts the conversion. The data outputs are always enabled and data can be latched with the $\overline{BUSY}$ rising edge. Mode 1a shows operation with a narrow logic low $\overline{CONVST}$ pulse. Mode 1b shows a narrow logic high $\overline{CONVST}$ pulse.

In mode 2 (Figure 8) $\overline{CS}$ is tied low. The falling edge of $\overline{CONVST}$ signal again starts the conversion. Data outputs are in three-state until read by the MPU with the $\overline{RD}$ signal. Mode 2 can be used for operation with a shared MPU databus.

In slow memory and ROM modes (Figures 9 and 10) $\overline{CS}$ is tied low and $\overline{CONVST}$ and $\overline{RD}$ are tied together. The MPU starts the conversion and reads the output with the $\overline{RD}$ signal. Conversions are started by the MPU or DSP (no external sample clock).

In slow memory mode the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$), starting the conversion. $\overline{BUSY}$ goes low, forcing the processor into a Wait state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; $\overline{BUSY}$ goes high releasing the processor; the processor applies a logic high to $\overline{RD}$ (= $\overline{CONVST}$) and reads the new conversion data.

In ROM mode, the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$), starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

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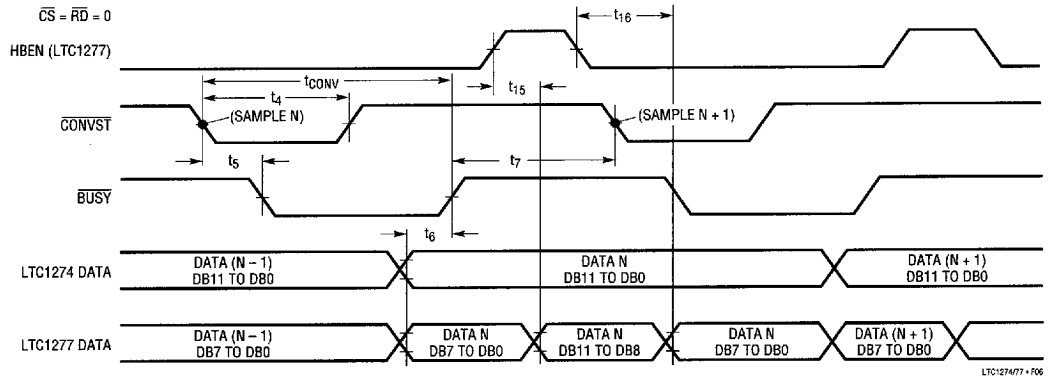

Figure 6. Mode 1a. $\overline{\text{CONVST}}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{\text{CONVST}}$ = ⊓⊔⊓⊔)

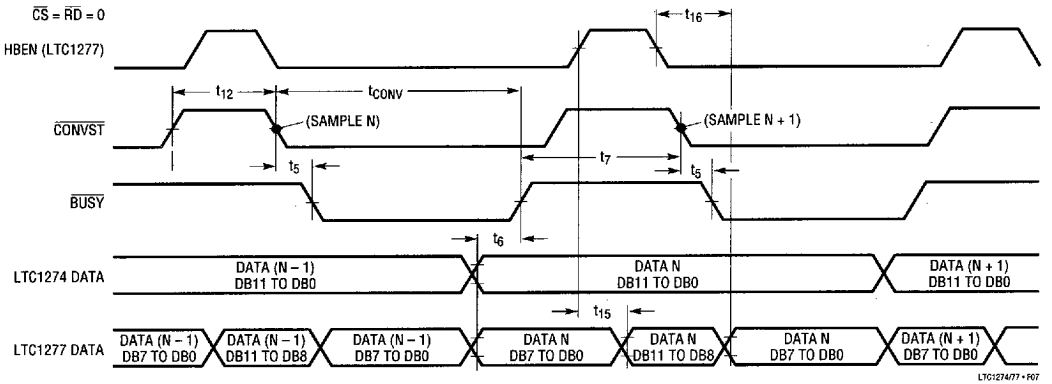

Figure 7. Mode 1b. $\overline{\text{CONVST}}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{\text{CONVST}}$ = ⊔⊓⊔⊓)

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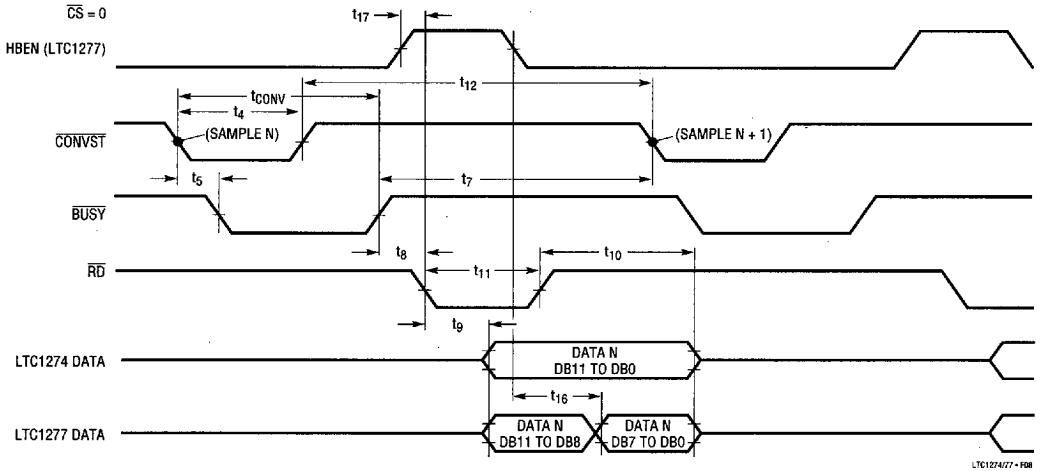

Figure 8. Mode 2. $\overline{\text{CONVST}}$ Starts a Conversion. Data is Read by $\overline{\text{RD}}$

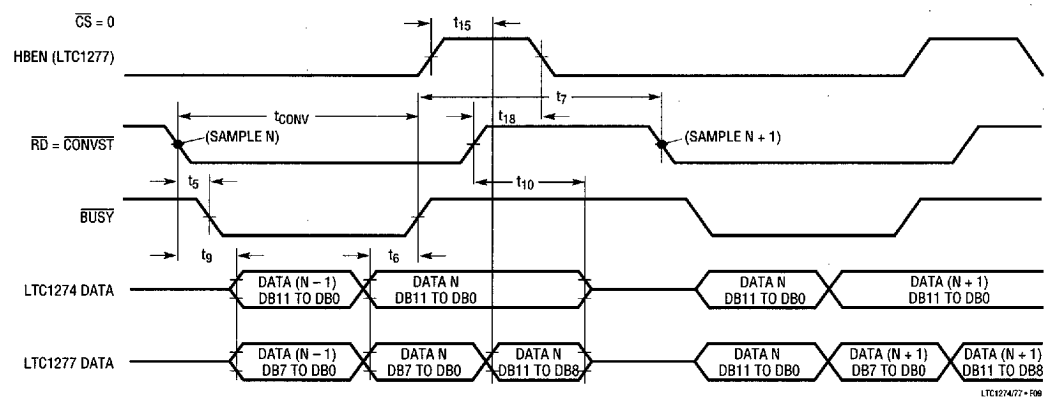

Figure 9. Slow Memory Mode

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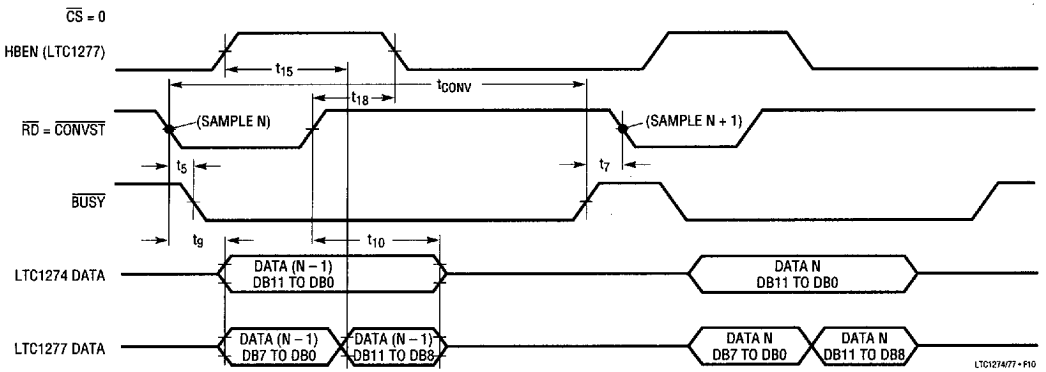

Figure 10. ROM Mode Timing

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1272	12-Bit, 3µs, 250kHz Sampling A/D Converter	Single 5V, Sampling 7572 Upgrade
LTC1273/75/76	12-Bit, 300ksps Sampling A/D Converters with Reference	Complete with Clock, Reference
LTC1278	12-Bit, 500ksps Sampling A/D Converter with Shutdown	70dB SINAD at Nyquist, Low Power
LTC1279	12-Bit, 600ksps Sampling A/D Converter with Shutdown	70dB SINAD at Nyquist, Low Power
LTC1282	12-Bit, 140ksps Sampling A/D Converter with Reference	3V or ±3V ADC with Reference, Clock
LTC1409	12-Bit, 800ksps Sampling A/D Converter with Shutdown	Fast, Complete Low Power ADC
LTC1410	12-Bit, 1.25Msps Sampling A/D Converter with Shutdown	Fast, Complete Wideband ADC