INITIAL RELEASE
Final Electrical Specifications
LTC1325

Microprocessor-Controlled Battery Management System

June 1994

FEATURES

- Fast Charge Nickel Cadmium, Nickel Hydride or Lead Acid Batteries under µP Control
- Flexible Current Regulation:
  - Programmable 111kHz PWM Current Regulator with Built-In PFET Driver
  - PFET Current Gating for Use with External Current Regulator or Current Limited Transformer
- Discharge Mode
- Measures Battery Voltage, Battery Temperature and Ambient Temperature with Internal 10-Bit ADC
- Battery Voltage, Temperature and Charge Time Fault Protection
- Built-In Voltage Regulator and Programmable Battery Attenuator
- Easy to Use 3- or 4-Wire Serial µP Interface
- Accurate Gas Gauge Function
- Wide Supply Range: V_{DD} = 4.5V to 16V
- Can Charge Batteries Greater Than V_{DD}
- Can Charge Batteries from Charging Supplies Greater Than V_{DD}
- Digital Input Pins Are High Impedance in Shutdown Mode

APPLICATIONS

- System Integrated Battery Charger

DESCRIPTION

The LTC1325 provides the core of a flexible, cost-effective solution for a system integrated battery mangement system. The monolithic CMOS chip controls the fast charging of nickel cadmium, nickel hydride, or lead acid batteries under microprocessor control. The device features a programmable 111kHz PWM constant current source controller with built-in FET driver, 10-bit ADC, internal voltage regulator, discharge-before-charge controller, programmable battery voltage attenuator, and an easy to use serial interface.

The chip may operate in one of five modes: power shutdown, idle, discharge, charge, or gas gauge. In power shutdown the supply current drops to 30µA and in the idle mode, an ADC reading may be made without any switching noise affecting the accuracy of the measurement. In the discharge mode, the battery is discharged by an external transistor while the battery is being monitored by the LTC1325 for fault conditions. The charge mode is terminated by the µP while monitoring any combination of battery voltage and temperature, ambient temperature and charge time. The LTC1325 also monitors the battery for fault conditions before and during charging. In the gas gauge mode the LTC1325 allows the total charge leaving the battery to be calculated.

TYPICAL APPLICATION

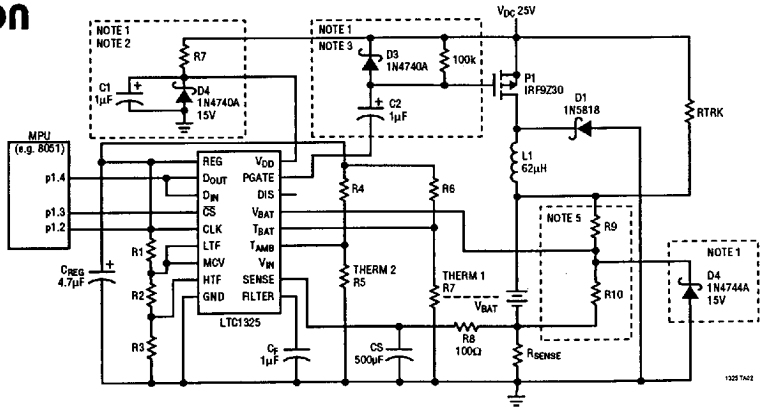
NOTE 1: NEEDED WHEN V_{DC} > 16V OR MAXIMUM BATTERY VOLTAGE, V_{BAT} > 16V.

NOTE 2: REGULATOR. OMIT THIS BLOCK AND SHORT V_{DD} TO V_{DC} WHEN V_{DC} < 16V.

NOTE 3: LEVEL SHIFTER. OMIT THIS BLOCK AND SHORT PGATE TO P1 GATE WHEN V_{DC} < 16V.

NOTE 4: ZENER TO CLAMP V_{BAT} TO BELOW V_{DD}. OMIT WHEN V_{DC} > 16V.

NOTE 5: EXTERNAL BATTERY DIVIDER. NEEDED WHEN MAXIMUM BATTERY VOLTAGE, V_{BAT} > 16V.



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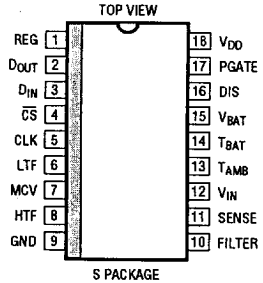
ABSOLUTE MAXIMUM RATINGS
(Note 1, 2)

V_{DD} to GND ..... −0.3V to 17V
All Other Pins ..... −0.3V to V_{DD} + 0.3V
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
18-LEAD PLASTIC SOL

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LTC1325CN LTC1325CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS
V_{DD} = 12V ±5%, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD}	V_{DD} Supply Voltage		4.5		16	V
I_{DD}	V_{DD} Supply Current	All TTL Inputs = 0V or 5V, No Load on REG		1200	2000	µA
I_{PD}	V_{DD} Supply Current	Power-Down Mode, All TTL Inputs = 0V or 5V		30	50	µA
V_{REG}	Regulator Output Voltage	No Load	3.037	3.072	3.107	V
LD_{REG}	Regulator Load Regulation	Sourcing Only, I_{REG} = 0mA to 2mA		−1	−5	mV/mA
LI_{REG}	Regulator Line Regulation	No Load, V_{DD} = 4.5V to 16V		−60	−100	µV/V
TC_{REG}	Regulator Output Tempco	No Load, 0°C < T_A < 70°C		50		ppm/°C
$V_{ERR(CHRG)}$	PWM Sense Voltage Error	V_{DAC} = 150mV V_{DAC} = 150mV V_{DAC} = 50mV V_{DAC} = 30mV or 15mV		±3 ±4 ±3 ±2		% mV mV mV
V_{HYST}	Fault Comparator Hysterisis	V_{HTF} = 1V, V_{EDV} = 0.9V, BATR V_{MCV} = V_{LTF} = 2V		±20 ±10		mV mV
V_{OS}	Fault Comparator Offset	V_{HTF} = 1V, V_{EDV} = 0.9V, BATR V_{MCV} = V_{LTF} = 2V		±50		mV
V_{BATR}	V_{BAT} for BATR = 1			100		mV
V_{BATP}	V_{BAT} for BATP = 1		V_{DD} − 1.8			V
V_{EDV}	Internal EDV Voltage		860	900	940	mV
V_{LTF}, V_{LTF}	LTF, MCV Voltage Range		1.6		2.8	V
V_{HTF}	HTF Voltage Range		0.5		1.3	V
$A_{(GG)}$	Gas Gauge Gain	−0.4V < V_{SENSE} < 0V		−4		
$V_{OS(GG)}$	Gas Gauge Offset	−0.4V < V_{SENSE} < 0V (Note 6)		±1		LSB
R_F	Internal Filter Resistor			1000		Ω
TOL_{BATD}	Battery Divider Tolerance	All Division Ratios		±2		%
V_{IL}	Input Low Voltage	CLK, $\overline{CS}$, D_{IN}	0.8	1.3		V
V_{IH}	Input High Voltage	CLK, $\overline{CS}$, D_{IN}		1.7	2.4	V
I_{IL}	Low Level Input Current	V_{CLK}, $V_{\overline{CS}}$ or V_{DIN} = 0V	−2.5		2.5	µA
I_{IH}	High Level Input Current	V_{CLK}, $V_{\overline{CS}}$ or V_{DIN} = 5V	−2.5		2.5	µA

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ELECTRICAL CHARACTERISTICS V_{DD} = 12V ±5%, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL}	Output Low Voltage	D_{OUT}, I_{OUT} = 1.6mA			0.4	V
V_{OH}	Output High Voltage	D_{OUT}, I_{OUT} = –1.6mA	2.4			V
I_{OZ}	Hi-Z Output Leakage	$V_{\overline{CS}}$ = 5V			±10	µA
V_{OHFET}	DIS or PGATE Output High	V_{DD} = 4.5V to 16V	V_{DD} – 0.05			V
V_{OLFET}	DIS or PGATE Output Low	V_{DD} = 4.5V to 16V			0.05	V
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Valid	See Test Circuits			600	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits			450	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits			400	ns
t_{hDO}	Time D_{OUT} Remains Valid After CLK↓	See Test Circuits		30		ns
t_{rDOUT}	D_{OUT} Rise Time	See Test Circuits			250	ns
t_{fDOUT}	D_{OUT} Fall Time	See Test Circuits			100	ns
f_{CLK}	Serial I/O Clock Frequency	CLK Pin	25		500	kHz
t_{rPGATE}	PGATE Rise Time	C_{LOAD} = 1500pF			120	ns
t_{fPGATE}	PGATE Fall Time	C_{LOAD} = 1500pF			120	ns
f_{OSC}	Internal Oscillator Frequency	Charge Mode, Fail-Safes Disabled	95	112	130	kHz
A/D Converter						
	Offset Error	V_{IN} Channel (Note 3)			±2	LSB
	Linearity Error	V_{IN} Channel (Notes 3, 4)		±0.5		LSB
	Full-Scale Error	V_{IN} Channel (Note 3)		±1		LSB
	On-Channel Leakage	V_{IN} Channel ON Only (Notes 3, 5)			±10	µA
	Off-Channel Leakage	V_{IN} Channel OFF (Notes 3, 5)			±10	µA

RECOMMENDED CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{hDI}	Hold Time, D_{IN} After CLK↑		150			ns
$t_{dsu\overline{CS}}$	Setup Time, $\overline{CS}$ Before First CLK↑		1			µs
t_{dsuDI}	Setup Time, D_{IN} Stable Before First CLK↑		400			ns
t_{WHCLK}	CLK High Time		0.8			µs
t_{WLCLK}	CLK Low Time		1			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfers		1			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transefer	MSBF = 1 MSBF = 0	43 52			CLK Cycles CLK Cycles

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to the GND pin.

Note 3: V_{REG} = 3.072mV ±20mV, CLK = 500kHz, unless otherwise stated.

Note 4: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 5: Channel leakage is measured after channel selection.

Note 6: Gas gauge offset excludes A/D offset error.

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PIN FUNCTIONS

REG (Pin 1): Internal Regulator Output. The regulator provides a steady 3.072V to the internal analog circuitry and provides a temperature stable reference voltage for generating MCV, HTF, LTF and thermistor bias voltages with external resistors. Requires a 4.7μF or greater bypass capacitor to ground.

D_{OUT} (Pin 2): TTL Data Output Signal for the Serial Interface. D_{OUT} and D_{IN} may be tied together to form a 3-wire interface, or remain separated to form a 4-wire interface. Data is transmitted on the falling edge of CLK (pin 5).

D_{IN} (Pin 3): TTL Data Input Signal for the Serial Interface. The data is latched into the chip on the rising edge of the CLK (pin 5).

$\overline{CS}$ (Pin 4): TTL Chip Select Signal for the Serial Interface.

CLK (Pin 5): TTL Clock for the Serial Interface.

LTF (Pin 6): Minimum Allowable Battery Temperature Analog Input. LTF may be generated by a resistive divider between REG (pin 1) and ground.

MCV (Pin 7): Maximum Allowable Cell Voltage Analog Input. MCV may be generated by a resistive divider between REG (pin 1) and ground.

HTF (Pin 8): Maximum Allowable Battery Temperature Analog Input. HTF may be generated by a resistive divider between REG (pin 1) and ground.

GND (Pin 9): Ground

FILTER (Pin 10): The external filter capacitor C_F is connected to this pin. The filter capacitor is connected to the output of the internal resistive divider across the battery to reduce the switching noise while charging. In the gas gauge mode, C_F along with an internal R_F = 1k form a lowpass filter to average the voltage across the sense resistor.

SENSE (Pin 11): The Sense pin controls the switching of the 111kHz PWM constant current source in the charging mode. The Sense pin is connected to an external sense resistor R_{SENSE} and the negative side of the battery. The charging loop forces the average voltage at the Sense pin to equal a programmable internal reference voltage V_{DAC}. The battery charging current is equal to V_{DAC}/R_{SENSE}.

In the gas gauge mode the voltage across the Sense pin is filtered by an RC network (R_F and C_F), amplified by an inverting gain of 4, then multiplexed to the ADC so the average discharge current through the battery may be measured, and the total charge leaving the battery calculated.

V_{IN} (Pin 12): General Purpose ADC Input.

T_{AMB} (Pin 13): Ambient Temperature Input. Connect to an external thermistor network. Tie to REG if not used. May be used as another general purpose ADC input.

T_{BAT} (Pin 14): Battery Temperature Input. Connect to an external NTC thermistor network. Tie to REG if not used.

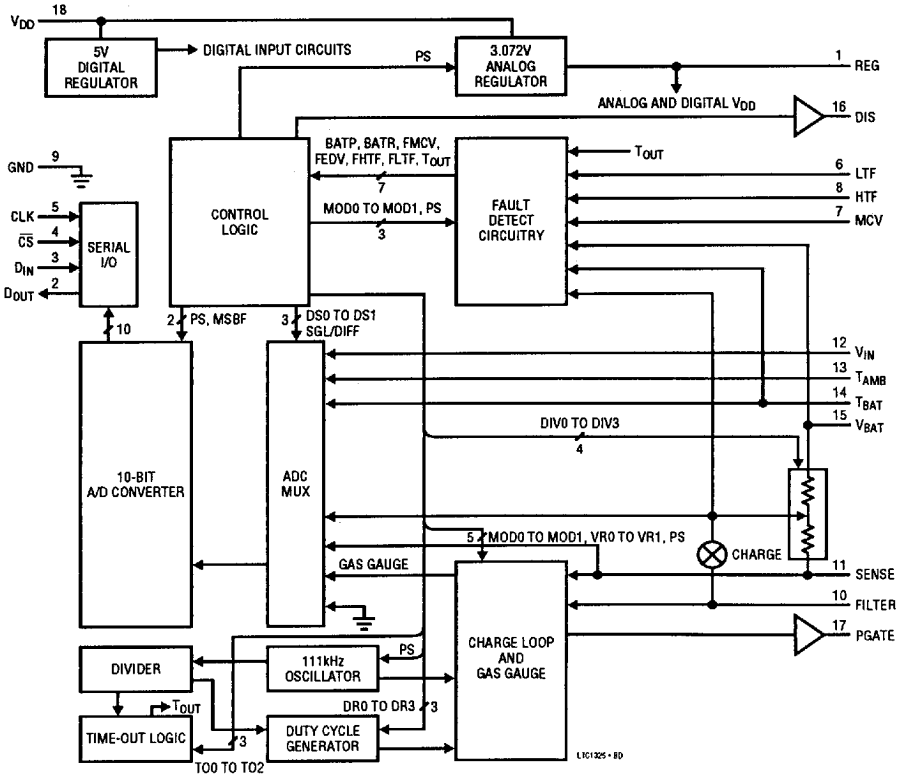
V_{BAT} (Pin 15): Battery Input. An internal voltage divider is connected between the V_{BAT} and Sense pins to normalize all battery measurements to one cell voltage. The divider is programmable to the following ratios: 1/1, 1/2, 1/3 . . . 1/15, 1/16. In shutdown and gas gauge modes the divider is disconnected.

DIS (Pin 16): Active High Discharge Control Pin. Used to turn on an external transistor which discharges the battery.

PGATE (Pin 17): FET Driver Output. Swings from GND to V_{DD}.

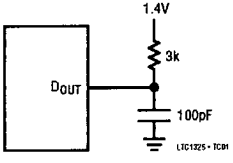
V_{DD} (Pin 18): Positive Supply Voltage. 4.5V < V_{DD} < 16V.

BLOCK DIAGRAM

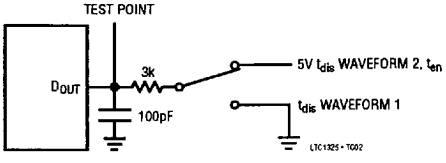


TEST CIRCUITS

Load Circuit for t_{dDO}, t_r and t_f



Load Circuit for t_{dis} and t_{en}



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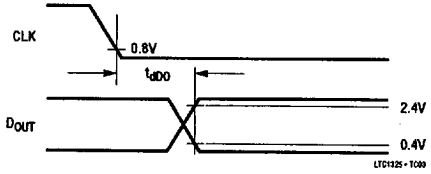
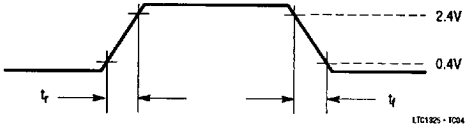
TEST CIRCUITS

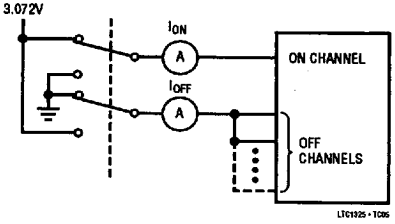
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



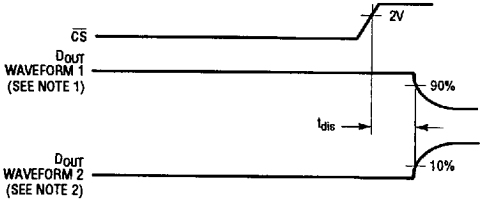
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



On and Off Channel Leakage



Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY $\overline{CS}$.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY $\overline{CS}$.

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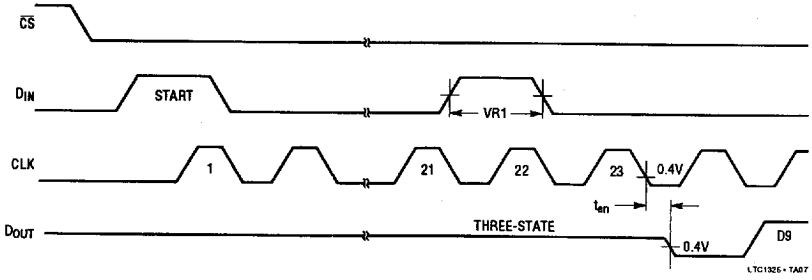
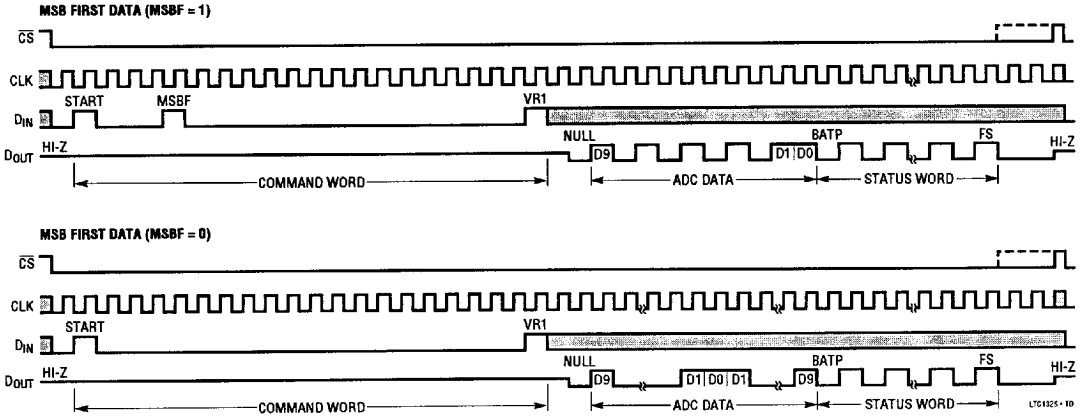
Voltage Waveforms for t_{en}



TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

During normal operation, a command word is shifted into the chip via the serial interface, then an ADC measurement is made and the 10-bit reading and chip status word are shifted out. The command word configures the LTC1325 and forces it into one of five modes: power shutdown, idle, discharge, charge or gas gauge mode.

In the power shutdown mode, the analog section is turned off and the supply current drops to 30μA. The voltage regulator, which provides power to the internal analog circuitry and external bias networks, is shut down. The voltage divider across the battery is disconnected and only the voltage regulator for the serial interface logic is left on.

During the idle mode, the chip is fully powered but the discharge, charge, and gas gauge circuits are off. The chip may be placed in the idle mode momentarily while charging the battery, allowing an ADC measurement to be made without any switching noise from the PWM current source affecting the accuracy of the reading. The mode command bits are picked off as they appear at D_{IN}, allowing the charging loop to turn off and settle while the remainder of the command word is being shifted in.

During the discharge mode, the battery is discharged by an external transistor and series resistor. The battery is monitored for fault conditions.

In the charge mode, the μP monitors the battery's voltage, temperature, and ambient temperature via the 10-bit ADC. Termination methods such as $-\Delta V_{BAT}$, $\Delta V_{BAT}/\Delta Time$, ΔT_{BAT}, $\Delta T_{BAT}/\Delta Time$, $\Delta(T_{BAT} - T_A)$, maximum temperature, maximum voltage and maximum charge time may be accurately implemented in software. The LTC1325 also monitors the battery for fault conditions.

In the gas gauge mode, the average voltage across the sense resistor can be measured to determine the average battery load current. The sense voltage is filtered by an RC circuit, multiplied by an inverting gain of four, then converted by the ADC. The μP can then accumulate the ADC measurements and do a time average to determine the total charge leaving the battery. The RC circuit consists of an internal 1k resistor R_F and an external capacitor C_F connected to the Filter pin.

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FUNCTIONAL DESCRIPTION

COMMAND WORD

The command word is 22 bits long and contains all the information needed to configure and control the chip. On power-up all bits are cleared to logical "0."

1	2	3	4	5	6	7	8
START	MOD0	MOD1	SGL/ DIFF	MSBF	D80	D81	D82

9	10	11	12	13	14	15	16
DIV0	DIV1	DIV2	DIV3	PS	DR0	DR1	DR2

17	18	19	20	21	22
FSCLR	TO0	TO1	TO2	VR0	VR1

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Figure 1. Command Word

Bit 1: Start Bit (Start)

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer and all leading zeros which precede this logical one will be ignored. After the start bit is received, the remaining bits of the command word will be clocked in.

START	DESCRIPTION
0	Wait
1	Start Reading Bits

Bits 2 and 3: Mode Select (MOD0 and MOD1)

The two mode bits determine which of four modes the chip will be in: idle, discharge, charge, or gas gauge.

MOD1	MOD0	DESCRIPTION
0	0	Idle
0	1	Discharge
1	0	Charge
1	1	Gas Gauge

Bit 4: Single-Ended Differential Conversion (SGL/DIFF)

SGL/DIFF determines whether the ADC makes a single-ended measurement with respect to ground or a differential measurement with respect to the Sense pin.

SGL/DIFF	DESCRIPTION
0	Single-Ended ADC Conversion
1	Differential ADC Conversion (with respect to Sense)

Bit 5: MSB-First/LSB-First (MSBF)

The ADC data is programmed for MSB-first or LSB-first sequence using the MSBF bit. See Serial I/O description for details.

MSBF	DESCRIPTION
0	LSB-First Data Follows MSB-First Data
1	MSB-First Data Only

Bits 6 to 8: ADC Data Input Select (DS0 to DS2)

DS0, DS1 and DS2 select which circuit is connected to the ADC input. Do not use unlisted combinations.

DS2	DS1	DS0	DESCRIPTION
0	0	0	Gas Gauge Output
0	0	1	T_{BAT} Pin
0	1	0	T_{AMB} Pin
0	1	1	Battery Cell Voltage, V_{CELL}
1	0	0	V_{IN} Pin

Bits 9 to 12: Battery Divider Ratio Select (DIV0 to DIV3)

DIV3, DIV2, DIV1 and DIV0 select the division ratio for the voltage divider across the battery.

DIV3	DIV0	DIV1	DIV0	DESCRIPTION
0	0	0	0	$(V_{BAT} - V_{SENSE})/1$
0	0	0	1	$(V_{BAT} - V_{SENSE})/2$
0	0	1	0	$(V_{BAT} - V_{SENSE})/3$
0	0	1	1	$(V_{BAT} - V_{SENSE})/4$
0	1	0	0	$(V_{BAT} - V_{SENSE})/5$
0	1	0	1	$(V_{BAT} - V_{SENSE})/6$
0	1	1	0	$(V_{BAT} - V_{SENSE})/7$
0	1	1	1	$(V_{BAT} - V_{SENSE})/8$
1	0	0	0	$(V_{BAT} - V_{SENSE})/9$
1	0	0	1	$(V_{BAT} - V_{SENSE})/10$
1	0	1	0	$(V_{BAT} - V_{SENSE})/11$
1	0	1	1	$(V_{BAT} - V_{SENSE})/12$
1	1	0	0	$(V_{BAT} - V_{SENSE})/13$
1	1	0	1	$(V_{BAT} - V_{SENSE})/14$
1	1	1	0	$(V_{BAT} - V_{SENSE})/15$
1	1	1	1	$(V_{BAT} - V_{SENSE})/16$

FUNCTIONAL DESCRIPTION

Bit 13: Power Shutdown (PS)

PS selects between the normal operating mode, or the shutdown mode.

PS	DESCRIPTION
0	Normal Operation
1	Shutdown All Circuits Except Digital Inputs

Bits 14 to 16: Duty Ratio Select (DR0 to DR2)

DR2, DR1 and DR0 select the duty cycle of the charging loop. The last three selections place the chip into a test mode and should not be used.

DR2	DR1	DR0	DESCRIPTION
0	0	0	1/16
0	0	1	1/8
0	1	0	1/4
0	1	1	1/2
1	0	0	1
1	0	1	Test Mode 1
1	1	0	Test Mode 2
1	1	1	Test Mode 3

Bit 17: Fail-Safe Latch Clear (FSCLR)

When FSCLR bit is set to one, the internal fail-safe timer is reset to 0, and the fail-safe latches are reset. FSCLR is automatically reset to 0 when $\overline{CS}$ goes high.

FSCLR	DESCRIPTION
0	No Action
1	Reset Fail-Safe Timer and Latches

Bits 18 to 20: Time-Out Period Select (TO0 to TO2)

TO2, TO1 and TO0 select the desired fail-safe time-out period. On power-up, the default time-out is 5 minutes.

TO2	TO1	TO0	TIME-OUT (MINUTES)
0	0	0	5
0	0	1	10
0	1	0	20
0	1	1	40
1	0	0	80
1	0	1	160
1	1	0	320
1	1	1	Indefinite (No Time-Out)

Bits 21 and 22: Charging Loop Reference Voltage Select (VR0 and VR1)

VR1 and VR0 select the desired reference voltage V_{CHRG} for the charging loop. The charging loop will force the average voltage at the Sense pin to be equal to V_{DAC}. The average charging current is V_{DAC}/R_{SENSE}.

VR1	VR0	V_{DAC} (mV)
0	0	15
0	1	30
1	0	50
1	1	150

STATUS WORD

The status word is 8 bits long and contains the status of the internal fail-safe circuits.

1	2	3	4	5	6	7	8
BATP	BATR	FMCV	FEDV	FHTF	FLTF	T_{OUT}	FS

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Figure 2. Status Word

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FUNCTIONAL DESCRIPTION

Bit 1: Battery Present (BATP)

The BATP bit indicates the presence of a battery. The bit is set to 1 when the voltage at the V_{BAT} pin falls 1.6V below V_{DD}.

BATP	CONDITIONS
0	$(V_{DD} - 1.8) < V_{BAT} < V_{DD}$
1	$V_{BAT} < (V_{DD} - 1.8)$

Bit 2: Battery Reversed (BATR) or Shorted

The BATR bit indicates when the battery is connected backwards or shorted. The bit is set when the battery cell voltage at the output of the battery divider V_{CELL} is below 100mV.

BATR	CONDITIONS
0	$V_{CELL} > 100mV$
1	$V_{CELL} < 100mV$

Bit 3: Maximum Cell Voltage (FMCV)

The MCV bit indicates when the battery cell voltage has exceeded the preset limit. The bit is set when V_{CELL} is greater than the voltage at the MCV pin.

FMCV	CONDITIONS
0	$V_{CELL} < V(MCV)$
1	$V_{CELL} > V(MCV)$

Bit 4: End Discharge Voltage (FEDV)

The EDV bit indicates when the battery cell voltage has dropped below an internally preset limit. The bit is set when the battery cell voltage at the output of the voltage divider V_{CELL} is less than 900mV.

FEDV	CONDITIONS
0	$V_{CELL} > 900mV$
1	$V_{CELL} < 900mV$

Bit 5: High Temperature Fault (FHTF)

The HTF bit indicates when the battery temperature is too high. Using a negative TC thermistor, the bit is set when the voltage at the T_{BAT} pin is less than the voltage at the HTF pin.

FHTF	CONDITIONS
0	$T_{BAT} > V(HTF)$
1	$T_{BAT} < V(HTF)$

Bit 6: Low Temperature Fault (FLTF)

The LTF bit indicates when the battery temperature is too low. Using a negative TC thermistor, the bit is set when the voltage at the TBAT pin is greater than the voltage at the LTF pin

FLTF	CONDITIONS
0	$T_{BAT} < V(LTF)$
1	$T_{BAT} > V(LTF)$

Bit 7: Time-Out (T_{OUT})

The T_{OUT} bit indicates that the battery charging time has exceeded the preset limit. The bit is set when the internal timer exceeds the limit set by the command bits TO0, TO1 and TO2.

T_{OUT}	CONDITIONS
0	No Time-Out Has Occurred
1	Time-Out Has Occurred

Bit 8: Fail-Safe Occurred (FS)

The FS bit indicates that one of the fault detection circuits halted the discharging or charging cycle. The bit is set when an EDV, LTF, HTF, or T_{OUT} fault occurs during discharge. During charging, the bit is set when a MCV, LTF, HTF, or T_{OUT} fault occurs. The bit is reset by the command word bit FSCLR.

FS	CONDITIONS
0	No Fail-Safe Has Occurred
1	Fail-Safe Has Occurred

FUNCTIONAL DESCRIPTION

DETAILED DESCRIPTION

Fault Conditions

The LTC1325 monitors the battery for fault conditions before and during discharge and charge (See Figure 3). They include: battery removed/present (BATP), battery reversed/shorted (BATR), maximum cell voltage exceeded (MCV), minimum cell voltage exceeded (EDV), high temperature limit exceeded (HTF), low temperature limit exceeded (LTF), and time limit exceeded (T_{OUT}). When a fault condition occurs, the discharge and charge loops are disabled or prevented from turning on and the fail-safe bit (FS) is set. The chip is reset by shifting in a new command word with the fail-safe clear FSCLR bit set. The 8-bit status word contains the state of each fault condition.

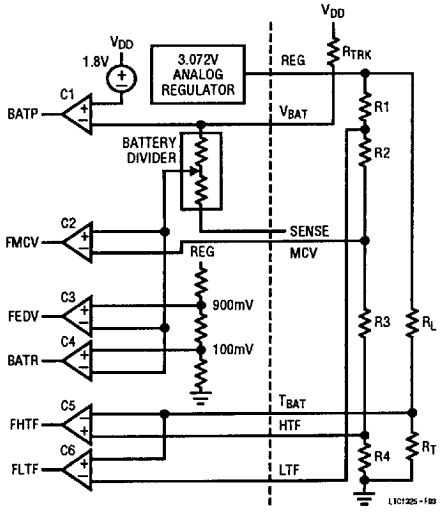

Figure 3. Fail-Safe or Fault Detection circuitry

Power Shutdown Mode

Command: MOD1 = X, MOD0 = X, PS = 1

Status: BATP = X, BATR = X, FMCV = X, FEDV = X, FHTF = X, FLTF = X, T_{OUT} = X

In the power shutdown mode, the analog section is turned off and the supply current drops to 30μA. The voltage regulator, which provides power to the internal analog circuitry and external bias networks, is shut down. The voltage divider across the battery is disconnected and the only circuit left on is the voltage regulator for the serial interface logic.

Idle Mode

Command: MOD1 = 0, MOD0 = 0, PS = 0

Status: BATP = X, BATR = X, FMCV = X, FEDV = X, FHTF = X, FLTF = X, T_{OUT} = X

The chip enters the idle mode when the proper mode command bits are set and the power shutdown command bit is cleared. During the idle mode, the chip is fully powered, but the discharge, charge, and gas gauge circuits are off. The chip may be placed in the idle mode momentarily while charging the battery, allowing an ADC measurement to be made without any switching noise from the PWM current source affecting the accuracy of the reading. The mode command bits are picked off as they appear at D_{IN}, so that while the rest of the command word is being shifted in, the charging loop has time to settle before an ADC measurement is made.

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FUNCTIONAL DESCRIPTION

Discharge Mode

Command: MOD1 = 0, MOD0 = 1, PS = 0

Status: BATP = 1, BATR = 0, FMCV = X, FEDV = 0, FHTF = 0, FLTF = 0, TOUT = 0

The chip enters the discharge mode when the proper mode command bits are set and the power shutdown command bit is clear. If a fault condition does not exist, then the DIS pin is pulled up to V_{DD} by the internal driver. The DIS voltage is used to turn on an external transistor which discharges the battery through an external series resistor R_{DIS}.

Discharging will continue until a new command word is input to change the mode or a fault condition occurs.

Charge Mode

Command: MOD1 = 1, MOD0 = 0, PS = 0

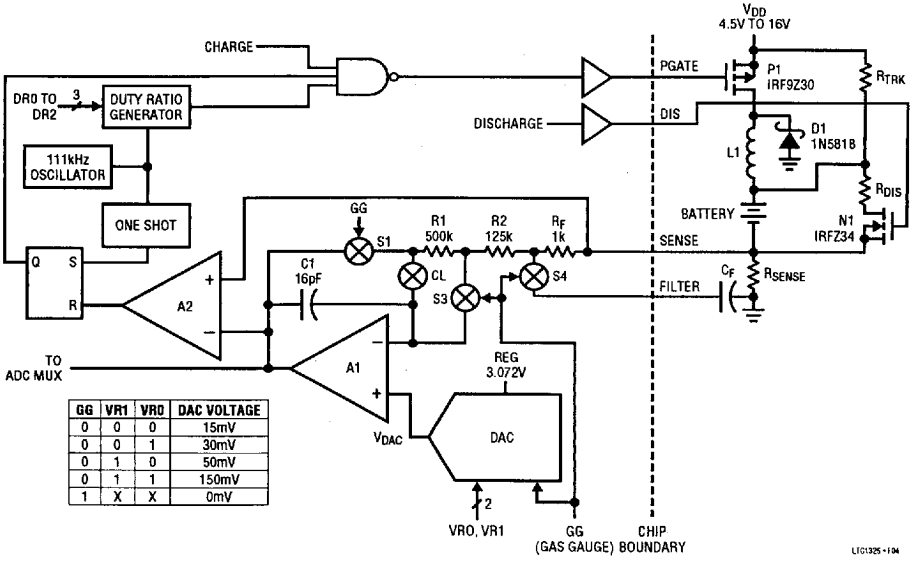
Status: BATP = 1, BATR = 0, FMCV = 0, FEDV = X, FHTF = 0, FLTF = 0, TOUT = 0

The chip enters the charge mode when the proper mode command bits are set and the power shutdown command bit is clear. If a fault condition does not exist then charging can begin. Charging will continue until a new command word is input to change the mode or a fault condition occurs.

The charge current may be regulated by a programmable 111kHz PWM buck current regulator, or by using the PFET to gate an external current regulator or current limited transformer.

111kHz PWM Controller

The block diagram of the charging loop connected as a PWM buck current regulator is shown in Figure 4. The PWM may operate in either continuous or discontinuous mode. The loop forces the average voltage across the sense resistor to be equal to the voltage at the output of the DAC, so that the charging current becomes V_{DAC}/R_{SENSE}.



GG	VR1	VR0	DAC VOLTAGE
0	0	0	15mV
0	0	1	30mV
0	1	0	50mV
0	1	1	150mV
1	X	X	0mV

Figure 4. Charging Loop Block Diagram

FUNCTIONAL DESCRIPTION

With switch S2 on and the others off, amplifier A1 along with C1, R1 and R2 are configured as an integrator with 16kHz bandwidth. The output of the integrator is the average difference between the voltage across the sense resistor and the DAC output voltage.

The rising edge of the oscillator waveform triggers the one shot which sets the flip-flop output high. This turns on the external PFET P1 by pulling its gate low via the FET driver. With P1 on, the current through the inductor L1 starts to rise as does the voltage across the sense resistor. When the voltage across the sense resistor is greater than the output of the integrator, comparator A2 changes state. This resets the flip-flop and P1 is turned off. Catch diode D1 clamps the drain of P1 one diode drop below ground when the inductor flies back and the current through the inductor starts to drop. The voltage across the sense resistor also drops and may reach zero and stay there until the next clock cycle begins.

The average charging current is set by the output of the DAC (V_{DAC}) and the duty cycle generator. V_{DAC} can be programmed to 150mV, 50mV, 30mV or 15mV. The duty cycle can be set to 1/16, 1/8, 1/4, 1/2 or 1. When the duty cycle is 1, the duty cycle generator output is always low and the charge loop operates continuously (see Figure 4). At other duty cycle settings, the duty generator output is a square wave with a period of 42 seconds. The time for which the generator output is low varies with the duty cycle setting. For example, if a duty cycle of 1/2 is programmed, the generator output is low only for 1/2×42 or 21 seconds. Since the loop operates for only 21 out of every 42 seconds, the average charging current is halved. In general, the average charging current is:

$$I_{CHRG} = V_{DAC} \times (\text{Duty Cycle})/R_{SENSE}$$

Gated PFET Controller

When using an external current regulator or current limited wall pack, simply remove the inductor L1 and catch diode D1. Set the DAC output voltage to 150mV and select the desired duty ratio. By insuring that the voltage at the Sense pin is never greater than 150mV, the output of the integrator A1 will saturate high, and the comparator A2 will never trip and turn the loop off. This can be achieved by removing the sense resistor and grounding the Sense pin or if the gas gauge is to be used, selecting R_{SENSE} so that $R_{SENSE}/I_{CHRG} < 150mV$.

Gas Gauge Mode

Command: MOD1 = 1, MOD0 = 1, PS = 0

Status: BATP = X, BATR = X, FMCV = X, FEDV = X, FHTF = X, FLTF = X, T_{OUT} = X

In the gas gauge mode, the average voltage across the sense resistor can be measured to determine the average battery load current. The output of the DAC is set to ground and switches S1, S3 and S4 are closed. A1 is configured as an inverting amplifier with R1 and R2 setting the gain to −4. The voltage across the sense resistor is filtered by an RC circuit (R_F, C_F) amplified by A1, then converted by the ADC.

The microprocessor can then accumulate the ADC measurements and do a time average to determine the total charge leaving the battery. The Sense pin voltage should not be more negative than −450mV to ensure linearity.

The R_FC_F circuit consists of an internal 1k resistor and an external capacitor connected to the Filter pin. R_FC_F should be longer than the measurement interval. With the serial clock running at 100kHz, it take 380µs to shift in the command word and shift out the ADC measurement and status word.

Trickle Resistor

An external trickle resistor has several functions. First, it provides a continuous trickle charge current for topping off the battery and countering the effects of self-discharge. Second, it can be used to condition a deeply discharged battery for charging. The LTC1325 will not charge a battery unless its cell voltage is above 100mV (BATR). Finally, the resistor is required by the battery detect circuit to pull the V_{BAT} pin high when the battery is removed.

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FUNCTIONAL DESCRIPTION

SERIAL INTERFACE

The LTC1325 communicates with microprocessors and other external circuitry via a synchronous, half duplex, 4-wire serial interface. The clock CLK synchronizes the data transfer with each bit being transmitted on the falling edge and captured on the rising CLK edge in both transmitting and receiving systems. The LTC1325 first receives input data and then transmits back the A/D conversion result and status word (half duplex). Because of the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just three wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}).

Data transfer if initiated by a falling chip select $\overline{CS}$ signal. After $\overline{CS}$ falls, the LTC1325 looks for a start bit on D_{IN}. The start bit is the first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low. The LTC1325 will ignore all leading zeros which precede this logical one. After the start bit is received, a 22-bit input word is shifted into the D_{IN} input which configures the LTC1325 and starts a conversion. After one null bit, the result of the conversion is output on the D_{OUT} pin followed by 8 status bits. At the end of the data exchange, $\overline{CS}$ should be brought high.

MSB-First/LSB-First (MSBF Control Bit)

The output data of the LTC1325 is programmed for MSB-first or LSB-first sequence using the MSFB control bit. When MSBF = 1, data will appear on D_{OUT} in MSB-first format. This is followed by the 8 status bits. Logical zeros will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When MSBF = 0, LSB-first data will follow the MSB-first data. Regardless of the state of MSBF, the status bits are always shifted out in the same order (see Figure 2).

Accommodating Microprocessors with Different Word Lengths

The LTC1325 will fill zeros indefinitely after the transmitted data until $\overline{CS}$ is brought high. At that time D_{OUT} is disabled (three-stated). This makes for easy interfacing to MPU serial ports with different transfer increments including 4 bits (e.g., COP400) and 8 bits (e.g., SPI and MICROWIRE/PLUS). Any word length can be accommodated by the correct positioning of the start bit in the input word.

Operation with D_{IN} and D_{OUT} Tied Together

The LTC1325 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate with the microprocessor. Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1325 will take control of the dataline and drive it low after the 23rd falling CLK edge after the start bit is received. Therefore the processor port must be switched to an input before this happens to avoid a conflict.

Power-Up After Shutdown

When a control word with the PS bit set to one is written to the LTC1325, it enters shutdown mode in which the V_{DD} supply current is reduced to 30μA. In this mode the on-chip 3V regulator and all circuits powered off it are shut down. The only circuits that remain alive are D_{IN}, $\overline{CS}$ and CLK input buffers. To take the LTC1325 out from shutdown mode, a high to low edge must be applied to the $\overline{CS}$ pin. Either D_{IN} or CLK must be low when $\overline{CS}$ is low to prevent a false control word from being transmitted to the LTC1325. The 3V output decays with a time constant of 300ms with C_{REG} = 4.7μF. The microprocessor should wait three seconds before applying a wake-up edge to the $\overline{CS}$ pin to ensure proper power-up.

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APPLICATIONS INFORMATION

TEMPERATURE SENSING

NTC (Negative Temperature Coefficient) Thermistors

The simplest method to sense temperature (battery or ambient) with an NTC thermistor is to use a voltage divider powered by the REG pin. This divider consists of a load resistor R_L in series with a thermistor R_T as shown in Figure 3. For a given thermistor, there is a value of R_L which makes V_{DIV} (T) linear over a narrow but adequate temperature range. The easiest method (Inflection Point Method) to calculate R_L is to set the second temperature derivative of the divider output to 0. The equations relevant to this method are:

$$\frac{V_{DIV}(T)}{V_{REG}} = \frac{1}{\left(\frac{1+R_L}{R_T}\right)} = f(T) \quad (1)$$

$$\frac{R_T}{R_{TO}} = \exp\left[\beta \times \left(\frac{1}{T} - \frac{1}{T_O}\right)\right] \quad (2)$$

$$R_L = R_{TO} \times \frac{\beta - 2T_O}{\beta + 2T_O} \quad (3)$$

$$\beta = \left[T \times \frac{T_O}{T_O - T}\right] \times \ln\left(\frac{R_T}{R_{TO}}\right) \quad (4)$$

$$\alpha = \frac{1}{R_T} \times \frac{dR_T}{dT} \quad (5)$$

$$\alpha = \frac{-\beta}{T^2} \quad (6)$$

$$\frac{dV_{DIV}}{dT} = V_{DIV}(T_O) \times \left(-\frac{-\beta}{2T_O^{\,2}} + \frac{1}{T_O}\right) \quad (7)$$

where,

V_{DIV} (T) is the output of the divider,

V_{REG} is the voltage at the REG pin (3.072V nominal),

R_T is the thermistor resistance at some temperature T,

R_{TO} is the thermistor resistance at some reference temperature T_O,

β is a constant dependent on thermistor material,

α is the temperature coefficient (in %/°C) of R_T at T_O, and

all temperatures are in °K (i.e., T°C + 273)

There are two assumptions in the derivation of the above equations. β is assumed to be constant and the temperature coefficient of R_L is small compared to that of the thermistor.

Most thermistor data sheets specify R_{TO}, β, R_T/R_{TO} ratios for two temperatures, α, and tolerances for β and R_{TO}. Given β, and R_{TO}, it is easy to calculate R_L from equation (3). Alternatively, β may be calculated from the R_T/R_{TO} ratio using equation (4) or from α, using equation (6).

As a numerical example, consider the Panasonic ERT-D2FHL103S thermistor which has the following characteristics:

1. R_T (25°C) = R_{TO} = 10k
2. α = −4.6%/°C at T_O = 25°C
3. Ratio R_{25}/R_{50} = 2.9

Using equation (4), and R_{25}/R_{50} = 2.9, $\beta = (323 \times 298) \times \ln(2.9)/(298-323) = 4099$K. Alternatively, using equation (6) and $\alpha = -4.6\%/°C$, $\beta = -(-0.046) \times (298)^2 = 4085$K.

Both values of β are close to each other. Substituting β = 4085K into equation (3) gives R_L = 10k × [4085 − (2 × 298)]/[4085 + (2 × 298)] = 7.45k. The nearest 1% resistor value is 7.5k. Figure 5 shows a plot of V_{DIV}(T) measured at various temperatures for this thermistor with a 7.5k R_L.

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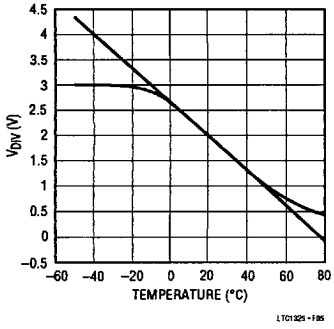

Figure 5. ERT-D2FHL103S Divider

There are two methods of calculating battery or ambient temperature from ADC readings of the T_{BAT} or T_{AMB} channels. The first method is to store the $V_{DIV}(T)$ vs T curve as a lookup table. The second method is to use a straight line approximation. The equation of this line may be calculated from the slope dV_{DIV}/dT at T_O [see equation (7)] and assuming that the line passes through the point $[T_O, V_{DIV}(T_O)]$ on the curve. For the ERT-D2FHL103S, the slope is minus 34mV/°C and the equation of the line is $T = [2.605 - V_{DIV}(T)]/0.034$. The straight line approximation is accurate to within 2°C over a temperature range of 5°C to 45°C, assuming a 3% β and 10% R_{TO} tolerances.

PTC (Positive Temperature Coefficient) Thermistors

Positive Temperature Coefficient (PTC) thermistors may be used in battery chargers that do not require accurate temperature measurements. The resistance vs temperature characteristics of PTC exhibits a sharp increase at a selectable switch temperature T_S. This sharp change is exploited in chargers which use TCO (Temperature Cutoff) or ΔTCO (Difference between battery and ambient temperature). With TCO termination, a voltage divider consisting of a PTC and a low temperature coefficient load resistor is connected between REG and GND with the top end of the PTC at REG. The PTC is mounted on the battery to sense its temperature. The divider output is tied to T_{BAT}. When the switch temperature is reached, the PTC resistance increases sharply causing T_{BAT} to fall below HTF. This causes an HTF fault and charging is terminated. To implement ΔTCO termination the load resistor can be replaced by a matching PTC and the divider now responds to differences between battery and ambient temperature. With both TCO and ΔTCO terminations, the position of the battery temperature PTC can be swapped with the load resistor or ambient temperature PTC. In both cases, an LTF fault terminates charge when the trip point is reached.

HARDWARE DESIGN PROCEDURE

This section discusses the considerations in selecting each component of a simple battery charger (see Figures 3 and 4).

1. R_{SENSE}

There are three factors in selecting R_{SENSE}:

a. LTC1325 V_{REF} and Duty Ratio Settings

b. Sense Resistor Dissipation

c. $I_{LOAD} \times R_{SENSE} < -450mV$ for Gas Gauge Linearity

The LTC1325 has five duty ratio and four V_{REF} settings giving 20 possible charge rates (for a given value of R_{SENSE}) as shown in the following table. For any combination of V_{DAC} and duty ratio, the average charging current is given by:

$$AVG\ I_{CHRG} = V_{DAC} \times (\text{Duty Ratio})/R_{SENSE}$$

	DUTY RATIO				
V_{REF}	1	1/2	1/4	1/8	1/16
150mV (1)	1	1/2	1/4	1/8	1/16
50mV (1/3)	1/3	1/6	1/12	1/24	1/48
30mV (1/5)	1/5	1/10	1/20	1/40	1/80
15mV (1/10)	1/10	1/20	1/40	1/80	1/160

Note that in the table, the 150mV, 100% duty ratio entry is given a weighting of 1. For a battery charged at 1C rate with V_{REF} of 150mV and 100% duty ratio, the charge rate (in C-units) for other V_{REF} and duty ratio combinations can be read straight off the table. For a battery charged at 4C rate at 150mV, 100% duty ratio, all entries should be multiplied by 4 and so on. In general, V_{REF} and duty ratio settings are changed by the microprocessor to charge batteries of different capacities or to alter charge rates when charging the same battery in several stages. For best accuracy, V_{REF} should be set to 150mV where possible.

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The power dissipation of the sense resistor varies between charge, discharge and gas gauge modes and should be calculated for all three modes. Typically, dissipation is higher in discharge and gas gauge modes since batteries can deliver higher currents than they can be charged with.

In gas gauge mode, the load current supplied by the battery should not exceed $450mV/R_{SENSE}$ for the gas gauge to remain linear in response. R_{SENSE} should be low enough to ensure that $I_{LOAD} \times R_{SENSE}$ does not fall below ground by 1 diode drop.

2. V_{DD} Supply

The minimum V_{DD} supply must be greater than the end-of-charge voltage V_{EC} times the number of cells (n) in the battery plus drops across the on-resistance of the PFET, inductor (V_L), battery internal resistance R_{INT} and sense resistor R_{SENSE}.

$$\text{Min } V_{DD} = I_{CHRG} \times [R_{DS(ON)}(P1) + R_{SENSE} + n \times R_{INT}] + n \times V_{EC} + V_L$$

Assuming $V_{EC} = 2V$, the LTC1325 will charge up to 8 cells with a 16V supply. For a higher number of cells, an external level shifter and regulator are needed.

3. Inductor L

To minimize losses, the inductor should have low winding resistance. It should be able to handle expected peak charging currents without saturation. If the inductor saturates, the charging current is limited only by the total PFET $R_{DS(ON)}$, inductor winding resistance, R_{SENSE} and V_{DD} source resistance. This fault current may be high enough to damage the battery or cause the maximum power ratings of the PFET, inductor or R_{SENSE} to be exceeded.

4. Catch Diode D1

The catch diode should have a low forward drop and fast reverse recovery time to minimize power dissipation. Total power loss is given by:

$$P_{dD1} = V_F \times I_F + V_R \times f \times t_{RR} \times I_F'$$

where

I_F = forward diode current,

I_F' = forward diode current just prior to turn-off,

V_F = forward drop,

V_R = reverse diode voltage (approximately equal to V_{DD}),

f = PWM frequency (111kHz), and

t_{RR} = reverse recovery time

The power and maximum reverse voltage ratings of the diode should be greater than P_{dD1} and V_{DD} respectively. The catch diode should also have fast turn-on times to reduce the voltage glitch at its cathode when turning on.

Schottky diodes have fast switching times and low forward drops and are recommended for D1.

5. Trickle Resistor R_{TRK}

R_{TRK} sets the desired trickle current in the battery to compensate for self-discharge which is in the order 1% and 2% of capacity per day for NiCd and NiMH batteries respectively. Trickle charge rates are typically in the C/30 to C/50 range, where C is battery capacity.

$$I_{TRK} = (V_{DD} - V_{BAT})/R_{TRK}$$

where V_{BAT} is the voltage of a full charged battery. Note that I_{TRK} varies as the battery is being charged.

6. Thermistor R_{THERM} and Load R_L

The total resistance of the thermistor network should be greater than 30k at the high temperature extreme to minimize effects of load regulation (see REG pin loading).

7. Fault Setting Resistors R1, R2, R3 and R4

The voltage levels at the LTF, HTF and MCV pins are tapped from a resistor divider powered by the REG pin. The voltage levels are selected taking into account:

a. Manufacturer Recommended Temperature and Voltage limits,

b. Loading on the REG Pin (< 2mA)

c. Input Voltage Ranges of the LTF, HTF and MCV Comparators:

$1.6V < V_{LTF}, V_{MCV} < 2.8V$ and
$0.5V < V_{HTF} < 1.3V$

d. Thermistor Divider Temperature Curve

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Typical temperature limits for both NiCd and NiMH batteries are shown below.

BATTERY TYPE	DISCHARGE TEMP RANGE (°C)		DISCHARGE TEMP RANGE (°C)	
	MIN	MAX	MIN	MAX
Standard	−20	45/50	0	45/50
Quick	−20	45/50	10	45/50
Fast or Rapid	−20	45/50	15	45/50
Trickle	−20	45/50	0	45/50

Note that the discharge limits are wider than the charge limits. To prolong battery life, manufacturers generally recommend discharge temperatures that are similar to the charge limits. For this reason, the LTC1325 recognizes the same LTF and HTF limits in both charge and discharge modes. MCV should be set just above the charging voltage per cell given in battery specifications. The voltage at the LTF and HTF pins should be set to correspond to narrowest temperature range. These are typically 15°C and 45°C. The corresponding voltages may be read from the thermistor divider temperature curve such as that shown in Figure 5. For this thermistor, it works out to be about for 2.12V for LTF and for 1.13V for HTF. The MCV may be conveniently tied to LTF since MCV is typically 2V. If desired, external analog switches under microprocessor control may be used to vary the LTF, HTF and MCV voltages between modes or for different charge rates. The values of R1, R2, R3 and R4 in Figure 3 can be calculated from the following equations:

$$R4 = V(HTF) \times RE/V_{REG}$$

$$R3 = V(MCV) \times RE - R4$$

$$R2 = V(LTF) \times RE - (R3 + R4)$$

$$R1 = RE - (R2 + R3 + R4)$$

where RE = R1 + R2 + R3 + R4 is chosen to minimize loading on the REG pin. A minimum value of 30k is recommended. Note that V(LTF) is assumed to be greater than V(MCV). If this is not the case, V(LTF) and V(MCV) in the above equations should be swapped. If the MCV and LTF pins are shorted to the same point, R2 should be set to 0.

8. REG Pin Loading

The 3.072V regulator has a load regulation specification of −5mV/mA. Since the ADC uses the same regulator as reference, it is desirable to reduce loading effects on the REG pin especially over temperature. Thermistors with R_{TO} values of at least 10k at 25°C are recommended. At 50°C, the thermistor resistance could drop by a factor of 3 from its value at 25°C. R_L is chosen as explained in the section on Temperature Sensing. The temperature coefficient of R_L is not critical since the thermistor tempco dominates the sensing circuit.

9. R_{DIS}

R_{DIS} is selected to limit the discharge current to a value within the battery discharge specifications and must have a power rating above $I_{DIS}^2 \times R_{DIS}$ where:

$$I_{DIS} = V_{BAT}/[R_{DIS} + R_{DS(ON)}(N1)]$$

10. PFET(P1) and NFET(N1)

For operation of the charge and discharge loops, $|V_{GS}| < V_{DD}$ since the PGATE and DIS pins swing between 0 and V_{DD}. $|V_{GS}| \ll V_{DD}$ to minimize power dissipation. The power ratings of P1 and N1 should be above $I_{CHRG}^2 \times R_{DS(ON)}(P1)$ and $I_{DIS}^2 \times R_{DS(ON)}(N1)$ respectively. $V_{DS(MAX)}$ should be above V_{DD}.

Charging From Supplies Above 16V

In many applications, the charging supply is greater than the 16V maximum V_{DD} rating of the LTC1325. The LTC1325 can easily be adapted to charge the batteries from a charging supply (V_{DC}) above 16V by adding 3 external sub-circuits:

1) A regulator to drop V_{DC} down to within the supply range of the LTC1325.
2) A level shifter between the PGATE and the gate of the PFET, P1, to ensure that P1 can be completely turned offwhen PGATE rises to V_{DD}.
3) A voltage clamp on the V_{BAT} pin to prevent R_{TRK} from pulling V_{BAT} above V_{DD}.

The Typical Application circuit on page 1 shows low cost implementations of all 3 sub-circuits. C1, R7 and D4 generate a 15V V_{DD} for the LTC1325. D3 and C2 form a level shifter. The zener D3 is chosen to clamp the source-gate voltage of the PFET to within the maximum gate-source voltage rating of the latter. Finally, D5 clamps V_{BAT} to 15V.

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APPLICATIONS INFORMATION

Charging Batteries With Voltages above 16V

To charge a battery with a maximum (fully charged) voltage of above 16V, the charging supply V_{DC} must be above 16V. Thus the charger will need the regulator, level shifter and clamp mentioned in the previous section. In addition, an external battery divider must be added to limit the voltage at the V_{BAT} pin to less than V_{DD}. This is shown in the Typical Application circuit on page 1. The resistors R9 and R10 are selected to divide the battery voltage by the number of cells in the battery and the battery divider internal to the LTC1325 is set to divide -by-1. The external divider prevents V_{BAT} from ever rising to V_{DD} and this causes the B_{ATP} (Battery Present Flag) to be high regardless of whether the battery is physically present or not. This does not affect the other operations of the LTC1325.

SOFTWARE DESIGN

A general charging algorithm consists of the following stages:

Discharge Before Charge

Fast Charge

Top Off Charge

Trickle Charge

Under some operating conditions, NiCd and NiMH batteries may not provide full capacity. Examples are repeated shallow charge and discharge cycles which causes the "memory effect" in NiCd batteries and long term storage at high temperatures. In order to restore full capacity (battery conditioning), these batteries have to be subjected to several deep discharge/charge cycles which will be provided by repetitions of the above algorithm.

Figure 6 shows a simplified flowchart of a charging algorithm. In practice, this flowchart has to be augmented to take into account the occurrence of fail-safes at any point in the algorithm. For example, the battery temperature could rise above HTF during discharging or charging. Table 1 shows the corresponding command word the microprocessor sends to the LTC1325 in each step of the flowchart. General programming notes are as follows:

1. The start bit is always high.
2. The SGL/DIFF bit is generally set to low so that the ADC makes conversions with respect to ground.
3. The MSBF bit is set depending on whether the microprocessor clocks in serial data with MSB- or LSB-first.
4. The DS0 to DS2 bits can be anything except when entering idle mode or when requesting for ADC readings. In these cases, DS0 to DS2 are set to select the desired reading: T_{BAT}, V_{CELL} or T_{AMB}.
5. The PS bit should always be 0 so that the LTC1325 does not go into shutdown mode.
6. The DR0 to DR2 should not select any of the test modes. It may assume different settings between Fast charge and Top Off charge in order to alter the charging current.
7. The FSCLR bit should be set to 1 to clear any faults and reset the timer when starting Discharge, Fast charge or Top Off. The status bits that the LTC1325 returns during the same I/O operation (that FSCLR is set to 1) should be checked to determine if faults were indeed cleared, i.e., discharging or charging has begun. This is not shown in the simplified flowchart of Figure 6. For commands other than the START commands, FSCLR should be set to 0 so as not to reset the timer.
8. The TO0 to TO2 bits should all be set to 1 in discharge mode to ensure discharge does not end prematurely due to a time-out fault. During Fast charge or Top Off charge, these bits are set to a value suitable for the charge rate used. For example, if the charge rate is 1C, the time-out period should be set to 80 minutes.
9. In charge mode, the C_F capacitor filters the V_{CELL} node and sees a small ripple due to ripple at the Sense pin. Prior to taking an ADC reading, the LTC1325 is put in idle mode to minimize noise. The microprocessor should either disregard readings or wait for a second or so before taking a reading. This is to allow V_{CELL} to decay to the correct cell voltage. The worst case time constant is $150k\Omega \times C_F$.
10. Prior to the first START command, the battery divider setting may be incorrect so that C_F may charge to a voltage that causes EDV, BATR or MCV faults. The worst case time constant is as in (9). The microprocessor should check faults during the transmission of a START command and resend the START command again when C_F has been given enough time to charge up to the correct value.

LINEAR TECHNOLOGY

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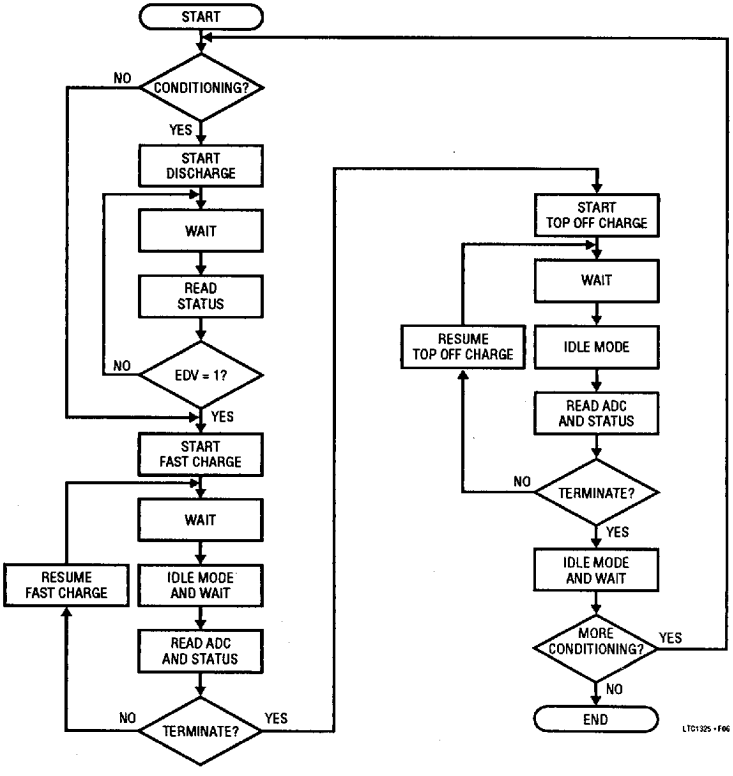


Figure 6. Simple Charging Algorithm

APPLICATIONS INFORMATION

Table 1. Commands for Flowchart in Figure 6

		COMMAND WORD																						
NO	STEP	START	MOD1	MOD0	SGL/DIFF	MSBF	DS0	DS1	DS2	DIV0	DIV1	DIV2	DIV3	PS	DR0	DR1	DR2	FSCLR	TO0	TO1	TO2	VR0	VR1
1	Start Discharge	1	1	0	0	m	x	x	x	b	b	b	b	0	?	?	?	1	1	1	1	x	x
2	Read Status	1	1	0	0	m	x	x	x	b	b	b	b	0	?	?	?	0	1	1	1	x	x
3	Start Fast Charge	1	0	1	0	m	x	x	x	b	b	b	b	0	d1	d1	d1	1	t1	t1	t1	v1	v1
4	Idle Mode and Wait	1	0	0	0	m	c	c	c	b	b	b	b	0	d1	d1	d1	0	t1	t1	t1	v1	v1
5	Read ADC and Status	1	0	0	0	m	c	c	c	b	b	b	b	0	d1	d1	d1	0	t1	t1	t1	v1	v1
6	Resume Fast Charge	1	0	1	0	m	x	x	x	b	b	b	b	0	d1	d1	d1	0	t1	t1	t1	v1	v1
7	Start Top Off Charge	1	0	1	0	m	x	x	x	b	b	b	b	0	d2	d2	d2	1	t2	t2	t2	v2	v2
8	Idle Mode and Wait	1	0	0	0	m	c	c	c	b	b	b	b	0	d2	d2	d2	0	t2	t2	t2	v2	v2
9	Read ADC and Status	1	0	0	0	m	c	c	c	b	b	b	b	0	d2	d2	d2	0	t2	t2	t2	v2	v2
10	Resume Top Off Charge	1	0	1	0	m	x	x	x	b	b	b	b	0	d2	d2	d2	0	t2	t2	t2	v2	v2

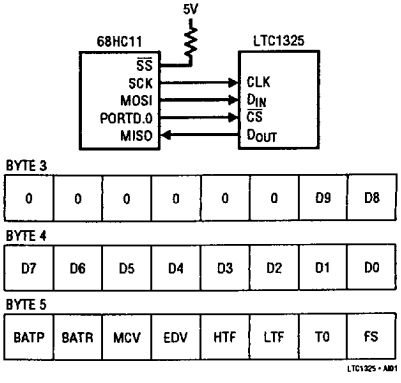
Note: c refers to one of the ADC channels (TBAT, T_A, V_{CELL}), b is the battery divider ratio, d1 is the duty ratio for Fast charge, d2 is the duty ratio for Top Off charge, t1 is the timout for Fast charge, t2 is the timout for Top Off charge, v1 is the V_{REF} setting for Fast charge, v2 is the V_{REF} setting for Top Off charge.

MICROPROCESSOR INTERFACES

The LTC1325 can interface directly to either synchronous, serial or parallel I/O ports of most popular microprocessors. With a parallel port, 3 or 4 I/O lines can be programmed to form a serial link to the LTC1325.

Motorola SPI (68HC11)

The 68HC11 has a dedicated synchronous serial interface called the Serial Peripheral Interface (SPI) which transfers data with MSB-first and in 8-bit increments. To communicate with this microprocessor, the LTC1325 MSBF control bit should be set to 1. The SPI has 4 lines: Master In Slave Out (MISO), Master Out Slave In (MOSI), Serial Clock (SCK) and Slave Select ($\overline{SS}$). The 68HC11 is configured as a Master by tying the $\overline{SS}$ line high. A control byte is written to the Serial Peripheral Control Register to select master mode, set baud rate and clock timing relationship. Another byte is written to the Port D Direction Register to set MOSI, SCK and bit 0 ($\overline{CS}$ of LTC1325) as outputs. The 68HC11 clocks in data from the LTC1325 simultaneously under the control of SCK. The microprocessor transmits the LTC1325 command word in 3 bytes. This is followed by 2 more dummy bytes (with all bits set low) in order to clock in the remaining LTC1325 ADC and status bits.



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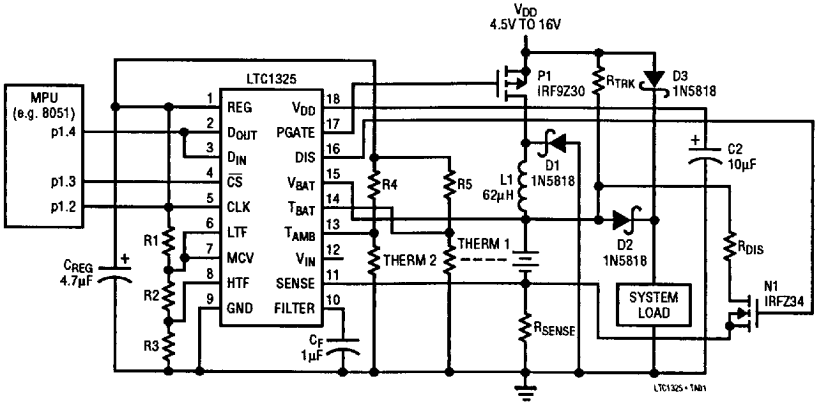
LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#01010101B	Write control byte to the SPCR
	STAA	$1028	
	LDAA	#00100001B	Setup Port D
	STAA	$1009	
	LDX	#$1000	Base adress of SPI registers
MSBF1	BCLR	$08,#0	Take $\overline{CS}$ low
	LDAA	#$00	Send Byte 1 (MSB)
	STAA	$102A	
LOOP1	TST	$1029	
	BPL	LOOP1	
	LDAA	#$FF	Send Byte 2
	STAA	$102A	
LOOP2	TST	$1029	
	BPL	LOOP2	
	LDAA	#$00	Send Byte 3
	STAA	$102A	
LOOP3	TST	$1029	
	BPL	LOOP3	
	LDAA	#$FF	Send Byte 4 (dummy)
	STAA	$102A	
LOOP4	TST	$1029	
	BPL	LOOP4	
	LDAA	#$FF	Send Byte 5 (dummy)
	STAA	$102A	
LOOP5	TST	$1029	
	BPL	LOOP5	
	BSET	$08,X,#01	Take $\overline{CS}$ high
	END	MSBF1	End of MSBF = 1 code

TYPICAL APPLICATION