DALLAS SEMICONDUCTOR

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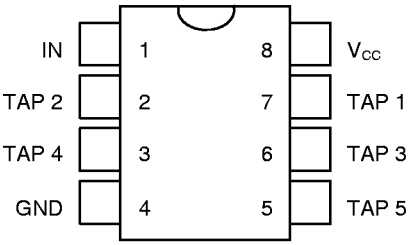
DS1100
5-Tap Economy Timing Element (Delay Line)

FEATURES
- All-silicon timing circuit
- 5-taps equally spaced
- Delays are stable and precise
- Both leading and trailing edge accuracy
- Improved replacement for DS1000
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Fast turn prototypes
- Delays specified over both commercial and industrial temperature ranges

PIN ASSIGNMENT



DS1100M 8-PIN DIP (300 MIL)
DS1100Z 8-PIN SOIC (150 MIL)
DS1100U 8-PIN MICRO-SOP

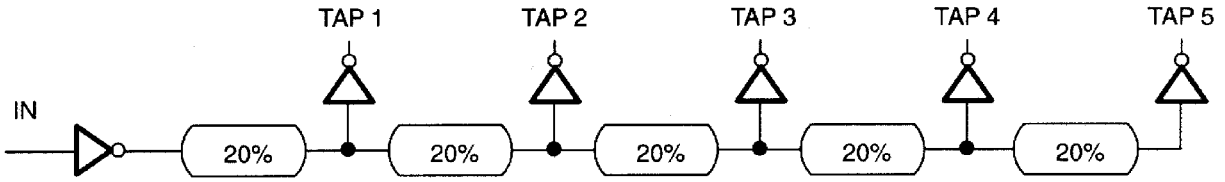
PIN DESCRIPTION

TAP 1-TAP 5	- TAP Output Number
V_{CC}	- +5 Volts
GND	- Ground
IN	- Input

DESCRIPTION
The DS1100 series delay lines have five equally spaced taps providing delays from 4 ns to 300 ns. These devices are offered in 8-pin DIPs and surface mount packages to save PC board area. Low cost and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. The DS1100 5-Tap Silicon Delay Line reproduces the input logic state at the output after a fixed delay as specified by the extension of the part number after the dash. The DS1100 is designed to reproduce both leading and trailing edges with equal precision. Each tap is capable of driving up to ten 74LS loads.

Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (972) 371-4348.

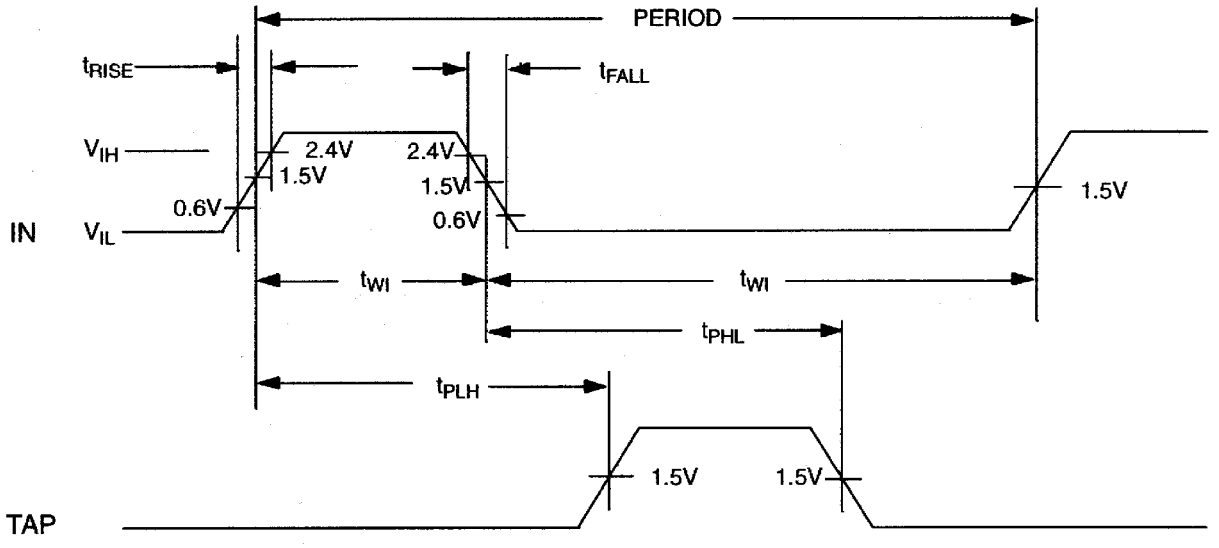
LOGIC DIAGRAM Figure 1



DS1100 PART NUMBER DELAY TABLE (all values in ns) Table 1

PART # DS1100	NOMINAL DELAYS				
	TAP 1	TAP 2	TAP 3	TAP 4	TAP 5
-20	4	8	12	16	20
-25	5	10	15	20	25
-30	6	12	18	24	30
-35	7	14	21	28	35
-40	8	16	24	32	40
-45	9	18	27	36	45
-50	10	20	30	40	50
-60	12	24	36	48	60
-75	15	30	45	60	75
-100	20	40	60	80	100
-125	25	50	75	100	125
-150	30	60	90	120	150
-175	35	70	105	140	175
-200	40	80	120	160	200
-250	50	100	150	200	250
-300	60	120	180	240	300

TIMING DIAGRAM: SILICON DELAY LINE Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	5
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	5
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	5
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC}=Max; Period=Min.		30	50	mA	6, 8
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}		20% of Tap 5 t_{PLH}			ns	
Input-to-Tap Delay Tolerance (Delays ≤ 40 ns)	t_{PLH} t_{PHL}	25°C 5V	-2	Table 1	+2	ns	1, 3, 4, 7
		0°C to 70°C	-3	Table 1	+3	ns	1, 2, 3, 4, 7
		-40°C to +85°C	-4	Table 1	+4	ns	1, 2, 3, 4, 7
Input-to-Tap Delay Tolerance (Delays > 40 ns)	t_{PLH} t_{PHL}	25°C 5V	-5	Table 1	+5	%	1, 3, 4, 7
		0°C to 70°C	-3	Table 1	+3	%	1, 2, 3, 4, 7
		-40°C to +85°C	-8	Table 1	+8	%	1, 2, 3, 4, 7
Power-up Time	t_{PU}				200	us	
Input Period	Period	$2(t_{WI})$				ns	

CAPACITANCE (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. Initial tolerances are ± with respect to the nominal value at 25°C and 5V for both leading and trailing edge.

2. T & V tolerance is with respect to the actual measured (at 25° C and 5V) delay value over the stated temperature range, and a supply voltage range of 4.75 to 5.25V.

3. All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP 1 slows down, all other taps also slow down; TAP3 can never be faster than TAP2.

4. Intermediate delay values are available on a custom basis. For further information, call (972) 371-4348.

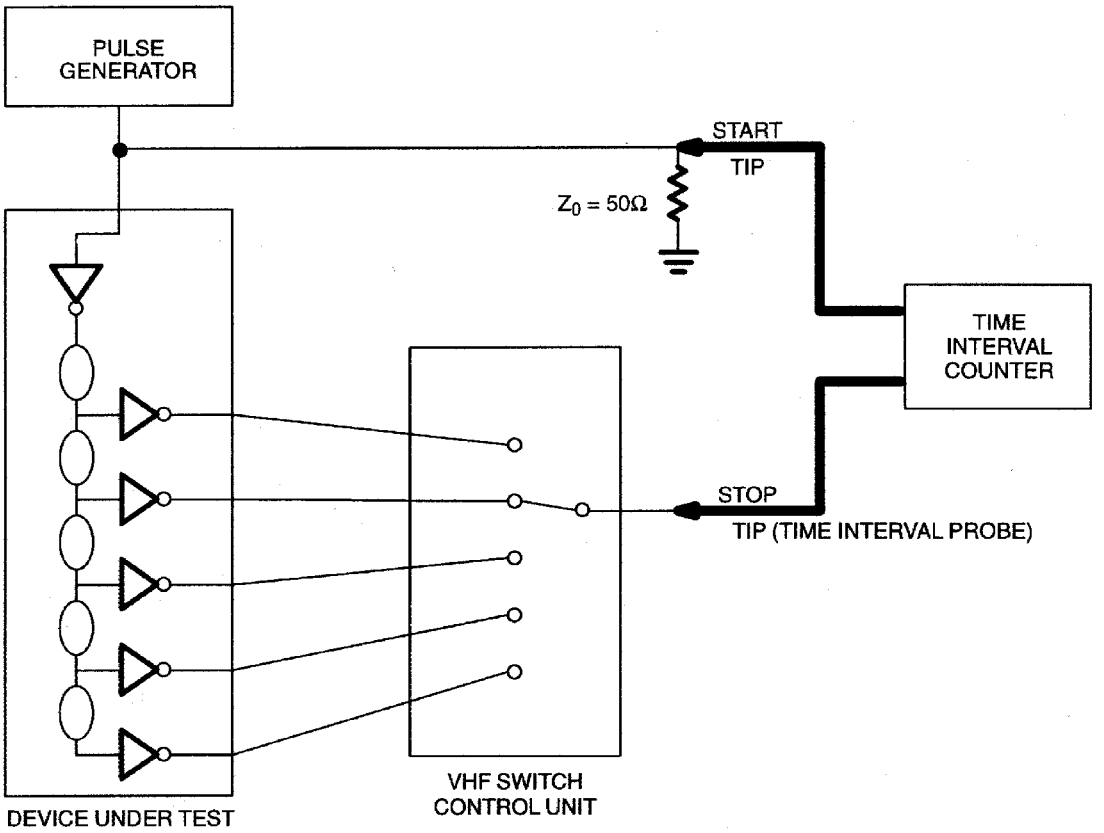
5. All voltages are referenced to ground.

6. Measured with outputs open.

7. See "Test Conditions" section at the end of this data sheet.

8. I_{CC} values apply to a -20 operating at 1MHz. Longer delays will consume less current.

TESTCIRCUIT Figure 3



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1100. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS INPUT :

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 Ohm Max.
Rise and Fall Time:	3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width:	500 ns
Period:	1 µs

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

ORDERING INFORMATION