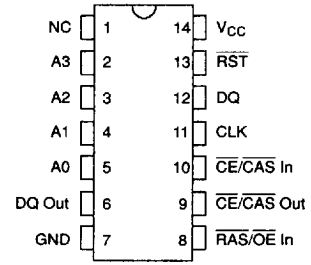
DALLAS SEMICONDUCTOR

DS1206
Phantom Serial Interface Chip

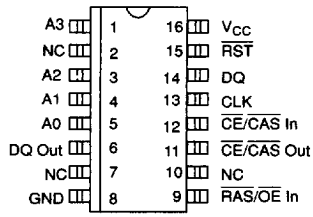
FEATURES

- Minimum expense add-on serial port
- Converts standard bytewide or DRAM memory waveforms into a 3-wire serial port
- Operation is transparent to memory
- Software-generated memory cycles activate serial port and transfer data
- High bandwidth – 1-bit data transfer per two memory cycles
- Intercepts memory signals so that pass-through connections to memory can be maintained
- Controls communications for as many as ten DS1201 Electronic Tags, DS1204U Electronic Keys, DS1207 TimeKeys or DS1290 Eliminators
- Low-power CMOS circuitry
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



14-Pin DIP (300 MIL)
See Mech. Drawing Pg. 480



16-Pin SOIC (300 MIL)
See Mech. Drawing Pg. 484

PIN DESCRIPTION

NC	–	No Connection
A0–A3	–	Memory Address Bus
DQ Out	–	Data Out To Memory Bus
GND	–	Ground
$\overline{RAS}/\overline{OE}$ In	–	Output Enable or $\overline{RAS}$ input from memory bus
$\overline{CE}/\overline{CAS}$ In	–	Chip enable or $\overline{CAS}$ from memory bus
$\overline{CE}/\overline{CAS}$ Out	–	Chip enable or $\overline{CAS}$ to memory circuit
CLK	–	Clock for Serial Port
DQ	–	Data I/O for Serial Port
$\overline{RST}$	–	Reset for Serial Port
V_{CC}	–	+5 Volts

DESCRIPTION

The DS1206 Phantom Serial Interface Chip is a CMOS circuit which intercepts the standardized memory bus found in computer systems and adapts the bus to a 3-wire serial port. Multiple memory cycles are used as a basis for generating the appropriate signals to control the serial port. A sequence of software-generated memory cycles encodes commands and transfers data with low pin count. The serial port signaling is derived from the memory address bus lines A0 through A3, the $\overline{CE}/\overline{CAS}$ signal and $\overline{RAS}/\overline{OE}$ signal without affecting

address space, thereby maintaining transparency to the memory bus. Communications are established under software control by an address pattern recognition sequence (serial port protocol) which disables a bytewide or DRAM memory via $\overline{CE}/\overline{CAS}$ output. An additional address sequence is required to generate the 3-wire port signals: $\overline{RESET}$ ($\overline{RST}$), Data (DQ), and Clock (CLK). The add-on serial port provides a minimum cost interface to the DS1201, DS1204U, DS1207, DS1223, and DS1290.

OPERATION

The main parts of the DS1206 are shown in the block diagram of Figure 1. Information presented on address inputs is latched into the DS1206 on the falling edge of a strobe signal derived from the logical combination of $\overline{CE}/\overline{CAS}$ In and $\overline{RAS}/\overline{OE}$ In. When redirecting information from a DRAM memory bus, both $\overline{RAS}$ and $\overline{CAS}$ inputs are required and the column addresses are used for signaling.

For a bytewide memory bus, only a $\overline{CE}$ input is required and the $\overline{RAS}/\overline{OE}$ input can be tied low or connected to the memory $\overline{OE}$ input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 4-bit serial interface protocol and to logic which will generate signals for the serial port. The serial interface protocol is derived from address inputs A0, A1, and A2.

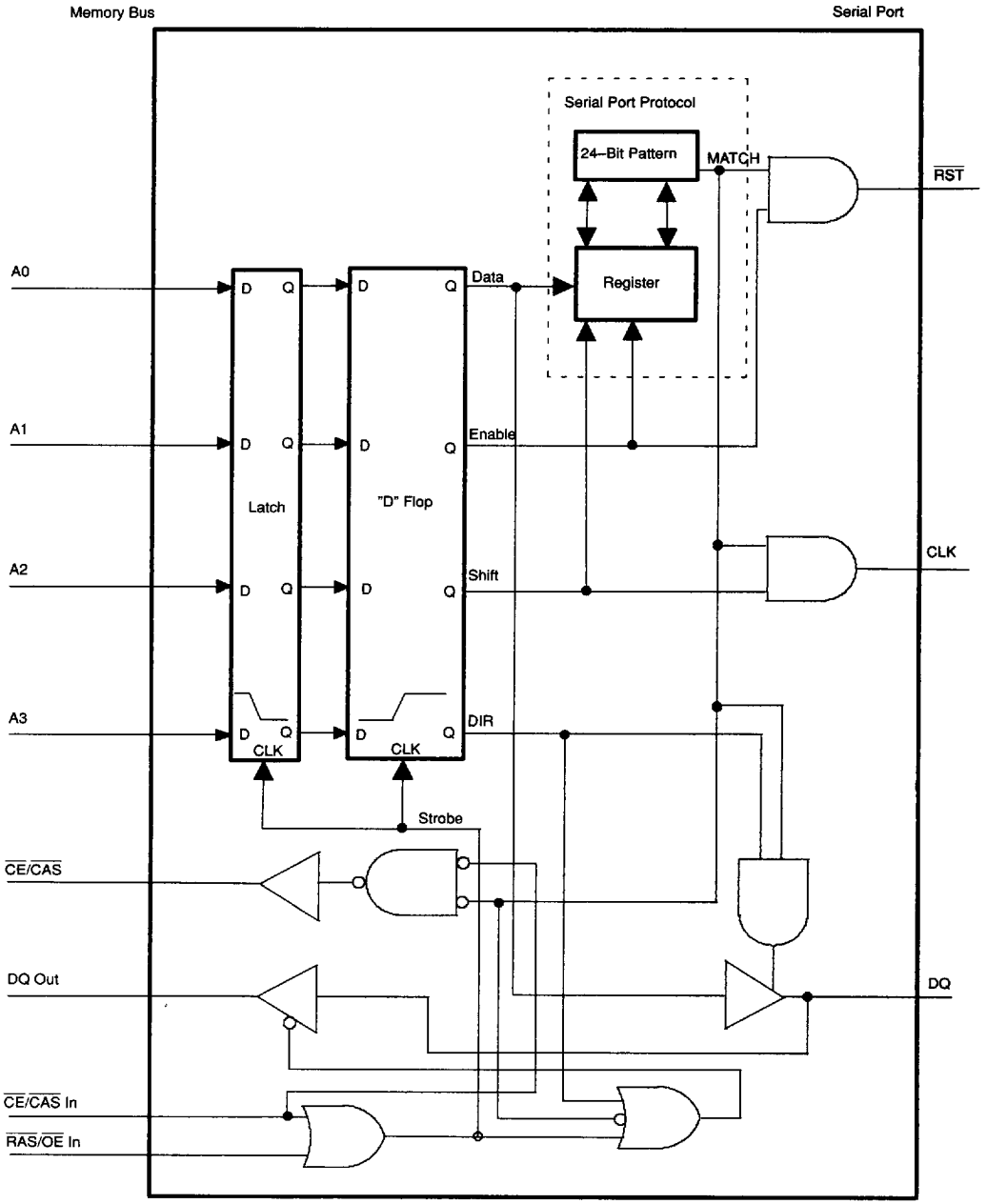
A1 is an enable signal which activates the communications sequence. A0 defines the data which is compared for recognition. A2 is used to clock in information defined by A0. Initially the A1 input must be set high to enable serial interface communications. A1 must remain high during the pattern recognition sequence and subsequent communications with the serial port after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and future access to the serial port is denied.

Data transfer through the serial interface occurs by matching a 24-bit pattern as shown in Figure 2. This pattern is presented to a register on each rising edge of strobe. Data is input for comparison to the serial interface protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24-bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal which causes data to enter the 24-bit register for comparison to the 24-bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles.

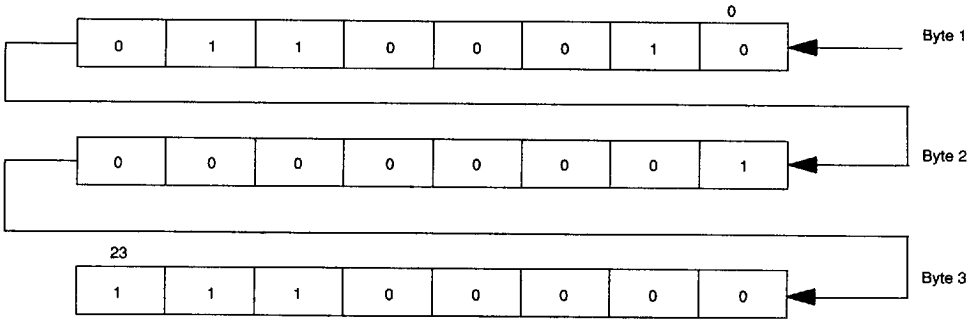
The first memory cycle sets A2 low and establishes the shift clock low. The second memory cycle sets A2 high and causes the transition necessary to shift a bit of data into the 24-bit register. Data on A0 is kept at the correct level for both memory cycles. Address input A3 is used to control the direction of data going to and from the serial port. This input is not used during pattern recognition of the protocol. After the 24-bit pattern has been correctly entered, a match signal is generated. The match signal is logically combined with the enable signal to generate the $\overline{RST}$ signal for the serial port. The match signal is also used to disable Chip Enable to the memory bus and to enable a gate which allows the serial port DQ to drive the DQ out line to the memory bus.

When $\overline{RST}$ is driven high, devices attached to the serial port become active. Subsequent shift signals derived from A2 will now be recognized as the serial port clock. The data signal for the serial bus is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on the serial port DQ. When A3 is set low, devices attached to the serial port can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the serial port DQ.

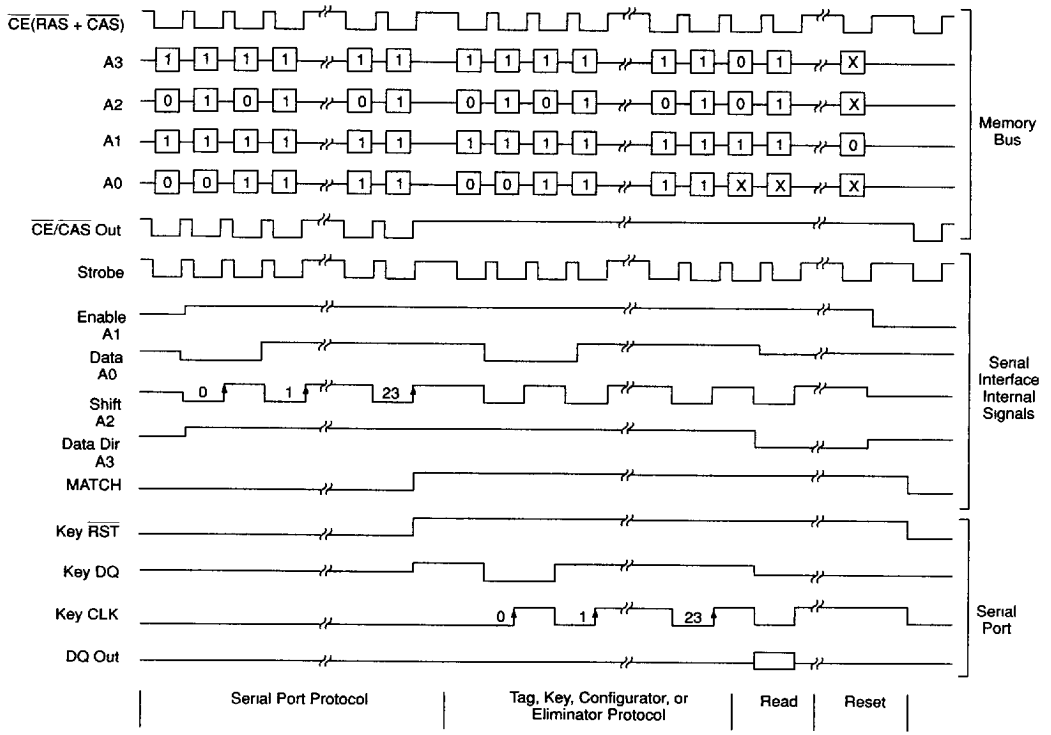
PHANTOM SERIAL INTERFACE BLOCK DIAGRAM Figure 1



SERIAL INTERFACE 24-BIT PROTOCOL Figure 2



PHANTOM SERIAL INTERFACE SIGNALS Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC} + 0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1		1	µA	
Output Leakage	I_{LO}			1	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ .4V	I_{OL}	+4			mA	
$\overline{RST}$ Output Current @ 3.8V	I_{OHR}	16			mA	
Supply Current	I_{CC}			6	mA	2

CAPACITANCE

(t_A=25°C)

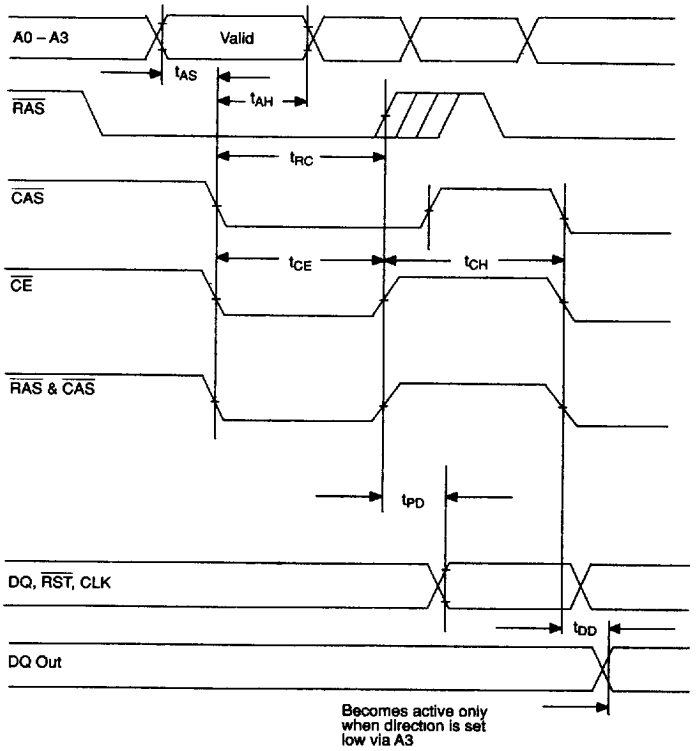
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
$\overline{RAS}$ to $\overline{CAS}$ Overlap	t_{RC}	60			ns	
$\overline{CE}$ Pulse Width	t_{CE}	60			ns	
Key Signals Valid	t_{PD}			60	ns	3
Key Data Out	t_{DD}	10			ns	3
$\overline{CE}$ Inactive	t_{CH}	30			ns	

MEMORY BUS INPUTS



NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Measured with a load as shown in Figure 4.

OUTPUT LOAD Figure 4