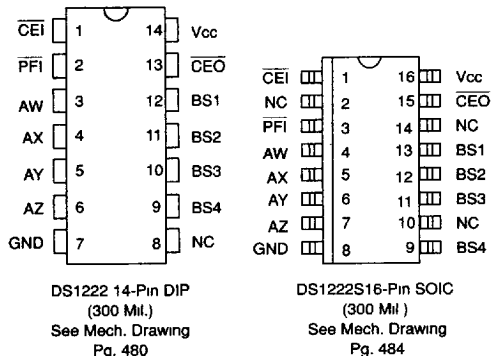# DALLAS
SEMICONDUCTOR

DS1222
BankSwitch Chip

FEATURES

- Provides bank switching for 16 banks of memory

- Bank switching is software-controlled by a pattern recognition sequence on four address inputs

- Automatically sets all 16 banks off on power-up

- Bank switching logic allows only one bank on at a time

- Custom recognition patterns are available to prevent unauthorized access

- Full ±10% operating range

- Low-power CMOS circuitry

- Can be used to expand the address range of microprocessors and decoders

- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT

DS1222 14-Pin DIP
(300 Mil.)
See Mech. Drawing
Pg. 480

DS1222S16-Pin SOIC
(300 Mil.)
See Mech. Drawing
Pg. 484

PIN DESCRIPTION

A_W-A_Z	– Address Inputs
$\overline{CEI}$	– Chip Enable Input
$\overline{CEO}$	– Chip Enable Output
NC	– No Connection
BS1,BS2,	– Bank Select Outputs
BS3,BS4	– Bank Select Outputs
$\overline{PFI}$	– Power Fail Input
V_{CC}	– +5 Volts
GND	– Ground

DESCRIPTION

The DS1222 BankSwitch Chip is a CMOS circuit designed to select one of sixteen memory banks under software control. Memory bank switching allows for an increase in memory capacity without additional address lines. Continuous blocks of memory are enabled by selecting the proper memory bank through a pattern recognition sequence on four address inputs. Custom patterns available from Dallas Semiconductor can provide security through uniqueness and prevent unauthorized access. By combining the DS1222 with the DS1212 Nonvolatile Controller x16 Chip, up to 16 banks of static RAMs can be selected.

OPERATION – BANK SWITCHING

Initially, on power-up all four bank select outputs are low and the chip enable output ($\overline{CEO}$) is held high. (Note: the power fail input [$\overline{PFI}$] must be low prior to power-up to assure proper initialization.) Bank switching is achieved by matching a predefined pattern stored within the DS1222 with a 16-bit sequence received on four address inputs. Prior to entering the 16-bit pattern, which sets the bank switch, a read cycle of 1111 on address inputs AW through AZ should be executed to guarantee that pattern entry starts with bit 0. Each set of address inputs is clocked into the DS1222 when $\overline{CEI}$ is driven low. All 16 inputs must be consecutive read cycles. The first eleven cycles must match the exact bit pattern as

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shown in Table 1. The last five cycles must match the exact bit pattern as shown for addresses AX, AY, and AZ. However, address line AW defines the bank number to be enabled as per Table 2.

Switching to a selected bank of memory occurs on the rising edge of $\overline{\text{CEI}}$ when the last set of bits is input and a match has been established. After bank selection $\overline{\text{CEO}}$ always follows $\overline{\text{CEI}}$ with a maximum propagation delay of 15 ns. The bank selected is determined by the levels set on Bank Select 1 through Bank Select 4 as per Table 2. These levels are held constant for all memory cycles until a new memory bank is selected.

ADDRESS BIT SEQUENCE Table 1

ADDRESS INPUTS	BIT SEQUENCE															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A_W	1	0	1	0	0	0	1	1	0	1	0	x	x	x	x	x
A_X	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_Y	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_Z	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X See Table 2

BANK SELECT CONTROL Table 2

Bank Selected	A_W Bit Sequence					Outputs			
	11	12	13	14	15	BS1	BS2	BS3	BS4
*Banks Off	0	X	X	X	X	Low	Low	Low	Low
Bank 0	1	0	0	0	0	Low	Low	Low	Low
Bank 1	1	0	0	0	1	High	Low	Low	Low
Bank 2	1	0	0	1	0	Low	High	Low	Low
Bank 3	1	0	0	1	1	High	High	Low	Low
Bank 4	1	0	1	0	0	Low	Low	High	Low
Bank 5	1	0	1	0	1	High	Low	High	Low
Bank 6	1	0	1	1	0	Low	High	High	Low
Bank 7	1	0	1	1	1	High	High	High	Low
Bank 8	1	1	0	0	0	Low	Low	Low	High
Bank 9	1	1	0	0	1	High	Low	Low	High
Bank 10	1	1	0	1	0	Low	High	Low	High
Bank 11	1	1	0	1	1	High	High	Low	High
Bank 12	1	1	1	0	0	Low	Low	High	High
Bank 13	1	1	1	0	1	High	Low	High	High
Bank 14	1	1	1	1	0	Low	High	High	High
Bank 15	1	1	1	1	1	High	High	High	High

*$\overline{\text{CEO}}$ = V_{IH} independent of $\overline{\text{CEI}}$

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS   (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS   (0°C to 70°C; V_{CC} = 5V $\pm$ 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	2
Output Current @ 0.4V	I_{OL}			+4.0	mA	2
Operating Current	I_{CC}			15	mA	

CAPACITANCE   (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS   (0°C to 70°C; V_{CC} = 5V $\pm$ 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	5			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
Propagation Delay	t_{PD}			15	ns	2
Power Fail Input to First $\overline{CE1}$	t_{PF}	50			ns	
Chip Enable Low	t_{CW}	110			ns	

NOTES:

1. All voltages are referenced to ground.

2. Measured with a load as shown in Figure 1.

OUTPUT LOAD Figure 1

Output Load
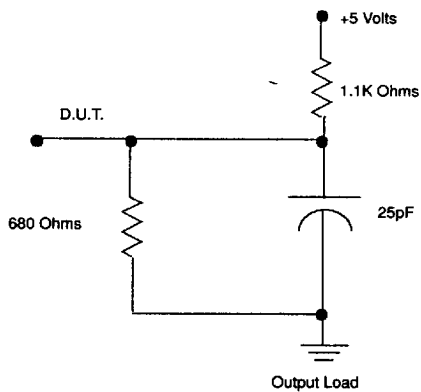
TIMING DIAGRAM-ACCESS TO BANK SWITCH