

DALLAS

SEMICONDUCTOR

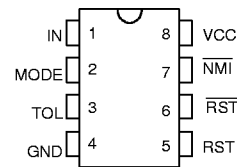
DS1231/S

Power Monitor Chip

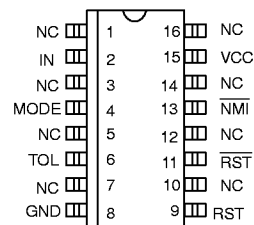
FEATURES

- Warns processor of an impending power failure
- Provides time for an orderly shutdown
- Prevents processor from destroying nonvolatile memory during power transients
- Automatically restarts processor after power is restored
- Suitable for linear or switching power supplies
- Adjusts to hold time of the power supply
- Supplies necessary signals for processor interface
- Accurate 5% or 10% V_{CC} monitoring
- Replaces power-up reset circuitry
- No external capacitors required
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



DS1231 8-Pin DIP
(300 MIL)
See Mech. Drawings
Section



DS1231S 16-Pin SOIC
(300 MIL)
See Mech. Drawings
Section

PIN DESCRIPTION

IN	– Input
MODE	– Selects input pin characteristics
TOL	– Selects 5% or 10% V_{CC} detect
GND	– Ground
RST	– Reset (Active High)
$\overline{\text{RST}}$	– Reset (Active Low, open drain)
NMI	– Non-Maskable Interrupt
V_{CC}	– +5V Supply
NC	– No Connections

DESCRIPTION

The DS1231 Power Monitor Chip uses a precise temperature-compensated reference circuit which provides an orderly shutdown and an automatic restart of a processor-based system. A signal warning of an impending power failure is generated well before regulated DC voltages go out of specification by monitoring high voltage inputs to the power supply regulators. If line isolation is required a UL-approved opto-isolator can be directly interfaced to the DS1231. The time for processor

shutdown is directly proportional to the available hold-up time of the power supply. Just before the hold-up time is exhausted, the Power Monitor unconditionally halts the processor to prevent spurious cycles by enabling Reset as V_{CC} falls below a selectable 5 or 10 percent threshold. When power returns, the processor is held inactive until well after power conditions have stabilized, safeguarding any nonvolatile memory in the system from inadvertent data changes.

OPERATION

The DS1231 Power Monitor detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. The main elements of the DS1231 are illustrated in Figure 1. As shown, the DS1231 actually has two comparators, one for monitoring the input (Pin 1) and one for monitoring V_{CC} (Pin 8). The V_{CC} comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6) when V_{CC} falls below a preset trip level as defined by TOL (Pin 3).

When TOL is connected to ground, the RST and $\overline{RST}$ signals will become active as V_{CC} goes below 4.75 volts. When TOL is connected to V_{CC} , the RST and $\overline{RST}$ signals become active as V_{CC} goes below 4.5 volts. The RST and $\overline{RST}$ signals are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC} . On power-up, RST and $\overline{RST}$ are kept active for a minimum of 150 ms to allow the power supply to stabilize (see Figure 2).

The comparator monitoring the input pin produces the $\overline{NMI}$ signal (Pin 7) when the input threshold voltage (V_{TP}) falls to a level as determined by Mode (Pin 2). When the Mode pin is connected to V_{CC} , detection occurs at V_{TP-} . In this mode Pin 1 is an extremely high impedance input allowing for a simple resistor voltage divider network to interface with high voltage signals. When the Mode pin is connected to ground, detection occurs at V_{TP+} . In this mode Pin 1 sources 30 μA of current allowing for connection to switched inputs, such as a UL-approved opto-isolator. The flexibility of the input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time allotted between $\overline{NMI}$ and $\overline{RST}$. On power-up, $\overline{NMI}$ is released as soon as the input threshold voltage (V_{TP}) is achieved and V_{CC} is within nominal limits. In both

modes of operation the input pin has hysteresis for noise immunity (Figure 3).

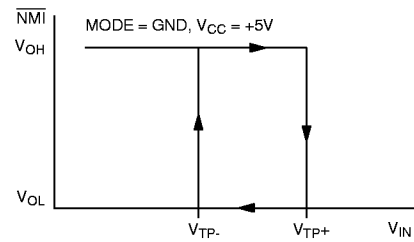
APPLICATION – MODE PIN CONNECTED TO V_{CC}

When the Mode pin is connected to V_{CC} , pin 1 is a high impedance input. The voltage sense point and the level of voltage at the sense point are dependent upon the application (Figure 4). The sense point may be developed from the AC power line by rectifying and filtering the AC. Alternatively, a DC voltage level may be selected which is closer to the AC power input than the regulated +5-volt supply, so that ample time is provided for warning before regulation is lost.

Proper operation of the DS1231 requires a maximum voltage of 5 volts at the input (Pin 1), which must be derived from the maximum voltage at the sense point. This is accomplished with a simple voltage divider network of R1 and R2. Since the IN trip point V_{TP-} is 2.3 volts (using the -20 device), and the maximum allowable voltage on pin 1 is 5 volts, the dynamic range of voltage at the sense point is set by the ratio of $2.3/5.0 = .46$ min. This ratio determines the maximum deviation between the maximum voltage at the sense point and the actual voltage which will generate $\overline{NMI}$.

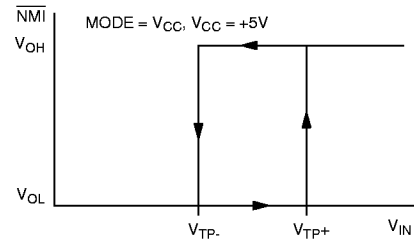
Having established the desired ratio, and confirming that the ratio is greater than .46 and less than 1, the proper values for R1 and R2 can be determined by the equation as shown in Figure 4. A simple approach to solving this equation is to select a value for R2 which is high enough impedance to keep power consumption low, and solve for R1. Figure 5 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is connected to V_{CC} .

INPUT PIN HYSTERESIS Figure 3

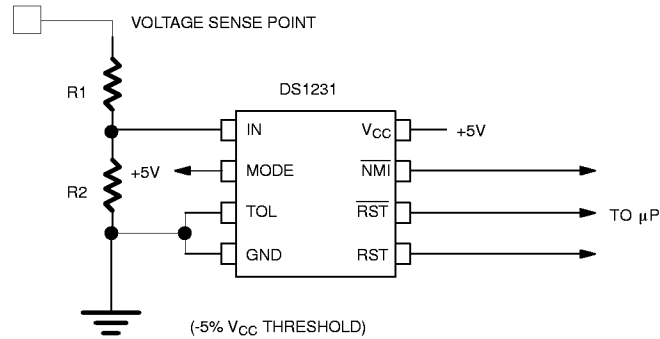


	-20	-35	-50
V _{TP-}	2.3	2.15	2.0
V _{TP+}	2.5	2.5	2.5

NOTE: HYSTERESIS TOLERANCE IS ±60 mV



APPLICATION WITH MODE PIN CONNECTED TO V_{CC} Figure 4



$$V \text{ SENSE} = \frac{R1 + R2}{R2} \times 2.3 \quad V \text{ MAX} = \frac{V \text{ SENSE}}{V_{TP-}} \times 5.0$$

EXAMPLE: V SENSE = 8 VOLTS AT TRIP POINT AND A
MAXIMUM VOLTAGE OF 17.5V WITH R2 = 10K

$$\text{THEN } 8 = \frac{R1 + 10K}{10K} \times 2.3 \quad R1 = 25K$$

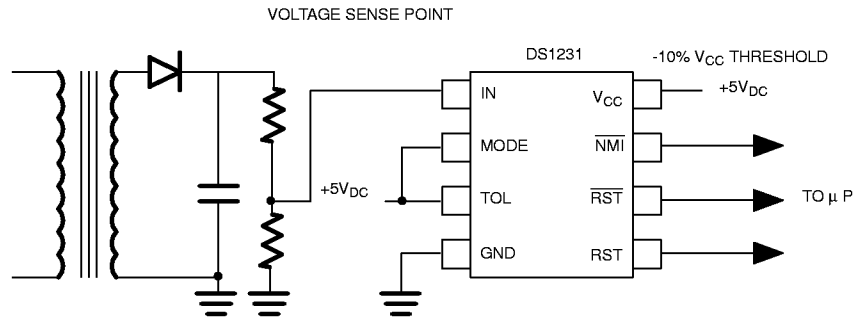
NOTE: $\overline{\text{RST}}$ requires a pull-up resistor.

APPLICATION – MODE PIN CONNECTED TO GROUND

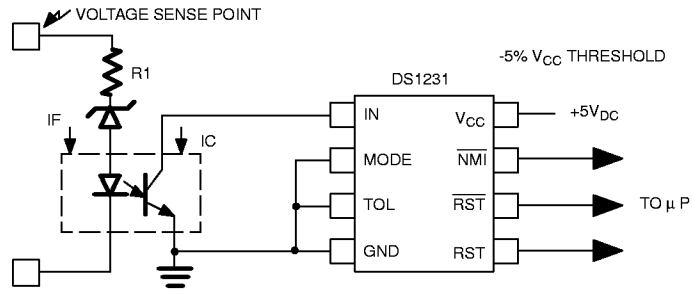
When the Mode pin is connected to ground, pin 1 is a current source of 30 μA with a V_{TP+} of 2.5 volts. Pin 1 is held below the trip point by a switching device like an opto-isolator as shown in Figure 6. Determination of the sense point has the same criteria as discussed in the previous application. However, determining component values is significantly different. In this mode, the maximum dynamic range of the sense point versus desired trip voltage is primarily determined by the selection of a zener diode. As an example, if the maximum voltage at the sense point is 200V and the desired trip point is 150V, then a zener diode of 150V will approximately set

the trip point. This is particularly true if power consumption on the high voltage side of the opto-isolator is not an issue. However, if power consumption is a concern, then it is desirable to make the value of R1 high. As the value of R1 increases, the effect of the LED current in the opto-isolator starts to affect the IN trip point. This can be seen from the equation shown in Figure 6. R1 must also be low enough to allow the opto-isolator to sink the 30 μA of collector current required by pin 1 and still have enough resistance to keep the maximum current through the opto-isolator's LED within data sheet limits. Figure 7 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is grounded.

AC VOLTAGE MONITOR WITH TRANSFORMER ISOLATION Figure 5



NOTE: $\overline{\text{RST}}$ requires a pull-up resistor.

APPLICATION WITH MODE PIN GROUNDING Figure 6

$$\text{VOLTAGE SENSE POINT (TRIP VALUE)} = V_Z + \frac{I_C}{CTR} \times R_1$$

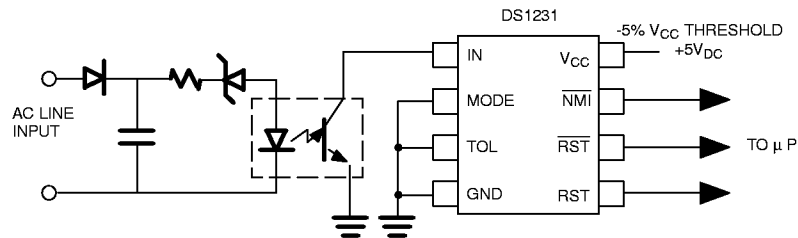
$$CTR = \frac{I_C}{I_F} \quad CTR = \text{CURRENT TRANSFER RATIO}$$

$$V_Z = \text{ZENNER VOLTAGE}$$

EXAMPLE: $CTR = 0.2$ $I_C = 30 \mu A$ $I_F = 150 \mu A$
 VOLTAGE SENSE POINT = 105 AND
 $V_Z = 100 \text{ VOLTS}$

$$\text{THEN } 105 = 100 + \frac{30}{0.2} \times R_1 \quad R_1 = 33K$$

NOTE: $\overline{RST}$ requires a pull-up resistor.

AC VOLTAGE MONITOR WITH OPTO-ISOLATION Figure 7

NOTE: $\overline{RST}$ requires a pull-up resistor.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	-0.5V to $V_{CC} + 0.5V$
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Pin 1	V_{IN}			V_{CC}	V	1

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{CC} = 4.5$ to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ -500 μA	V_{OH}	$V_{CC}-0.5V$	$V_{CC}-0.1V$		V	1, 6
Input Leakage	I_{IL}	-10		+10	μA	2
Output Current @2.4V	I_{OH}	1.0	2.0		mA	5
Output Current @0.4V	I_{OL}	2.0	3.0		mA	
Operating Current	I_{CC}		0.5	2.0	mA	3
Input Pin 1 (Mode=GND)	I_C	15	25	50	μA	
Input Pin 1 (Mode= V_{CC})	I_C			0.1	μA	
IN Trip Piont (Mode=GND)	V_{TP}	See Figure 3				1
IN Trip Point (Mode= V_{CC})	V_{TP}					1
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL= V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

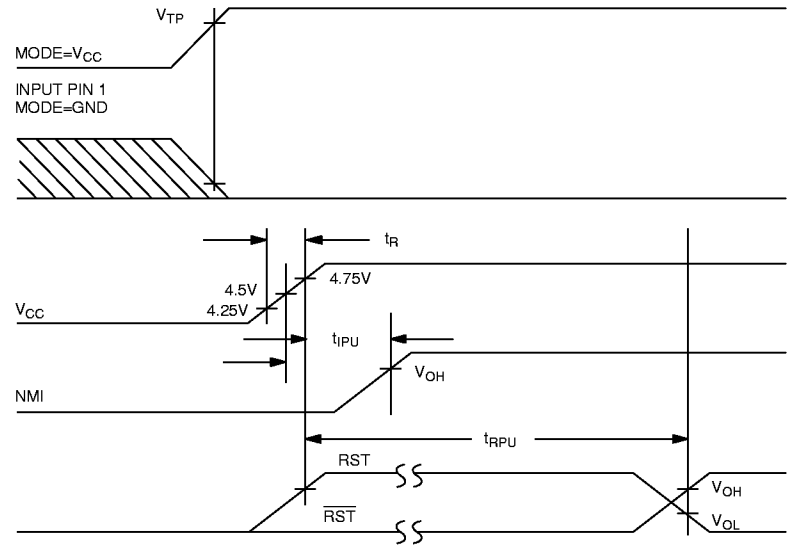
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{TP} to $\overline{NMI}$ Delay	t_{IPD}			1.1	μs	
V_{CC} Slew Rate 4.75-4.25V	t_F	300			μs	
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Detect to $\overline{NMI}$	t_{IPU}			200	μs	4
V_{CC} Detect to RST and $\overline{RST}$	t_{RPU}	150	500	1000	ms	4
V_{CC} Slew Rate 4.25-4.75V	t_R	0			ns	

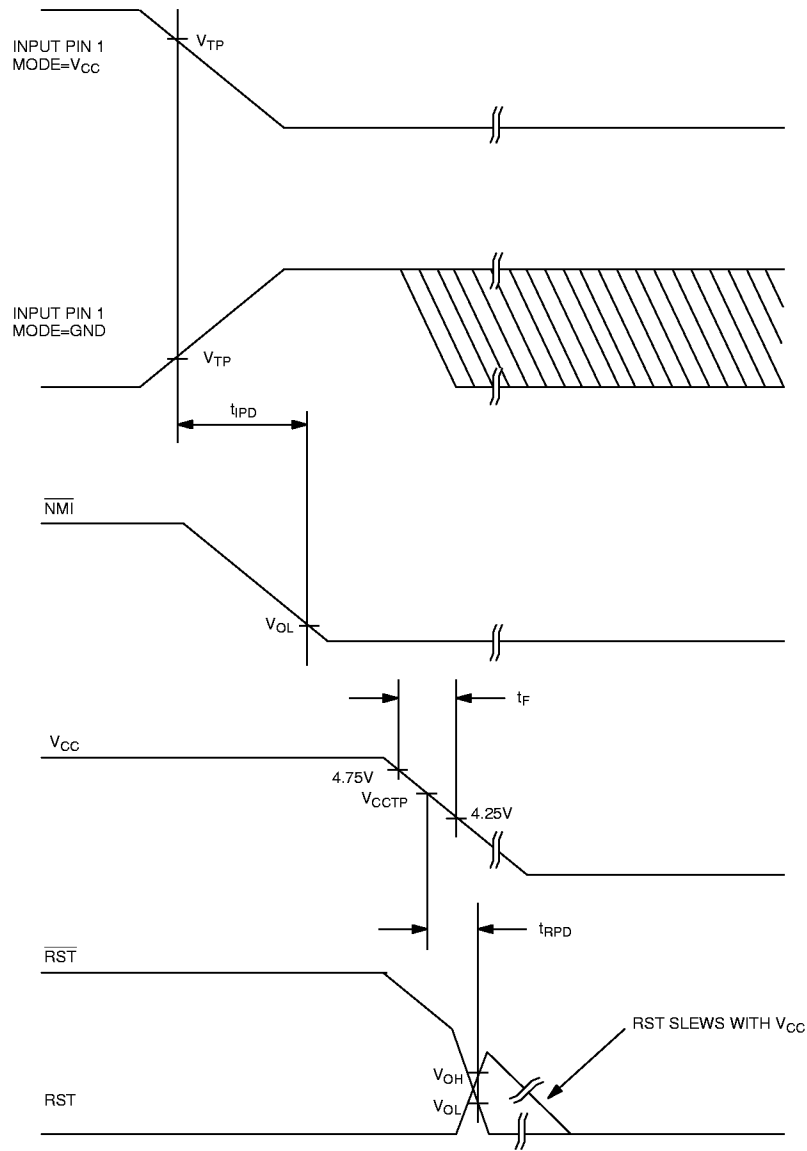
NOTES:

1. All voltages referenced to ground.
2. $V_{CC} = +5.0$ volts with outputs open.
3. Measured with outputs open.
4. $t_R = 5 \mu s$.
5. $\overline{RST}$ is an open drain output and requires a pull-up resistor.
6. RST remains within 0.5V of V_{CC} on power-down until V_{CC} drops below 2.0V. $\overline{RST}$ remains within 0.5V of GND on power-down until V_{CC} drops below 2.0V.

TIMING DIAGRAM: POWER-UP

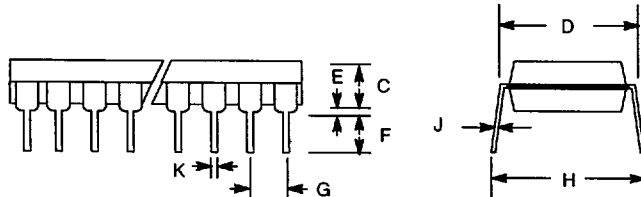
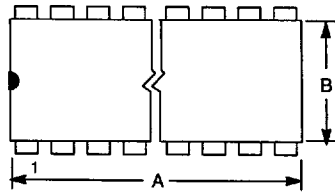


TIMING DIAGRAM: POWER-DOWN



MECHANICAL DRAWINGS

8- TO 28-PIN DIP (300 MIL)



Includes:

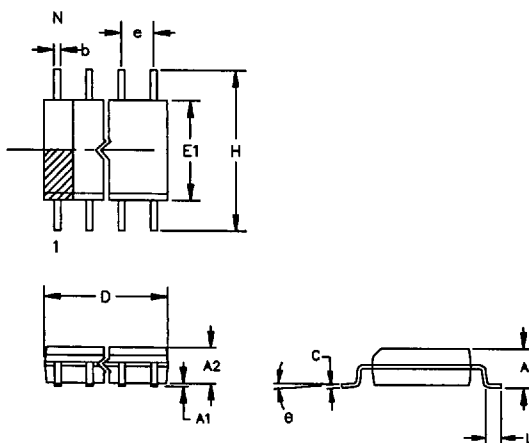
DS1000	DS1211	DS1621
DS1000M	DS1215	DS1625
DS1003	DS1221	DS1632
DS1003M	DS1222	DS1640
DS1004M	DS1228	DS1651
DS1005	DS1229	DS1652
DS1005M	DS1231	DS1652B
DS1007	DS1232	DS1653
DS1010	DS1232LP	DS1666
DS1012M	DS1234	DS1667
DS1013	DS1236	DS1669
DS1013M	DS1237	DS1802
DS1020	DS1238	DS1830
DS1033M	DS1239	DS1832
DS1035M	DS1259	DS1867
DS1040M	DS1267	DS1868
DS1044	DS1275	DS1869
DS1045	DS1291	DS2009D
DS1200	DS1293	DS2010D
DS1206	DS1336	DS2011D
DS1210	DS1620	DS2013D

PKG	8-PIN		10-PIN		14-PIN		16-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.360	0.400	0.480	0.520	0.740	0.780	0.740	0.780
MM	9.14	10.16	12.19	13.21	18.80	19.81	18.80	19.81
B IN.	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260
MM	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.62	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.02
F IN.	0.120	0.140	0.110	0.130	0.120	0.140	0.120	0.140
MM	3.04	3.56	2.79	3.30	3.04	3.56	3.04	3.56
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
H IN.	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370
MM	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40
J IN.	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53

Continued on following page.

MECHANICAL DRAWINGS

16-, 20-, 24-, 28-PIN SOIC (300 MIL)



Includes:

DS1000S	DS1227S	DS1360S
DS1005S	DS1231S	DS1380S
DS1007S	DS1228S	DS1609S
DS1010S	DS1229S	DS1610S
DS1013S	DS1232S	DS1620
DS1020S	DS1232LPS	DS1632S
DS1021S	DS1234S	DS1640S
DS1045S	DS1236S	DS1653S
DS1200S	DS1237S	DS1710S
DS1205S	DS1238S	DS2107AS
DS1206	DS1239S	DS2107S
DS1209S-B1	DS1259S	DS2175S
DS1210S	DS1267S	DS2186S
DS1211S	DS12885S	DS2187S
DS1215S	DS1336S	DS2188S
DS1221S	DS1359S	
DS1222S		

The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

PKG	16-PIN		20-PIN		24-PIN		28-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN. MM	0.094 2.38	0.105 2.68	0.094 2.38	0.105 2.68	0.094 2.38	0.105 2.68	0.094 2.39	0.105 2.67
A1 IN. MM	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51	0.013 0.33	0.020 0.51	0.013 0.33	0.020 0.51	0.013 0.33	0.020 0.51
C IN. MM	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33
D IN. MM	0.398 10.11	0.412 10.46	0.498 12.65	0.511 12.99	0.598 15.19	0.612 15.54	0.698 17.73	0.712 18.08
e IN. MM	0.050 BSC 1.27 BSC						0.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62	0.290 7.37	0.300 7.62	0.290 7.37	0.300 7.62	0.290 7.37	0.300 7.62
H IN. MM	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57
L IN. MM	0.016 0.40	0.040 1.02	0.016 0.406	0.040 1.20	0.016 0.40	0.040 1.02	0.016 0.40	0.040 1.02
Θ	0°	8°	0°	8°	0°	8°	0°	8°