T-46-23-37

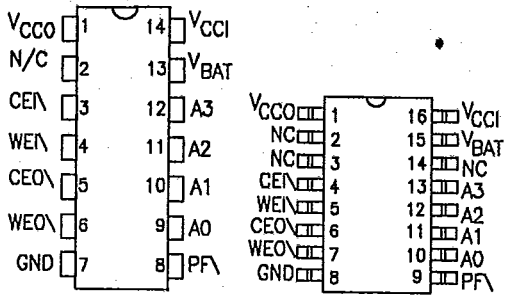
DALLAS SEMICONDUCTOR

DS1234
Conditional Nonvolatile Controller Chip

FEATURES

- Converts CMOS static RAMs into nonvolatile memories
- Software controlled write inhibit
- Software controlled battery disconnect extends battery life
- Unconditionally write protects when V_{CC} is out of tolerance
- Consumes less than 100 nA of battery current
- Power fail signal can be used to interrupt processor on power failure
- Low forward voltage drop on the V_{CC} switch
- Optional 16-pin SOIC surface mount package

PIN DESCRIPTION



DS1234
14-Pin DIP (300 Mil)

DS1234S
16-Pin SOIC (300 Mil)

PIN NAMES (\ Denotes Condition Low)

Pin#	Pin Name	Description
1	V_{CCO}	RAM Supply
2	N/C	No Connection
3	CE1\	Chip Enable Input
4	WE1\	Write Enable Input
5	CE0\	Chip Enable to RAM
6	WE0\	Write Enable to RAM
7	GND	Ground
8	PF\	Power Fail Output
9-12	A0-A3	Address Inputs
13	V_{BAT}	Battery Input
14	V_{CCI}	+5V Supply

DESCRIPTION

The DS1234 is a CMOS circuit that converts CMOS RAM into nonvolatile memory and adds two software selectable switches. Incoming power is monitored for an out-of-tolerance condition. When such a conditions is detected, chip enable and write enable to the RAM are inhibited to accomplish write protection, and the battery is switched on to supply the memory with uninterrupted power. The two software selectable switches provided by the DS1234 are capable of inhibiting both the write enable to the RAM and the battery backup circuitry by a pattern recognition sequence across four address lines. Inhibiting the write enable to the nonvolatile RAM provides data integrity by isolating the memory contents from external change. The second switch provides added flexibility and increases battery life to the system by enabling/disabling the battery for shipment or storage, or when battery backup is not needed.

T-46-23-37

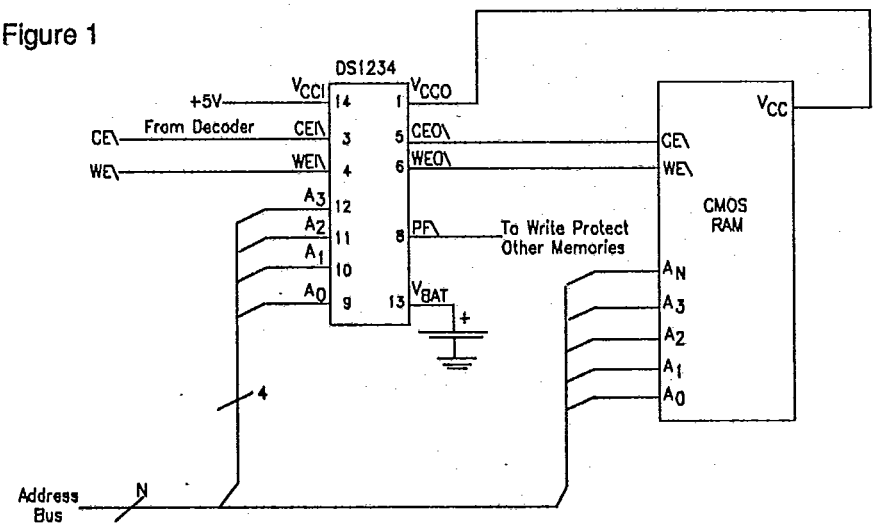
OPERATION

The DS1234 Conditional Nonvolatile Controller performs three circuit functions required to battery backup a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CCI}), depending on which is greater. This switch has a voltage drop of less than 0.2V. The second function is power fail detection. The DS1234 constantly monitors the incoming supply. When the supply goes out-of-tolerance, a comparator detects power fail and inhibits chip enable and write enable. The threshold voltage, V_{TP}, at which power fail is detected is defined as 1.26 times V_{BAT}. The third function of write protection is accomplished by holding the CEO\ and WEO\ output signals to within 0.2 volts of the V_{CCI} or battery supply.

In addition to the nonvolatile controller functions, the DS1234 supplies two software selectable switches for master control of the write enable and the nonvolatile controller itself. The switches are controlled by a 16-cycle pattern recognition sequence across four address lines (see Tables 1 and 2). Prior to entering the pattern recognition sequence that will define the two switch settings, a read cycle of 1111 on address inputs A0 through A3 should be executed to initialize the compare pointer of clock zero. Each four-bit compare word is clocked into the DS1234 on the negative edge of CE\. A0, A1 and A2 must match the compare pattern on all 16 consecutive cycles while A3 must match only the first eleven; the last five are used to define the switch settings. The eleventh address cycle, starting at zero, defines the switch that inhibits the write enable to the RAM (WEO\). A logic one in this location allows read/write operations so that WEO\ will follow WE\ and data can be updated. A zero on cycle eleven turns the RAM into a read-only memory (ROM). The next four address cycles, 12 thorough 15, define whether the nonvolatile controller operation is enabled or disabled. A bit pattern of 1010 activates the nonvolatile controller; data in the RAM is maintained on power loss. Any pattern other than 1010 will disable the nonvolatile controller operation.

At the completion of the 16th cycle, if the pattern recognition sequence is correct, the switch settings defined in cycles 11 though 15 are transferred and are active for the next memory cycle. When external battery power is applied for the first time, the DS1234 will come up with the nonvolatile controller off. Upon initial V_{CC} power, the write enable will be set in read/write operation (WE\=WEO\).

Figure 1



T-46-23-37

ADDRESS INPUT PATTERN Table 1

	CYCLE NUMBER															
Address Inputs	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A3	1	0	1	0	0	0	1	1	0	1	0	*	*	*	*	*
A2	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A1	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A0	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

* See Table 2

CONTROL SELECT Table 2

WE\ Battery Control					**Operation**
11	**12**	**13**	**14**	**15**	
0	X	X	X	X	Read Only Operation
1	X	X	X	X	Read/Write Operation
X	1	0	1	0	Enables Nonvolatile Controller*

X = Don't Care

*Any other combination turns controller off

T-46-23-37

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	2
Supply Current @ $V_{CCO} = V_{CCI}$ - 0.2	I_{CCO}			80	mA	3
Input Leakage	I_{IL}	-1.0		+1.0	uA	
Output Leakage	I_{LO}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	4
Output Current @ 0.4V	I_{OL}	4.0			mA	4

(0°C to 70°C, $V_{CCI} < V_{BAT}$)

CE0\, WE0\ Output	V_{OHL}	V_{BAT}-0.2			V	6
Battery Current	I_{BAT}			0.1	uA	7
Battery Backup Current @ $V_{CCO} = V_{BAT}$ - 0.3V	I_{CCO1}			100	uA	5

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTIC

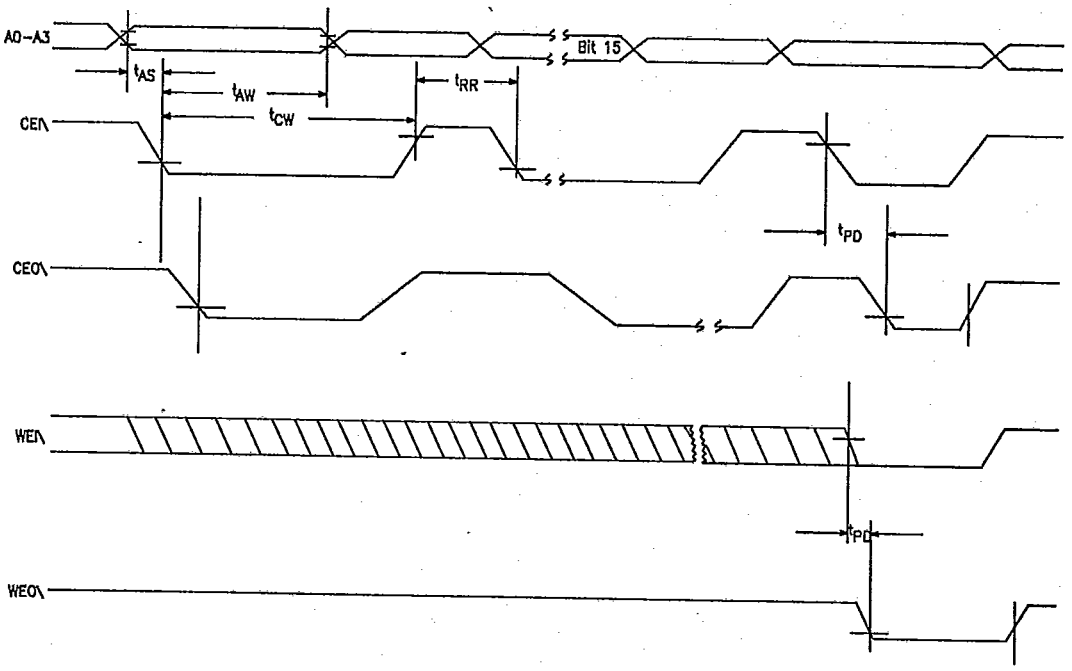
($0^{o}C$ to $70^{o}C$, V_{cc} = 5V+/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
CE\ Pulse Width	t_{CW}	110			ns	
Propagation Delay	t_{PD}			20	ns	

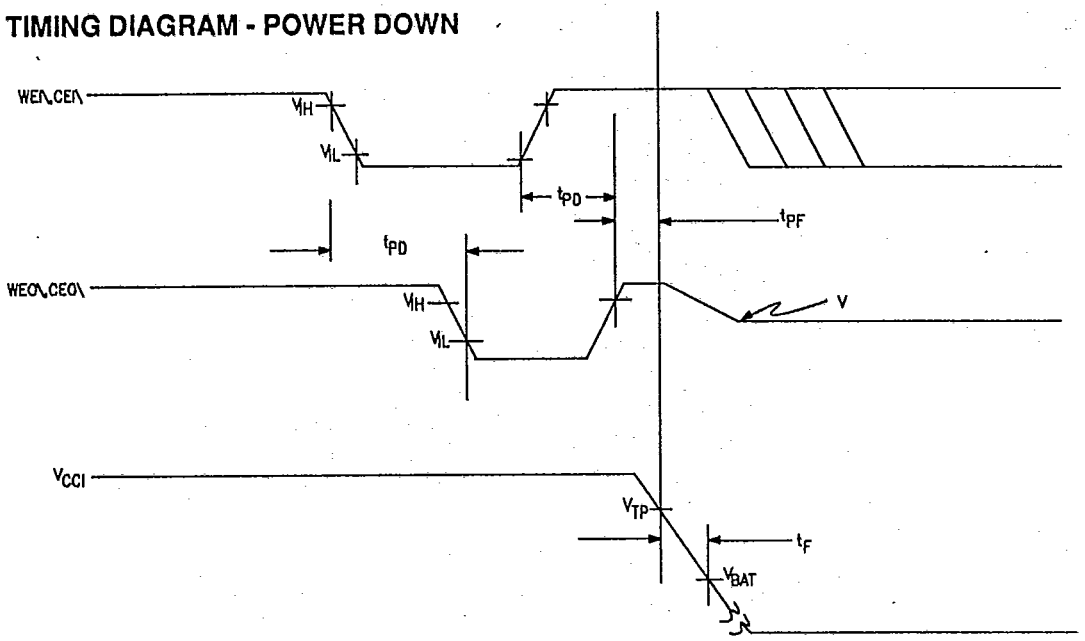
($0^{o}C$ to $70^{o}C$, $V_{cc} < V_{TP}$)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate Power Down	t_{F}	0			us	
V_{CC} Slew Rate Power Up	t_{R}	0			us	
CE\ High to Power Fail	t_{PF}	0			ns	

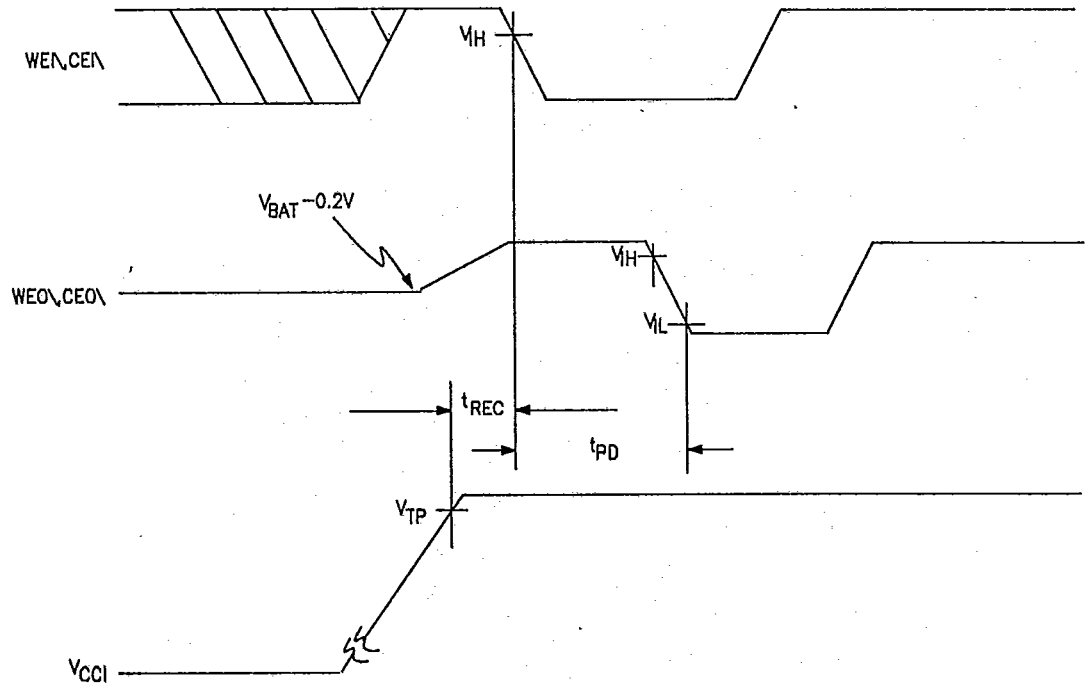
TIMING DIAGRAM - SWITCH SETTING



TIMING DIAGRAM - POWER DOWN



TIMING DIAGRAM - POWER UP



T-46-23-37

NOTES:

1. All voltages are referenced to ground.
2. Measured with V_{CCO}, CE0\ and WE0\ open.
3. I_{CCO} is the maximum average load which the DS1234 can supply to the memories.
4. Measured with a load as shown in Figure 2.
5. I_{CCO1} is the maximum average load current which the DS1234 can supply to the memories in the battery backup mode.
6. Chip Enable, CEO\, and Write Enable, WEO\, outputs can only sustain leakage current in the battery backup mode.
7. I_{BAT} is the total load current which the DS1234 uses from the battery input pin with V_{CCO}, CE0\, and WEO\ open.

OUTPUT LOAD Figure 2