National Semiconductor

DS1647/DS3647, DS1677/DS3677, DS16147/DS36147, DS16177/DS36177 Quad TRI-STATE® MOS Memory I/O Registers

General Description

The DS1647/DS3647 series are 4-bit I/O buffer registers intended for use in MOS memory systems. The circuits employ a fall-through latch for data storage. This method of latching captures the data in parallel with the output, thus eliminating the delays encountered in other designs. The circuits use Schottky-clamped transistor logic for minimum propagation delay and employ PNP input transistors so that input currents are low, allowing large fan-out to these circuits needed in a memory system.

Two pins per bit are provided, and data transfer is bi-directional so that the register can handle both input and output data. The direction of data flow is controlled through the input enables. The latch control, when taken low, will cause the register to hold the data present at that time and display it at the outputs. Data can be latched into the register independent of the output disables or EXPANSION input. Either or both of the outputs may be taken to the high-impedance state with the output disables. The EXPANSION pin disables both outputs to facilitate multiplexing with other I/O registers on the same data lines.

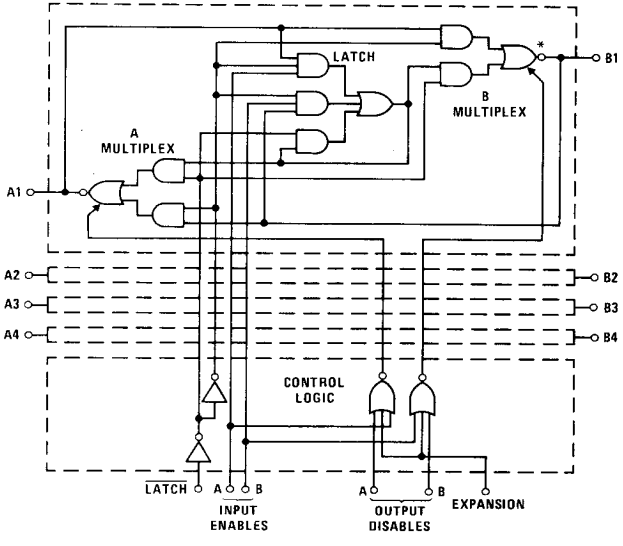
The "B" port outputs in the DS16147/DS36147 and DS16177/DS36177 are open collectors, and in the DS1647/DS3647 and DS1677/DS3677 they are TRI-STATE. The "B" port outputs are also designed for use in bus organized data transmission systems and can sink 80 mA and source −5.2 mA. The "A" port outputs in all four types are TRI-STATE.

Data going from port "A" to port "B" is inverted in the DS1647/DS3647 and DS16147/DS36147 and is not inverted in the DS1677/DS3677 and DS16177/DS36177. Data going from port "B" to port "A" is inverted in all four types.

Features

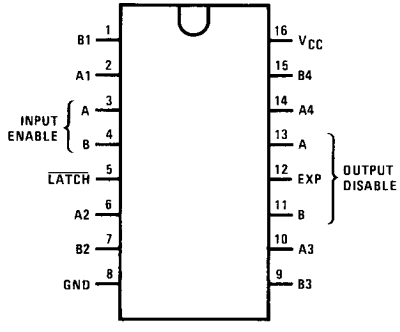
- PNP inputs minimize loading
- Fall-through latch design
- Propagation delay of only 15 ns
- TRI-STATE outputs
- EXPANSION control
- Bi-directional data flow
- TTL compatible
- Transmission line driver output

Logic and Connection Diagrams



*Inverting DS1647/DS3647 and DS16147/DS36147 only

Dual-In-Line Package



TOP VIEW

Order Number DS1647D, DS3647D, DS1677D, DS3677D, DS16147D, DS36147D, DS16177D, DS36177D, DS3647N, DS3677N, DS36147N or DS36177N
See NS Package D16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	−1.5V to +7V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1647, DS1677, DS16147, DS16177	−55	+125	°C
DS3647, DS3677, DS36147, DS36177	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logic "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logic "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logic "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V	Latch, Disable Inputs		0.1	40	μA
			Expansion		0.2	80	μA
			A Ports, B Ports		0.2	100	μA
			Enable Inputs		0.4	200	μA
$I_{IN(0)}$	Logic "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V	Latch, Disable Inputs		−25	−250	μA
			Expansion		−50	−500	μA
			A Ports, B Ports		−50	−500	μA
			Enable, Inputs		−0.1	−1.25	mA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.6	−1.2	V
$V_{OL(A)}$	Logic "0" Output Voltage A Ports	V_{CC} = 4.5V, I_{OL} = 20 mA			0.4	0.5	V
$V_{OL(B)}$	Logic "0" Output Voltage B Ports	V_{CC} = 4.5V	I_{OL} = 30 mA		0.3	0.4	V
			I_{OL} = 50 mA		0.4	0.5	V
$V_{OH(A)}$	Logic "1" Output Voltage A Ports	I_{OH} = −1 mA	V_{CC} = 5V	3.0	3.4		V
			V_{CC} = 4.5V	2.5	3.4		V
$V_{OH(B)}$	Logic "1" Output Voltage B Ports	I_{OH} = −5.2 mA, (Note 4)	V_{CC} = 5V	2.9	3.3		V
			V_{CC} = 4.5V	2.4	3.3		V
$I_{OS(A)}$	Output Short-Circuit Current A Port	V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V, (Note 5)		−30	−50	−100	mA
$I_{OS(B)}$	Output Short-Circuit Current B Port	V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V, (Notes 4 and 5)		−30	−60	−100	mA
I_{CC}	Power Supply Current	Exp = 3V, A Ports = 0V, B Ports Open, All Other Pins = 0V	DS1647, DS16147		100	110	mA
			DS3647, DS36147		100	140	mA
		Enable A, Latch = 3V, A Ports = 0V, B Ports Open, All Other Pins = 0V	DS1647, DS16147		70	80	mA
			DS3647, DS36147		70	105	mA
		Exp = 3V, A Ports = 0V, B Ports Open, All Other Pins = 0V	DS1677, DS16177		105	115	mA
			DS3677, DS36177		105	145	mA
		Enable A, Latch, A Ports = 3V, B Ports Open, All Other Pins = 0V	DS1677, DS16177		75	85	mA
			DS3677, DS36177		75	110	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1647, DS1677, DS16147, DS16177 and across the 0°C to +70°C range for the DS3647, DS3677, DS36147, DS36177. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

Note 4: Not applicable to DS16147/DS36147 or DS16177/DS36177.

Note 5: Only one output at a time should be shorted.

Switching Characteristics (V_{CC} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DATA TRANSFER B PORT TO A PORT, ALL DEVICES						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, R_L = 280 Ω, *(Figures 1 and 4)*		7.5	15	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 280 Ω, *(Figures 1 and 4)*		6.0	12	ns
A PORT CONTROL FROM OUTPUT DISABLE A INPUT, ALL DEVICES						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 1 and 5)*		13	20	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 1 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 1 and 7)*		10	15	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 1 and 8)*		25	35	ns
DATA TRANSFER A PORT TO B PORT, DS1647/DS3647						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		6.5	12	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		8.0	15	ns
DATA TRANSFER A PORT TO B PORT, DS1677/DS3677						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		12.5	20	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		8.5	15	ns
DATA TRANSFER A PORT TO B PORT DS16147/DS36147						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, *(Figures 3 and 4)*		18	25	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, *(Figures 3 and 4)*		7.0	15	ns
DATA TRANSFER A PORT TO B PORT, DS16177/DS36177						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, *(Figures 3 and 4)*		13.5	21	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, *(Figures 3 and 4)*		18	25	ns
B PORT CONTROL FROM OUTPUT DISABLE B INPUT, DS1647/DS3647, DS1677/DS3677						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 2 and 5)*		15	25	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 2 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 2 and 7)*		10	16	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 2 and 8)*		25	35	ns
B PORT CONTROL FROM OUTPUT DISABLE B INPUT, DS16147/DS36147, DS16177/DS36177						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 3 and 5)*		15	25	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 3 and 7)*		11	17	ns
LATCH SET-UP AND HOLD TIMES, ALL DEVICES						
t_{SET-UP}	Set-Up Time of Data Input Before $\overline{\text{Latch}}$ Goes Low		10	0		ns
t_{HOLD}	Hold Time of Data Input After $\overline{\text{Latch}}$ Goes Low		0			ns

Product Description

DEVICE NUMBER	B PORT TO A PORT FUNCTION	A PORT TO B PORT FUNCTION	A PORT OUTPUTS	B PORT OUTPUTS
DS1647/DS3647	Inverting	Inverting	TRI-STATE	TRI-STATE
DS1677/DS3677	Inverting	Non-Inverting	TRI-STATE	TRI-STATE
DS16147/DS36147	Inverting	Inverting	TRI-STATE	Open-Collector
DS16177/DS36177	Inverting	Non-Inverting	TRI-STATE	Open-Collector

Truth Table

INPUT ENABLES		$\overline{\text{LATCH}}$	OUTPUT DISABLES		EXPANSION	A PORTS A1–A4 ALL DEVICES	B PORTS B1–B4 DS1647, DS16147 DS3647, DS36147	B PORTS B1–B4 DS1677, DS16177 DS3677, DS36177	COMMENTS
A	B		A	B					
1	0	1	0	0	0	Hi-Z	$\overline{A}$	A	Data In on A, output to B
0	1	1	0	0	0	$\overline{B}$	Hi-Z	Hi-Z	Data In on B, output to A
1	0	0	0	0	0	Hi-Z	$\overline{A}$	A	Data stored which is present when $\overline{\text{latch}}$ goes low
0	1	0	0	0	0	$\overline{B}$	Hi-Z	Hi-Z	Data stored which is present when $\overline{\text{latch}}$ goes low
1	0	X	0	1	0	Hi-Z	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data In on A, may be latched
0	1	X	1	0	0	Hi-Z	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data In on B, may be latched
X	X	X	X	X	1	Hi-Z	Hi-Z	Hi-Z	Both A and B in Hi-Z state

AC Test Circuits

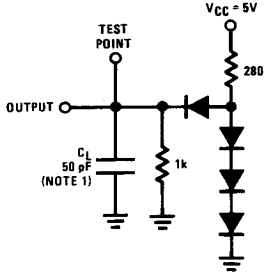


FIGURE 1. A Port Load, All Circuits

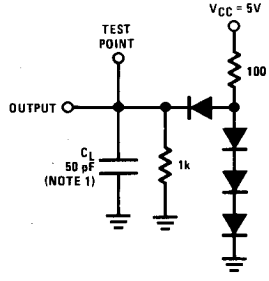


FIGURE 2. B Port Load, DS3647, DS3677

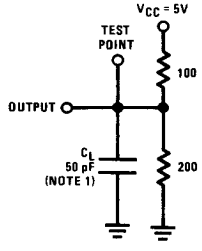
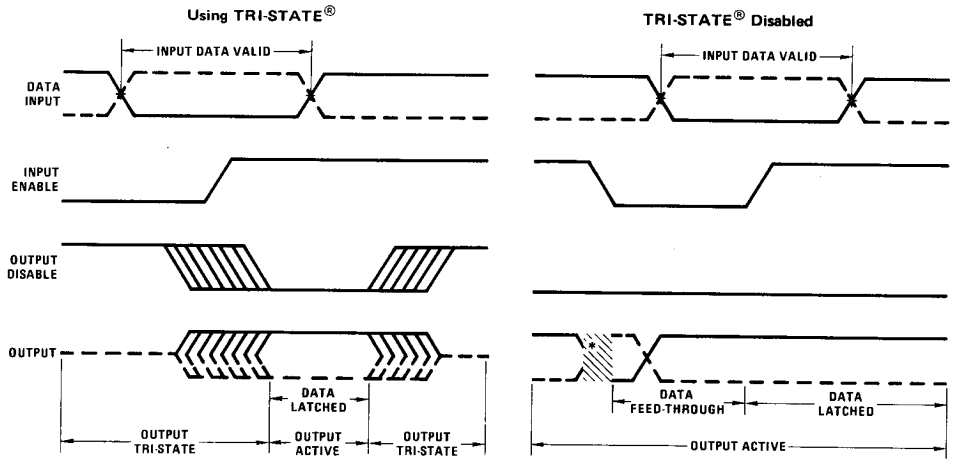


FIGURE 3. B Port Load, DS36147, DS36177

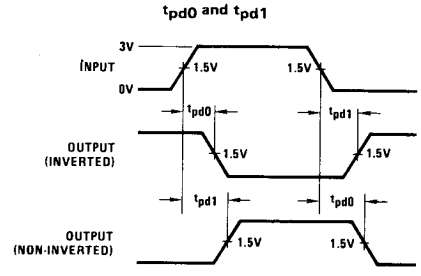
Note 1: C_L includes probe and jig capacitance.

Operating Waveforms



*When the Input Enable makes a negative transition, the output will be indeterminate for a short duration. The negative transition of the Input Enable normally occurs during a don't-care timing state at the output.

Switching Time Waveforms



Input Characteristics: f = 1 MHz, $t_R = t_F \leq 5$ ns (10% to 90% points), duty cycle = 50%, $Z_{OUT} = 50\ \Omega$

FIGURE 4

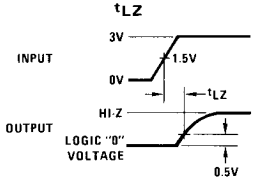


FIGURE 5

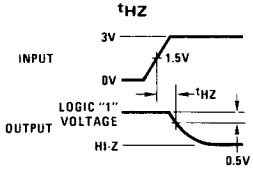


FIGURE 6

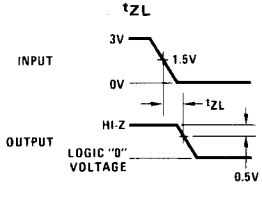


FIGURE 7

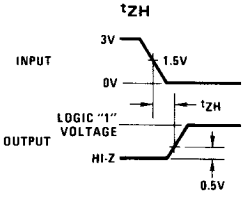
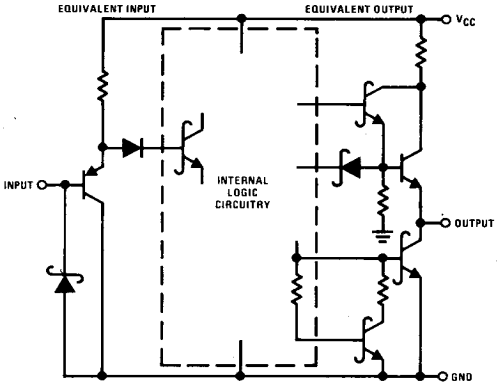


FIGURE 8

Schematic Diagram



Note. Data pins A1–A4 and B1–B4 consist of an input and an output tied together.

Typical Application

The diagram below shows how the DS3677 can be used as a register capable of multiplexing data lines.