

**DALLAS**  
**SEMICONDUCTOR**
**DS1658Y/AB**  
**Partitionable 128K x 16 NV SRAM**
**FEATURES**

- 10 year minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Write protects selected blocks of memory when programmed
- Separate upper byte and lower byte chip selection inputs
- Unlimited write cycles
- Low-power CMOS
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full  $\pm 10\%$   $V_{CC}$  operating range (DS1658Y)
- Optional  $\pm 5\%$   $V_{CC}$  operating range (DS1658AB)
- Optional industrial temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (designated IND)

**PIN ASSIGNMENT**

$\overline{\text{CEU}}$	1	40	$V_{CC}$
$\overline{\text{CEL}}$	2	39	$\overline{\text{WE}}$
DQ15	3	38	A16
DQ14	4	37	A15
DQ13	5	36	A14
DQ12	6	35	A13
DQ11	7	34	A12
DQ10	8	33	A11
DQ9	9	32	A10
DQ8	10	31	A9
GND	11	30	GND
DQ7	12	29	A8
DQ6	13	28	A7
DQ5	14	27	A6
DQ4	15	26	A5
DQ3	16	25	A4
DQ2	17	24	A3
DQ1	18	23	A2
DQ0	19	22	A1
$\overline{\text{OE}}$	20	21	A0

 40-PIN EXCAPSULATED PACKAGE  
 740 MIL EXTENDED

**PIN DESCRIPTION**

A0–A16	– Address Inputs
DQ0–DQ15	– Data In/Data Out
$\overline{\text{CEU}}$	– Chip Enable Upper Byte
$\overline{\text{CEL}}$	– Chip Enable Lower Byte
$\overline{\text{WE}}$	– Write Enable
$\overline{\text{OE}}$	– Output Enable
$V_{CC}$	– Power Supply (+5V)
GND	– Ground

**DESCRIPTION**

The DS1658 128K x 16 NV SRAMs are 2,097,152 bit fully static, nonvolatile SRAMs, organized as 131,072 words by 16 bits. Each NV SRAM has a self contained lithium energy source and control circuitry which constantly monitors  $V_{CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. In addition, the DS1658 has the ability to unconditionally

write protect blocks of memory so that inadvertent write cycles do not corrupt programs and important data. DS1658 devices can be used in place of solutions which build nonvolatile 128K x 16 memory by utilizing a variety of discrete components. There is no limit on the number of write cycles that can be executed, and no additional support circuitry is required for microprocessor interfacing.

**READ MODE**

The DS1658 devices execute a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high), either/both of  $\overline{CEU}$  or  $\overline{CEL}$  (Chip Enables) are active (low) and  $\overline{OE}$  (Output Enable) is active low. The unique address specified by the 17 address inputs (A0–A16) defines which of the 131,072 words of data is to be accessed. The status of  $\overline{CEU}$  and  $\overline{CEL}$  determines whether all or part of the addressed word is accessed. If  $\overline{CEU}$  is active with  $\overline{CEL}$  inactive, then only the upper byte of the addressed word is accessed. If  $\overline{CEU}$  is inactive with  $\overline{CEL}$  active, then only the lower byte of the addressed word is accessed. If both the  $\overline{CEU}$  and  $\overline{CEL}$  inputs are active (low), then the entire 16-bit word is accessed. Valid data will be available to the 16 data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CEU}$ ,  $\overline{CEL}$  and  $\overline{OE}$  access times are also satisfied. If  $\overline{OE}$ ,  $\overline{CEU}$ , and  $\overline{CEL}$  access times are not satisfied, then data access must be measured from the later occurring signal, and the limiting parameter is either  $t_{CO}$  for  $\overline{CEU}$ ,  $\overline{CEL}$ , or  $t_{OE}$  for  $\overline{OE}$  rather than address access.

**WRITE MODE**

The DS1658 devices execute a write cycle whenever  $\overline{WE}$  and either/both of  $\overline{CEU}$  or  $\overline{CEL}$  are active (low) after address inputs are stable. The unique address specified by the 17 address inputs (A0–A16) defines which of the 131,072 words of data is accessed. The status of  $\overline{CEU}$  and  $\overline{CEL}$  determines whether all or part of the addressed word is accessed. If  $\overline{CEU}$  is active with  $\overline{CEL}$  inactive, then only the upper byte of the addressed word is accessed. If  $\overline{CEU}$  is inactive with  $\overline{CEL}$  active, then only the lower byte of the addressed word is accessed. If both the  $\overline{CEU}$  and  $\overline{CEL}$  inputs are active (low), then the entire 16-bit word is accessed. The write cycle is terminated by the earlier rising edge of  $\overline{CEU}$  and/or  $\overline{CEL}$ , or  $\overline{WE}$ . All address inputs must be kept valid throughout the write cycle.  $\overline{WE}$  must return to the high state for a minimum recovery time ( $t_{WR}$ ) before another cycle can be initiated. The  $\overline{OE}$  control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ( $\overline{CEU}$  and/or  $\overline{CEL}$ , and  $\overline{OE}$  active) then  $\overline{WE}$  will disable outputs in  $t_{ODW}$  from its falling edge.

**READ/WRITE FUNCTION Table 1**

$\overline{OE}$	$\overline{WE}$	$\overline{CEL}$	$\overline{CEU}$	V <sub>CC</sub> CURRENT	DQ0–DQ7	DQ8–DQ15	CYCLE PERFORMED
H	H	X	X	I <sub>CCO</sub>	High–Z	High–Z	Output Disabled
L	H	L	L	I <sub>CCO</sub>	Output	Output	Read Cycle
L	H	L	H		Output	High–Z	
L	H	H	L		High–Z	Output	
X	L	L	L	I <sub>CCO</sub>	Input	Input	Write Cycle
X	L	L	H		Input	High–Z	
X	L	H	L		High–Z	Input	
X	X	H	H	I <sub>CCS</sub>	High–Z	High–Z	Output Disabled

### DATA RETENTION MODE

The DS1658AB provides full functional capability for  $V_{CC}$  greater than 4.75 volts, and write protects by 4.5 volts. The DS1658Y provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The nonvolatile static RAMs constantly monitor  $V_{CC}$ . Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.75 volts for the DS1658AB and 4.5 volts for the DS1658Y.

### FRESHNESS SEAL

Each DS1658 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When  $V_{CC}$  is first applied and remains at a level of greater than  $V_{TP}$ , the lithium energy source is enabled for battery backup operation.

### PARTITION PROGRAMMING MODE

The register controlling the partitioning logic is selected by recognition of a specific binary pattern which is sent

on address lines A13–A16. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles, using both  $\overline{CEU}$  and  $\overline{CEL}$ , with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycles will load the partition register. Since there are 16 protectable partitions, the size of each partition is 128K/16 or 8K x 16. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycles as defined by A13 through A16 and shown in Table 2. A logical 1 in a bit location write protects the corresponding partition. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A14 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1658 devices to internally inhibit  $\overline{WE}$  for all write accesses where A16 A15 A14 A13=0101. Note that while programming the partition register, data which is being accessed from the RAM should be ignored, since the purpose of the 24 read cycles is to program the partition register, not to read data from RAM.

**PATTERN MATCH TO WRITE PARTITION REGISTER Table 2**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A13	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A14	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A15	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A16	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST BITS ENTERED

**PARTITION REGISTER MAPPING Table 3**

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A <sub>16</sub> A <sub>15</sub> A <sub>14</sub> A <sub>13</sub> )
A13	BIT 21	PARTITION 0	0000
A14	BIT 21	PARTITION 1	0001
A15	BIT 21	PARTITION 2	0010
A16	BIT 21	PARTITION 3	0011
A13	BIT 22	PARTITION 4	0100
A14	BIT 22	PARTITION 5	0101
A15	BIT 22	PARTITION 6	0110
A16	BIT 22	PARTITION 7	0111
A13	BIT 23	PARTITION 8	1000
A14	BIT 23	PARTITION 9	1001
A15	BIT 23	PARTITION 10	1010
A16	BIT 23	PARTITION 11	1011
A13	BIT 24	PARTITION 12	1100
A14	BIT 24	PARTITION 13	1101
A15	BIT 24	PARTITION 14	1110
A16	BIT 24	PARTITION 15	1111

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground

-0.3V to 7.0V

Operating Temperature

0°C to +70°C, -40°C to +85°C for IND parts

Storage Temperature

-40°C to +70°C, -40°C to +85°C for IND parts

Soldering Temperature

260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**(t<sub>A</sub>: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1658Y Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	
DS1658AB Power Supply Voltage	V <sub>CC</sub>	4.75	5.0	5.25	V	
Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub>	V	
Logic 0	V <sub>IL</sub>	0.0		+0.8	V	

**DC ELECTRICAL CHARACTERISTICS**(V<sub>CC</sub>=5V ± 5% for DS1658AB)  
(t<sub>A</sub>: See Note 10) (V<sub>CC</sub>=5V ± 10% for DS1658Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I <sub>IL</sub>	-2.0		+2.0	μA	
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	I <sub>IO</sub>	-1.0		+1.0	μA	
Output Current @ 2.4V	I <sub>OH</sub>	-1.0			mA	
Output Current @ 0.4V	I <sub>OL</sub>	2.0			mA	
Standby Current $\overline{CEU}$ , $\overline{CEL}=2.2V$	I <sub>CCS1</sub>		10	20	mA	
Standby Current $\overline{CEU}$ , $\overline{CEL}=V_{CC} - 0.5V$	I <sub>CCS2</sub>		6	10	mA	
Operating Current	I <sub>CCO1</sub>			170	mA	
Write Protection Voltage (DS1658Y)	V <sub>TP</sub>	4.25	4.37	4.5	V	
Write Protection Voltage (ds1658AB)	V <sub>TP</sub>	4.50	4.62	4.75	V	

**CAPACITANCE**(t<sub>A</sub> = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		20	25	pF	
Input/Output Capacitance	C <sub>I/O</sub>		5	10	pF	

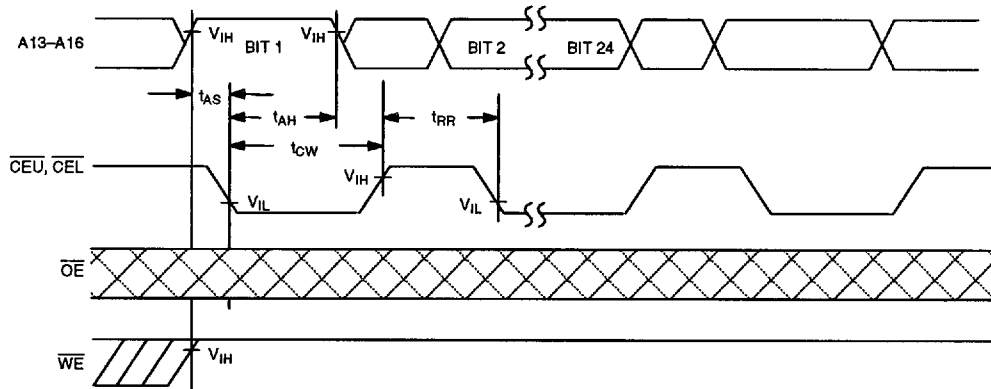
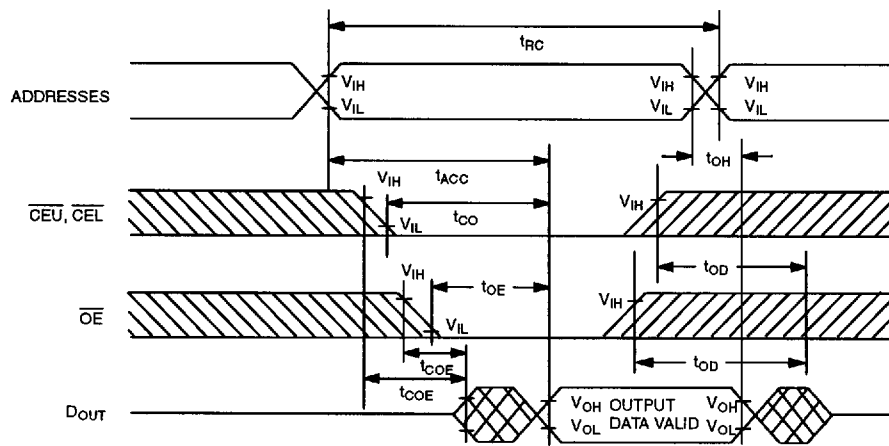
**AC ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub>=5V ± 5% for DS1658AB)  
(t<sub>A</sub>: See Note 10) (V<sub>CC</sub>=5V ± 10% for DS1658Y)

PARAMETER	SYMBOL	DS1658Y-70 DS1658AB-70		DS1658Y-100 DS1658AB-100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t <sub>RC</sub>	70		100		ns	
Access Time	t <sub>ACC</sub>		70		100	ns	
$\overline{OE}$ to Output Valid	t <sub>OE</sub>		35		50	ns	
$\overline{CE}$ to Output Valid	t <sub>CO</sub>		70		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t <sub>COE</sub>	5		5		ns	5
Output High Z from Deselection	t <sub>OD</sub>		25		35	ns	5
Output Hold from Address Change	t <sub>OH</sub>	5		5		ns	
Write Cycle Time	t <sub>WC</sub>	70		100		ns	
Write Pulse Width	t <sub>WP</sub>	55		75		ns	3
Address Setup Time	t <sub>AW</sub>	0		0		ns	
Write Recovery Time	t <sub>WR1</sub>	10		10		ns	12
	t <sub>WR2</sub>	10		10		ns	13
Output High Z from $\overline{WE}$	t <sub>ODW</sub>		25		35	ns	5
Output Active from $\overline{WE}$	t <sub>OEW</sub>	5		5		ns	5
Data Setup Time	t <sub>DS</sub>	30		40		ns	4
Data Hold Time	t <sub>DH1</sub>	5		5		ns	12
	t <sub>DH2</sub>	5		5		ns	13

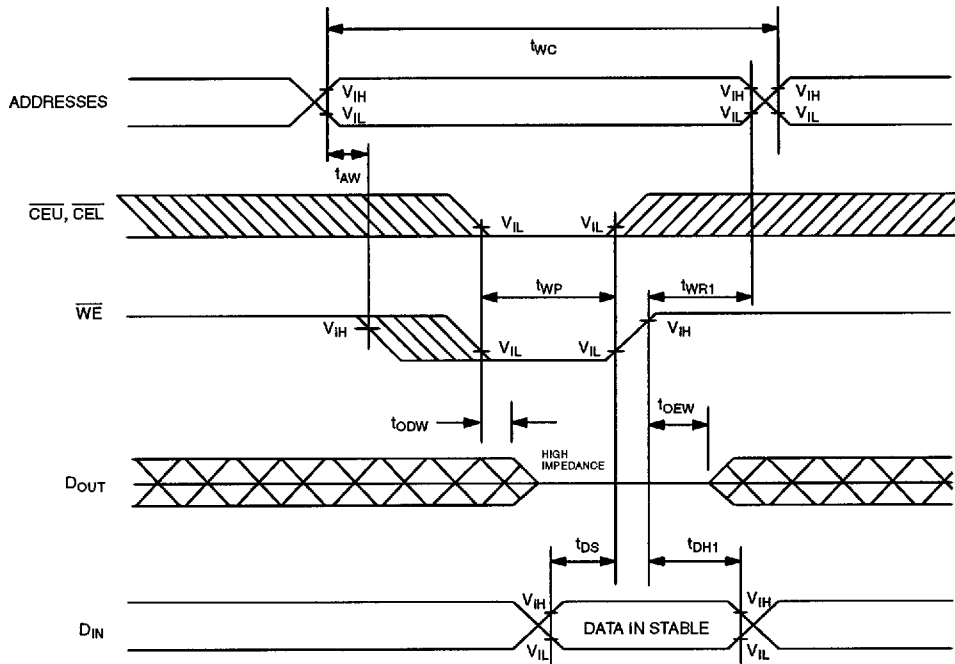
**AC ELECTRICAL CHARACTERISTICS** (t<sub>A</sub>: See Note 10) (V<sub>CC</sub>=4.5V to 5.5V)\*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t <sub>AS</sub>	0			ns	
Address Hold	t <sub>AH</sub>	50			ns	
Read Recovery	t <sub>RR</sub>	20			ns	
$\overline{CE}$ Pulse Width	t <sub>CW</sub>	75			ns	

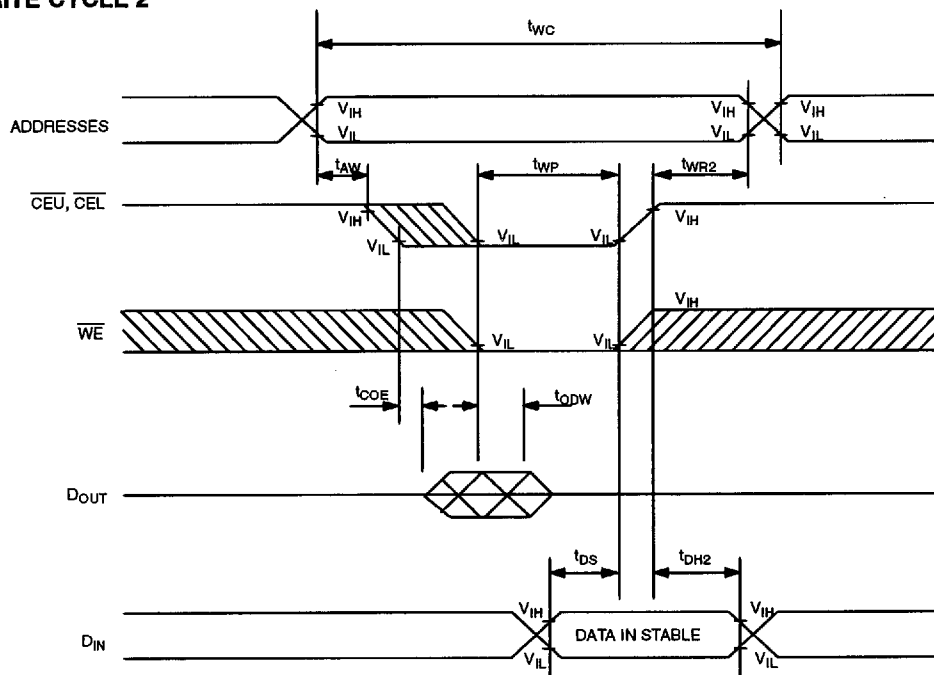
\*For loading partition register

**TIMING DIAGRAM: LOADING PARTITION REGISTER****READ CYCLE**

SEE NOTE 1

**WRITE CYCLE 1**

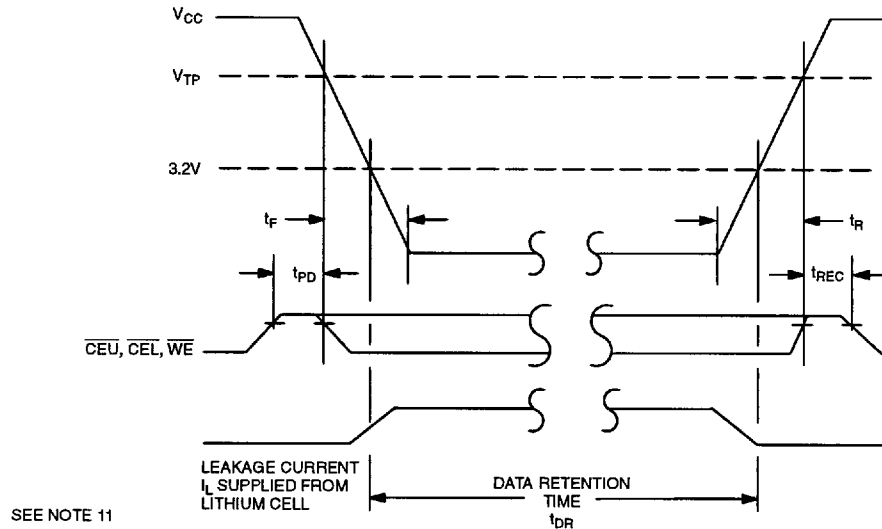
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

**WRITE CYCLE 2**

SEE NOTES 2, 3, 4, 6, 7, 8 AND 13



## POWER-DOWN/POWER-UP CONDITION



## POWER-DOWN/POWER-UP TIMING

(t<sub>A</sub>: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{\text{CEU}}, \overline{\text{CEL}}, \overline{\text{WE}}$ at V <sub>IH</sub> before Power-Down	t <sub>PD</sub>	0			μs	11
V <sub>CC</sub> Slew from V <sub>TP</sub> to 0V (CE at V <sub>IH</sub> )	t <sub>F</sub>	300			μs	
V <sub>CC</sub> Slew from 0V to V <sub>TP</sub> (CE at V <sub>IH</sub> )	t <sub>R</sub>	0			μs	
$\overline{\text{CEU}}, \overline{\text{CEL}}, \overline{\text{WE}}$ at V <sub>IH</sub> after Power-Up	t <sub>REC</sub>	25		125	ms	

(t<sub>A</sub> = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t <sub>DR</sub>	10			years	9

## WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

## NOTES:

1.  $\overline{\text{WE}}$  is high for a read cycle.
2.  $\overline{\text{OE}} = \text{V}_{\text{IH}}$  or  $\text{V}_{\text{IL}}$ . If  $\overline{\text{OE}} = \text{V}_{\text{IH}}$  during write cycle, the output buffers remain in a high impedance state.
3. t<sub>WP</sub> is specified as the logical AND of  $\overline{\text{CEU}}$  or  $\overline{\text{CEL}}$  and  $\overline{\text{WE}}$ . t<sub>WP</sub> is measured from the latter of  $\overline{\text{CEU}}$ ,  $\overline{\text{CEL}}$  or  $\overline{\text{WE}}$  going low to the earlier of  $\overline{\text{CEU}}$ ,  $\overline{\text{CEL}}$  or  $\overline{\text{WE}}$  going high.

4.  $t_{DS}$  is measured from the earlier of  $\overline{CEU}$  or  $\overline{CEL}$  or  $\overline{WE}$  going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the  $\overline{CEU}$  or  $\overline{CEL}$  low transition occurs simultaneously with or later than the  $\overline{WE}$  low transition, the output buffers remain in a high impedance state during this period.
7. If the  $\overline{CEU}$  or  $\overline{CEL}$  high transition occurs prior to or simultaneously with the  $\overline{WE}$  high transition, the output buffers remain in high impedance state during this period.
8. If  $\overline{WE}$  is low or the  $\overline{WE}$  low transition occurs prior to or simultaneously with the  $\overline{CEU}$  or  $\overline{CEL}$  low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1658 has a built-in switch that disconnects the lithium source until  $V_{CC}$  is first applied by the user. The expected  $t_{DR}$  is defined as accumulative time in the absence of  $V_{CC}$  starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is -40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on  $V_{CC}$ .
12.  $t_{WR1}$ ,  $t_{DH1}$  are measured from  $\overline{WE}$  going high.
13.  $t_{WR2}$ ,  $t_{DH2}$  are measured from  $\overline{CEU}$  OR  $\overline{CEL}$  going high.

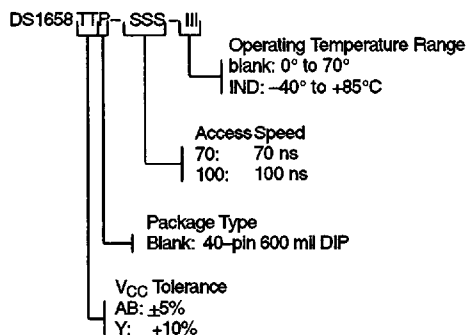
#### DC TEST CONDITIONS

Outputs Open  
 Cycle = 200 ns  
 All voltages are referenced to ground

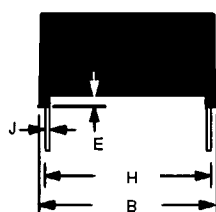
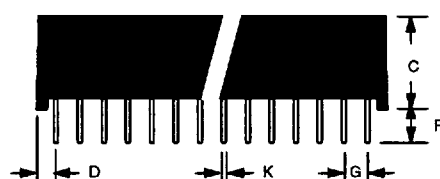
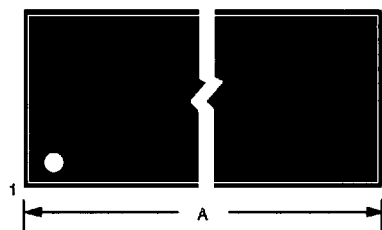
#### AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate  
 Input Pulse Levels:  
 0.0 to 3.0 volts  
 Timing Measurement Reference Levels  
 Input: 1.5V  
 Output: 1.5V  
 Input Pulse Rise and Fall Times: 5 ns

#### ORDERING INFORMATION



## DS1658Y/AB NONVOLATILE SRAM, 40-PIN 740 MIL EXTENDED MODULE



PKG	40-PIN	
DIM	MIN	MAX
A IN. MM	2.080 52.83	2.100 53.34
B IN. MM	0.715 18.16	0.740 18.80
C IN. MM	0.345 8.76	0.365 9.27
D IN. MM	0.085 2.16	0.115 2.92
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.120 3.05	0.160 4.06
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.43	0.025 0.58