Preliminary Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

LUC3X01
100Base-T4 Physical Layer Device

Features and Benefits

- VLSI CMOS Physical Layer Device supports the *IEEE** 802.3u, 100Base-T4 CSMA/CD specification.
- Works with four-pair UTP cable enabling (CAT3) 100 Mbits/s transmission over 10Base-T wiring installations:
  - — Three on-chip transmitters and receivers for data transmission with a smart squelch† for collision detection.
  - — Uses ternary line coding (8B6T) to provide a low baud rate for FCC conformance.
- Designed for use in both adapter card and repeater applications:
  - — Direct connection to the 802.3u media-independent interface (MII).
  - — On-chip encoder/decoder can be bypassed to minimize latency in repeater applications.
  - — A common system clock can be used to drive multiple LUC3X01s, which minimizes cost in repeater applications.
- High level of integration.
- Management features provide extensive diagnostics and improve ease of use:
  - — Management interface provides status information and configuration control.
  - — Loopback function provides for system diagnostics capability.
  - — Autopolarity indication and correction simplifies installation.
  - — Support of Auto-Negotiation.
- Fabricated in a low-power CMOS technology requiring a single 5 V supply.
- 84-pin PLCC.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
† Patented by Lucent Technologies Inc. Patent #5,199,049.

Description

The LUC3X01 device implements the physical layer of the *IEEE* 802.3u 100 Mbits/s CSMA/CD Fast Ethernet LAN specification. All of the transceiver functions required to implement one complete physical layer are provided. The LUC3X01 block diagram is shown in Figure 1. The chip consists of five major sections: receiver, transmitter, collision detect and link control, management interface, and internal loopback. Each LUC3X01 contains three active receive channels and three active transmit channels that are coupled through transformers to four pairs of category 3, 4, or 5 UTP cable. Two pairs are bidirectional and are used for data transmission in each direction, one pair is dedicated for transmission, and one pair is dedicated for reception, in order to achieve robust collision detection. The 8B6T ternary (three-level) data encoding scheme is used to reduce the signaling rate on each twisted-pair cable to 25 Msymbols/s (25 MHz clock rate) for FCC emissions conformance.

The LUC3X01 is a versatile building block for 100Base-T4 systems and can be used in the following applications:

- Adapter cards
- Switching hubs
- Motherboards
- Repeaters
  - — Transparent
  - — Translating
- Bridges
- Routers

Note: Advisories are issued as needed to update product information. When using this data sheet for design purposes, please contact your Lucent Technologies Microelectronics Group Account Manager to obtain the latest advisory on this product.

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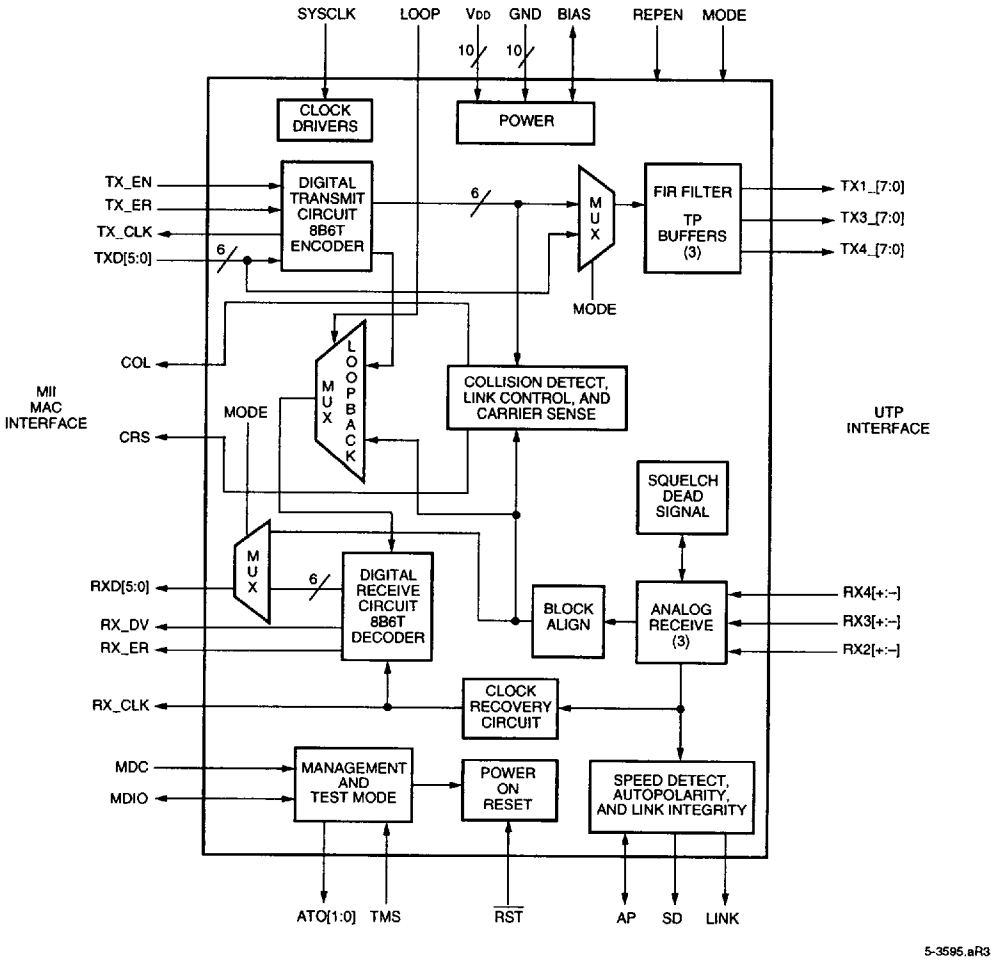


Figure 1. LUC3X01 Functional Block Diagram

Pin Information

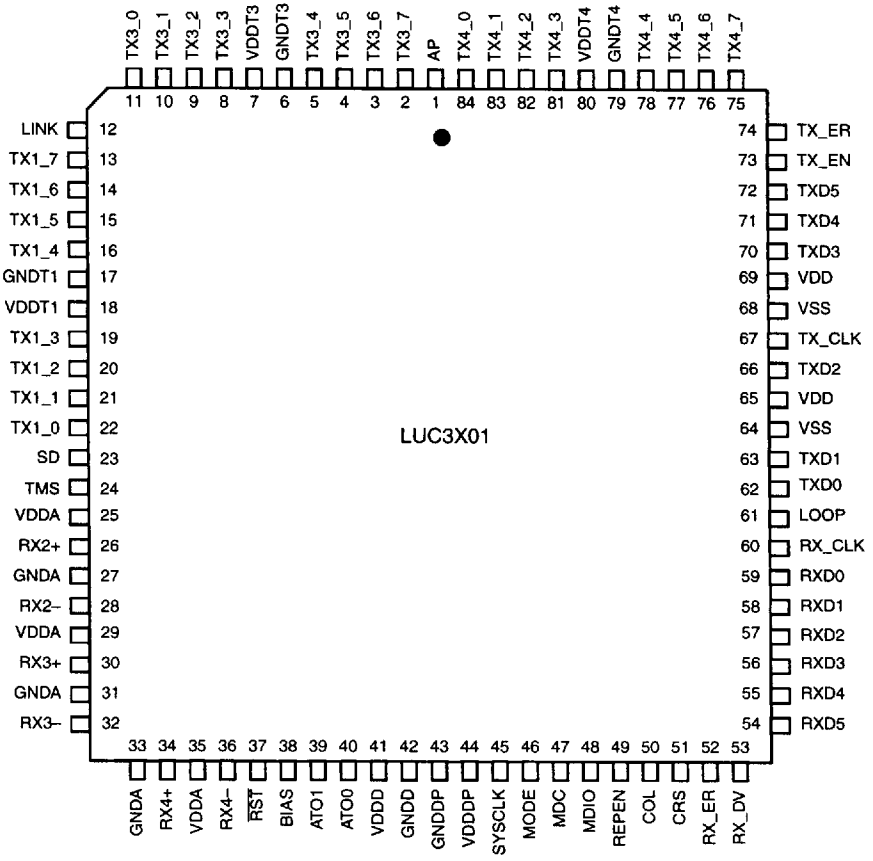


Figure 2. Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	Type*	Name/Description
45	SYSCLK	I-D	**System Clock.** This is a CMOS clock input of 25 MHz ± 100 ppm, with a worst-case 40%—60% duty cycle. This clock must be present at all times.
67	TX_CLK	O-MII	**Transmit Clock.** This output is a delayed version of SYSCLK. It will have a duty cycle no worse than 40%—60%. The inputs TXD[5:0] and TX_EN are sampled on the rising edge of TX_CLK. This pin is not used in repeater mode.
62—63 66 70—72	TXD[5:0]	I-MII	**Transmit Data.** In DTE mode, pins [3:0] are used to input unencoded NRZ data in nibble format, and pins [5:4] are ignored and should be tied LOW. In repeater mode, pins [5:0] are used to serially input the digital representation of the 8B6T encoded data for transmission onto the respective device channel. These pins are sampled on the rising edge of TX_CLK in DTE mode and SYSCLK in repeater mode.
73	TX_EN	I-MII	**Transmit Enable.** This input should be driven HIGH when the inputs TXD[5:0] contain valid data.
74	TX_ER	I-MII	**Transmit Error.** This input, valid in DTE mode only, causes the encoder to intentionally corrupt the byte being transferred across the MII when this signal is driven HIGH. This input is not used when the device is placed in repeater mode.
13—16 19—22 2—5 8—11 75—78 81—84	TX[1, 3, 4]_[7:0]	O-A	**UTP Data Outputs.** These outputs, three sets of eight pins each, are used for driving the ternary data onto the three physical wire pairs. They are combined off-chip using summing resistors. Each pin is driven with a digital buffer whose source resistance is 10 Ω or less and whose rise/fall times are between 2 ns and 12 ns.
26, 28, 30, 32, 34, 36	RX[2,3,4]+,–	I-A	**UTP Data Inputs.** Each pair is ac-coupled to the off-chip analog filter output which itself interfaces to the UTP wire media. These analog differential inputs have an input resistance of greater than 10 kΩ. The common-mode voltage for these pins is generated on chip. The maximum differential input amplitude should be limited to 3.85 V differential peak. The differential input signal has a positive polarity when the voltage at the RX+ pin with respect to ground is larger than the voltage at the RX– pin.
60	RX_CLK	O-MII	**Receive Clock.** This output clock is derived from the data received on device channel RX_D2. It is nominally 25 MHz and is asserted HIGH or LOW during clock acquisition at the beginning of a new receive packet. The outputs RXD[5:0], RX_DV, and RX_ER should be sampled on the rising edge of RX_CLK. This pin is 3-stated when the part is in repeater mode and REPEN is low.
54—59	RXD[5:0]	O-MII	**Receive Data.** In DTE mode, pins [3:0] are used to output decoded NRZ data in nibble format, and pins [5:4] are no connects. In repeater mode, pins [5:0] are used to output the digital representation of the 8B6T encoded data to the repeater core for eventual retransmission onto the other ports of the repeater. This pin is 3-stated when operating in repeater mode and REPEN is low.

* See Table 2.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Description
53	RX_DV	O-MII	**Receive Data Valid.** In DTE mode, this pin is driven HIGH when the data on pins RXD[3:0] is considered valid. In repeater mode, this pin is driven active HIGH when the data on pins RXD[5:0] is considered valid. This pin is 3-stated when operating in repeater mode and REPEN is low.
52	RX_ER	O-MII	**Receive Data Error.** This pin goes HIGH, in either DTE or repeater modes, when the part determines there is an error in the receive data. The output may go HIGH multiple times during the reception of a single packet. This pin is 3-stated when operating in repeater mode and REPEN is low.
51	CRS	O-MII I-A	**Carrier Sense.** This is driven active HIGH whenever there is either transmit or receive activity on the wire. It is an asynchronous output that is the logical OR of TX_EN and receive activity. CRS is asserted when TX_EN is asserted in loopback mode. This pin is also used to set the <PHYAD>, bit 2, (see Table 12) in the management interface by using an external programming resistor.
50	COL	O-MII	**Collision.** This is driven active HIGH whenever there is transmit and receive activity on the UTP media. It is essentially the logical AND of TX_EN and receive activity and is an asynchronous output. This pin is 3-stated when operating in repeater mode and REPEN is low.
46	MODE	I-D	**Mode of Operation.** A logical LOW input configures the device for operation in DTE mode, and a logical HIGH input configures the part for repeater mode operation. An internal pull-down resistor causes this input to be set for the default mode of DTE operation if the pin is left unconnected.
12	LINK	O-D I-A	**Link Pass.** This output is driven HIGH if the part determines that the link is a 100Base-T4 link and link pulses are successfully being received from the other end of the link segment. Otherwise, it is asserted low. This pin is also used to set the <PHYAD>, bit 3, (see Table 12) in the management interface by using an external programming resistor.
23	SD	O-D	**Speed Detect.** This output is driven logical HIGH if the part determines that the link is intended for 100Base-T4 operation. It is driven logical LOW otherwise. This pin is also used to set the <PHYAD>, bit 4, (MSB) (see Table 12) in the management interface by using an external programming resistor.
1	AP	IO-A I-A	**Autopolarity.** This is a dual-function pin that enables and displays the status or disables the autopolarity function. This function is enabled if the pin is left floating. This function is disabled if the pin is driven LOW. **WARNING: Under no circumstances should this pin be shorted to V_{DD}. Either a series resistor or LED must always be used.**
37	$\overline{RST}$	I-D	**Reset (Active-Low).** This pin must be driven LOW for a minimum of 200 ns to assert an internal full-chip reset, which has a duration of 500 ms. During a reset, all activity at the input pins will be ignored. The device will also be internally reset at powerup, and may be reset through the management interface. This pin requires a 10 kΩ pull-up resistor. All outputs are 3-stated when $\overline{RST}$ is asserted low.

* See Table 2.

Section 3.1

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Description
24	TMS	I-D	**Test Mode Select.** This input, with an internal pull-down resistor, configures the part for normal operation when the pin is logical LOW. If the pin is externally driven logical HIGH, the part will be placed into an internal test mode. The internal test mode is used for production testing of the device only.
47	MDC	I-MII	**Management Data Clock.** This is a clock input of 1 MHz—2.5 MHz. The input/output MDIO will be driven off the falling edge of MDC when MDIO is in the output mode. MDIO will be sampled on the rising edge of MDC when MDIO is in the input mode.
48	MDIO	IO-MII	**Management Data Input/Output.** A serial input/output of management data on the MII.
39, 40	ATO[1:0]	O-A I-A	**Analog Test Outputs (PHY Address Inputs).** These pins are used to set the <PHYAD>, ATO[1] bit 1, ATO[0] bit 0, (see Table 12) in the management frame structure and should be pulled either HIGH or LOW through off-chip programming resistors. In internal test mode operation, these analog output pins are used for manufacturing test.
38	BIAS	IO-A	**Bias.** This pin is connected through a 24.9 kΩ ± 1% resistor to ground in order to provide temperature-independent internal biasing of internal analog circuits. Parasitic load capacitance should not exceed 15 pF.
61	LOOP	I-D	**Loopback.** When this input is driven HIGH, the transmit data present at the TXD[5:0] pins will be looped back to the receive path through the PCS receive function and output on RXD[5:0] pins. No data, or link pulses, will be transmitted onto the UTP media when this mode is asserted. This pin has an internal pull-down resistor to provide a default condition of normal transmit and receive functions. If TX_EN is driven HIGH when the part is configured in loopback mode, CRS is asserted, and all wire activity is ignored.
—	(10)VDD	—	**Power.** 5 V ± 5%.
—	(10)GND, VSS	—	**Ground.**
49	REPEN	I-D	**Repeater Enable.** This input enables the digital data outputs RX_DV, RXD[5:0], RX_ER, RX_CLK, and COL, when this input is held logic HIGH. When the part is configured for repeater mode operation (as selected by MODE pin), and the pin is held logic LOW, the above listed outputs are tristated. When operating in DTE mode, this pin must be held low.

* See Table 2.

Table 2. Pin Type Definitions

Name	Description	Name	Description
I-A	Input, analog.	O-MII	Output, media independent interface.
O-A	Output, analog.	IO-A	Input/output, analog.
I-D	Input, digital.	IO-D	Input/output, digital.
O-D	Output, digital.	IO-MII	Input/output, media independent interface.
I-MII	Input, media independent interface.		

Functional Description

Overview

The LUC3X01 is suitable for both DTE station and repeater applications. The protocol utilizes half-duplex transmission over four pairs of category 3, 4, or 5 UTP (100 m maximum length). Figure 3 shows how the four pairs of UTP cables are utilized: two pairs are bidirectional and are used for data transmission in each direction. The other two pairs are unidirectional and are used for transmitting or receiving only. The unidirectional pairs are used for robust collision detection (receive only). Figure 4 shows how the LUC3X01 can be used in a typical DTE application.

DTE Mode

When the LUC3X01 is configured for operation in a station or DTE application, the full functionality of the device is used. The media independent interface (MII) is used to connect the MAC with the circuitry used to transmit and receive signals from the wire media. To transmit data, 8-bit bytes are encoded into blocks of six ternary symbols each. These blocks are then evenly separated into three channels, sent through the pulse shaping FIR filter and then through the transmit buffers that drive off-chip passive circuitry to introduce the ternary symbols onto the media.

In the receive direction, three analog receivers are utilized. Separate squelch and link-integrity circuits ensure proper operation of these functions even with an improperly tuned equalizer. A linear channel properly shapes the received signal for both clock and data recovery. This is done using automatic gain control and an equalizer. The recovered data is realigned so the three data streams are correctly staggered and all in a single clock domain. The three streams are then decoded and passed up to the MAC via the MII interface.

Repeater Mode

When the device is configured for operation in a repeater, only the physical medium attachment (PMA) portion of the device is actually used, the physical coding sublayer (PCS) is bypassed. Those functions normally associated with the PCS are implemented inside the repeater core, if at all.

The transmit operation has the LUC3X01 receiving three staggered streams of transmit data, already encoded into the binary representation of ternary symbols. These streams, which include valid preamble, start of packet (SOP), and end of packet (EOP) sequences, are sent through the pulse shaping FIR filter, and then through the transmit buffers that drive off-chip passive circuitry to introduce the ternary symbols onto the media.

The receiver operation uses the three linear channels to obtain recovered clock and data. These three data streams are then realigned for correct staggering, put into a single clock domain, and driven off-chip for use by the repeater core. (The PCS is again bypassed.)

Functional Description (continued)

Overview (continued)

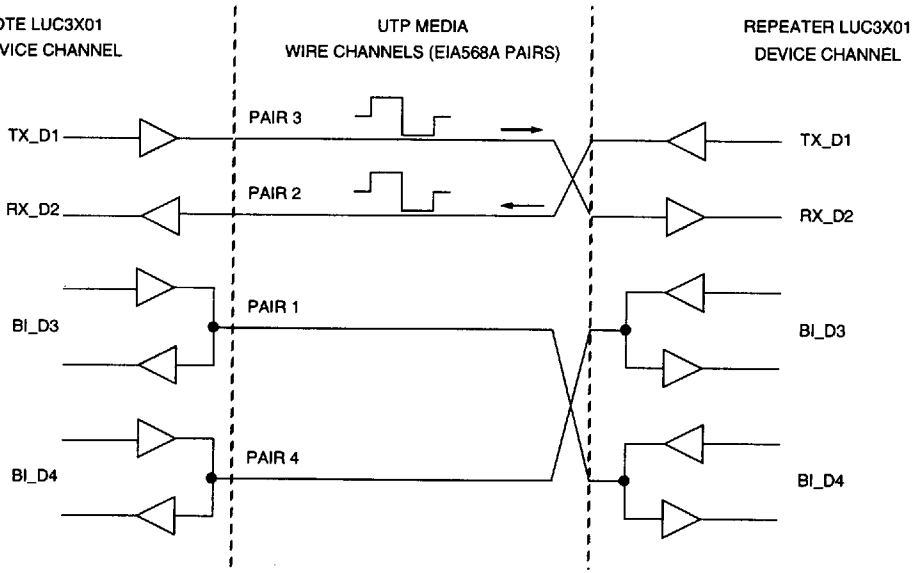
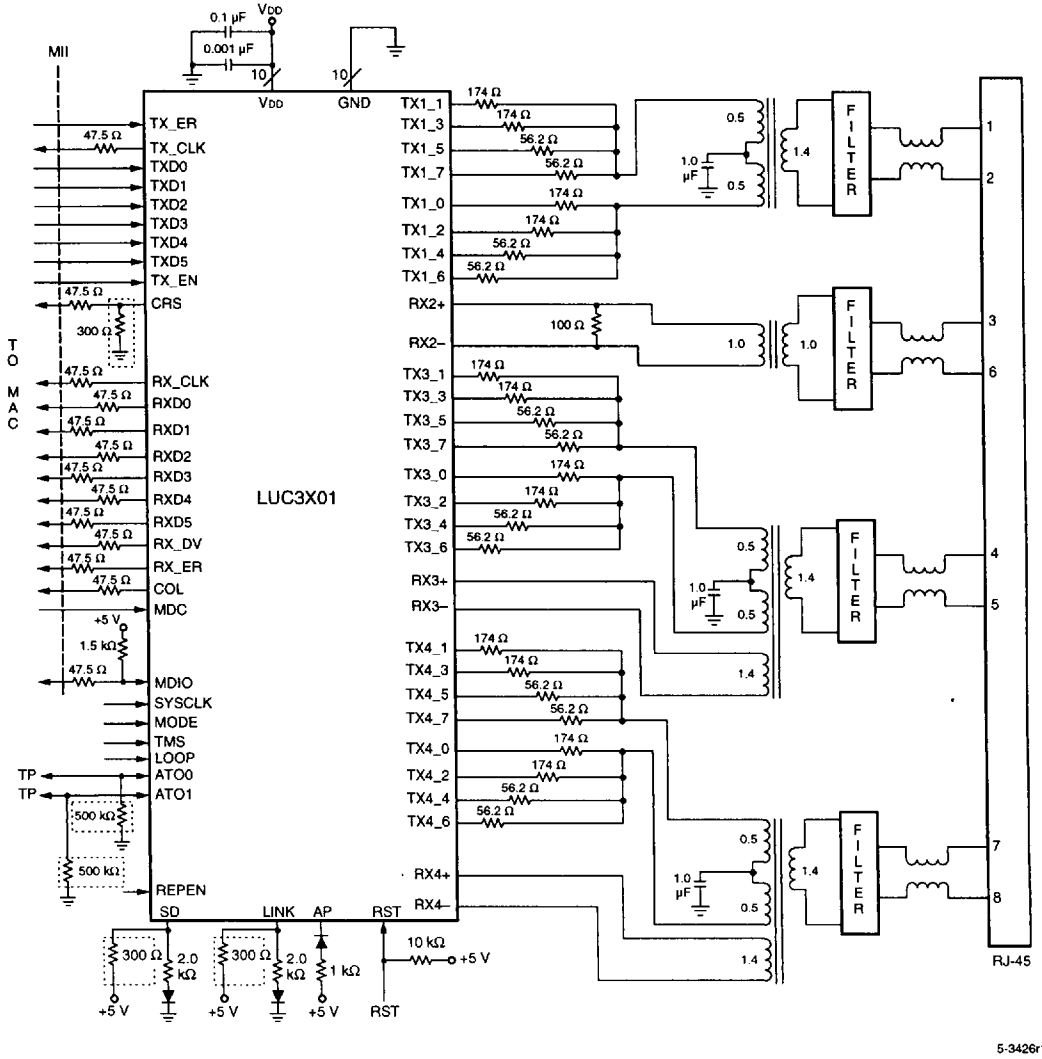


Figure 3. Flow of Ternary Data on a Basic Link Segment

Functional Description (continued)

Overview (continued)



Notes:
The dotted boxes denote <PHYAD> programming resistors.

The 47.5 Ω series MII resistors are for an exposed MII interface. For a nonexposed MII interface (NIC card), 200 Ω series MII resistors should be used to reduce switching transients.

Figure 4. Typical DTE Application

Functional Description (continued)

DTE Mode

This section provides a general description of the function of the LUC3X01 device when configured for operation in the DTE environment.

Figure 1 may prove to be a useful visual aid in understanding the functionality of the device.

Transmit Path

Data transmission begins with the assertion of TX_EN, and ends after the EOP blocks have been appended to the end of the frame.

When TX_EN is asserted, the LUC3X01 begins clocking in the data on TXD[3:0]. The first 8 bytes, sampled nibble by nibble, are replaced by internal codes designed to produce the ternary blocks start of stream A (SOSA) (first 5) and start of stream B (SOSB) (last 3). These bytes are the frame preamble. In addition, the device adds the 100Base-T4 code words P3 and P4 before SOSA on channels BI_D3 and BI_D4, respectively.

All following bytes are, once assembled, clocked through the 8B6T encoder and then serially shifted onto one of the three transmit channels. To allow for pipelining, each transmit channel has its data blocks staggered from the data blocks on the other channels.

At the end of the frame, the encoder function is responsible for appending proper EOP sequences to each of the data streams. The first stream to end is appended with the sequence EOP1 followed by EOP4. The second stream to end is appended with EOP2 followed by EOP5. The third and final data stream to complete data transmission is appended with EOP3 only.

Before actually transmitting a given symbol onto the media, it must be filtered to spectrally shape the pulse. This helps minimize the intersymbol interference at the receiver and improves the bit error rate.

A transformer and filter module connects the signal to the twisted-pair wire providing the required dc isolation and voltage gain. A passive LC doubly terminated filter structure is used which, in addition to providing pulse shaping, reduces the signal energy at frequencies above 30 MHz to help in complying with FCC regulations.

Receive Path

When an incoming frame reaches the LUC3X01, several things happen in parallel until data is decoded. In general, the decoding process is the reverse of the encoding process, in that the staggered streams are recombined, decoded, and then passed across the MII nibble by nibble. In all cases, the preamble at the front of the frame is stripped, and the 802.3 MAC SSD is added as required in DTE mode. Also, the EOP blocks added when the frame was transmitted are not passed onto the MII. The following paragraphs describe in more detail the squelch process, the clock recovery process, and the equalization process, along with data recovery and block alignment. The decoding process and the transmission of data across the MII are also described.

When an incoming frame starts arriving, the LUC3X01 squelch function is responsible for determining whether it is actually a correct frame and not a noise burst. It does this by requiring that the input signal exceed a certain minimum magnitude, often referred to as the squelch voltage. It also requires that the input signal exceed the squelch voltage with specific polarity and timing requirements. This is the smart squelch function. The polarity and timing requirements are chosen so that random thermal noise, NEXT, impulse noise, analog telephony ringing noise, and link-integrity pulses do not cause a false unsquelch or a false assertion of carrier sense. The preamble at the beginning of each incoming frame will unsquelch the LUC3X01 and eventually cause the assertion of carrier status. This is done on each of the three receive channels.

Following the assertion of carrier status, the clock recovery circuitry begins acquiring phase-lock to each of the incoming data streams. In order to correctly decode the data, phase lock is acquired before the receiver sees the start of packet (SOP) which is the last four symbols of SOSB on each channel.

Functional Description (continued)

DTE Mode (continued)

Receive Path (continued)

Prior to incoming data reaching the clock recovery, it passes through an adaptive equalizer which compensates for the distortion caused by the media. The settings of the equalizer are adjusted as often as required based on link pulse amplitudes.

Once the clock recovery has achieved phase-lock, the data stream may be strobed to determine the ternary symbols. The binary representations of these symbols are then justified into a single clock domain, and given the correct staggering between the data streams.

The three streams, which are now correctly staggered and in a single clock domain, are combined into a single stream of ternary symbols. The decoder converts the ternary symbols into binary data which is then clocked, nibble by nibble, across the MII.

Repeater Mode

In repeater applications, each repeater core chip may handle multiple LUC3X01 devices. Repeater core chips may be cascaded to allow for expansion in the number of ports. The data buses of all LUC3X01 devices are connected to all repeater cores to reduce latency. The following characterize the MII connection and operation when the LUC3X01 device is in repeater mode.

- Bus architecture for TXD[5:0], RXD[5:0], RX_DV, RX_ER, and COL pins.
- Unconnected TX_CLK; all devices, including repeater core, are driven by a single version of SYSCLK to ensure no setup/hold time violations between chips.
- Independent (dedicated) connection to the repeater core of the following pins: TX_EN, CRS, MDC, and MDIO.
- Pins RXD[5:0], RS_DV, RX_ER, RX_CLK, and COL are tristated when the pin REPEN is held LOW. When REPEN is HIGH, these pins output received data and the information as indicated.

All other non-MII I/O pins are connected independently.

Transmit Path

The LUC3X01, with the assertion of TX_EN, samples the input binary representation of the three symbol streams at TXD[5:0] using the rising edge of SYSCLK. Because the repeater architecture is expected to be a bus architecture with several LUC3X01s in parallel, the output pin TX_CLK is not used.

The binary representation of the ternary data streams, which have already had SOSA, SOSB, P3, and P4 inserted, and the EOP sequences appended appropriately, are passed to the on-chip digital filter, with the resulting signals being driven off-chip for summation by precision resistors.

Because the three ternary data streams already have the EOP sequences added, the LUC3X01 will stop transmitting when TX_EN is deasserted.

Receive Path

The reception of data from the twisted-pair wire media in the repeater mode is very similar to the operation when the LUC3X01 is configured in DTE mode.

The squelch, equalization, clock, and data recovery functions are exactly the same. The block alignment function is also unchanged. The major differences are the bypassing of the decoding process and the change in functionality of RX_DV and RX_ER.

Functional Description (continued)

Repeater Mode (continued)

Receive Path (continued)

Because of the propagation delay inherent in the decoding process, it is expected that most repeaters will be line-level repeaters, and simply regenerate the received ternary symbols. As such, the decoding process is bypassed in repeater mode. As in the DTE mode, CRS is asserted as soon as the PMA detects incoming preamble on all three channels. RX_DV is asserted with the first valid ternary symbol presented on the pins RXD[5:0]. Also, as in DTE mode, the block alignment function strips all of the preamble and the repeater core regenerates it.

The difference in RX_DV between DTE mode and repeater mode is also seen at the end of a packet. In repeater mode, RX_DV is deasserted when the last symbol of EOP4 has been output on RXD[5:0].

Because the decoding process is bypassed, the errors associated with code violations cannot be detected. Thus, RX_ER is only asserted with an SSD error.

Finally, because the LUC3X013X01 is expected to be connected to the repeater core using a bus architecture, RXD[5:0], RX_DV, RX_ER, RX_CLK, and COL are tristated when the pin REPEN is held LOW. When REPEN is HIGH, these pins output received data.

Operation During a Collision

The following sections describe the basic sequence of events during a collision. The first section describes the effect of a collision on the transmit path in the LUC3X01, and the second section describes the effect of the collision on the receive path.

LUC3X01 Transmitting in Either DTE or Repeater Mode During a Collision

1. COL will be asserted HIGH.
2. The device channels BI_D3 and BI_D4 will transmit ternary 0s.
3. The data stream from the MAC or Repeater Core intended for device channel TX_D1 will be transmitted in its entirety (excepting EOP sequences) until TX_EN deasserts. Data in the 8B6T encoder and/or analog
transmit block pipeline is transmitted.

LUC3X01 Receiving in Either DTE or Repeater Mode During a Collision

1. COL will be asserted HIGH.
2. The analog receivers for device channels BI_D3 and BI_D4 are ignored.
3. The LUC3X01 monitors the received serial 8B6T encoded data stream on device channel RX_D2. If seven consecutive ternary 0 symbols are seen, then CRS is deasserted ending the collision condition.

Section 3.1

Principles of Operation

This section of the document provides a more detailed description of each functional block contained within the device.

Analog Receive Data Function

The analog receive data function brings the differential input signal onto the chip, and adjusts the amplitude (via AGC) and pulse shape (via equalization) to provide a sufficiently open data eye to the slicers. The slicers then obtain the input ternary data pattern, as well as information for the timing recovery. The analog inputs accept a differential peak signal no larger than 3.85 V.

Clock Recovery Function

The clock recovery is responsible for recovering the data on channels RX_D2, BI_D3, and BI_D4 and aligning the data to the recovered clock from channel RX_D2.

Squelch Function

The on-board squelch function is implemented in two parts: the first is the comparator which requires the differential input signal on each device channel to exceed a nominal ±450 mV amplitude; the second is the smart squelch which requires that the signal exceed the above amplitude and occur with certain polarities and at certain time intervals for the squelch function to be turned off, indicating the presence of preamble.

Dead Signal Function

Once the receive path has been unsquelched, due to an incoming data packet, the dead signal function begins looking at the output of the comparators to determine when the incoming data stopped. When 14 or more consecutive zeros have been received, then the part asserts a dead signal condition.

The assertion of the dead signal causes the deassertion of CRS, shutting down the entire receive path.

Link-Integrity Pulse Detect

The 100Base-T4 and Auto-Negotiation link-integrity pulses are transmitted on device channel TX_D1 and received on device channel RX_D2. The squelch function comparator is used to determine if the differential input signal exceeds a predetermined level. If so, a link pulse received message is sent to the appropriate state machine. This function is responsible for detecting two types of link pulses: one is the Auto-Negotiation link pulse; and the other is the 100Base-T4 link pulse.

When the Auto-Negotiation state machine has set link_control = ENABLE or SCAN_FOR_CARRIER, the LI pulse detect function looks for 100Base-T4 link pulses and reports the occurrence of those events to the receive link-integrity (RLI) state machine.

Principles of Operation (continued)

Link-Integrity Pulse Detect (continued)

If the port is configured for operation in loopback mode, or a RESET condition exists, or the device is in power-down mode, all activity at the pins will be ignored, and no link pulses of any polarity or type will be reported as received.

Digital Receive Function

The digital receive function takes the three analog input channels and combines them into one serial data stream. It then decodes the 6T data and outputs the result on the MII interface.

The three received serial data streams of ternary symbols (represented internally by two binary bits each) from the three device channels are combined to output one received data stream of 6T code groups.

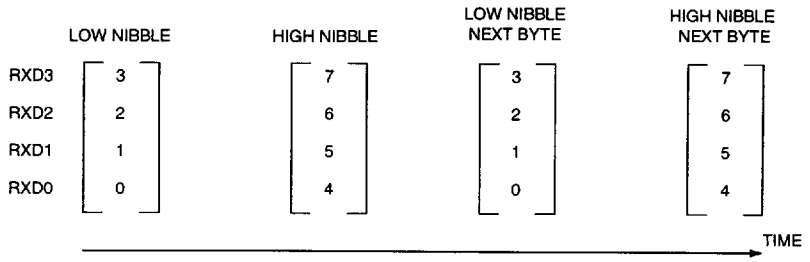
The basic function of the decoder is to decode the received 6T code group data stream into 8-bit binary bytes.

The decoded bytes are converted into 4-bit nibbles which are clocked off-chip synchronously with RX_CLK.

The first RX_CLK cycle will be taken to prestuff both the low- and high-order nibbles (1 byte) with the correct SSD for the 802.3 MAC. These nibbles will then be clocked out, low-order nibble first. Thereafter, the received data stream will be output, low-order nibble first, until the end of the packet.

Data Output (RXD[5:0])

DTE Mode. In DTE mode, only the outputs RXD[3:0] are used and outputs RXD[5:4] are internally grounded to output a logic LOW. The outputs are in nibble format after the conversion operation and come off of the chip with the low-order nibble first. This is shown in Figure 5. The output pins drive full CMOS logic levels.



Note: RXD[5,4] are not used and output a logic LOW.

Figure 5. Receive Data Output (DTE Mode in Nibble Format)

Prior to presenting decoded nibbles to the MII, the LUC3X01 must present both nibbles of the 802.3 MAC SSD as expected by the MAC. This pattern serially is 11010101 with the LSB on the right side. Decoded nibbles presented across the MII in nibble format are as shown in the Table 3.

Principles of Operation (continued)

Digital Receive Function (continued)

Data Output (RXD[3:0]) (continued)

Table 3. Nibble Format

Output	Data Valid Deassertion		Transfer of 802.3 SSD		Transfer of First Decoded Byte Across MII	
RXD3	X	X	0	1	D3	D7
RXD2	X	X	1	1	D2	D6
RXD1	X	X	0	0	D1	D5
RXD0	X	X	1	1	D0	D4
RX_DV	0	0	1	1	1	1

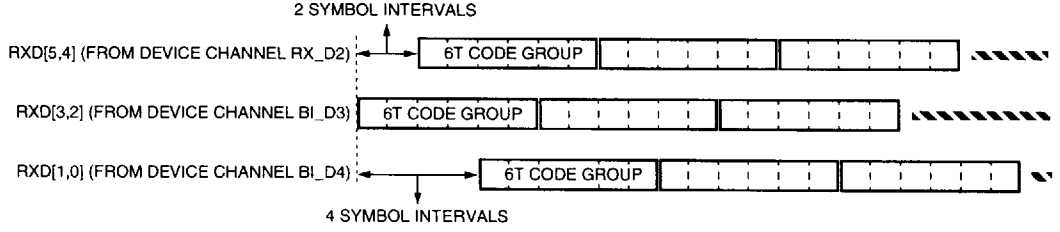
Repeater Mode. In repeater mode, all six pins are used. Each pair of pins (RXD[5, 4], RXD[3, 2], RXD[1, 0]) outputs a binary value corresponding to the value of the ternary symbol received at the input pins. The mapping table is shown in Table 4, and the bit and device channel assignments are shown in Table 5.

Since the three receive device channels have staggered symbol streams, with device channel BI_D3 starting first, the other device channels have (DON'T CARE) values. This is shown in Figure 6.

Because the device is expected to be connected to a bus when configured in this mode, RXD[5:0] output data when the pin REPEN is logic HIGH. When the part is configured in repeater mode and REPEN is LOW, these outputs are tristated.

Table 4. Repeater Mode Mapping

Voltage	Ternary Logic Symbol	MSB RXD[5,3,1}	LSB RXD{4,2,0]
–3.5 V	–1 or –	1	0
0 V*	0	0	0
+3.5 V	+1 or +	0	1



Notes:
Preamble has been stripped.

6T code groups are in 2-bit binary representation.

Figure 6. Receive Output Staggered Data Streams in Repeater Mode

Principles of Operation (continued)

Digital Receive Function (continued)

Data Output (RXD[5:0]) (continued)

The assignment of the individual bits for each device channel to the pins used to drive the receive data off-chip is shown in Table 5.

Table 5. Bit and Device Channel Assignments

Pin Name	Device Channel	Bit
RXD5	RX_D2	MSB
RXD4	RX_D2	LSB
RXD3	BI_D4	MSB
RXD2	BI_D4	LSB
RXD1	BI_D3	MSB
RXD0	BI_D3	LSB

Receive Data Valid

The RX_DV pin asserts a logical HIGH when the part considers the data on the RXD[5:0] to be valid. This signal is synchronous with the rising edge of RX_CLK.

DTE Mode. In DTE mode, the RX_DV pin is asserted synchronously with the first valid nibble of data (preamble or 802.3 MAC SSD) to be presented on outputs RXD[3:0]. It is deasserted (logical LOW) on the first rising edge of RX_CLK after the last nibble of valid data has been presented to the MII. RX_DV will also be deasserted by the detection of seven consecutive zeros on channel RX_D2 when, for example, there is a collision.

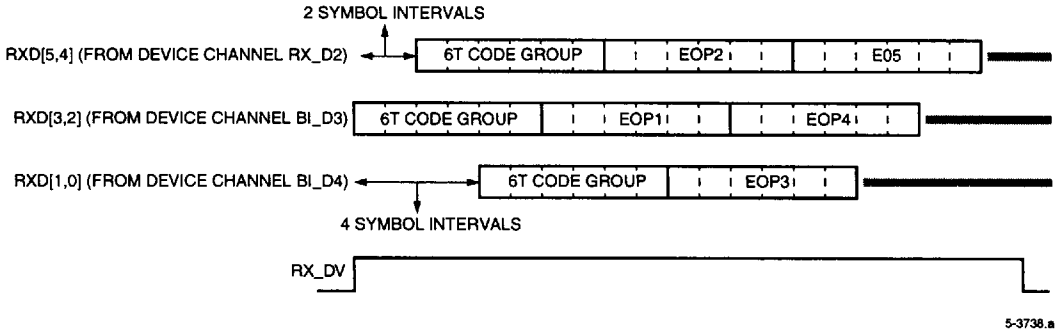
Repeater Mode. When the device is configured in repeater mode, RX_DV is asserted synchronously with RX_CLK with the first nonpreamble, non-SOP symbol on any of the three receive device channels, provided the pin REPEN is logic HIGH. If the pin REPEN is logic LOW when the part is in repeater mode, the output RX_DV is tristated.

The output RX_DV is deasserted after the last symbol of EOP4 has been output on RXD[5:0].

Principles of Operation (continued)

Digital Receive Function (continued)

Receive Data Valid (continued)



Notes:
Preamble has been stripped.

EOP 1—5 may occur on any device channel.

6T code groups are in 2-bit binary representation.

Example above for unrealistic short packet.

Figure 7. Receive Data Valid Signal in Repeater Mode

Receive Data Error

The RX_ER pin is asserted when there is an error in the received data stream.

DTE Mode. When configured in this mode, the LUC3X01 will identify and report four errors associated with receiving a packet. These errors are as follows:

- A skew error during frame alignment. If the skew_error being reported is due to the skew between receiving channels exceeding 60 ns, or a corrupted SOP, RX_ER will be asserted for the entire packet.
- An EOP violation. RX_ER must be asserted during the transfer of the last decoded data nibble across the MII*.
- A dc balance violation. RX_ER must be asserted during the transfer of both affected data nibbles across the MII.
- An 8B6T code violation. RX_ER must be asserted during the transfer of both affected data nibbles across the MII.

These errors can occur on any of the three receive device channels.

Repeater Mode. When configured in this mode, the LUC3X01 does not decode the 8B6T data, and thus only skew error during frame alignment is reported.

RX_ER output is tristated unless the REPEN pin is held logic HIGH when the part is configured for operation in repeater mode.

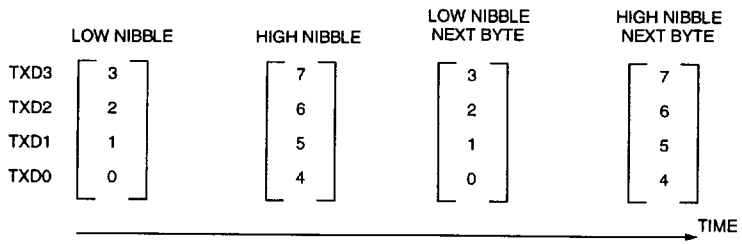
* This is one RX_CLK faster than the other error conditions.

Principles of Operation (continued)

Digital Transmit Function

Input Data (TXD[5:0])

DTE Mode. When the device is configured for operation in a DTE, only pins TXD[3:0] are used to input data in nibble format with the low-order nibble first. Pins TXD[5:4] are not used, and should be shorted to GND off-chip. Figure 8 shows pictorially how the transmit data is brought on chip. TXD[0] is the least significant bit of the nibble.



Note: TXD[5,4] not used.

Figure 8. Transmit Data Input (DTE Mode in Nibble Format)

Repeater Mode. Table 6 identifies which TXDn inputs are associated with which transmit device channel when the device is configured for repeater mode operation.

Table 6. TXDn Inputs

Pin Name	Device Channel	Bit
TXD5	TX_D1	MSB
TXD4	TX_D1	LSB
TXD3	BI_D3	MSB
TXD2	BI_D3	LSB
TXD1	BI_D4	MSB
TXD0	BI_D4	LSB

Transmit Enable (TX_EN)

The common view is that the input signal TX_EN represents a data enable line on a flip-flop. This enables the flip-flop to sample the data on the rising edge of TX_CLK when TX_EN is logical HIGH and the device is configured for DTE mode. When the device is in repeater mode, the data is sampled on the rising edge of SYSCLK. When TX_EN is deasserted, the signals on TXD[5:0] are ignored.

DTE Mode. When the part is configured for DTE mode, TX_EN is expected to go logical HIGH for valid data which includes 802.3 preamble, 802.3 SSD payload, and CRC.

Repeater Mode. When the part is configured for repeater mode, TX_EN is expected to go logical HIGH for valid data which includes the 2-bit binary representation of 8B6T encoded preamble, SOP, payload, CRC, and the EOP sequences.

Because the EOP sequences do not all end at the same time TX_EN will remain asserted until at least one symbol after EOP5. The repeater core will pad the data streams after EOP3, EOP4, and EOP5 with the zero symbol pattern until TX_EN is deasserted.

Principles of Operation (continued)

Digital Transmit Function (continued)

Transmit Error (TX_ER)

This input is valid in the DTE mode only, and the pin is ignored when the part is configured for operation in repeater mode.

TX_ER, which is synchronous with TX_CLK, may be asserted for one or more nibble intervals. For each byte that has one or both nibbles transferred across the MII with TX_ER asserted, the encoder replaces the corresponding 6T code group with an illegal code word. The illegal code word is − − − + + + with the left most symbol transmitted first. This code is not subject to any of the dc balance rules and thus is never transmitted as + + + − − −. When this code is transmitted, the RDS for the device channel over which this code is transmitted is not changed.

If TX_ER is asserted while TX_EN is deasserted, it will be ignored.

8B6T Encoder (DTE Mode only)

The 8B6T encoder, after clocking in the binary data, encodes the correct preamble sequences (SOSA, SOSB, P3, P4) and the raw binary data. Using appropriate rules, the data stream is encoded in such a way that dc balance is maintained on a device channel basis. The ternary symbols, represented in a binary format, are then clocked out on their respective channel with the appropriate EOP sequences.

Analog Transmit Function

This section accepts the digital representation of the ternary symbols from the digital transmitter and launches the symbols onto the media. The section consists of the delay chain for a spectral shaping filter and the eight UTP output buffers.

Filter

The purpose of the filter is to spectrally shape the transmitted pulse shape to ease the burden on the receiver. It is used both in T4 link pulses and the generation of pulse shapes within a packet.

Figure 9 shows the connection of the off-chip summing registers.

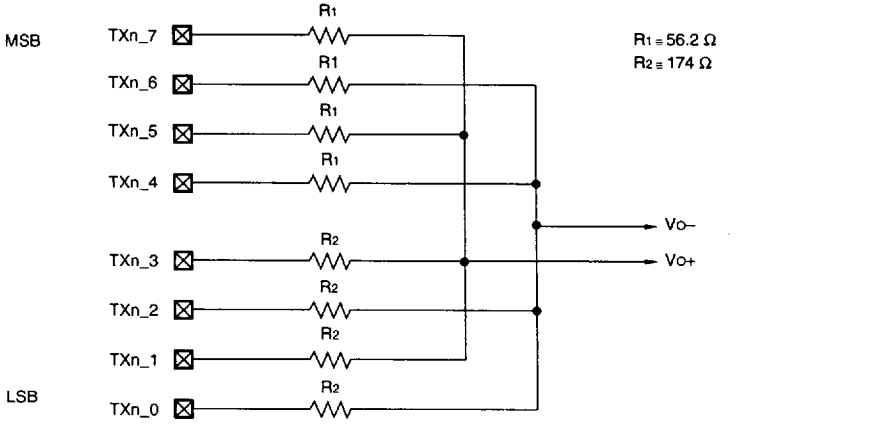


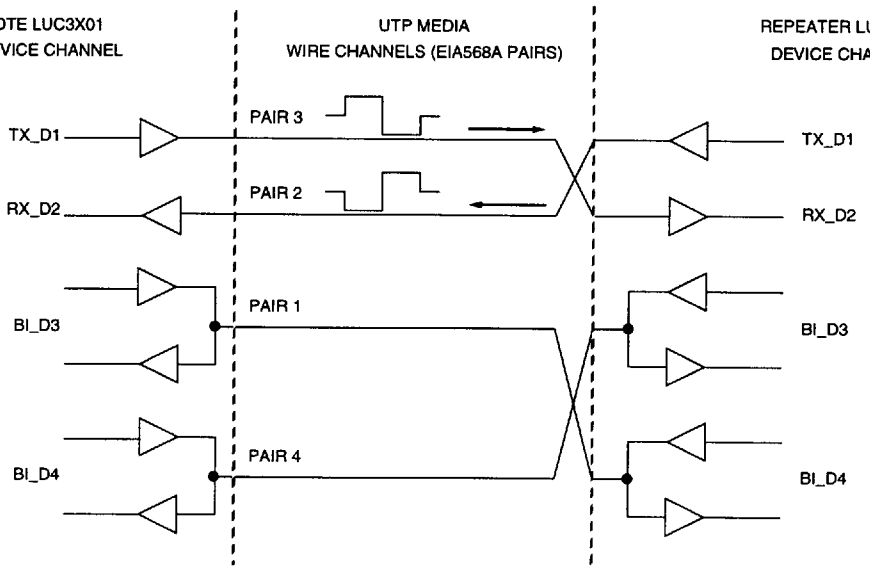
Figure 9. Off-Chip Summing Registers

Principles of Operation (continued)

State Machines

Transmit Link Integrity

The link-integrity pulse is a −1 symbol followed by a +1 symbol and is transmitted on device channel TX_D1 and received on device channel RX_D2 (the wire cross-over is in the repeater). Figure 10 shows the direction of travel of link pulses for a given link segment.



Note: Crossover shown at repeater end.

Figure 10. Flow of Link-Integrity Pulses on a Basic Link Segment

100Base-T4 link-integrity pulses are transmitted every 1.2 ms ± 0.6 ms whenever the state machine is enabled. This timer starts over again after each link pulse is transmitted, or after TX_EN is deasserted following transmission of a packet. The value of the counter is not affected by reception of a packet. In the unlikely event that a link pulse and a packet are to be transmitted at the same time, the transmission of the packet will take precedence.

Auto-Negotiation fast link pulses (FLP) can also be transmitted when required.

Receive Link Integrity

This state machine counts the number of link pulses received by the analog receiver within certain timing windows and determines if the local link between the DTE and hub is up and running with T4 link pulses.

Autopolarity

The device can determine if the receive twisted-pair link has been wired with a polarity reversal. If so, the device automatically corrects for this error condition, when the function is enabled. The AP pin itself can be connected to an LED to display the status of the polarity of the receive twisted-pair link.

Principles of Operation (continued)

Auto-Negotiation

Auto-Negotiation is the means by which two connected nodes agree (if possible) upon the signaling to be used to exchange data between them. Currently, only 100Base-T4 is supported by the LUC3X01 device. It supports the basic Auto-Negotiation function, but does not support next page messaging.

The Auto-Negotiation function uses five registers (two MII registers and three Auto-Negotiation-specific registers):

- MII control (register 0)
- MII status (register 1)
- Auto-Negotiation advertisement (register 4)
- Auto-Negotiation link-partner ability (register 5)
- Auto-Negotiation expansion (register 6)

In register 4, the technology ability field is read-only for all bits. All other bits are hard-coded 0, since no technologies other than T4 are supported. The selector field is read-only. Bit S0 will be a 1, and all other S bits are 0, indicating that *IEEE* 802.3 is selected. The next page bit is read-only and hard-coded to 0; this feature is not supported.

Register 5 indicates what the LUC3X01 has determined to be the capabilities of the link partner (LP) to which it is connected. All bits of this register are read-only.

Register 6 is the Auto-Negotiation expansion register.

The Auto-Negotiation circuit in the LUC3X01 is comprised primarily of six cooperating state machines, two of which are T4 technology dependent and four of which are not:

1. Auto-Negotiation transmit state machine
2. Auto-Negotiation receive state machine
3. Arbitration state machine
4. T4 transmit link-integrity state machine
5. T4 receive link-integrity state machine

The function of the Auto-Negotiation transmit state machine is to send bursts of 17 to 33 fast link pulses (FLPs) during a 2 ms window. These bursts of link pulses occur with a separation between bursts of 14 ms nominally. The reason the number of pulses in a burst can range from 17 to 33 is that there are always 17 clock pulses, while there can be from 0 to 16 data pulses. Data 1 is indicated by the presence of a pulse between two clock pulses (clock pulses are separated by 125 µs) while a data 0 is the absence of a pulse. Therefore, in a FLP burst with data of all 0s, there will be 17 pulses. The number of pulses is 17 plus the number of data 1s.

The function of the Auto-Negotiation receive state machine is to receive FLPs and determine the data content of the pulse burst. The machine checks if a legal number of pulses was received and if the bursts are properly separated.

Principles of Operation (continued)

Auto-Negotiation (continued)

The arbitration state machine uses information provided by the technology-dependent link-integrity state machines and the NLP receive link-integrity state machine to determine the traffic type. It then will enable the appropriate technology-dependent state machines to complete connection. On the LUC3X01, the link partner must support the 100Base-T4 protocol for a communication link to be established.

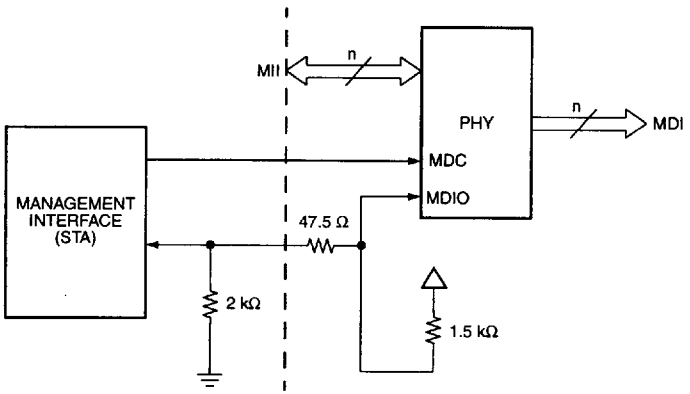
The T4 receive link-integrity state machine determines the status of the link as a T4 entity. It reports this status to the arbitration state machine and is also controlled by it.

When enabled, the T4 transmit link-integrity state machine will cause T4 link pulses to be transmitted every 1.2 ms (± 0.6 ms) in the absence of packet transmission.

Management Data Block (MDB)

Basic Operation

The main function of this block is to transfer the PHY's control and status information to a management entity. The clock input MDC, which has a minimum period of 400 ns and a maximum period of 2 µs, and a primary input/output pin (MDIO) are used to accomplish this function in both DTE and repeater modes. The following block diagram shows a typical application connection.



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Notes:
MDIO is driven in this mode with open-drain outputs.

The resistors shown are off-chip and required by the application.

The 47.5 Ω series MII resistors are for an exposed MII interface. For a nonexposed MII interface (NIC card), 200 Ω series MII resistors should be used to reduce switching transients.

Figure 11. Typical Interface Between PHY and Management Entity

The management interface uses MDC and MDIO to physically transport information between the PHY and the STA. A specific set of registers and their contents, as described below, defines the content of the information transferred across this interface. A specific frame format and some basic timing requirements dictate the method by which register contents are read or written.

Principles of Operation (continued)

Management Data Block (MDB) (continued)

Basic Register Set

Register 0 (Control). The assignment of bits in the control register is shown in the table below, with descriptions of the functions following.

Table 7. Control Register Bit Definitions

Bit(s)	Name	Description	R/W*	Default
0.15	Reset	1 = PHY reset 0 = normal operation	R/W SC	0
0.14	Loopback	1 = loopback mode 0 = normal operation	R/W	0
0.13	Speed Selection	1 = 100 Mbits/s	RO	1
0.12	Auto-Negotiation Enable	1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process	R/W	1
0.11	Powerdown	1 = powerdown 0 = normal operation	R/W	0
0.10	Isolate	1 = electrically isolate PHY from MII 0 = normal operation	R/W	0
0.9	Restart Auto-Negotiation	1 = restart Auto-Negotiation process 0 = normal operation	R/W SC	0
0.8	Duplex Mode	0 = half duplex	RO	0
0.7	Collision Test	1 = test COL signal 0 = normal loopback operation	R/W	0
0.[6—0]	Reserved	—	R/W	—

* R/W = read/write, SC = self-clearing, RO = read only.

- RESET—If this self-clearing bit is set, the device will completely reset itself as described elsewhere in this document.
- Loopback—Setting this bit to a logic HIGH has the same effect as asserting the device pin LOOP logic HIGH.
- Speed Selection—This is a read-only bit set to a logic HIGH, corresponding to 100 Mbits/s operation. All attempts to write to this bit will be ignored.
- Auto-Negotiation Enable—The Auto-Negotiation process is enabled if this bit is a logic HIGH (default). If it is set to a logic LOW, the Auto-Negotiation state machines are disabled and the device is configured for 100Base-T4 operation immediately.
- Powerdown—Writing a logic HIGH to this bit forces the chip into powerdown mode. In powerdown mode, all on-chip circuitry is reset, and shutdown except for the serial management interface. (Identical to isolate mode.)
- Isolate—If this bit is asserted, the chip is effectively isolated from the MII interface. The following output pins are tristated: TX_CLK, RX_CLK, RXD[5:0], RX_DV, RX_ER, CRS, and COL. The following input pins are ignored: TXD[5:0], TX_EN, and TX_ER. The management interface functions normally in this mode. (Identical to powerdown mode.)

Principles of Operation (continued)

Management Data Block (MDB) (continued)

Basic Register Set (continued)

- Restart Auto-Negotiation—If this self-clearing bit is set, then the device automatically begins the Auto-Negotiation process from the beginning and any previously learned information is discarded. It is similar to a RESET, but the analog blocks are not RESET, and hence occurs faster. The pins are not tristated to determine a new value of <PHYAD>. This bit clears as soon as the Auto-Negotiation state machine is in the Auto-Negotiation enable state.
- Duplex Mode—This read-only bit is always logic LOW. The LUC3X01 does not support full-duplex operation.
- Collision Test—If this bit is asserted, then the COL pin is asserted whenever the TX_EN pin is asserted and the part has been placed in loopback mode via the external loop pin. The COL pin may also be set by setting a register bit via the management interface. When this bit is deasserted (logic LOW), normal loopback mode prevails.
- Reserved—These bits are not used: attempted writes are ignored and data is always 0 during a read.

Register 1 (Status). The assignment of bits in the status register is shown in the table below. A description of the functions follows.

Table 8. Status Register Bit Definitions

Bit(s)	Name	Description	R/W*
1.15	100Base-T4	1 = PHY able to perform 100Base-T4	RO
1.14	100Base-X Full-Duplex	0 = PHY not able to perform full-duplex 100Base-X	RO
1.13	100Base-X Half-Duplex	0 = PHY not able to perform full-duplex 100Base-X	RO
1.12	10 Mbits/s Full-Duplex	0 = PHY not able to operate at 10 Mbits/s in full-duplex mode	RO
1.11	10 Mbits/s Half-Duplex	0 = PHY not able to operate at 10 Mbits/s in half-duplex mode	RO
1.[10—6]	Reserved	—	RO
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete	RO
1.4	Remote Fault	0 = no remote fault condition detected	RO
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation	RO
1.2	Link Status	1 = link is up 0 = link is down	RO LL
1.1	Jabber Detect	0 = no jabber condition detected	RO
1.0	Extended Capability	1 = extended register capabilities	RO

* RO = read only, LL = latching low, LH = latching high.

Principles of Operation (continued)

Management Data Block (MDB) (continued)

Basic Register Set (continued)

- 100Base-T4
- 100Base-TX Full-Duplex
- 100Base-TX Half-Duplex
- 10Base-T Full-Duplex
- 10Base-T Half-Duplex

The capabilities of the LUC3X01 are limited to 100Base-T4. Therefore, the bits are set to the indicated values.

- Reserved—These bits are not used. These bits are set to ZERO (logic LOW).
- Auto-Negotiation Complete—When read as a logic ONE, this bit indicates the Auto-Negotiation process has been completed, and the contents of registers 4, 5, and 6 are valid. When this bit is a logic ZERO, the Auto-Negotiation process has not yet been completed, and the contents of registers 4, 5, and 6 are meaningless. This bit is set to ZERO if the Auto-Negotiation enable bit in the control register has been cleared.
- Remote Fault—This bit is always set to a logic ZERO indicating that the LUC3X01 has not detected a remote fault.
- Auto-Negotiation Ability—This bit is set logic HIGH.
- Link Status—This bit is set to a logic ONE following a read if the link is determined to be good as determined by the receive link-integrity state machine. The bit is set to a ZERO if the link is not up, or, if the link status is unknown. Once cleared, the bit remains in the ZERO state until the register is read via the management interface.
- Jabber Detect—This bit is always cleared to a logic ZERO.
- Extended Register Capability—This bit is set to a logic ONE implying the extended registers 2—6, inclusive, are included.

Extended Registers 2 and 3. These two registers are not implemented.

Auto-Negotiation Advertisement Register (#4). The contents of this register are the 16 bits that are encoded and transmitted to the PHY at the far end of the link. The following table describes the contents of the register, with appropriate descriptions following. This is a read-only register.

Table 9. Auto-Negotiation Advertisement Register Bit Definitions

Bit(s)	Name	Description
4.15	NP	Next Page = 0
4.14	Ack	Acknowledge
4.13	RF	Remote Fault = 0
4.[12—5]	A[7:0]	Technology Ability
4.[4—0]	S[4:0]	Selector Field

Principles of Operation (continued)

Management Data Block (MDB) (continued)

Basic Register Set (continued)

- Next page—This bit is set to a logic ZERO.
- Acknowledge—Acknowledge is used by the Auto-Negotiation algorithm to indicate that a station has successfully received the Link Code Word from the PHY at the far end of the link. This bit is set to a logic ONE after reception of three consecutive and consistent FLP bursts.
- Remote Fault—This bit shall be set to ZERO.
- Technology Ability—The value of these bits, A[7:0], is <0001 0000>.
- Selector Field—The value of these bits, S[4:0], is <00001>.

Auto-Negotiation Partner Ability Register (#5). This register contains the advertised ability of the PHY at the other end of the link. The bit definitions and positions for this register are identical to those for register #4. The register is read only. The value of each bit is obtained from the state machine that decodes the reception of fast link pulses.

Auto-Negotiation Expansion Register (#6). The following table lists the bits contained in this register, with descriptions following.

Table 10. Auto-Negotiation Expansion Register Bit Definitions

Bit(s)	Name	R/W
6.[15:5]	Reserved	—
6.4	Multiple Link Fault	RO/SC
6.3	Link Partner Next Page Able	RO
6.2	Next Page Able = 0	RO
6.1	Page Received	RO/SC
6.0	Link Partner Auto-Negotiation Able	RO

- Multiple Link Fault—If set to logic ONE, this bit indicates that zero, or more than one, of the NLP 100Base-TX 100Base-T4, RLI state machines indicate that the link is up, when the Auto-Negotiation_wait_timer expires. This bit is cleared to a logic ZERO when the register contents are read via the management interface.
- Link Partner Next Page Able—This bit, if set logic HIGH, indicates that the link partner supports the next page function.
- Next Page Able—This bit is set to a logic ZERO indicating the LUC3X01 does not support the next page function.
- Page Received—This bit, if set logic HIGH, indicates that a link code word has been received and is cleared to a logic ZERO whenever the register is read via the management interface.
- Link Partner Auto-Negotiation Able—This bit is set to a logic ONE if the link partner is able to participate in the Auto-Negotiation algorithm.

Principles of Operation (continued)

Management Data Block (MDB) (continued)

Frame Structure

Table 11 shows the basic frame structure for both the read and write functions.

Table 11. Basic Frame Structure

	<IDLE>	<ST>	<OP>	<PHYAD>	<REGAD>	<TA>	<DATA>	<IDLE>
READ	—	<01>	<10>	<AAAAA>	<RRRRR>	<Z0>	<DDDDDDDDDDDDDDDD>	—
WRITE	—	<01>	<01>	<AAAAA>	<RRRRR>	<10>	<DDDDDDDDDDDDDDDD>	—

The following list describes each part of the frame structure shown above.

- IDLE condition. <IDLE> The IDLE condition on the two-wire interface is a logic ONE. All open-drain drivers are disabled, and the default pull-up resistor pulls the MDIO line to a logic ONE. Prior to initiating any other transaction, the station management entity sends a sequence of 32 contiguous logic ONE bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can use to establish synchronization. A PHY observes a sequence of contiguous one bits on MDIO with 32 corresponding cycles on the MDC before it responds to any other transactions.
- Start of Frame. <ST> The start of frame is indicated by a <01> pattern. This pattern ensures transitions from the default logic ONE line state to zero and back to one.
- Operation Code. <OP> The operation code for a read is a <10>. The operation code for a write is <01>.
- PHY Address. <PHYAD> The PHY address is 5 bits, allowing 31 unique PHY addresses, and the 00000 broadcast address. The first PHY address bit transmitted and received is the MSB of the address. The value of the <PHYAD> is programmed at the board level and is sensed by the LUC3X01 during a RESET condition. The <PHYAD> is determined by sensing the logic levels of the pins listed below, with the ordering shown. Resistor pull-ups or pull-downs are used to program the values.

Table 12. PHY Address

Bit	Pin
4 (MSB)	SD
3	LINK
2	CRS
1	ATO1
0 (LSB)	ATO0

- Register Address. <REGAD> The register address is 5 bits, allowing 32 individual registers to be addressed within each PHY. The register accessed at register address zero <00000> is the control register, and the register accessed at register address <00001> is the status register.
- Turnaround. <TA> A bit time during which no device actively drives the MDIO signal is inserted between the register address field and the second TA bit during a read transaction in order to avoid contention. During a read transaction, the PHY drives a 0 bit onto MDIO for the bit time following the first TA bit and preceding the data field. During a write transaction, the station management entity fills these two bit times with a one bit followed by a zero bit.
- Data. <DATA> The data field is 16 bits. The first bit transmitted and received is the MSB of the data payload.

Principles of Operation (continued)

CRS and COL Functionality

CRS Functionality

The CRS pin indicates that there is activity, either transmit or receive, on the wire media.

It is asynchronously asserted and deasserted as appropriate, and the timing requirements for this pin are set out in the Timing Characteristics section.

The following sections first cover the two basic cases of only receiving a packet and only transmitting a packet. The next section describes the way these are combined for colliding packets, and the last two sections discuss the various exception conditions resulting from the Auto-Negotiation and receive link-integrity functions, as well as operating the device in repeater mode.

Receiving a Packet Only. The CRS pin is asserted logic HIGH to indicate that the process of receiving a packet has begun. This occurs when the smart squelch function for each channel detects the incoming preamble on each channel. This assertion of CRS is asynchronous.

The CRS pin is deasserted when the chip has detected seven or more consecutive ternary ZERO symbols on channel RX_D2, or when the decoding process has identified the EOP sequences.

Transmitting a Packet Only. The CRS pin is asserted logical HIGH after the assertion of the pin TX_EN is detected. This is a synchronous process.

To allow for the pipelining of the encoding process and for the EOP sequences to be appended to the frame, CRS remains asserted after the deassertion of TX_EN. After this, the CRS pin is deasserted, as shown in the timing diagram.

Colliding Packets. Given that CRS is nominally the logical OR of carrier_status and transmit enable, the case is fairly straightforward.

CRS is asserted according to the rules of whichever happens first, receive activity or transmit enable.

CRS is deasserted according to the rules of whichever happens last, receive activity or transmit enable.

Effect of Receive Link Integrity on CRS. The pin CRS is held logic LOW unless the link has been judged OK.

COL Functionality

COL Assertion. The COL pin will be asserted asynchronously, after both receive activity and transmit enable are active.

If the device is transmitting, then receive energy will be asserted when the smart squelch block detects incoming preamble on channel RX_D2 only. This assertion of receive energy causes the COL pin to be asserted. This is different than the typical receive-only case where the smart squelch function must see preamble on all three channels before asserting receive energy.

If the device is configured for operation in the repeater mode, the COL pin is tristated unless the pin REPEN is held logic HIGH.

Principles of Operation (continued)

Internal Loopback Mode

Internal loopback mode is provided to enable a system test of the chip without actually putting any signals onto the wire media. Internal loopback mode is invoked when either the LOOP pin is asserted logic HIGH, or the loopback bit (0.14) is set via the management interface.

When the loopback is invoked in DTE mode, the transmit data after encoding is directed to the receive path. Here the data goes through the receive path and, after decoding, is sent off-chip.

When loopback is invoked in repeater mode, the digital representation of the ternary symbols is looped from the transmit path to the receive. As might be expected, the crossover from channel 3 to 4 and vice-versa is implemented in the loopback of data from the transmit path to the receive path.

When TX_EN is asserted in loopback mode, the CRS pin behaves as it would during normal operation. It is asserted after TX_EN is HIGH, and held asserted until TX_EN is deasserted, and all of the data is through the receive path pipeline.

Normally, the COL is held logic LOW when the part is in internal loopback mode, regardless of the status of TX_EN and CRS. However, if bit 0.7 of the control register is set to a logic HIGH via the management register, the COL pin will be asserted logic HIGH when the part is configured in loopback mode and the TX_EN has been asserted HIGH.

When the part is configured for internal loopback, no signals of any sort are transmitted onto the media, and all signals received from the media are ignored. Also, the delay from the assertion of TX_EN to the assertion of RX_DV must be less than 512 µs.

Reset

The LUC3X01 is reset on powerup or by setting a register bit via the management interface, or by pulling the $\overline{\text{RST}}$ pin LOW. This pin requires an external 10 kΩ pull-up resistor.

When the device is powered up, it enters the RESET state through a powerup circuit, with all inputs and outputs in a quiescent condition. The duration of the RESET state is maintained for a duration not to exceed 500 ms in order to ensure all internal circuits have stabilized. The RESET state timer does not begin until the input SYSCLK is seeing a stable 25 MHz clock input.

In addition to entering the RESET state at powerup, there are two other ways to enter this state. One way is to pull the $\overline{\text{RST}}$ pin LOW for a minimum duration of 200 ns. The RESET state timer begins with the rising edge of $\overline{\text{RST}}$, even though the part enters the RESET state asynchronously with the logic LOW level at the pin.

The other way to enter the RESET state is to set the self-clearing register bit via the management interface. This method also has the same minimum duration as the other methods.

While in the RESET state, the logic levels at pins LINK, SD, CRS, ATO1, and ATO0 are sensed to determine the <PHYAD> used in the management frame structure.

The total chip reset does not exceed 500 ms.

Power Supplies and Biasing

Power

The device must never be supplied with voltage other than 5 V ± 5%. The device can exhibit undetermined behavior if a lower value (e.g., 3.3 V) is applied to the device and sustained for a period of time.

The device will accept a powerup ramp on V_{DD} from as fast as 1 V/100 ns to as slow as 1 V/20 ms.

All ground pins should be tied directly to the ground plane of the system. Under no circumstances should the ground pins be at different potentials.

Powerdown. The performance of the LUC3X01 is unspecified if V_{DD} drops below the minimum value for assured functionality (4.75 V) unless the $\overline{\text{RST}}$ pin is being held logic LOW.

If the pin $\overline{\text{RST}}$ is held LOW during power-removal, then the LUC3X01 will shut down without generating spurious signals on any of the outputs.

Section 3.1

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Maximum Supply Voltage	V_{DD}	—	7.0	V
Inputs/Outputs on Any Pin	—	–0.5	V_{DD} + 0.5	V
Ambient Operating Temperature	T_A	0	70	°C
Ambient Storage Temperature	T_{stg}	–40	125	°C
Maximum Power Dissipation	P_D	—	1.5	W
Maximum Power Dissipation Powerdown	P_{DD}	—	0.05	W

Electrical Characteristics

Output Buffers

LED Output Buffers

These buffers are used to drive LEDs to indicate the status of the T4 link, and if the local link is configured for 100 Mbits/s operation.

The analog buffers will present a high impedance to the pin, during a RESET condition generated either by pulling $\overline{RST}$ LOW, by setting a register bit via the management interface, or on powerup.

Also during a RESET condition, the voltage at the pin will be sensed (the output buffer is tristated). By connecting off-chip components as shown below, the logic level of the pins during a RESET condition can be forced. The logic levels of these pins (SD and LINK) constitute part of the address of the PHY used in the frame management structure. The following table delineates the electrical requirements.

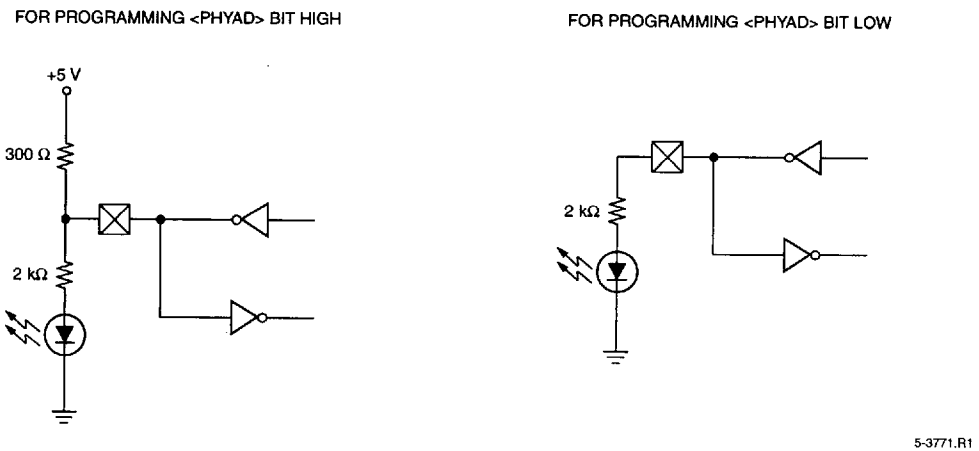


Figure 12. LED Output Buffers

Electrical Characteristics (continued)

Output Buffers (continued)

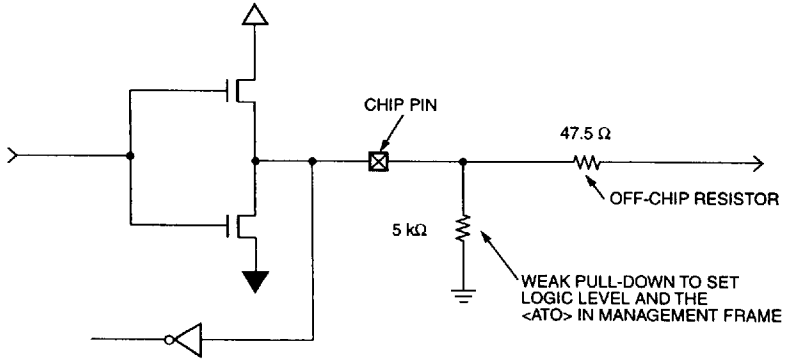
LED Output Buffers (continued)

Table 13. Electrical Requirements of LED Output Buffers

Parameter	Min	Typ	Max	Unit
Output Rise/Fall Time (70%/30%)	—	—	20	ns
VOH (sourcing 15 mA)	4.0	—	—	V
VOL (sinking 15 mA)	—	—	0.4	V
VIL (RESET condition)	—	—	2.0	V
VIH (RESET condition)	4.0	—	—	V

Media-Independent Interface (MII) Output Buffers

Using one of the internal test registers, all MII output buffers can be put into high-impedance state to facilitate production testing. When used in DTE mode, each MII output buffer has an off-chip resistor connected in series with it, as shown in the figure below.



Note: The 47.5 Ω series MII resistors are for an exposed MII interface. For a nonexposed MII interface (NIC card), 200 Ω series MII resistors should be used to reduce switching transients.

Figure 13. MII Output Buffer Connection in DTE Mode

The electrical requirements of the buffer itself, not including the off-chip resistor, are shown in the table below.

Table 14. Media-Independent Interface (Type O-MII) Output

Parameter	Conditions	Min	Typ	Max	Unit
Output Rise/Fall Time (70%/30%)	50 pF Load	—	—	6	ns
VOH	Sourcing 15 mA	4.0	—	—	V
VOL	Sinking 15 mA	—	—	0.4	V

Electrical Characteristics (continued)

Output Buffers (continued)

Media-Independent Interface (MII) Output Buffers (continued)

When the device is powered up, all MII output buffers are powered up in a high-impedance state. They are also set to a high-impedance state during a RESET condition.

When the device is configured for operation in repeater mode, most of the MII output buffers behave slightly differently. The output TX_CLK is driven and held logic LOW. The output CRS has the same electrical behavior as it does in DTE mode. The outputs RX_ER, RX_DV, RX_CLK, RXD[5:0], COL are tristated when the input pin REPEN is held LOW, and they are actively driven HIGH and LOW when the input REPEN is driven HIGH. These outputs are valid 40 ns after the pin REPEN is driven HIGH.

Operation During Reset Condition. During a reset condition generated by either pulling the $\overline{RST}$ LOW, setting a register bit via the management interface, or on powerup, all the MII output buffers are tristated. During the reset condition, the voltage at the CRS pin will be sensed (the output buffer is tristated). Weak off-chip pull-ups or pull-downs (5 kΩ nominal) set the sensed voltage. The logic levels of the CRS pin constitute part of the address of the PHY used in the frame management structure.

Analog Output Buffers

UTP Output Buffer. These drivers output CMOS logic levels with a source resistance of less than 10 Ω with a maximum current rating of 50 mA. When driving a purely capacitive load, the pins swing from rail to rail (V_{DD} to V_{SS}). When each pin is driving a 50 pF capacitive load, the rise and fall times will be between 3 ns and 12 ns. This reduces the possibility of high-frequency emissions and ground bounce levels. The output of the TP drivers is a high-impedance during a RESET condition, and when the device has been placed in powerdown mode via the serial interface.

Analog Test Output Pins. During a RESET condition generated by either pulling the $\overline{RST}$ LOW, setting a register bit via the management interface, or on powerup, the voltage at the pin will be sensed. Weak, off-chip pull-ups and pull-downs (500 kΩ minimum) set the sensed voltage. The logic levels of these pins, ATO[0:1], constitute part of the address of the PHY used in the frame management structure.

Input Buffers

Digital Input Buffers

The digital input buffers are TTL compatible CMOS logic, divided loosely into regular and MII type input buffers, whose electrical characteristics are identical and are described in the tables below.

Table 15. Digital (Type I-D) and Media-Independent Interface (Type I-MII) Inputs

Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	—	2.0	—	—	V
V_{IL}	—	—	—	0.8	V
Input Leakage Currents	—	—	—	10	µA
Input Capacitance	—	—	—	5	pF
Input t_{RISE}/t_{FALL}	30%—70%	—	—	5	ns

Note: For the mode and TMS input pins, the nominal value of the on-chip pull-down resistor attached to the pad is 100 kΩ.

Electrical Characteristics (continued)

Input Buffers (continued)

Analog Input Buffers

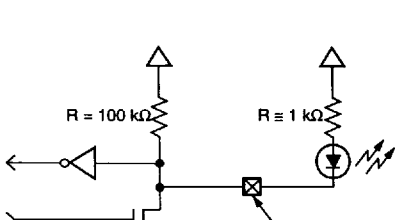
Table 16. UTP (Type I-A) Input Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Differential Input Resistance	Measured at Pins	10	—	—	kΩ
Peak Differential Input Voltage	Measured at Pins	—	—	3.85	V
Peak Differential Squelch Voltage	Measured at Pins	—	450	—	mV

Input/Output Pins

Autopolarity (AP) Pin

The AP pin has a dual function in that it may enable or disable the function. If the function is enabled, the pin can drive an LED to provide a visual indication if one of the three data pairs has its wire polarity reversed. The LED is lit by using an n-channel device in an open-drain configuration with the LED connected to the pin as shown in the figure.



5-3753

Figure 14. Autopolarity Pin

If no visual indication is desired, then only the resistor pull-up is needed to enable the function. Alternatively, the function may be enabled if the pin is left floating where a weak on-chip pull-up resistor is used to pull the pin HIGH. If the autopolarity function is to be disabled, then the pin should be shorted to ground off-chip.

BIAS Pin

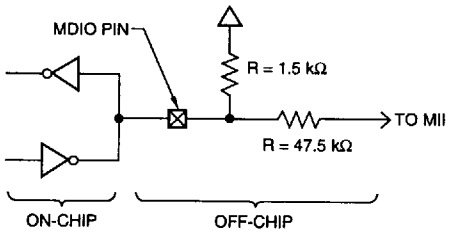
This pin is used to generate an on-chip current reference which provides temperature-independent biasing of internal analog circuits. This pin is connected to a 24.9 kΩ ± 1% resistor to ground, and the parasitic loading on this pin must not exceed 15 pF.

Electrical Characteristics (continued)

Input/Output Pins (continued)

MDIO Pin

Normal Mode. This pin inputs and outputs data on the rising edge of MDC. It reads in the data until a write instruction tells it to output the contents of the appropriate register. The value of the off-chip pull-up resistor attached to this pin is 1.5 kΩ.

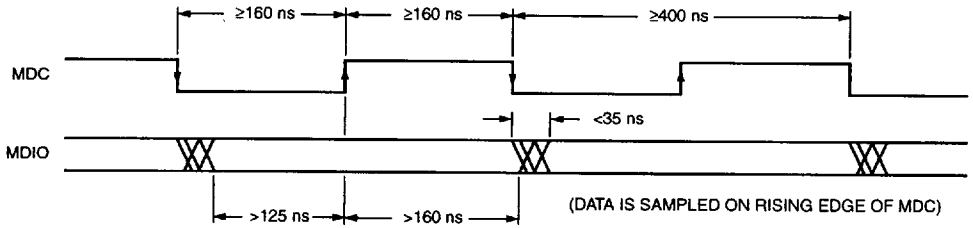


5-3754.R3

Figure 15. Normal Mode

The MDIO pin is sampled on the rising edge of MDC by either the PHY or the STA, depending on whether a READ or WRITE operation is taking place. The direction of data transfer is determined by the OP bits of the management frame (see clause 22 of *IEEE* 802.3).

When the PHY is driving this pin as an output during data READ, data is changed on the falling edge of MDC. Given that the minimum low or high cycle portion of the MDC period is specified in the standard to be 160 ns, the result is a minimum setup time of 125 ns, allowing 35 ns for data to change and a minimum hold time of 160 ns; see the figure below.



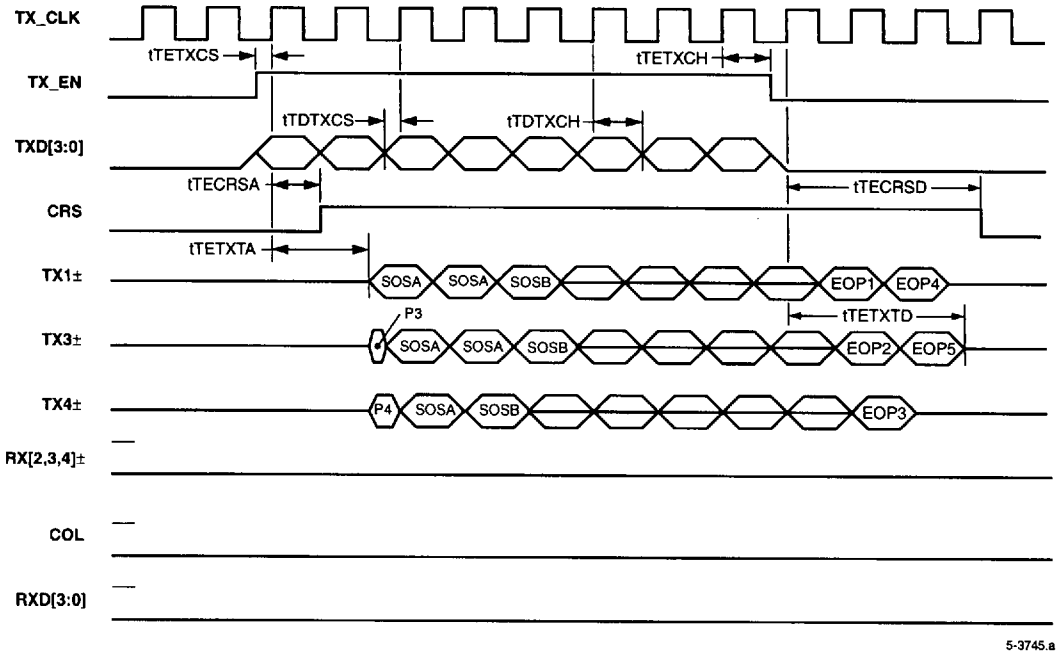
5-4236

Figure 16. MDIO Output Timing (During Data Read)

Timing Characteristics

Table 17. Transmit Timing with No Collisions (DTE Mode)

Symbol	Parameter	Min	Max	Unit
tTETXCS	TX_EN to Transmit Clock Setup Time	10	—	ns
tTETXCH	TX_EN to Transmit Clock Hold Time	0	—	ns
tTECRSA	Rising Edge of TX_CLK Following TX_EN Assertion to CRS Assertion	—	40	ns
tTDTXCS	Transmit Data in to Transmit Clock Setup Time	10	—	ns
tTDTXCH	Transmit Data in to Transmit Clock Hold Time	0	—	ns
tTETXTA	Rising Edge of TX_CLK Following TX_EN Assertion to TX1, TX3, and TX4 Activity	90	140	ns
tTECRSD	Rising Edge of TX_CLK Following TX_EN Deassertion to CRS Deassertion	280	360	ns
tTETXTD	Rising Edge of TX_CLK Following TX_EN Deassertion to No TX1, TX3, and TX4 Activity	560	740	ns



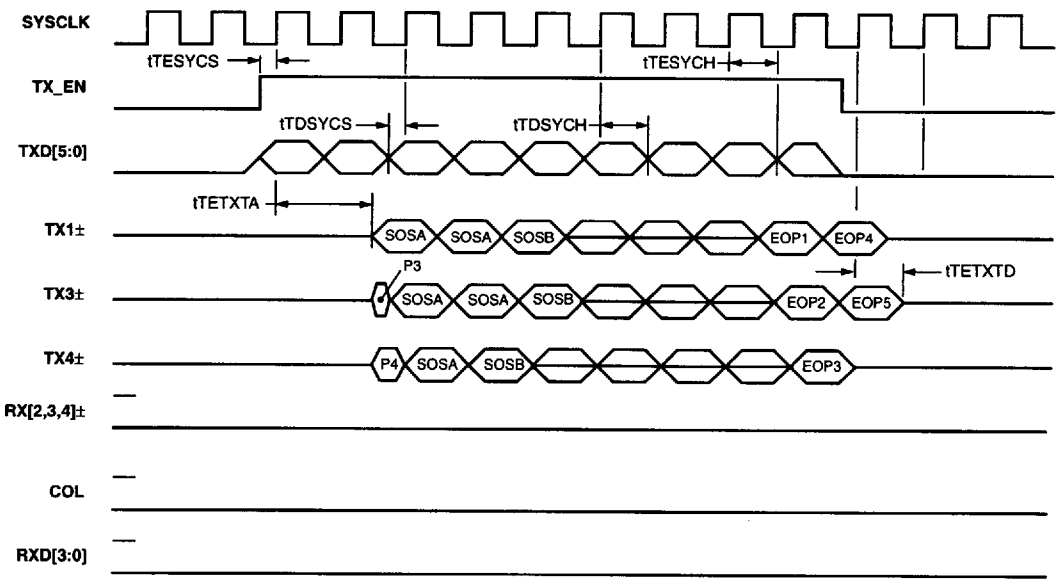
Note: 6T data on TX[1, 3, 4]± not drawn to scale, and EOP sequences can actually begin on any output pair, not just TX1± as is shown here.

Figure 17. Transmit Timing with No Collisions (DTE Mode)

Timing Characteristics (continued)

Table 18. Transmit Timing with No Collisions (Repeater Mode)

Symbol	Parameter	Min	Max	Unit
tTESYCS	TX_EN to SYSCLK Setup Time	15	—	ns
tTESYCH	TX_EN to SYSCLK Hold Time	0	—	ns
tTDSYCS	Transmit Data in to SYSCLK Setup Time	15	—	ns
tTDSYCH	Transmit Data in to SYSCLK Hold Time	0	—	ns
tTETXTA	Rising Edge of SYSCLK Following TX_EN Assertion to TX1, TX3, and TX4 Transmit Activity	—	50	ns
tTETXTD	Rising Edge of SYSCLK Following TX_EN Deassertion to No TX1, TX3, and TX4 Activity	—	90	ns



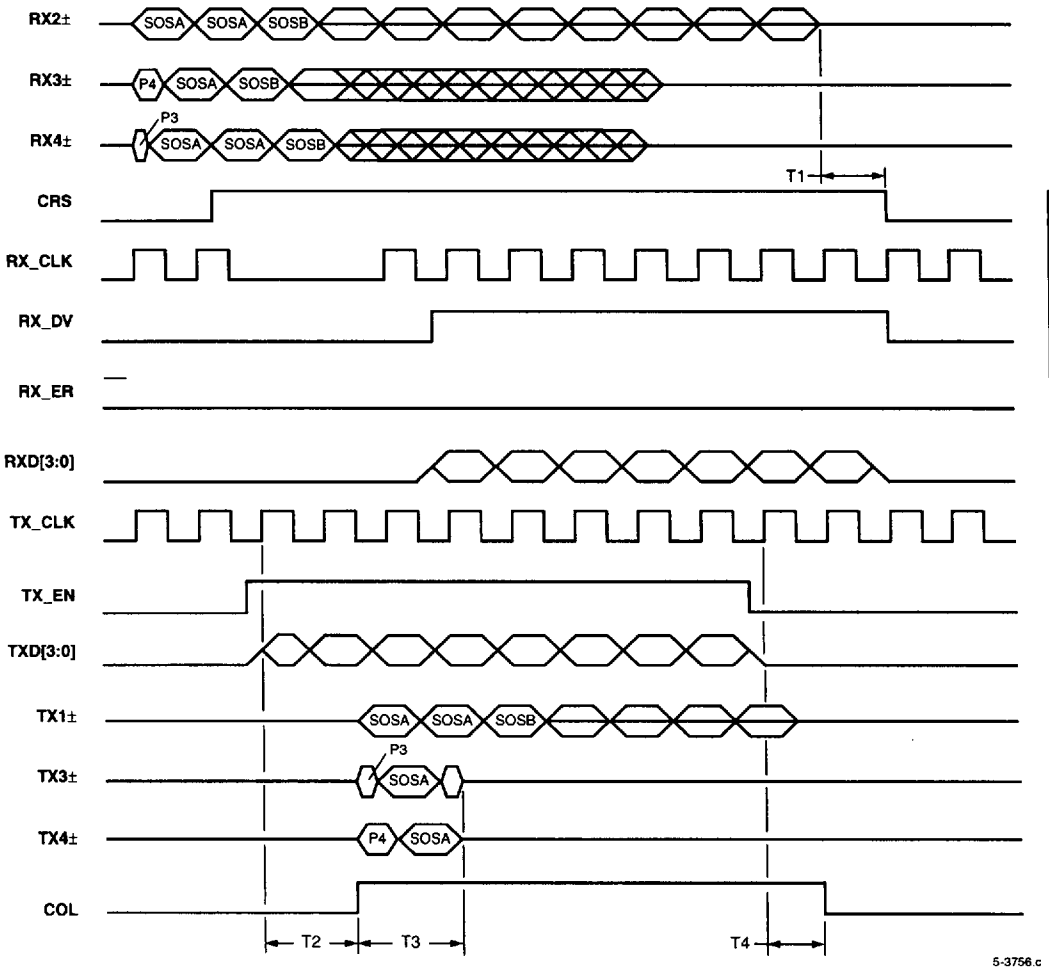
Note: 6T data on TX[1, 3, 4]± not drawn to scale, and EOP sequences can actually begin on any output pair, not just TX1± as is shown here.

Figure 18. Transmit Timing with No Collisions (Repeater Mode)

Timing Characteristics (continued)

Table 19. Transmit Timing with Collisions (DTE Mode)

Symbol	Parameter	Min	Max	Unit
T1	RX2, RX3, and RX4 Receive Activity Cease to CRS Deasserted	—	460	ns
T2	Rising Edge of TX_CLK Following TX_EN Assertion (given CRS asserted) to COL Assert	—	50	ns
T3	COL Assertion to TX3±, TX4± Cease Transmitting	—	300	ns
T4	Rising Edge of TX_CLK Following TX_EN Deassertion to COL Deassertion	0	50	ns



Notes:
Drawing not done to scale and is intended only to illustrate the times listed.

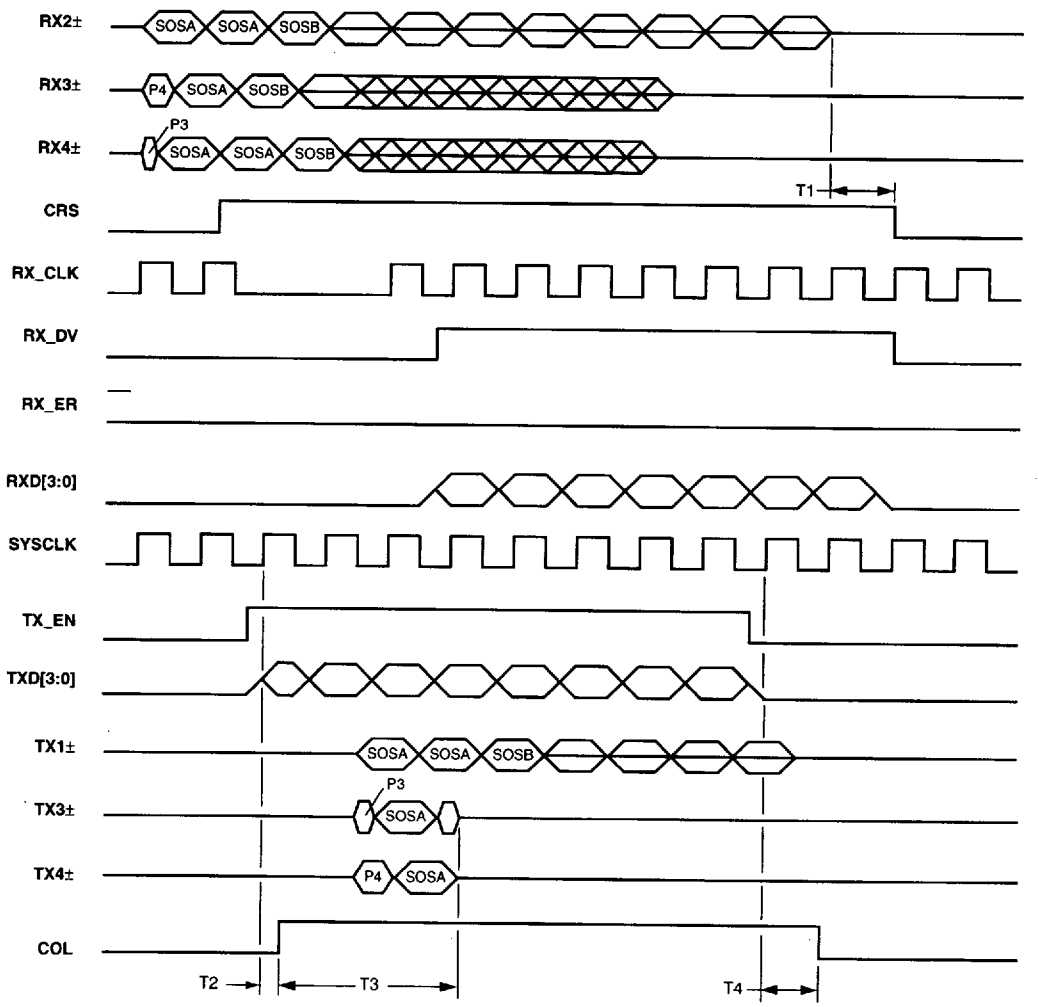
50 ns is allocated for magnetics module propagation delay from the LUC3X01 to the UTP (50 ns for transmit and 50 ns for receive).

Figure 19. Transmit Collision Timing (DTE Mode)

Timing Characteristics (continued)

Table 20. Transmit Timing with Collisions (Repeater Mode/Collision on Local Link Segment)

Symbol	Parameter	Min	Max	Unit
T1	RX2, RX3, and RX4 Receive Activity Cease to CRS Deasserted	—	460	ns
T2	Rising Edge of SYSCLK Following TX_EN Assert (given CRS asserted) to COL Assert	—	50	ns
T3	COL Assertion to TX3±, TX4± Cease Transmitting	—	300	ns
T4	Rising Edge of SYSCLK Following TX_EN Deassertion to COL Deassertion	0	50	ns



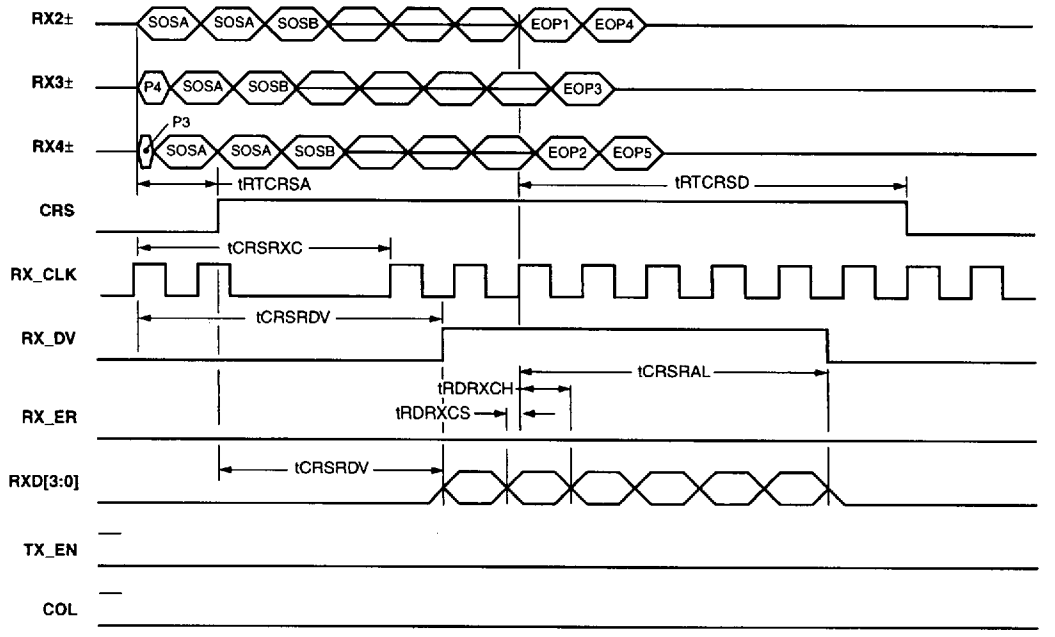
Note: Drawing not done to scale and is intended only to illustrate the times listed.

Figure 20. Transmit Collision Timing (Repeater Mode)

Timing Characteristics (continued)

Table 21. Receive Timing with No Errors or Collisions (DTE Mode)

Symbol	Parameter	Min	Max	Unit
tRTCRSA	RX2, RX3, and RX4 Receive Activity to CRS Asserted	—	150	ns
tCRSRXC	RX2, RX3, and RX4 Receive Activity to Receive Clock Valid	—	540	ns
tCRSRDV	RX2, RX3, and RX4 Receive Activity to Receive Data Valid	880	1230	ns
tRDRXCS	Receive Data Output to Receive Clock Setup Time	10	—	ns
tRDRXCH	Receive Data Output to Receive Clock Hold Time	10	—	ns
tRTCRSD	RX2, RX3, and RX4 Receive Activity Cease (start of EOP1) to CRS Deasserted	0	465	ns
tCRSRAL	RX2, RX3, and RX4 Receive Activity Cease (start of EOP1)to Receive Data Not Valid	—	580	ns



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Notes:
6T data on RX2±, RX3±, and RX4± not drawn to scale.

EOP sequences can actually begin on any input pair, not just RX2± as shown here.

All times shown here assume that incoming preamble starts simultaneously on all three device channels.

Timing diagrams accounting for the effects of cable skew present in practical systems are in the sections that follow.

RXD[5:0], RX_DV, and RX_ER are synchronous with the falling edge of RX_CLK.

The setup and hold times are from the perspective of the MAC end of the MII interface.

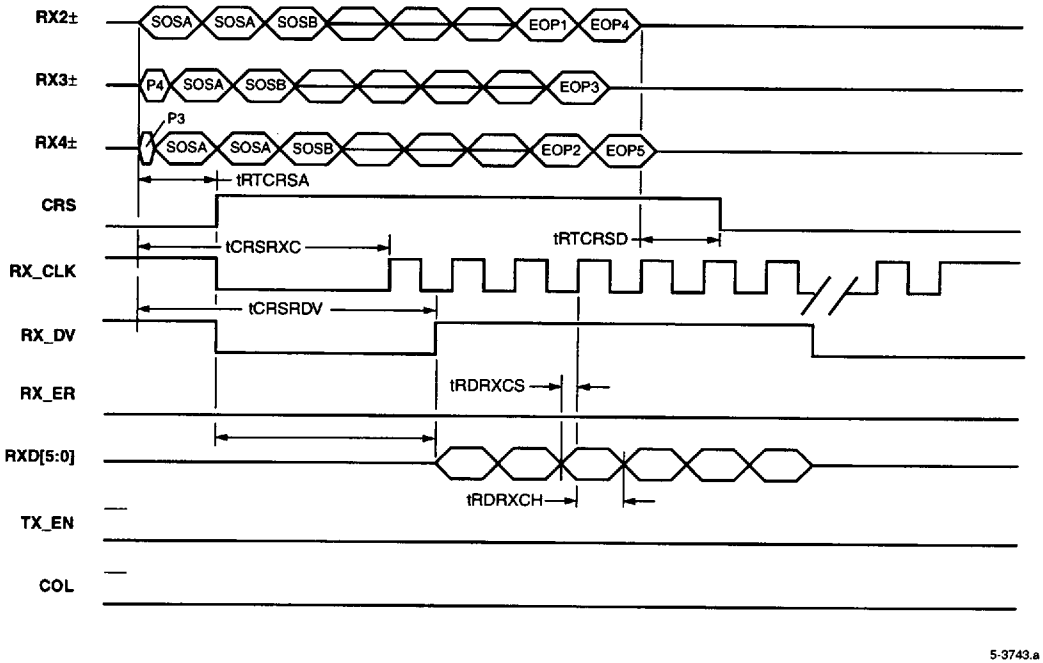
50 ns is allocated for magnetics module propagation delay time from the LUC3X01 to the UTP (50 ns for transmit and 50 ns for receive).

Figure 21. Receive Timing with No Errors or Collisions (DTE Mode)

Timing Characteristics (continued)

Table 22. Receive Timing with No Errors or Collisions (Repeater Mode)

Symbol	Parameter	Min	Max	Unit
tRTCRSA	RX2, RX3, and RX4 Receive Activity to CRS Asserted	—	150	ns
tCRSRXC	RX2, RX3, and RX4 Receive Activity to Receive Clock Valid	—	540	ns
tCRSRDV	RX2, RX3, and RX4 Receive Activity to Receive Data Valid	—	860	ns
tRDRXCS	Receive Data Output to Receive Clock Setup Time	10	—	ns
tRDRXCH	Receive Data Output to Receive Clock Hold Time	10	—	ns
tRTCRSD	RX2, RX3, and RX4 Receive Activity Cease (end of EOP4) to CRS Deasserted	—	200	ns



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Notes:
6T data on RX2±, RX3±, and RX4± not drawn to scale.

EOP sequences can actually begin on any input pair, not just on RX2±, as shown here.

RX_CLK continues for 15 cycles after CRS deassertion, then goes high impedance.

All times shown here assume that incoming preamble starts simultaneously on all three device channels.

Timing diagrams accounting for the effects of cable skew present in practical systems are in the sections that follow.

RXD[5:0], RX_DV, and RX_ER are synchronous with the following edge of RX_CLK.

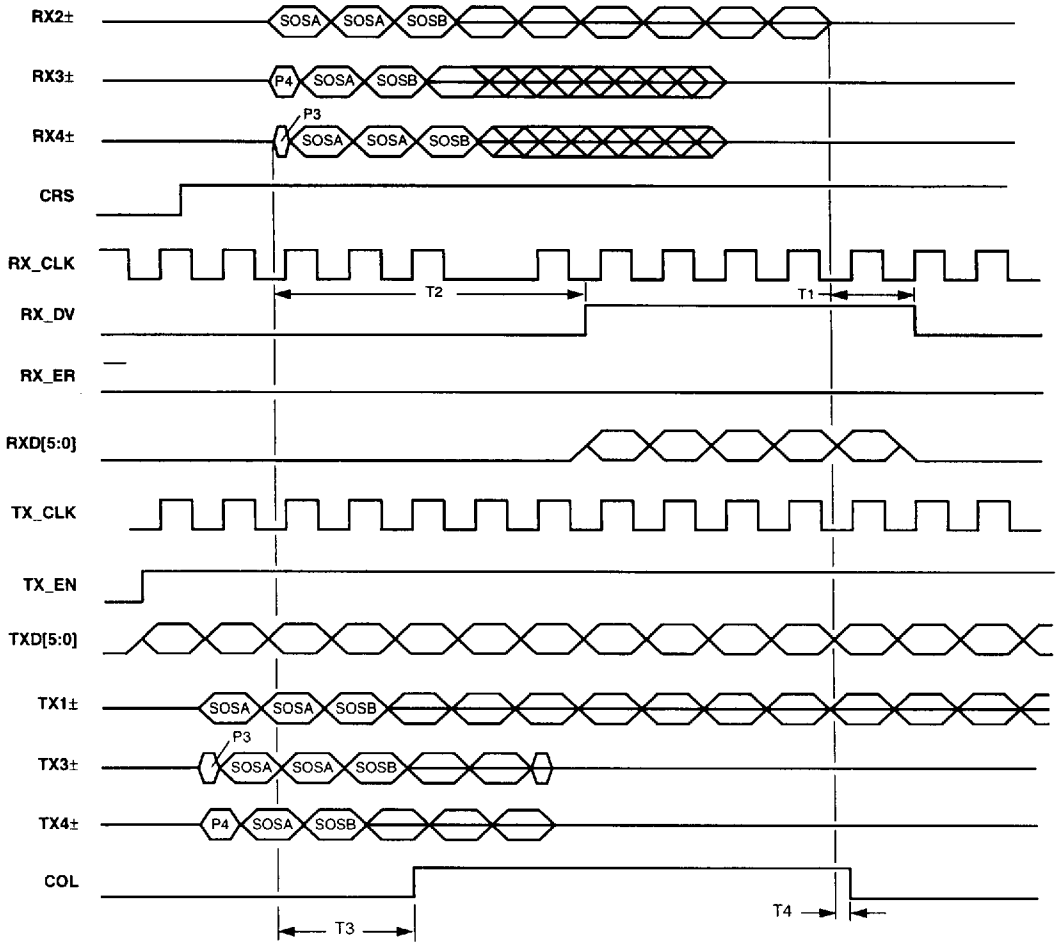
The setup and hold times are from the perspective of the repeater.

Figure 22. Receive Timing with No Errors or Collisions (Repeater Mode)

Timing Characteristics (continued)

Table 23. Receive Timing with Collisions (Repeater Mode)

Symbol	Parameter	Min	Max	Unit
T1	RX2, RX3, and RX4 Receive Activity Cease to RX_DV Deassert	—	470	ns
T2	RX2, RX3, and RX4 Receive Activity to RX_DV Assert	—	860	ns
T3	RX2, RX3, and RX4 Receive Activity to COL Assert	—	115	ns
T4	RX2, RX3, and RX4 Receive Activity Cease to COL Deassert	—	480	ns



Notes:
Drawing is not to scale and only intended to illustrate times shown.

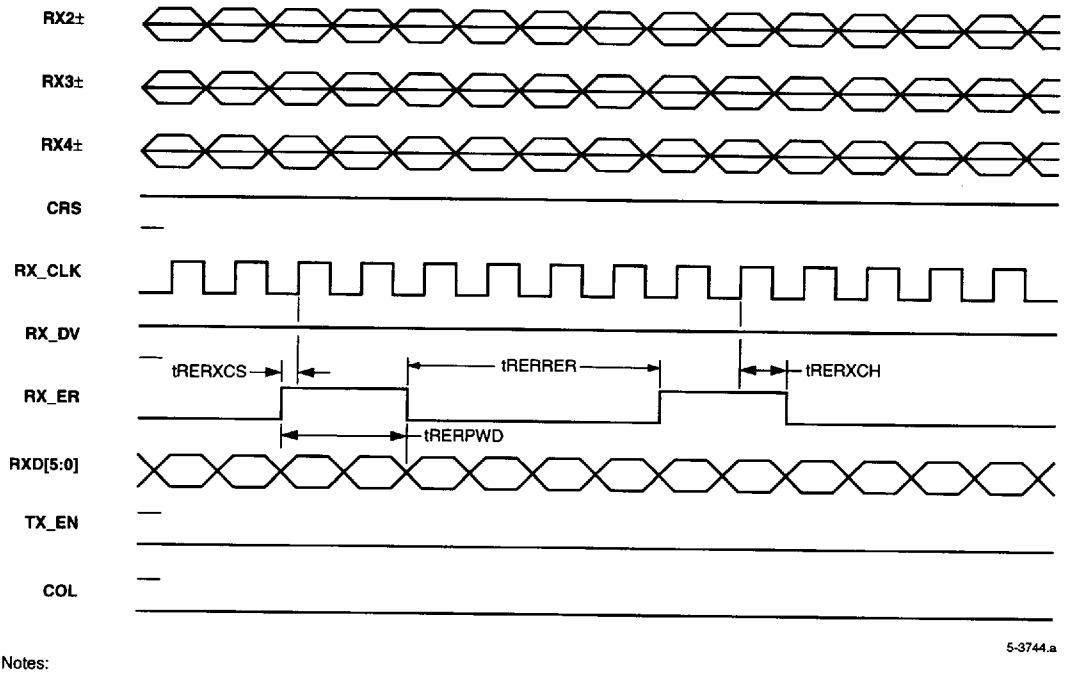
EOP sequences are not appended to TX1± at the end of the frame because of the collision condition.

Figure 23. Receive Collision Timing (Repeater Mode)

Timing Characteristics (continued)

Table 24. Receive Timing with Errors (DTE/Repeater Mode)

Symbol	Parameter	Min	Max	Unit
tRERXCS	Receive Error to Receive Clock Setup Time	10	—	ns
tRERXCH	Receive Error to Receive Clock Hold Time	10	—	ns
tRERPWD	Receive Error Pulse Width; Isolated Single Error	35	85	ns
tRERRER	Time Between Consecutive Assertions	0	—	ns



Notes:
6T data on RX2±, RX3±, and RX4± not drawn to scale.

RXD[5:0], RX_DV, and RX_ER are synchronous with the falling edge of RX_CLK.

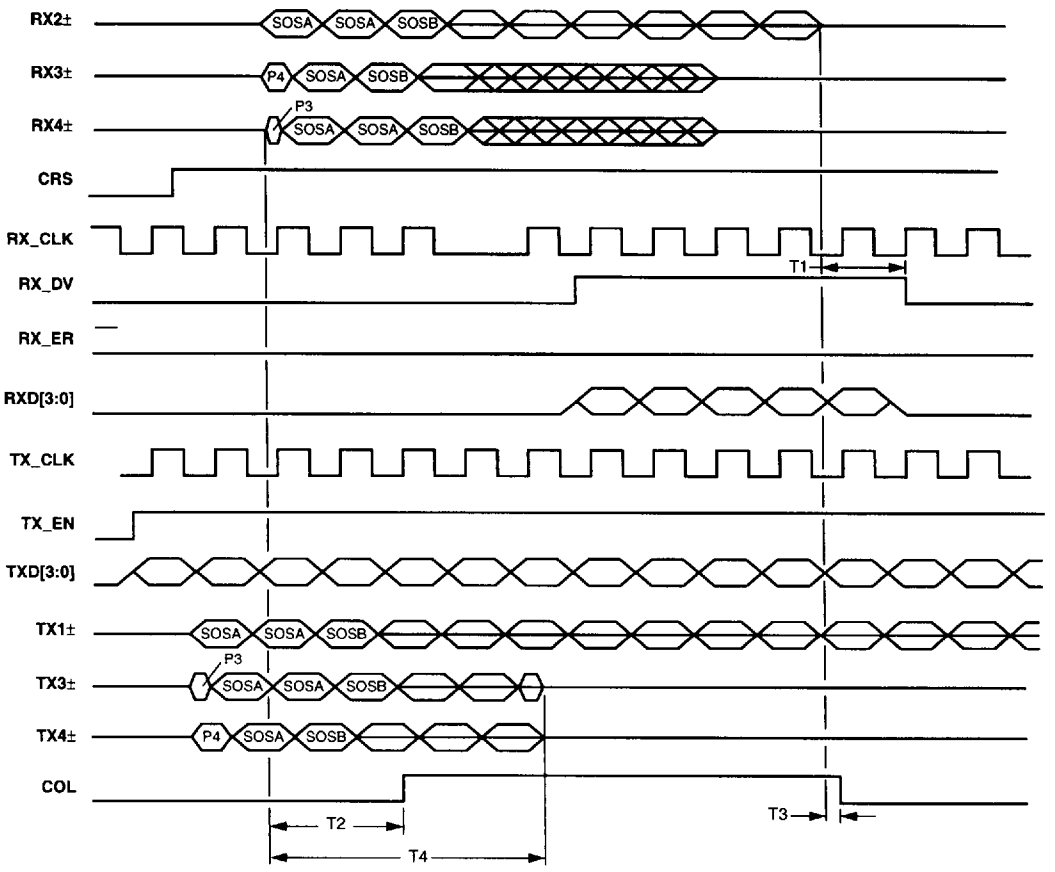
The setup and hold times are from the perspective of MAC/repeater.

Figure 24. Receive Timing with Errors (DTE/Repeater Mode)

Timing Characteristics (continued)

Table 25. Receive Timing with Collisions (DTE Mode)

Symbol	Parameter	Min	Max	Unit
T1	RX2, RX3, and RX4 Receive Activity Cease to RX_DV Deassert	—	470	ns
T2	RX2, RX3, and RX4 Receive Activity to COL Assert	—	115	ns
T3	RX2, RX3, and RX4 Receive Activity Cease to COL Deassert	—	480	ns
T4	RX2, RX3, and RX4 Receive Activity to TX3 and TX4 Cease	—	300	ns



Notes:
Drawing is not to scale and only intended to illustrate times shown.

EOP sequences are not appended to TX1± at the end of the frame because of the collision condition.

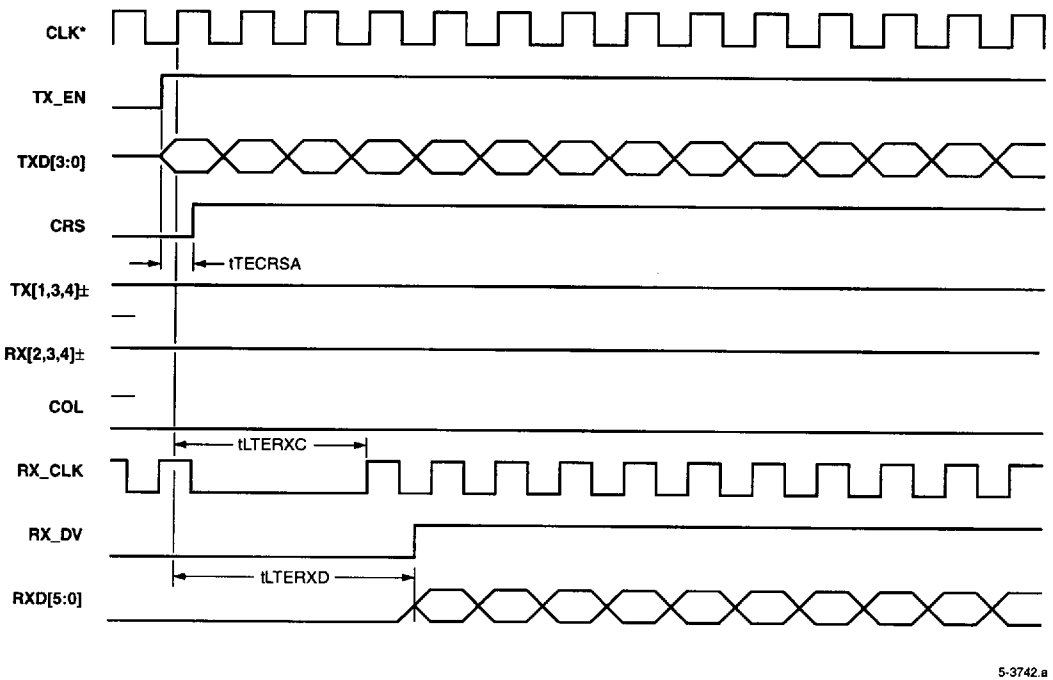
50 ns is allocated for magnetics module propagation delay from the LUC3X01 to the UTP (50 ns for transmit and 50 ns for receive).

Figure 25. Receive Collision Timing (DTE Mode)

Timing Characteristics (continued)

Table 26. Loopback Mode Timing

Symbol	Parameter	Min	Max	Unit
tLTERXC	Rising Edge of TX_CLK Following TX_EN Assertion to RX_CLK Valid	—	450	ns
tLTERXD	Rising Edge of TX_CLK Following TX_EN Assertion to RXD[5:0] Valid	—	450	ns
tTECRSA	TX_EN Asserted to CRS Asserted	—	50	ns



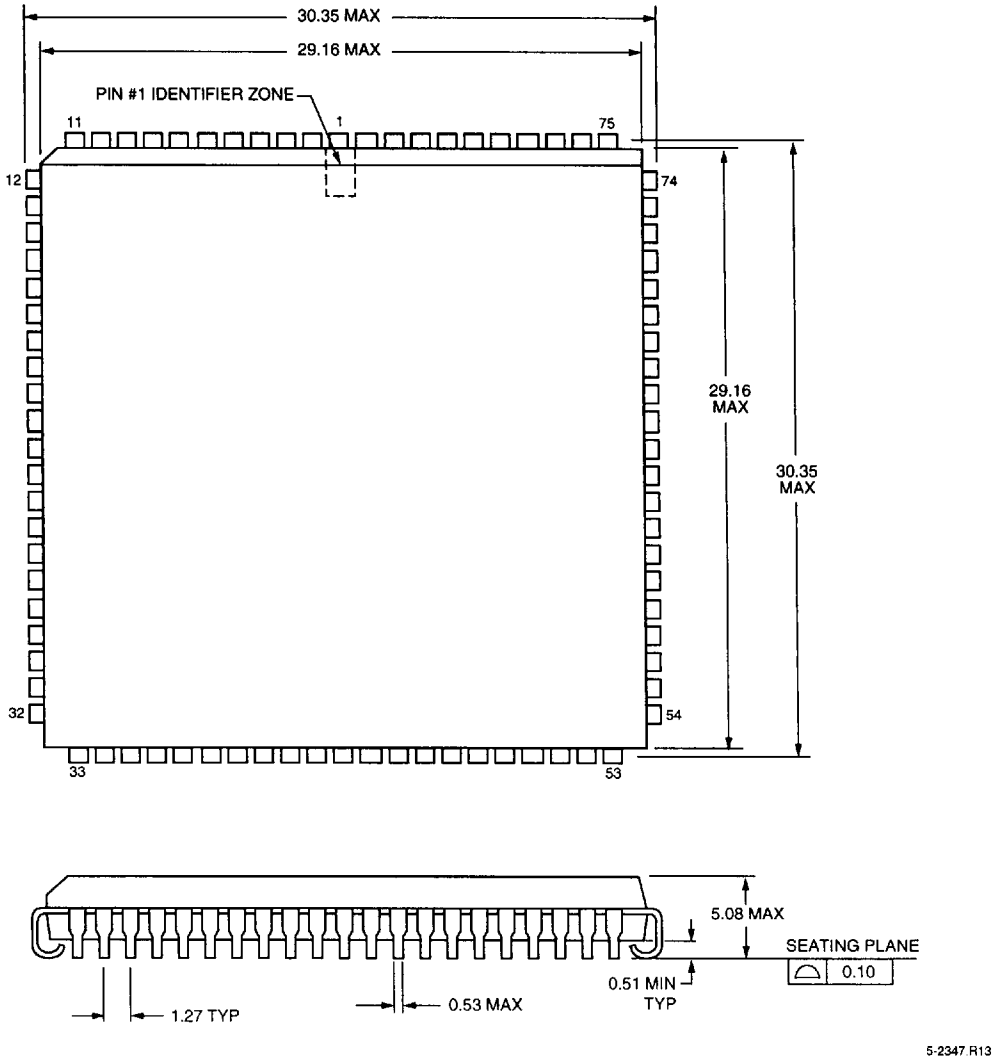
* CLK is TX_CLK in DTE mode and SYSCLK in repeater mode.

Figure 26. Loopback Mode Timing

Outline Diagram

Controlling dimensions are in millimeters.

84-Pin PLCC



Glossary

Baud—Rate at which signal level is changing (25 million symbols per second).

Baud Interval—The inverse of one baud or 40 ns.

Bit Rate (BR)—100 million bits per second.

Bit Time (BT)—The duration of one bit symbol as transferred to and from the media access controller (MAC). The bit time equals the inverse of bit rate or 10 ns.

Block—(1) A synonym for code group.

Code Group—A set of six ternary symbols (6T). The result of coding eight binary bits using 8B6T encoding. Internally in the LUC3X01, a code group is represented by 12 binary bits.

Data Terminal Equipment (DTE)—Also known as a DTE station and is usually a PC or workstation.

Dead Signal—Ten consecutive baud intervals where the differential input does not exceed 350 mV in either polarity.

Decoder—8B6T decoder. A circuit that maps a code group (6T) to 1 byte (8B). Internally in the LUC3X01, code groups are represented by 12 binary bits.

Device Channel—A transmit and/or receive data path through the LUC3X01 device.

Device Channel	Function
TX_D1	Transmit Only
RX_D2	Receive Only
BI_D3	Transmit/Receive
BI_D4	Transmit/Receive

Digital Sum Value (DSV)—Each code group is assigned a value –1, 0, and +1 to indicate its dc balance weight.

Encoder—8B6T encoder. A circuit that maps 1 byte (8B) to a code group (6T). Internally in the LUC3X01, code groups are represented by 12 binary bits.

End of Packet (EOP)—A collective set of five code groups appended to the transmit data stream after the CRC in a frame to designate the end of a packet. They are also used as part of the T4 dc balance restoration scheme. They are shown below with the rightmost symbol transmitted first.

Name	Code Group Symbols
EOP1	(+ 1 + 1 + 1 + 1 + 1 + 1) or (– 1 – 1 – 1 – 1 – 1 – 1)
EOP2	(– 1 –1 + 1 + 1 +1 +1) or (+ 1 +1 – 1 – 1 –1 –1)
EOP3	(0 0 – 1 – 1 + 1 + 1) or (0 0 + 1 + 1 – 1 – 1)
EOP4	(– 1 – 1 – 1 – 1 – 1 – 1) or (+ 1 + 1 + 1 + 1 + 1 + 1)
EOP5	(0 0 0 0 – 1 – 1) or (0 0 0 0 + 1 + 1)

EOP1, EOP2, EOP3, EOP4, and EOP5 are placed on the first, second, third, first, and second, respectively, device channel to finish transmitting a packet.

Frame—A group of symbols consisting of the destination and source addresses, length field, data field, pad field, and frame CRC. See packet.

Intersymbol Interference (ISI)—Generally, because of noise and other circuit considerations, it is impractical to restore a pulse transmitted over a transmission media to its original shape, or even to provide equalization which narrows to the extent that it is confined to one time slot. The shaped pulse will therefore have some spill over into the adjacent time slots. The sum of the precursors and tails from adjacent pulses that fall into a particular time slot is called the intersymbol interference.

Link-Integrity Pulse—A symbol pattern of –1 +1 symbols exactly two baud intervals long sent over UTP media between the DTE and repeater unit to determine if each other is operating and ready to transmit/receive packets.

Glossary (continued)

Media Access Control (MAC)—The data link sublayer that is responsible for transferring data to and from the physical layer. The LUC3X01 device uses the CSMA/CD method to access the transmission media.

Medium Attachment Unit (MAU)—The combination of PCS, PMA, and MDI sublayers (i.e., 3X01).

Media-Dependent Interface (MDI)—The mechanical and electrical interface between the UTP media and the MAU.

Media-Independent Interface (MII)—The interface between the physical layer device (PHY) or the LUC3X01 and the DTE whose primary goal is to allow media independence and multivendor interoperability. The MII defines the signals required for this interface and their clock to signal timing relationships.

Near-End Crosstalk (NEXT)—Crosstalk between two device channels whose power travels in the opposite direction to that of the signal in the disturbing device channel.

Packet—A group of symbols consisting of SOS code groups followed by the frame followed by the EOP code groups. See SOS, frame, and EOP.

Physical Coding Sublayer (PCS)—The portion of the MAU that provides logical functions coupling the MAU to the MII.

Physical Layer Device (PHY)—The combination of the PCS and PMA sublayers enclosed in an integrated circuit.

Physical Medium Attachment (PMA) Sublayer—The portion of the MAU that contains functional analog circuitry for transmission, reception, clock and skew-alignment.

Preamble—A code group of alternating +1 –1 symbols that precede the start of frame (SSD) delimiter. See SOS.

P3—The succession of two ternary symbols, – +, transmitted right to left.

P4—The succession of four ternary symbols, – + – +, transmitted right to left.

Running Digital Sum (RDS)—The continuous addition sum of the digital sum value (DSV) for each code group which is used to determine whether to invert a code group from the encoder prior to transmission in order to help maintain dc balance on the UTP media, or a received code group prior to input to the decoder while checking for dc balance violations.

Repeater—A mode of the LUC3X01 where block code groups are received and retransmitted without 8B6T decoding and encoding. This allows the LUC3X01 to act as a repeater unit in a star LAN type configuration.

Start of Stream Delimiter (SSD)—A binary byte which delimits the preamble from the data frame. This is the first byte of data to be passed across the MII when receiving a packet in the DTE mode.

Start of Packet (SOP)—This is the sequence – – + which are the last three ternary symbols in the SOSB code group. See also SOS.

Start of Stream (SOS)—SOS is a collective set of two code groups that precedes the transmit data stream to indicate the start of a packet. The code groups shown have the rightmost symbol transmitted first. See preamble and SSD.

Name	Code Group Symbols	Function
SOSA	(– 1 + 1 – 1 + 1 – 1 + 1)	Preamble
SOSB	(+ 1 –1 –1 +1 –1 + 1)	SSD

Symbol—A symbol representing one of three (ternary logical) signal (voltage) levels on the UTP media which occur in one baud interval as part of the 6T code. These levels are as shown in the table below.

Voltage Level	Symbol Representation	Alternate Symbol Representation
+3.5 V	+1	+
0 V	0	0
–3.5 V	–1	–

Symbol Rate (SR)—25 million symbols per second.

Symbol Time (T)—The duration of one ternary symbol or 40 ns (T = BT/4).

Wire Channel—A wire pair on the UTP media which may be designated by its EIA568 pair designation or RJ45 pin designation.

Section 3.1

Ordering Information

Device Code	Package	Temperature
LUC3X01	84-Pin PLCC	0 °C to 70 °C

General Packaging Information

Lucent Technologies recognizes that packaging has a dramatic effect on device and system performance. With today's accelerated development of smaller, more powerful devices, packaging technology has been compelled to react swiftly. Higher power ranges and tighter packaging densities are forcing engineers to re-evaluate the effectiveness of older, more traditional packaging technologies and styles.

Through the research efforts of Bell Laboratories, we are spearheading the development and acceptance of new packaging options in order to meet future demands for state-of-the-art devices and system applications. Because of our ongoing development efforts, we suggest that frequent inquiries be made regarding availability of new packaging options. In addition, Lucent Technologies offers assistance in resolving your special package needs.

Some of our newer packaging options include thermally and electrically enhanced high pin count, plastic quad flat packs (MQFP, SQFP, TQFP) and ball grid array (BGA) packages. Packages such as ball grid arrays and small-outline configurations bridge the gap of advancements in chip technology and the developments in automated circuit-board costs, while enhancing system performance.

Currently, we offer a choice of packages in both through-hole and surface-mount technologies. These packages accommodate high packaging densities with proven reliability.

Lucent Technologies has adopted the JEDEC packaging standards to allow for increased flexibility on our customers' behalf. As a member of JEDEC and its committees, Lucent Technologies has been instrumental in setting the standards for new packaging technologies. Our ongoing participation in JEDEC is your assurance that our packages meet industry standards and, in some cases, actually help establish those standards. Our devices are protected by our conformance with the United States Semiconductor Chip Protection Act of 1984. All of our packaging support services, including HSPICE modeling, sophisticated CAM systems, and state-of-the-art assembly testing procedures, enable us to provide total IC service to our customers. These are the qualities that help make Lucent Technologies a leader in integrated circuit technology.

For additional information regarding Lucent Technologies package offerings, please contact your Lucent Technologies Account Manager.

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Package Specifications

Following is the summary of package types currently available. Included in each table is thermal information.

Table A-1. PGA Package Summary

Package	Array Size	Lead Count	Thermal Resistance θ_{ja} (°C/Watt) (Free Convection)
Ceramic PGA	19 x 19	281	19
	33 x 33	365	18
	37 x 37	429	17
Plastic PGA	13 x 13†	121	22
	17 x 17	225	34
	18 x 18†	223	20
	20 x 20†	299	20

† Package contains thermal vias and copper planes.

Table A-2. BGA Package Summary*

Package	Ball Count Nominal (common)	Array Size	Ball Pitch (mm)	Body Size† (mm)	Structure	Signal I/O Count (Max)	Ball Count Options	Thermal Resistance (°C/Watt)
Overmolded Plastic Ball Grid Arrays (PBGA)	256	20 x 20	1.27	27 x 27 x 2.34	2 layer Overmolded	231 w/pwr & grd rings	256 w/ 4 outer rows	28
							272 w/ 4 x 4 center array‡	21
	352	26 x 26	1.27	35 x 35 x 2.56	2 layer Overmolded	304 w/pwr & grd rings	352 w/ 4 outer rows	25§
							388 w/ 6 x 6 center array‡	18§
Enhanced Ball Grid Arrays (EBGA)	168	17 x 17	1.27	23 x 23 x 1.65	*Super*BGA** Construction	168 w/pwr & grd rings	168 w/ 3 outer rows	25
	256	20 x 20	1.27	27 x 27 x 1.65	*Super*BGA Construction	192 w/pwr & grd rings	256 w/ 4 outer rows	16
	352	26 x 26	1.27	35 x 35 x 1.65	*Super*BGA Construction	300 w/pwr & grd rings	352 w/ 4 outer rows	12
	432	31 x 31	1.27	40 x 40 x 1.65	*Super*BGA Construction	348 w/pwr & grd rings	432 w/ 4 outer rows	10
	600	35 x 35	1.27	45 x 45 x 1.65	*Super*BGA Construction	460 w/pwr & grd rings	600 w/ 5 outer rows	8

* This information is for reference only. Please contact your Lucent Technologies design representative for details.
† (Width) x (Length) x (Height), Maximum height from the board to the top surface of the package before solder ball collapse.
‡ Center array options can be used as thermal enhancements, tie to ground plane only.
§ Estimated values.
** *Super*BGA is a registered trademark of Amkor/Anam Electronics, Inc.

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Table A-3. Plastic Package Summary

Package	Lead Count	Lead Material	Thermal Resistance θ_{ja} (°C/Watt)
Plastic DIP (PDIP) 0.300" Body	8	Cu	95
	14	Cu	84
	16	Cu	73
	18	Cu	68
	20	Cu	64
Plastic DIP (PDIP) 0.600" Body	24	Cu	57
	28	Cu	52
	32	Cu	49
	40	Cu	42
Plastic Leaded Chip Carrier (PLCC)	28	Cu	58
	44	Cu	49
	68	Cu	43
	84	Cu	40
Small Outline Package (SOP)	16	Cu	85
	20	Cu	80
	24	Cu	75
	28	Cu	70
Bumpered Quad Flat Pack (BQFP)	84	Cu	65
	100	Cu	55
	132	Cu Cu and H/S*	42 30
	164	Cu	37
Metric Quad Flat Pack (MQFP)	44	Alloy 42	117
	80	Cu	58
	100	Cu	57
	120	Cu Cu and H/S*	48 29
	128	Cu	48
	160	Cu Cu and H/S* *PQ2*†	40 28 16

* Cu and H/S = copper lead form and molded heat spreader.
† *PQ2* is a trademark of Amkor/Anam Electronics, Inc.

Table A-3. Plastic Package Summary (continued)

Package	Lead Count	Lead Material	Thermal Resistance θja (°C/Watt)
Shrink Quad Flat Pack (SQFP)	128	Cu	65
	208	Cu Cu and H/S* *PQ2*	37 27 16
	240	Cu Cu and H/S* *PQ2*	35 24 15
	304	Cu *PQ2*	33 12
Thin Quad Flat Pack (TQFP)	48	Cu	90
	64	Cu	73
	80	Cu	70
	100	Cu	64
	128	Cu	56
	144	Cu	52
	176	Cu *PQ2*	45 25

* Cu and H/S = copper lead form and molded heat spreader.
† *PQ2* is a trademark of Amkor/Anam Electronics, Inc.

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