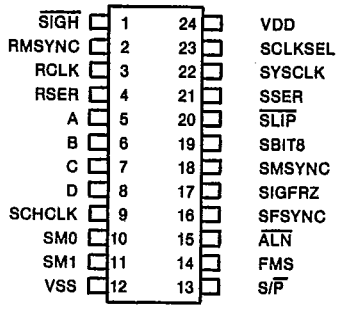
Dallas Semiconductor
T1 Receive Buffer

T-75-11-37
DS2176

FEATURES

- Synchronizes loop-timed and system-timed T1 data streams
- Two-frame buffer depth; slips occur on frame boundaries
- Output indicates when slip occurs
- Buffer may be recentered externally
- Ideal for 1.544 to 2.048 MHz rate conversion
- Interfaces to parallel or serial backplanes
- Extracts and buffers robbed-bit signalling
- Inhibits signalling updates during alarm or slip conditions
- Integration feature "debounces" signalling
- Slip-compensated output indicates when signalling updates occur
- Compatible with DS2180A T1 Transceiver
- Surface mount package available, designated DS2176Q
- Industrial temperature range of −40°C to +85°C available, designated DS2176IND

PIN CONNECTIONS



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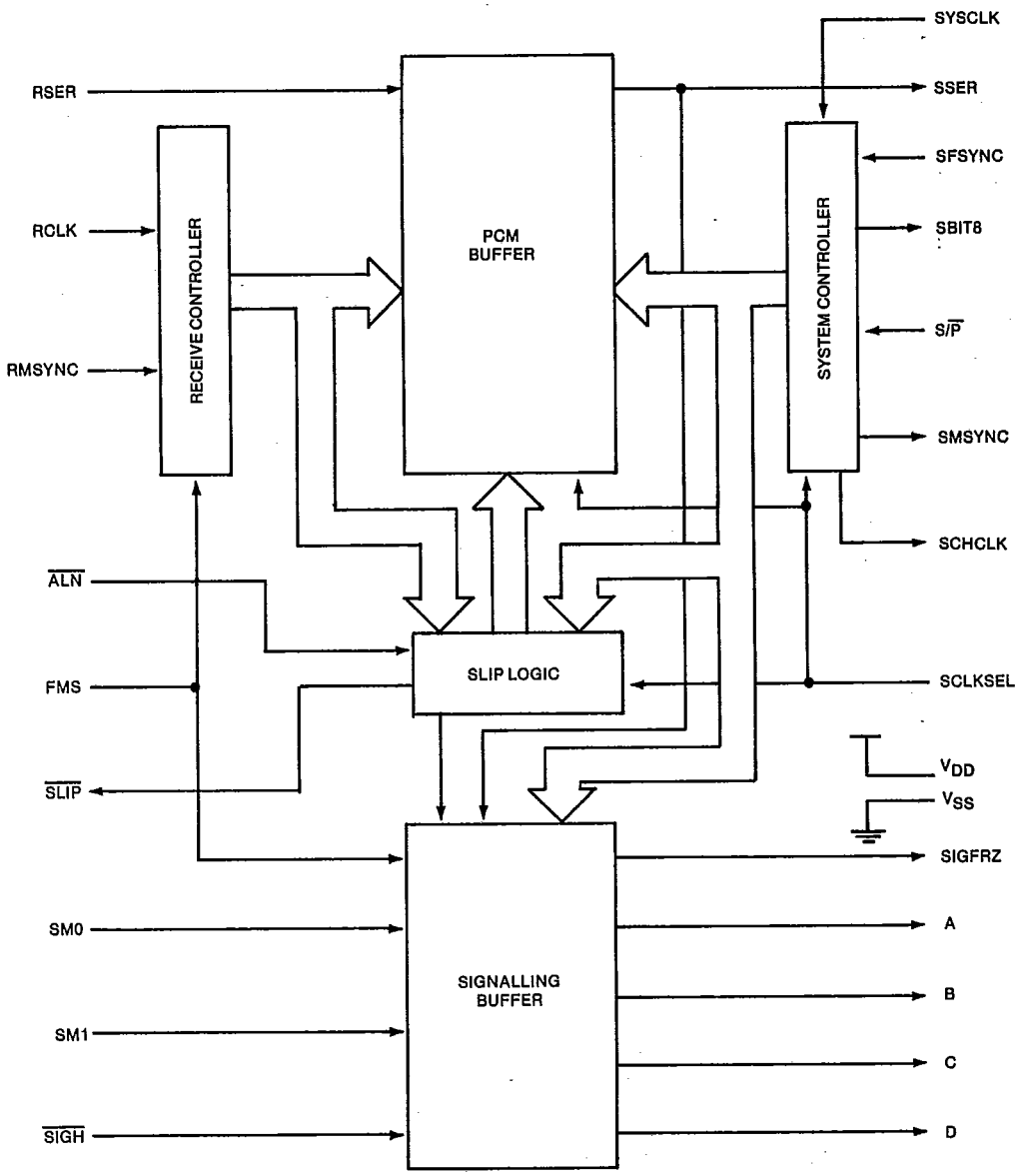
DESCRIPTION

The DS2176 is a low-power CMOS device specifically designed for synchronizing receive side loop-timed T-carrier data streams with system side timing. The device has several flexible operating modes which simplify interfacing incoming data to parallel and serial TDM backplanes. The device extracts, buffers and integrates ABCD signalling; signalling updates are prohibited during alarm or slip conditions. The buffer replaces extensive hardware in existing applications with one "skinny" 24-lead package. Application areas include digital trunks, drop and insert equipment, transcoders, digital cross-connects (DACS), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

DS2176 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

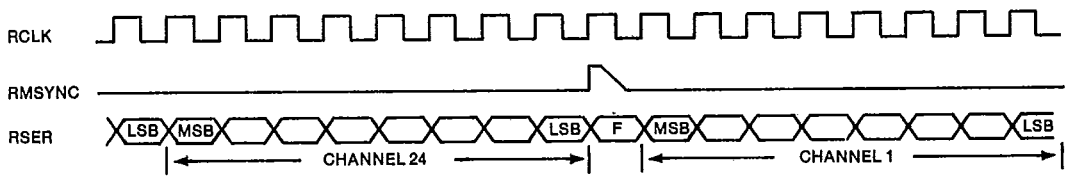
PIN	SYMBOL	TYPE	DESCRIPTION
1	$\overline{SIGH}$	I	**Signalling Inhibit.** When low, ABCD signalling updates are disabled for a period determined by SM0 and SM1, or until returned high.
2	RMSYNC	I	**Receive Multiframe Sync.** Must be pulsed high at multiframe boundaries to establish frame and multiframe alignment.
3	RCLK	I	**Receive Clock.** Primary 1.544 MHz clock.
4	RSER	I	**Receive Serial Data.** Sampled on falling edge of RCLK.
5 6 7 8	A B C D	O	**Robbed-Bit Signalling Outputs**
9	SCHCLK	O	**System Channel Clock.** Transitions high on channel boundaries; useful for serial to parallel conversion of channel data.
10 11	SM0 SM1	I	**Signalling Modes 0 and 1.** Select signalling supervision technique.
12	VSS	—	**Signal ground.** 0.0 volts.
13	S/$\overline{P}$	I	**Serial/Parallel Select.** Tie to VSS for parallel backplane applications, to VDD for serial.
14	FMS	I	**Frame Mode Select.** Tie to VSS to select 193S (D4) framing, to VDD for 193E (extended).
15	$\overline{ALN}$	I	**Align.** Recenters buffer on next system side frame boundary when forced low.
16	SFSYNC	I	**System Frame Sync.** Rising edge establishes start of frame.
17	SIGFRZ	O	**Signalling Freeze.** When high, indicates signalling updates have been disabled internally via a slip or externally by forcing $\overline{SIGH}$ low.
18	SMSYNC	O	**System Multiframe Sync.** Slip-compensated multiframe output; indicates when signalling updates are made.
19	SBIT8	O	**System Bit 8.** High during the LSB time of each channel. Used to reinsert extracted signalling into outgoing data stream.

20	$\overline{\text{SLIP}}$	O	**Frame Slip.** Active low, open collector output. Held low for 64 SYSCLK cycles when a slip occurs.
21	SSER	O	**System Serial Out.** Updated on rising edge of SYSCLK.
22	SYSCLK	I	**System Clock.** 1.544 or 2.048 MHz data clock.
23	SCLKSEL	I	**System Clock Select.** Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
24	VDD	—	**Positive Supply.** 5.0 volts.

OVERVIEW

The DS2176 performs two primary functions: 1) *synchronization* of received T1 PCM data (looped timed) to host backplane frequencies; 2) *supervision* of robbed-bit signalling data embedded in the data stream. The buffer, while optimized for use with the DS2180A T1 Transceiver, is also compatible with other transceiver devices. The DS2180A data sheet should serve as a valuable reference when designing with the DS2176.

RECEIVE SIDE TIMING Figure 2



DATA SYNCHRONIZATION

PCM BUFFER

The DS2176 utilizes a 2-frame buffer (386 bits) to synchronize incoming PCM data to the system backplane clock. The buffer samples data at RSER on the falling edge of RCLK. Output data appears at SSER and is updated on the rising edge of SYSCLK. A rising edge at RMSYNC establishes receive side frame and multiframe alignment. A rising edge at SFSYNC establishes system side frame alignment. The buffer depth is constantly monitored by on-board contention logic, a "slip" occurs when the buffer is completely emptied or filled. Slips automatically recenter the buffer to a one-frame depth and always occur on frame boundaries.

SLIP CORRECTION CAPABILITY

The 2-frame buffer depth is adequate for most T-carrier applications where short-term jitter synchronization, rather than correction of significant frequency differences, is required. The DS2176 provides an ideal balance between total delay and slip correction capability.

BUFFER RECENTERING

$\overline{SLIP}$ is held low for 65 SYSCLK cycles when a slip occurs. $\overline{SLIP}$ is an active-low, open-collector output.

BUFFER DEPTH MONITORING

SMSYNC is a system side output pulse which indicates system side multiframe boundaries. The distance between rising edges at RMSYNC and SMSYNC indicates the current buffer depth. Slip direction and/or an impending slip condition may be determined by monitoring RMSYNC and SMSYNC real time. SMSYNC is held high for 65 SYSCLK cycles.

CLOCK SELECT

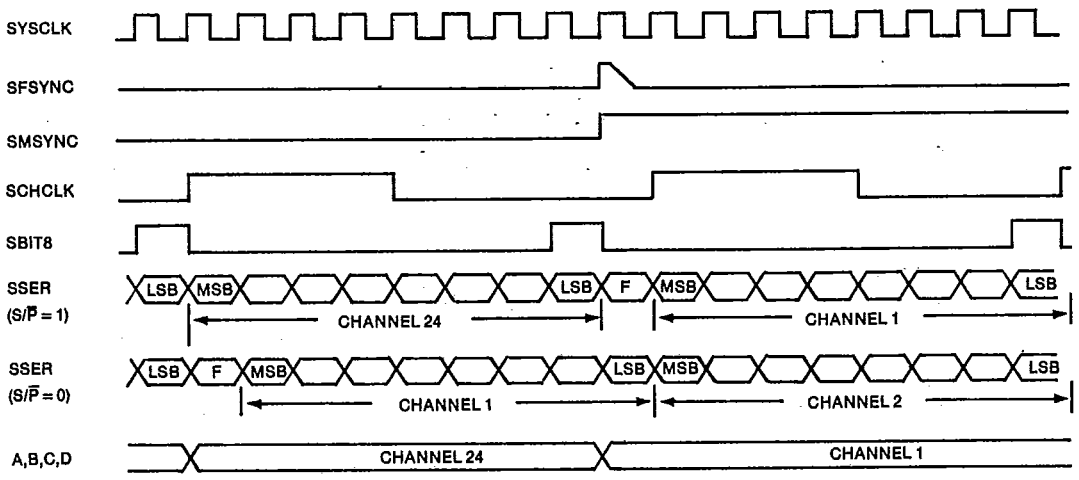
The device is compatible with 2 common backplane frequencies: 1.544 MHz, selected when SCLKSEL = 0; and 2.048 MHz, selected when SCLKSEL = 1. In 1.544 MHz applications the F-bit is passed through the receive buffer and presented at SSER immediately after a rising edge on SFSYNC. The F-bit is dropped in 2.048 MHz applications and the MSB of channel 1 appears at SSER one bit period after a rising edge at SFSYNC. SSER is forced to 1 in all channels greater than 24. See figures 3 and 4.

In 2.048 MHz applications (SCLKSEL = 1), the PCM buffer control logic establishes slip criteria different from that used in 1.544 MHz applications to compensate for the faster system-side read frequency.

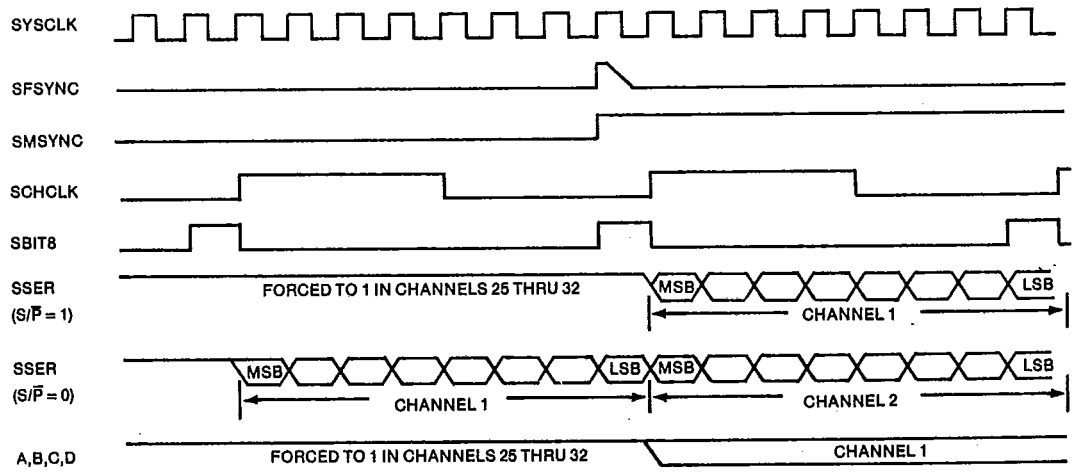
PARALLEL COMPATIBILITY

The DS2176 is compatible with parallel and serial backplanes. Channel 1 data appears at SSER after a rising edge at SFSYNC as shown in figures 3 and 4 (serial applications, $S/\overline{P} = 1$). The device utilizes a look-ahead circuit in parallel applications ($S/\overline{P} = 0$). Data is output 8 clocks earlier, allowing the user to parallel convert data externally.

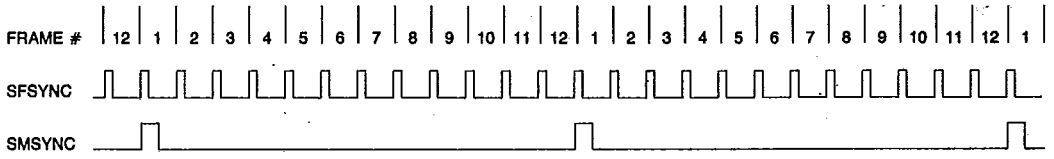
SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 1.544 MHZ) Figure 3



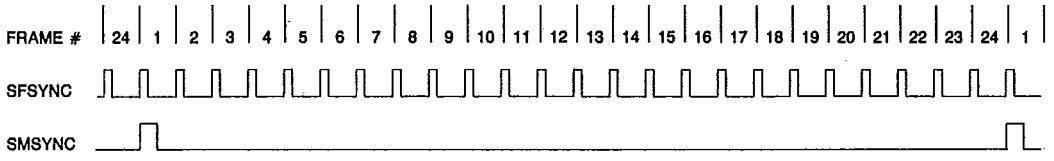
SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 2.048 MHZ) Figure 4



193S SYSTEM MULTIFRAME TIMING Figure 5



193E SYSTEM MULTIFRAME TIMING Figure 6



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SIGNALLING SUPERVISION

EXTRACTION

In digital channel banks, robbed-bit signalling data is inserted into the LSB position of each channel during signalling frames. In 193S framing (FMS = 0) applications, A signalling data is inserted into frame 6 and B signalling data is inserted into frame 12. 193E framing (FMS = 1) includes 2 additional signalling bits: C signalling is inserted into frame 18 and D signalling is inserted into frame 24. This embedded signalling data is synchronized to system side timing (via the PCM buffer) before being extracted and presented at outputs A,B,C and D. Outputs A,B,C and D are valid for each individual channel time and are repeated per channel for all frames of the multiframe. In 193S applications, outputs C and D contain the previous multiframe's A and B data. Signalling updates occur once per multiframe at the rising edge of SMSYNC unless prohibited by a freeze.

FREEZE

The signalling buffer allows the DS2176 to "freeze" (prevent update of) signalling information during alarm or slip conditions. A slip condition or forcing $\overline{\text{SIGH}}$ low freezes signalling; duration of the freeze is dependent on SM0 and SM1. Updates will be unconditionally prohibited when $\overline{\text{SIGH}}$ is held low. During freezing conditions "old" data is recirculated in the output registers and appears at A,B,C and D. SIGFRZ is held high during the freeze condition, and returns low on the next signalling update. Input to output delay of signalling data is equal to 1 multiframe (the depth of the signalling buffer) + the current depth of the PCM buffer (1 frame ± approximately 1 frame).

INTEGRATION

Signalling integration is another feature of the DS2176; when selected, it minimizes the impact of random noise hits on the span and resultant robbed-bit signalling corruption. Integration requires that per-channel signalling data be in the same state for 2 or more multiframes before appearing at A,B,C and D. SM0 and SM1 are used to select the degree of integration or to totally bypass the feature. Integration is limited to 2 multiframes during slip or alarm conditions to minimize update delay.

CLEAR CHANNEL CONSIDERATIONS

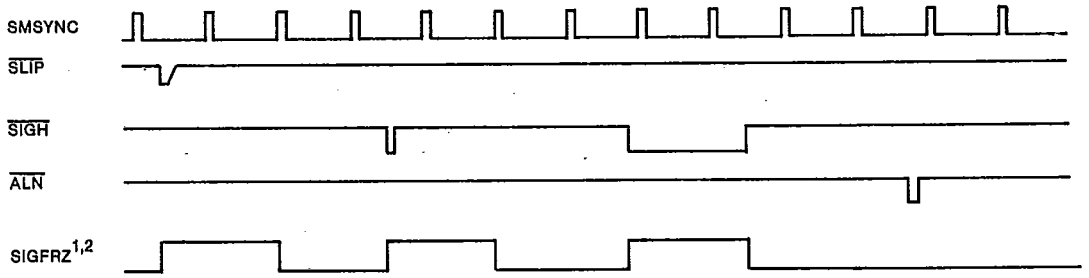
The DS2176 does not merge the "processed" signalling information with outgoing PCM data at SSER; this assures integrity of data in clear channel applications. SBIT8 indicates the LSB position of each channel; when combined with off-chip support logic, it allows the user to selectively re-insert robbed-bit signalling data into the outgoing data stream.

SIGNALLING SUPERVISION MODES Table 2

SM0	SM1	FMS	SELECTED MODE
0	0	0	193S framing, no integration, 1 multiframe freeze.
0	0	1	193E framing, no integration, 1 multiframe freeze.
0	1	0	193S framing, 2 multiframes integration and freeze.
0	1	1	193E framing, 2 multiframes integration and freeze.
1	0	0[1]	193S framing, 5 multiframes integration, 2 multiframes freeze.
1	0	1[1]	193E framing, 3 multiframes integration, 2 multiframes freeze.
1	1	0	Test mode.
1	1	1	Test mode.

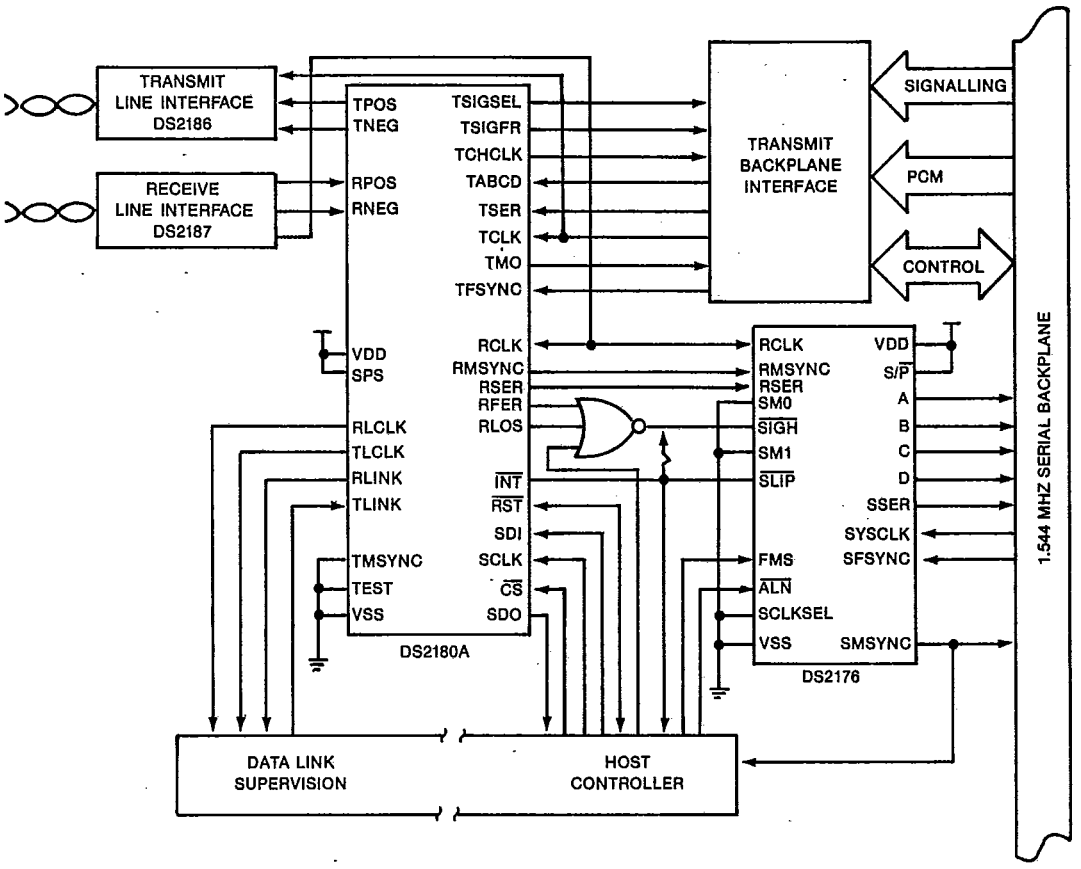
NOTES:
1. During slip or alarm conditions, integration is limited to 2 multiframes to minimize signalling delay.

SLIP AND SIGNALLING SUPERVISION LOGIC TIMING Figure 7



NOTES:
1. Integration feature disabled (SM0 = SM1 = 0) in timing set shown.
2. Depending on present buffer depth, forcing $\overline{\text{ALN}}$ low may or may not cause a slip condition.

SERIAL 1.544 MHZ BACKPLANE INTERFACE Figure 8



DS2176/DS2180A SYSTEM APPLICATION

Figure 8 shows how the DS2180A T1 Transceiver and DS2176 Receive Buffer interconnect in a typical application.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground −1.0V to + 7.0V
Operating Temperature 0 °C to 70 °C
Storage Temperature −55 °C to +125 °C
Soldering Temperature 260 °C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0 °C to 70 °C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{DD}+0.3$	V	
Logic 0	V_{IL}	−0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

D.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		6	10	mA	1,2
Input Leakage	I_{IL}	−1.0		+1.0	uA	
Output Current @2.4V	I_{OH}	−1.0			mA	3
Output Current @0.4V	I_{OL}	+4.0			mA	4
Output Leakage	I_{LO}	−1.0		+1.0	uA	5

NOTES:

1. TCLK = RCLK = 1.544 MHz
2. Outputs open
3. All outputs except $\overline{SLIP}$, which is open collector
4. All outputs
5. Applies to $\overline{SLIP}$ when tri-stated

CAPACITANCE ($t_A = 25°C$)

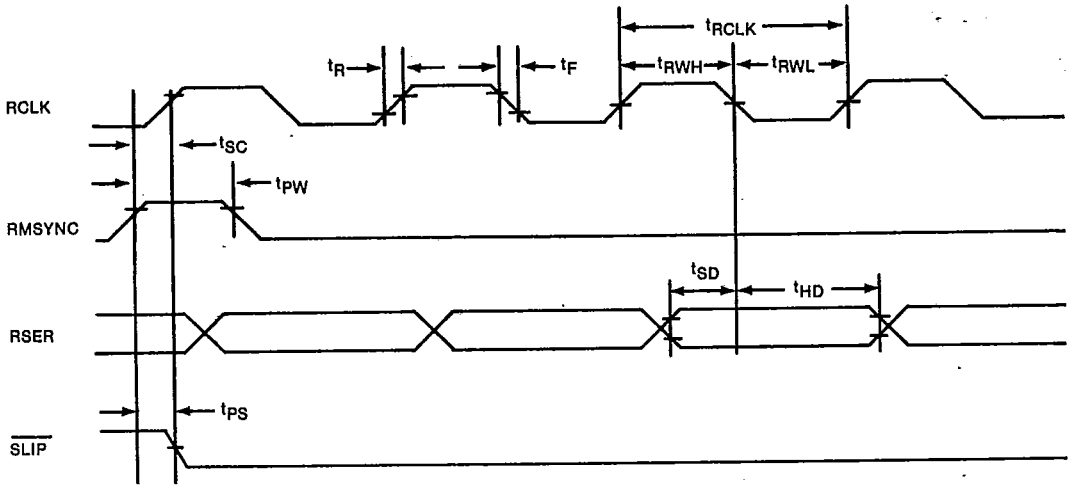
PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{DD} = 5V \pm 10\%$)

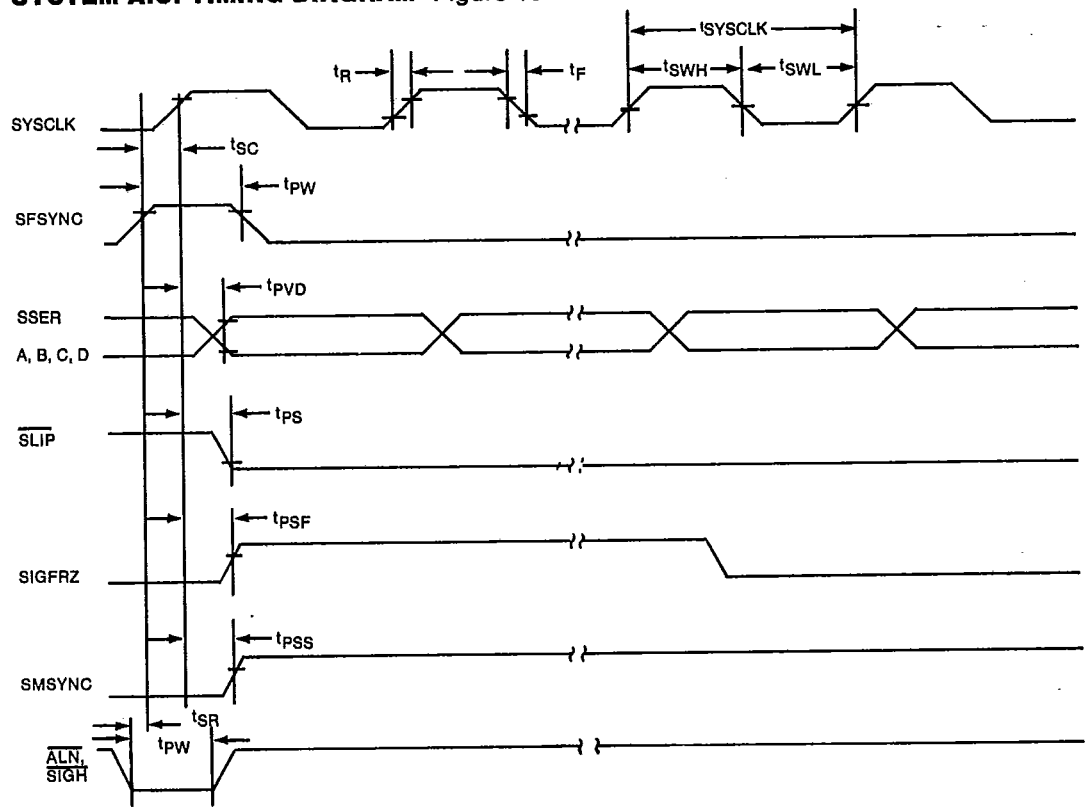
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{RCLK}	250	648		ns	
RCLK, SYSCLK Rise and Fall Times	t_R, t_F			20	ns	
RCLK Pulse Width	t_{RWH}, t_{RWL}	125	324		ns	
SYSCLK Pulse Width	t_{SWH}, t_{SWL}	100	244		ns	
SYSCLK Period	t_{SYSCLK}	200	488		ns	
RMSYNC Setup to RCLK Rising	t_{SC}	$-t_{RWH}/2$		$+t_{RWL}/2$	ns	
SFSYNC Setup to SYSCLK Rising	t_{SC}	$-t_{SWH}/2$		$+t_{SWL}/2$	ns	
$\overline{\text{RMSYNC}}$, SFSYNC, $\overline{\text{SIGH}}$ $\overline{\text{ALN}}$ Pulse Width	t_{PW}	100			ns	
RSER Setup to RCLK Falling	t_{SD}	50			ns	
RSER Hold from RCLK Falling	t_{HD}	50			ns	
Propagation Delay SYSCLK to $\overline{\text{SSER}}$, A,B,C,D	t_{PVD}			100	ns	
Propagation Delay SYSCLK to $\overline{\text{SMSYNC}}$ High	t_{PSS}			75	ns	
Propagation Delay SYSCLK or RCLK to $\overline{\text{SLIP}}$ Low	t_{PS}			100	ns	
Propagation Delay SYSCLK to SIGFRZ Low/High	t_{PSF}			75	ns	
$\overline{\text{ALN}}$, $\overline{\text{SIGH}}$ Setup to SFSYNC Rising	t_{SR}	500			ns	

NOTES:
1. Measured at $V_{IH} = 2.0V$, $V_{IL} = 0.8V$, and 10 ns maximum rise and fall times.
2. Output load capacitance = 100 pF.

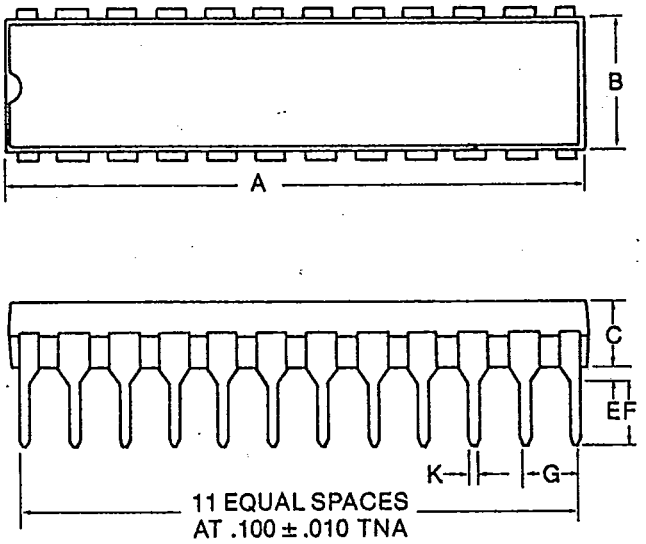
RECEIVE A.C. DIAGRAM Figure 9



SYSTEM A.C. TIMING DIAGRAM Figure 10



DS2176
T1 Receive Buffer



DIM.	INCHES	
	MIN.	MAX.
A	1.150	1.190
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.325	.375
J	.008	.012
K	.015	.021

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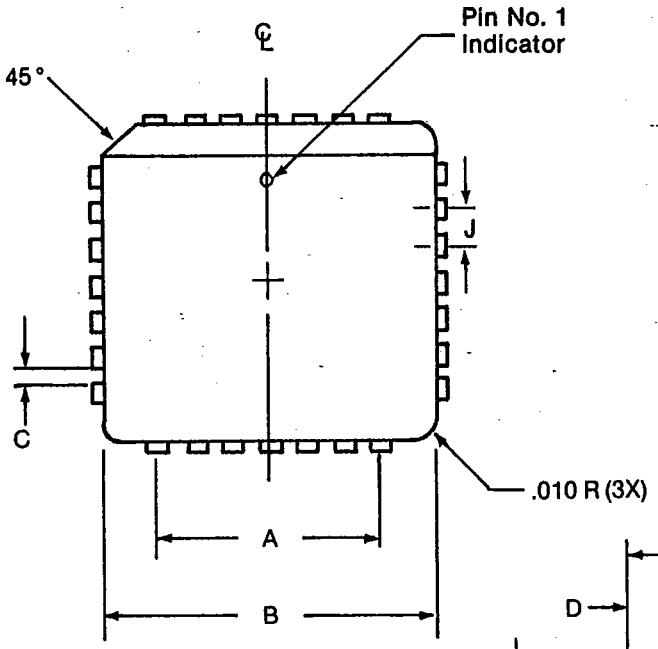
DS2176Q



DIM.	INCHES	
	MIN.	MAX.
A	.290	.310
B	.441	.451
C	.020	.024
D	.018	.022
E	.488	.492
F	.118	.122
G	.020	.030
H	.390	.430
I	.167	.173
J	.048	.052