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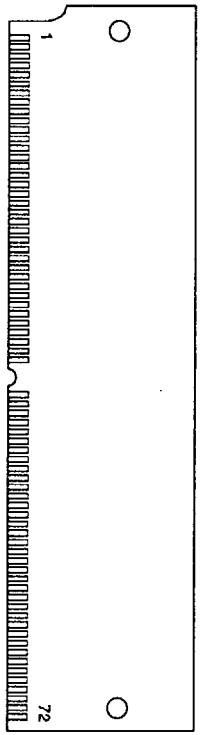
# DS2251(T)
## 128K Soft Microcontroller

### FEATURES

- 8051 compatible uC adapts to its task
  - 32, 64, or 128K bytes of nonvolatile SRAM for program and/or data storage
  - In–system programming via on–chip serial port
  - Capable of modifying its own program or data memory in the end system
  - Provides separate Byte–wide bus for peripherals
  - Performs CRC–16 check of NVRAM memory
- Crashproof Operation
  - Maintains all nonvolatile resources for over 10 years in the absence of power
  - Power–fail reset
  - Early Warning Power–fail Interrupt
  - Watchdog Timer
  - Lithium backed memory remembers system state
  - Precision reference for power monitor
- Fully 8051 Compatible
  - 128 bytes scratchpad RAM
  - Two timer/counters
  - On–chip serial port
  - 32 parallel I/O port pins
- Optional permanently powered Real–time Clock (DS2251T)

### PACKAGE OUTLINE




72–PIN SIMM

### DESCRIPTION

The DS2251(T) is an 8051 compatible microcontroller based on nonvolatile RAM technology. It is designed for systems that need large quantities of nonvolatile memory. Like other members of the Soft Micro family, it provides full compatibility with the 8051 instruction set, timers, serial port, and parallel I/O ports. By using NVRAM instead of ROM, the user can program, then reprogram the microcontroller while in–system. The application software can even change its own operation. This allows frequent software upgrades, adaptive programs, customized systems, etc. In addition, by using NVSRAM, the DS2251(T) is ideal for data logging applications. The DS2251T provides a powerful Real–time Clock with interrupts for time stamp and date. It keeps time to one hundredth of second using its on–board 32 KHz crystal.

The DS2251(T) provides the benefits of NVRAM without using I/O resources. Between 32K bytes and 128K bytes of on–board NVRAM are available. A non–multiplexed Byte–wide address and data bus is used for memory access. This bus, which is available at the connector, can perform all memory access and also provides decoded chip enables for off–board memory

mapped peripherals. This leaves the 32 I/O port pins free for application use.

The DS2251(T) provides crashproof operation in portable systems or systems with unreliable power. These features include the ability to save the operating state, Power–fail Reset, Power–fail Interrupt, and Watchdog Timer. All nonvolatile memory and resources are maintained for over 10 years at room temperature in the absence of power.

A user loads programs into the DS2251(T) via its on–chip Serial Bootstrap Loader. This function supervises the loading of software into NVRAM, validates it, then becomes transparent to the user. Software is stored in on–board CMOS SRAM. Using its internal Partitioning, the DS2251(T) can divide a common RAM into user selectable program and data segments. This Partition can be selected at program loading time, but can be modified anytime later. The micro will decode memory access to the SRAM, access memory via its Byte–wide bus and write–protect the memory portion designated as program (ROM).

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## ORDERING INFORMATION

| PART NUMBER | RAM SIZE | MAX CRYSTAL SPEED | TIMEKEEPING? |
|---|---|---|---|
| DS2251–32–12 | 32K bytes | 12 MHz | No |
| DS2251–32–16 | 32K bytes | 16 MHz | No |
| DS2251–64–12 | 64K bytes | 12 MHz | No |
| DS2251–64–16 | 64K bytes | 16 MHz | No |
| DS2251–128–12 | 128K bytes | 12 MHz | No |
| DS2251–128–16 | 128K bytes | 16 MHz | No |
| DS2251T–32–12 | 32K bytes | 12 MHz | Yes |
| DS2251T–32–16 | 32K bytes | 16 MHz | Yes |
| DS2251T–64–12 | 64K bytes | 12 MHz | Yes |
| DS2251T–64–16 | 64K bytes | 16 MHz | Yes |
| DS2251T–128–12 | 128K bytes | 12 MHz | Yes |
| DS2251T–128–16 | 128K bytes | 16 MHz | Yes |

Operating information is contained in the User's Guide section of the Soft Microcontroller Data Book. This data sheet provides ordering information, pinout, and electrical specifications.

## DS2251(T) BLOCK DIAGRAM Figure 1

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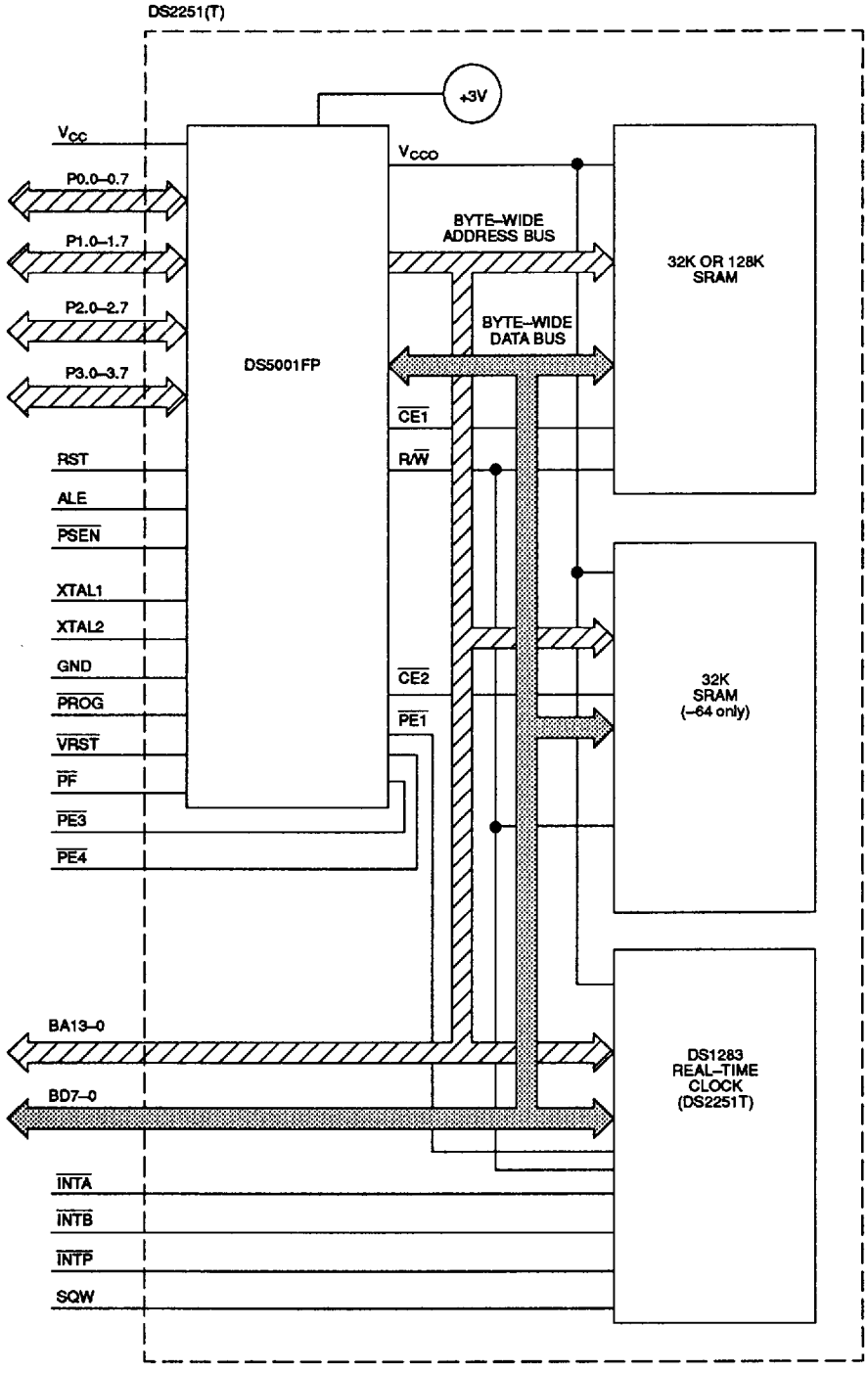

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## PIN ASSIGNMENT

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | P1.0 | 19 | XTAL2 | 37 | P0.2 | 55 | $\overline{INTB}$ |
| 2 | P1.1 | 20 | GND | 38 | P0.1 | 56 | BD0 |
| 3 | P1.2 | 21 | P2.0 | 39 | P0.0 | 57 | BD1 |
| 4 | P1.3 | 22 | P2.1 | 40 | $V_{CC}$ | 58 | BD2 |
| 5 | P1.4 | 23 | P2.2 | 41 | BA0 | 59 | BD3 |
| 6 | P1.5 | 24 | P2.3 | 42 | BA1 | 60 | BD4 |
| 7 | P1.6 | 25 | P2.4 | 43 | BA2 | 61 | BD5 |
| 8 | P1.7 | 26 | P2.5 | 44 | BA3 | 62 | BD6 |
| 9 | RST | 27 | P2.6 | 45 | BA4 | 63 | BD7 |
| 10 | P3.0 RXD | 28 | P2.7 | 46 | BA5 | 64 | R/$\overline{W}$ |
| 11 | P3.1 TXD | 29 | $\overline{PSEN}$ | 47 | BA6 | 65 | $\overline{PF}$ |
| 12 | P3.2 $\overline{INT0}$ | 30 | ALE | 48 | BA7 | 66 | $\overline{PE3}$ |
| 13 | P3.3 $\overline{INT1}$ | 31 | $\overline{PROG}$ | 49 | BA8 | 67 | $\overline{PE4}$ |
| 14 | P3.4 T0 | 32 | P0.7 | 50 | BA9 | 68 | $\overline{INTP}$ |
| 15 | P3.5 T1 | 33 | P0.6 | 51 | BA10 | 69 | $\overline{INTA}$ |
| 16 | P3.6 $\overline{WR}$ | 34 | P0.5 | 52 | BA11 | 70 | SQW |
| 17 | P3.7 $\overline{RD}$ | 35 | P0.4 | 53 | BA12 | 71 | $\overline{VRST}$ |
| 18 | XTAL1 | 36 | P0.3 | 54 | BA13 | 72 | BA15 |

## PIN DESCRIPTION

| PIN NUMBER | DESCRIPTION |
|---|---|
| 39–32 | P0.0–P0.7<br>General purpose I/O Port 0. This port is open–drain and can not drive a logic 1. It requires external pull–ups. Port 0 is also the multiplexed Expanded Address/Data bus. When used in this mode, it does not require pull–ups. |
| 1–8 | P1.0 – P1.7<br>General purpose I/O Port 1. |
| 21–28 | P2.0–P2.7<br>General purpose I/O Port 2. Also serves as the MSB of the Expanded Address bus. |
| 10 | P3.0 RXD<br>General purpose I/O port pin 3.0. Also serves as the receive signal for the on board UART. This pin should NOT be connected directly to a PC COM port. |
| 11 | P3.1 TXD<br>General purpose I/O port pin 3.1. Also serves as the transmit signal for the on board UART. This pin should NOT be connected directly to a PC COM port. |
| 12 | P3.2 $\overline{INT0}$<br>General purpose I/O port pin 3.2. Also serves as the active low External Interrupt 0. |
| 13 | P3.3 $\overline{INT1}$<br>General purpose I/O port pin 3.3. Also serves as the active low External Interrupt 1. |
| 14 | P3.4 T0<br>General purpose I/O port pin 3.4. Also serves as the Timer 0 input. |
| 15 | P3.5 T1<br>General purpose I/O port pin 3.5. Also serves as the Timer 1 input. |

| PIN NUMBER | DESCRIPTION |
|---|---|
| 16 | P3.6 $\overline{WR}$<br>General purpose I/O port pin. Also serves as the write strobe for Expanded bus operation. |
| 17 | P3.7 $\overline{RD}$<br>General purpose I/O port pin. Also serves as the read strobe for Expanded bus operation. |
| 9 | RST<br>Active high reset input. A logic 1 applied to this pin will activate a reset state. This pin is pulled down internally, can be left unconnected if not used. An RC power–on reset circuit is not needed and is NOT recommended. |
| 29 | $\overline{PSEN}$<br>Program Store Enable. This active low signal is used to enable an external program memory when using the Expanded bus. It is normally an output and should be unconnected if not used. |
| 30 | ALE<br>Address Latch Enable. Used to de–multiplex the multiplexed Expanded Address/Data bus on Port 0. This pin is normally connected to the clock input on a '373 type transparent latch. |
| 19, 18 | XTAL2, XTAL1<br>Used to connect an external crystal to the internal oscillator. XTAL1 is the input to an inverting amplifier and XTAL2 is the output. |
| 20 | GND<br>Logic ground. |
| 40 | $V_{CC}$<br>+5V |
| 72 | BA15<br>Monitor test point to reflect the logical value of A15. Not needed for memory access. |
| 54–41 | BA13–0<br>Byte–wide Address bus bits 13–0. This bus is combined with the non–multiplexed data bus (BD7–0) to access on–board NVSRAM and off–board peripherals. Peripheral decoding is performed using $\overline{PE3}$ and $\overline{PE4}$. These are on 16K boundaries, so BA14 or BA15 are not needed. Read/write access is controlled by R/$\overline{W}$. BA13–0 connect directly to memory mapped peripherals. |
| 63–56 | BD7–0<br>Byte–wide Data bus bits 7–0. This 8 bit bi–directional bus is combined with the non–multiplexed address bus (BA14–0) to access on–board NVSRAM and off–board peripherals. |
| 64 | R/$\overline{W}$<br>Read/Write. This signal provides the write enable to the SRAMs on the Byte–wide bus. It is controlled by the memory map and Partition. The blocks selected as Program (ROM) will be write protected. This signal is also used for the write enable to off–board peripherals. |
| 66 | $\overline{PE3}$<br>Peripheral Enable 3. Accesses data memory between addresses 8000h and BFFFh when the PES bit is set to a logic 1. $\overline{PE3}$ is not lithium backed and can be connected to any type of peripheral function. |
| 67 | $\overline{PE4}$<br>Peripheral Enable 4. Accesses data memory between addresses C000h and FFFFh when the PES bit is set to a logic 1. $\overline{PE4}$ is not lithium backed and can be connected to any type of peripheral function. |

| PIN NUMBER | DESCRIPTION |
|---|---|
| 31 | $\overline{PROG}$<br>Invokes the Bootstrap loader on a falling edge. This signal should be debounced so that only one edge is detected. If connected to ground, the micro will enter Bootstrap loading on power up. This signal is pulled up internally. |
| 71 | $\overline{VRST}$<br>This I/O pin indicates that the power supply ($V_{CC}$) has fallen below the $V_{CCMIN}$ level and the micro is in a reset state. When this occurs, the DS2251(T) will drive this pin to a logic 0. Because the micro is lithium backed, this signal is guaranteed even when $V_{CC}$=0V. Because it is an I/O pin, it will also force a reset if pulled low externally. This allows multiple parts to synchronize their power–down resets. |
| 65 | $\overline{PF}$<br>This output goes to a logic 0 to indicate that the micro has switched to lithium backup. It corresponds to $V_{CC} < V_{LI}$. Because the micro is lithium backed, this signal is guaranteed even when $V_{CC}$=0V. |
| 55 | $\overline{INTB}$<br>$\overline{INTB}$ from the Real–time Clock. This output may be connected to a micro interrupt input. |
| 68 | $\overline{INTP}$<br>$\overline{INTP}$ from the Real–time Clock. This open–drain output requires a pull–up and may beconnected to a micro interrupt input. |
| 69 | $\overline{INTA}$<br>$\overline{INTA}$ from the Real–time Clock. This output may be connected to a micro interrupt input. |
| 70 | SQW<br>SQW output from the DS1283 Real–time Clock. Can be programmed to output an 1024 Hz square wave. |

## INSTRUCTION SET

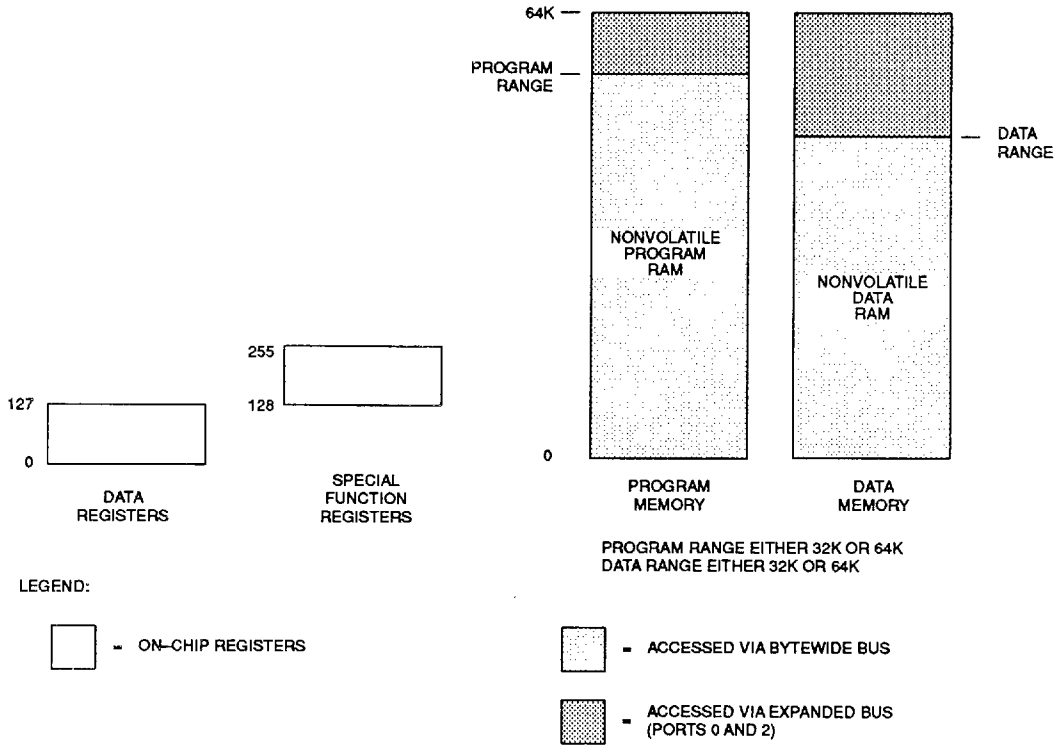
The DS2251(T) executes an instruction set that is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages such as assemblers and compilers that have been written for the 8051 are compatible with the DS2251(T).

A complete description of the instruction set and operation are provided in the User's Guide section of the Soft Microcontroller Data Book.

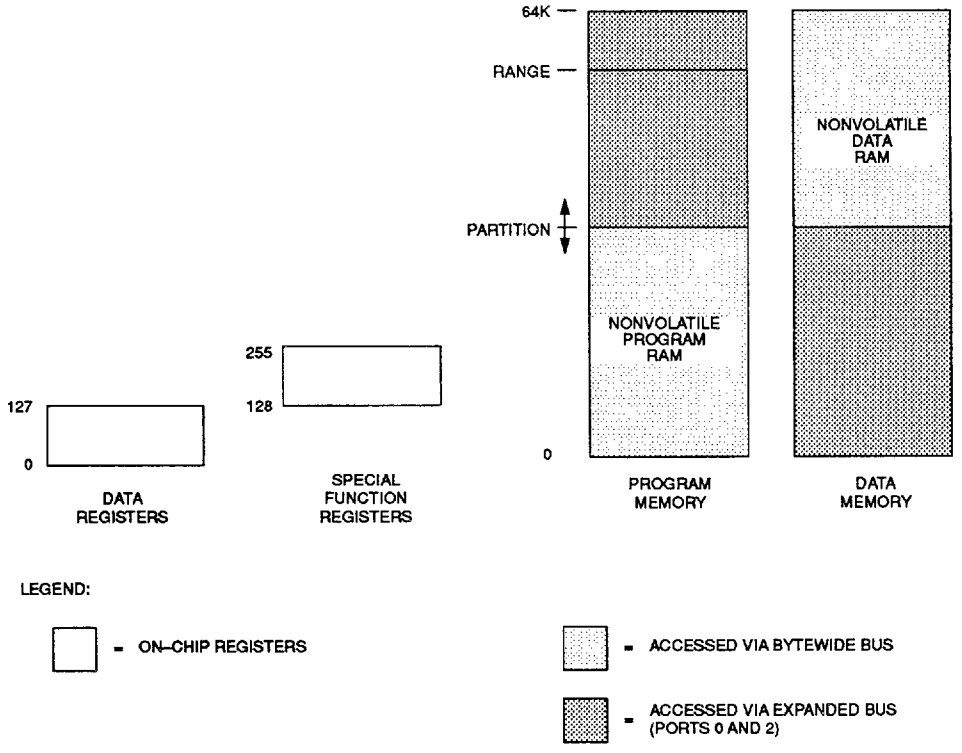
## MEMORY ORGANIZATION

Figure 2 illustrates the memory map accessed by the DS2251(T). The entire 64K of program and 64K of data are available to the Byte–wide bus. This preserves the I/O ports for application use. The user controls the portion of memory that is actually mapped to the Byte–wide bus by selecting the Program Range and Data Range. Any area not mapped into the NVRAM is reached via the Expanded bus on Ports 0 and 2. An alternate configuration allows dynamic Partitioning of a 64K space as shown in Figure 3. Selecting PES=1 provides access to the Real–time Clock on the DS2251T and enables $\overline{PE3}$ and $\overline{PE4}$ for peripheral access as shown in Figure 4. These selections are made using Special Function Registers. The memory map and its controls are covered in detail in the User's Guide section of the Soft Microcontroller Data Book.

**MEMORY MAP OF THE DS2251(T) WITH PM=1** Figure 2



**MEMORY MAP OF THE DS2251(T) WITH PM=0** Figure 3

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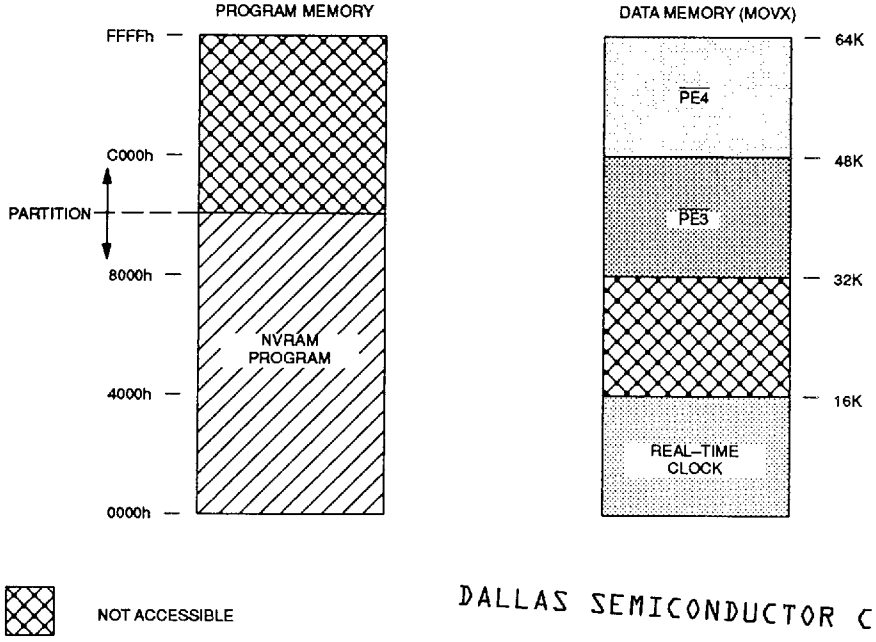
**MEMORY MAP OF THE DS2251(T) WITH PES=1** Figure 4

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## POWER MANAGEMENT

The DS2251(T) monitors $V_{CC}$ to provide Power–fail Reset, early warning Power–fail Interrupt, and switch over to lithium backup. It uses an internal band–gap reference in determining the switch points. These are called $V_{PFW}$, $V_{CCMIN}$, and $V_{LI}$ respectively. When $V_{CC}$ drops below $V_{PFW}$, the DS2251(T) will perform an interrupt vector to location 2Bh if the power fail warning was enabled. Full processor operation continues regardless. When power falls further to $V_{CCMIN}$, the DS2251(T) invokes a reset state. No further code execution will be performed unless power rises back above $V_{CCMIN}$. All decoded chip enables and the R/$\overline{W}$ signal go to an inactive (logic 1) state. The $\overline{VRST}$ signal will be driven to a a logic 0. $V_{CC}$ is still the power source at this time. When $V_{CC}$ drops further to below $V_{LI}$, internal circuitry will switch to the built–in lithium cell for power. The majority of internal circuits will be disabled and the remaining nonvolatile states will be retained. $\overline{PF}$ will be driven to a logic 0. The User's Guide has more information on this topic. The trip points $V_{CCMIN}$ and $V_{PFW}$ are listed in the electrical specifications.

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## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on Any Pin Relative to Ground | –0.3V to 7.0V |
| Operating Temperature | 0°C to +70°C |
| Storage Temperature | –40°C to 70°C |
| Soldering Temperature | 260°C for 10 seconds |

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## DC CHARACTERISTICS

($t_A$ = 0°C to70°C; $V_{CC}$ = 5V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | -0.3 | | 0.8 | V | 1 |
| Input High Voltage | $V_{IH1}$ | 2.0 | | $V_{CC}$ +0.3 | V | 1 |
| Input High Voltage RST, XTAL1 $\overline{PROG}$ | $V_{IH2}$ | 3.5 | | $V_{CC}$ +0.3 | V | 1 |
| Output Low Voltage @ $I_{OL}$=1.6mA (Ports 1, 2, 3) | $V_{OL1}$ | | 0.15 | 0.45 | V | 1 |
| Output Low Voltage @ $I_{OL}$=3.2mA (Ports 0, ALE, $\overline{PSEN}$, $\overline{PF}$, BA13–0, BD7–0, R/$\overline{W}$, $\overline{PE3–4}$) | $V_{OL2}$ | | 0.15 | 0.45 | V | 1 |
| Output High Voltage @ $I_{OH}$=-80µA (Ports 1, 2, 3) | $V_{OH1}$ | 2.4 | 4.8 | | V | 1 |
| Output High Voltage @ $I_{OH}$=-400 µA (Ports 0, ALE, $\overline{PSEN}$, $\overline{PF}$, BA13–0, BD7–0, R/$\overline{W}$, $\overline{PE3–4}$) | $V_{OH2}$ | 2.4 | 4.8 | | V | 1 |
| Input Low Current $V_{IN}$ = 0.45V (Ports 1, 2, 3) | $I_{IL}$ | | | -50 | µA | |
| Transition Current; 1 to 0 $V_{IN}$ = 2.0V (Ports 1, 2, 3) | $I_{TL}$ | | | -500 | µA | |
| Input Leakage Current 0.45 < $V_{IN}$ < $V_{CC}$ (Port 0) | $I_{IL}$ | | | ±10 | µA | |
| RST Pulldown Resistor | $R_{RE}$ | 40 | | 150 | KΩ | |
| $\overline{VRST}$ Pullup Resistor | $R_{VR}$ | | 4.7 | | KΩ | |
| $\overline{PROG}$ Pullup Resistor | $R_{PR}$ | | 40 | | KΩ | |
| Power Fail Warning Voltage | $V_{PFW}$ | 4.25 | 4.37 | 4.50 | V | 1 |
| Minimum Operating Voltage | $V_{CCmin}$ | 4.00 | 4.12 | 4.25 | V | 1 |
| Operating Current | $I_{CC}$ | | | 45 | mA | 2 |
| Idle Mode Current | $I_{IDLE}$ | | | 7.0 | mA | 3 |
| Stop Mode Current | $I_{STOP}$ | | | 80 | µA | 4 |
| Pin Capacitance | $C_{IN}$ | | | 10 | pF | 5 |
| Reset Trip Point in Stop Mode<br>w/BAT=3.0V<br>w/BAT=3.3V | | <br>4.0<br>4.4 | | <br>4.25<br>4.65 | V | 1 |

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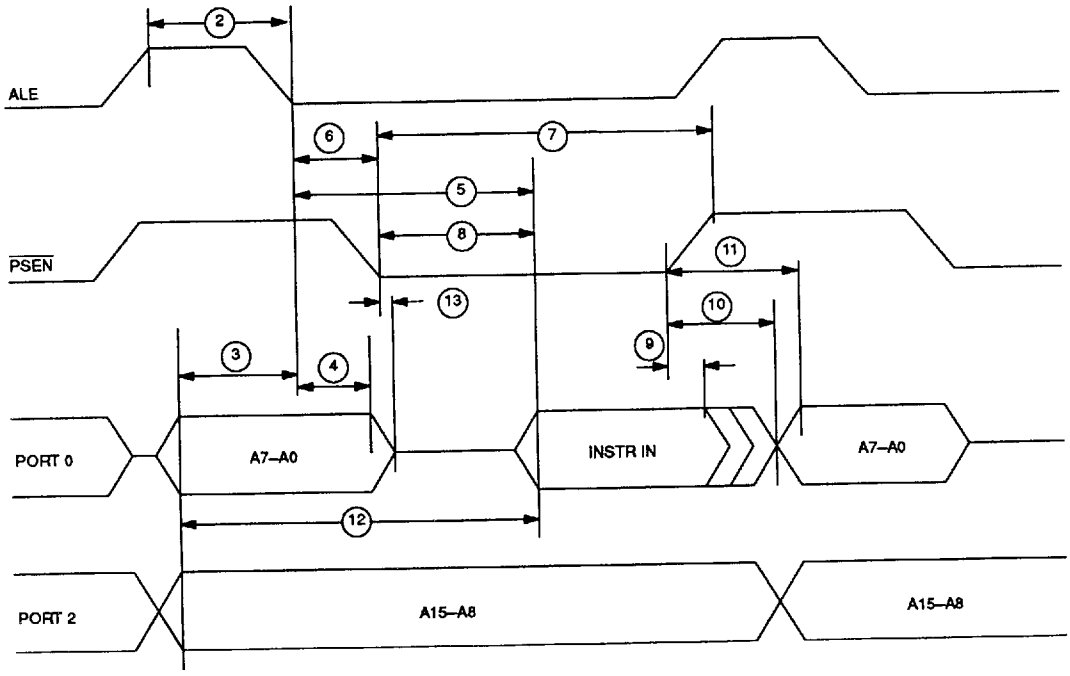
## AC CHARACTERISTICS
## EXPANDED BUS MODE TIMING SPECIFICATIONS

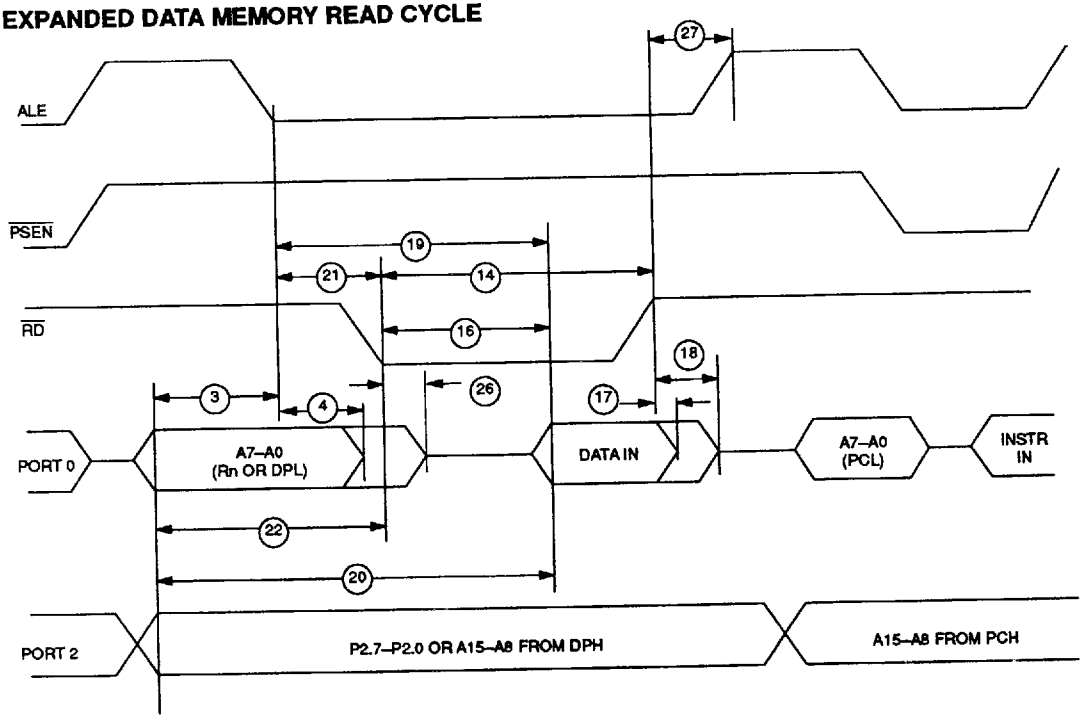
($t_A$ = 0°C to70°C; $V_{CC}$ = 5V ± 10%)

| # | PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| 1 | Oscillator Frequency | $1/t_{CLK}$ | 1.0 | 12 (-12)<br>16 (-16) | MHz |
| 2 | ALE Pulse Width | $t_{ALPW}$ | $2t_{CLK}$-40 | | ns |
| 3 | Address Valid to ALE Low | $t_{AVALL}$ | $t_{CLK}$-40 | | ns |
| 4 | Address Hold After ALE Low | $t_{AVAAV}$ | $t_{CLK}$-35 | | ns |
| 5 | ALE Low to Valid Instr. In @12 MHz<br>@16 MHz | $t_{ALLVI}$ | | $4t_{CLK}$-150<br>$4t_{CLK}$-90 | ns |
| 6 | ALE Low to $\overline{PSEN}$ Low | $t_{ALLPSL}$ | $t_{CLK}$-25 | | ns |
| 7 | $\overline{PSEN}$ Pulse Width | $t_{PSPW}$ | $3t_{CLK}$-35 | | ns |
| 8 | $\overline{PSEN}$ Low to Valid Instr. In @12 MHz<br>@16 MHz | $t_{PSLVI}$ | | $3t_{CLK}$-150<br>$3t_{CLK}$-90 | ns<br>ns |
| 9 | Input Instr. Hold after $\overline{PSEN}$ Going High | $t_{PSIV}$ | 0 | | ns |
| 10 | Input Instr. Float after $\overline{PSEN}$ Going High | $t_{PSIX}$ | | $t_{CLK}$-20 | ns |
| 11 | Address Hold after $\overline{PSEN}$ Going High | $t_{PSAV}$ | $t_{CLK}$-8 | | ns |
| 12 | Address Valid to Valid Instr. In @12 MHz<br>@16 MHz | $t_{AVVI}$ | | $5t_{CLK}$-150<br>$5t_{CLK}$-90 | ns<br>ns |
| 13 | $\overline{PSEN}$ Low to Address Float | $t_{PSLAZ}$ | 0 | | ns |
| 14 | $\overline{RD}$ Pulse Width | $t_{RDPW}$ | $6t_{CLK}$-100 | | ns |
| 15 | $\overline{WR}$ Pulse Width | $t_{WRPW}$ | $6t_{CLK}$-100 | | ns |
| 16 | $\overline{RD}$ Low to Valid Data In @12 MHz<br>@16 MHz | $t_{RDLDV}$ | | $5t_{CLK}$-165<br>$5t_{CLK}$-105 | ns<br>ns |
| 17 | Data Hold after $\overline{RD}$ High | $t_{RDHDV}$ | 0 | | ns |
| 18 | Data Float after $\overline{RD}$ High | $t_{RDHDZ}$ | | $2t_{CLK}$-70 | ns |
| 19 | ALE Low to Valid Data In @12 MHz<br>@16 MHz | $t_{ALLVD}$ | | $8t_{CLK}$-150<br>$8t_{CLK}$-90 | ns<br>ns |
| 20 | Valid Addr. to Valid Data In @12 MHz<br>@16 MHz | $t_{AVDV}$ | | $9t_{CLK}$-165<br>$9t_{CLK}$-105 | ns<br>ns |
| 21 | ALE Low to $\overline{RD}$ or $\overline{WR}$ Low | $t_{ALLRDL}$ | $3t_{CLK}$-50 | $3t_{CLK}$+50 | ns |
| 22 | Address Valid to $\overline{RD}$ or $\overline{WR}$ Low | $t_{AVRDL}$ | $4t_{CLK}$-130 | | ns |
| 23 | Data Valid to $\overline{WR}$ Going Low | $t_{DVWRL}$ | $t_{CLK}$-60 | | ns |
| 24 | Data Valid to $\overline{WR}$ High @12 MHz<br>@16 MHz | $t_{DVWRH}$ | $7t_{CLK}$-150<br>$7t_{CLK}$-90 | | ns<br>ns |
| 25 | Data Valid after $\overline{WR}$ High | $t_{WRHDV}$ | $t_{CLK}$-50 | | ns |
| 26 | $\overline{RD}$ Low to Address Float | $t_{RDLAZ}$ | | 0 | ns |
| 27 | $\overline{RD}$ or $\overline{WR}$ High to ALE High | $t_{RDHALH}$ | $t_{CLK}$-40 | $t_{CLK}$+50 | ns |

## EXPANDED PROGRAM MEMORY READ CYCLE




## EXPANDED DATA MEMORY READ CYCLE

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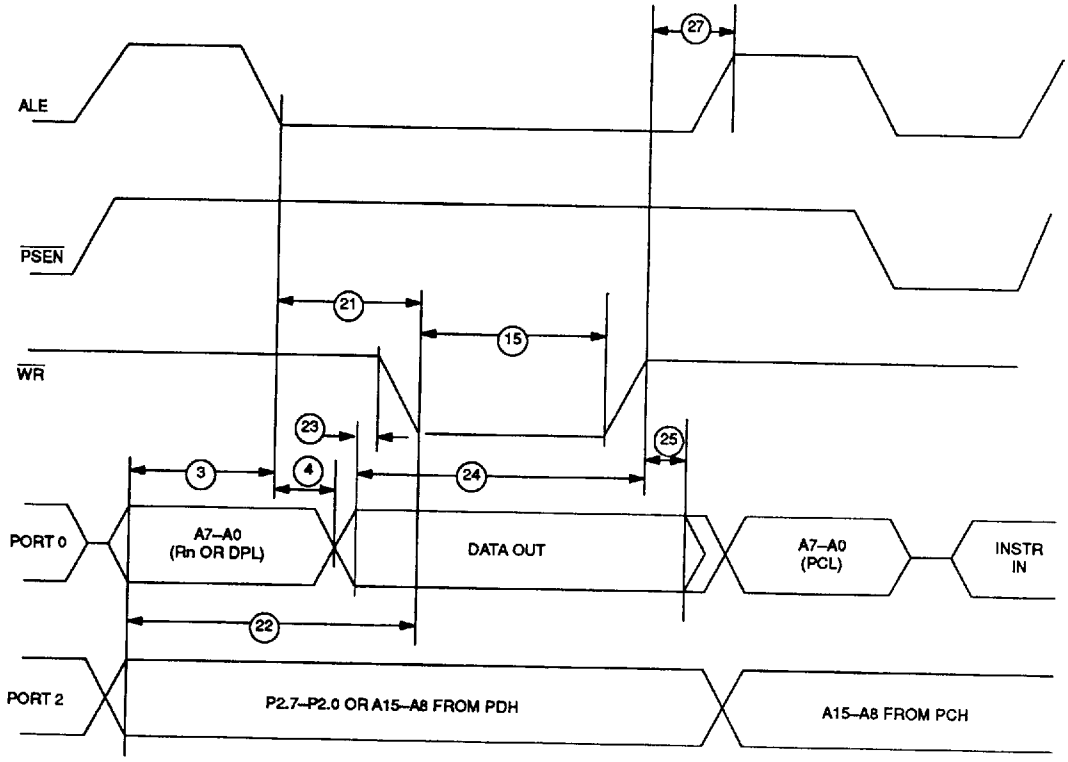
## EXPANDED DATA MEMORY WRITE CYCLE

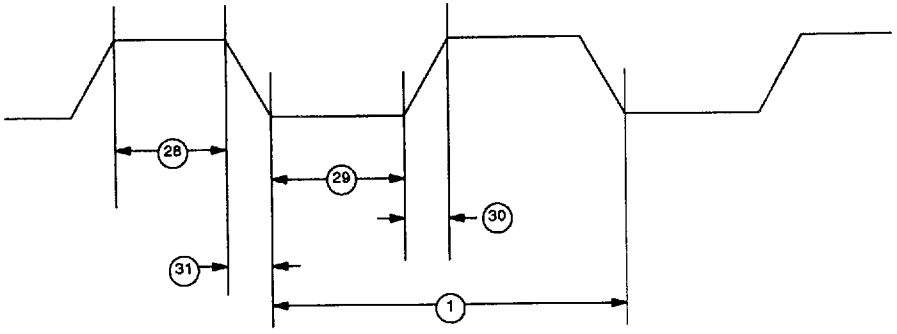



## AC CHARACTERISTICS (cont'd)
## EXTERNAL CLOCK DRIVE

($t_A$ = 0°C to70°C; $V_{CC}$ = 5V ± 10%)

| # | PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| 28 | External Clock High Time @12 MHz<br>@16 MHz | $t_{CLKHPW}$ | 20<br>15 | | ns<br>ns |
| 29 | External Clock Low Time @12 MHz<br>@16 MHz | $t_{CLKLPW}$ | 20<br>15 | | ns<br>ns |
| 30 | External Clock Rise Time @12 MHz<br>@16 MHz | $t_{CLKR}$ | | 20<br>15 | ns<br>ns |
| 31 | External Clock Fall Time @12 MHz<br>@16 MHz | $t_{CLKF}$ | | 20<br>15 | ns<br>ns |

## EXTERNAL CLOCK TIMING

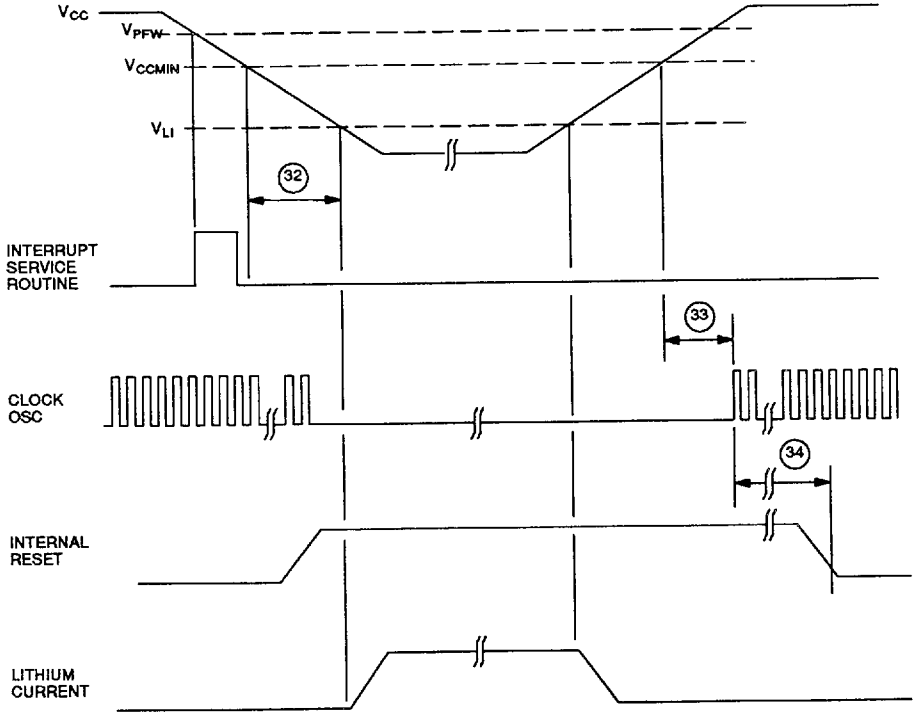



## AC CHARACTERISTICS (cont'd)
## POWER CYCLING TIMING

($t_A$ = 0°C to70°C; $V_{CC}$ = 5V ± 10%)

| # | PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| 32 | Slew Rate from $V_{CCMIN}$ to $V_{LI}$ | $t_F$ | 130 | | µs |
| 33 | Crystal Start up Time | $t_{CSU}$ | | (note 6) | |
| 34 | Power On Reset Delay | $t_{POR}$ | | 21504 | $t_{CLK}$ |

## POWER CYCLE TIMING



## AC CHARACTERISTICS (cont'd)

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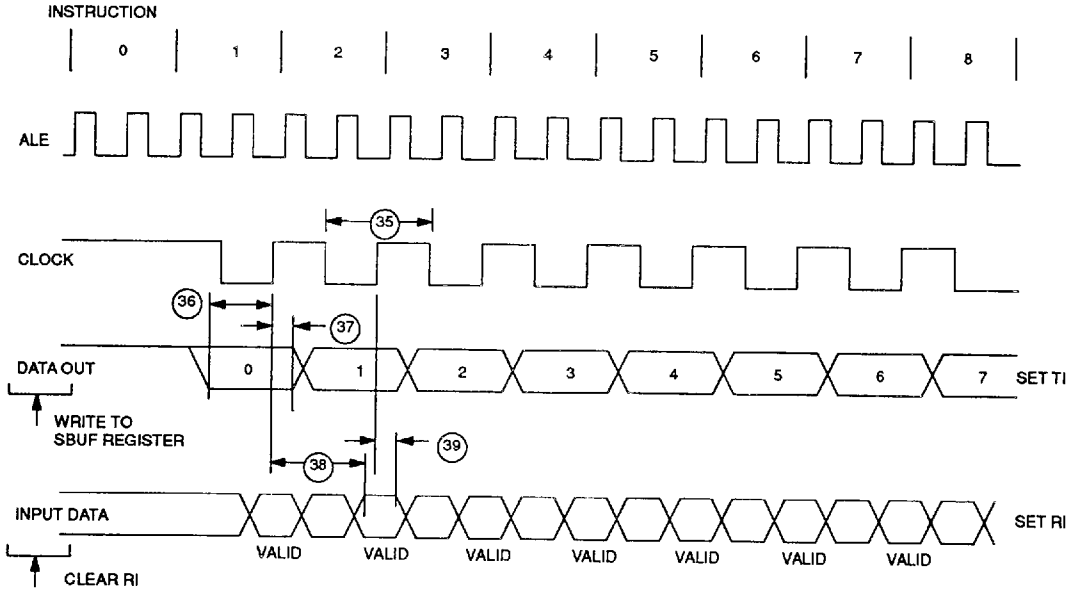
### SERIAL PORT TIMING – MODE 0

($t_A$ = 0°C to70°C; $V_{CC}$ = 5V ± 10%)

| # | PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| 35 | Serial Port Clock Cycle Time | $t_{SPCLK}$ | $12t_{CLK}$ | | µs |
| 36 | Output Data Setup to Rising Clock Edge | $t_{DOCH}$ | $10t_{CLK}$-133 | | ns |
| 37 | Output Data Hold after Rising Clock Edge | $t_{CHDO}$ | $2t_{CLK}$-117 | | ns |
| 38 | Clock Rising Edge to Input Data Valid | $t_{CHDV}$ | | $10t_{CLK}$-133 | ns |
| 39 | Input Data Hold after Rising Clock Edge | $t_{CHDIV}$ | 0 | | ns |

### SERIAL PORT TIMING – MODE 0



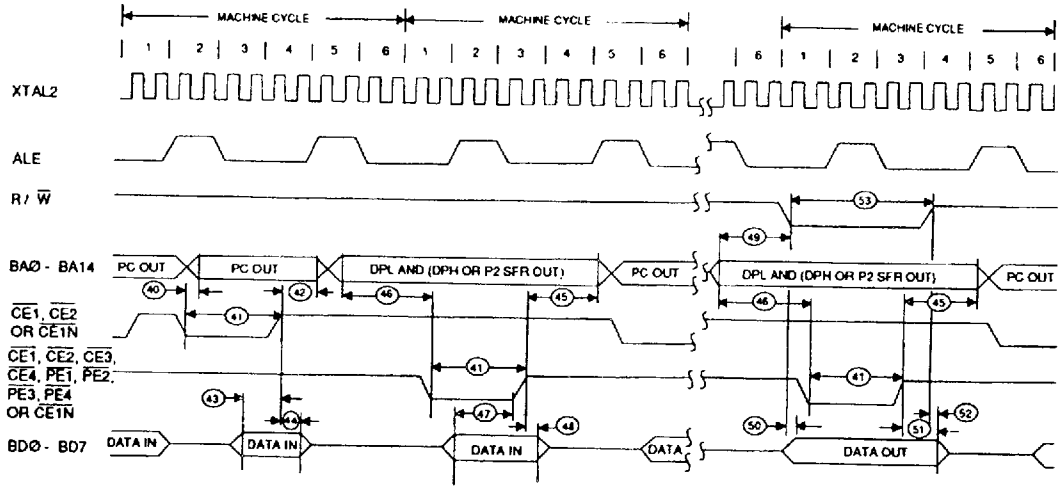
**AC CHARACTERISTICS** (cont'd)
**PARALLEL PROGRAM LOAD TIMING**

($t_A$ = 0°C to70°C; $V_{CC}$ = 5V ± 10%)

| # | PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| 40 | Delay to Byte–wide Address Valid from $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ Low During Opcode Fetch | $t_{CE1LPA}$ | | 30 | ns |
| 41 | Pulse Width of $\overline{CE1}$–4, $\overline{PE1}$–4 or $\overline{CE1N}$ | $t_{CEPW}$ | $4t_{CLK}$–35 | | ns |
| 42 | Byte–wide Address Hold after $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ High During Opcode Fetch | $t_{CE1HPA}$ | $2t_{CLK}$–20 | | ns |
| 43 | Byte–wide Data Setup to $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ High During Opcode Fetch | $t_{OVCE1H}$ | $1t_{CLK}$+40 | | ns |
| 44 | Byte–wide Data Hold after $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ High During Opcode Fetch | $t_{CE1HOV}$ | 10 | | ns |
| 45 | Byte–wide Address Hold after $\overline{CE1}$–4, $\overline{PE1}$–4, or $\overline{CE1N}$ High During MOVX | $t_{CEHDA}$ | $4t_{CLK}$–30 | | ns |
| 46 | Delay from Byte–wide Address Valid $\overline{CE1}$–4, $\overline{PE1}$–4, or $\overline{CE1N}$ Low During MOVX | $t_{CELDA}$ | $4t_{CLK}$–35 | | ns |
| 47 | Byte–wide Data Setup to $\overline{CE1}$–4, $\overline{PE1}$–4, or $\overline{CE1N}$ High During MOVX (read) | $t_{DACEH}$ | $1t_{CLK}$+40 | | ns |
| 48 | Byte–wide Data Hold after $\overline{CE1}$–4, $\overline{PE1}$–4, or $\overline{CE1N}$ High During MOVX (read) | $t_{CEHDV}$ | 10 | | ns |
| 49 | Byte–wide Address Valid to R/$\overline{W}$ Active During MOVX (write) | $t_{AVRWL}$ | $3t_{CLK}$–35 | | ns |
| 50 | Delay from R/$\overline{W}$ Low to Valid Data Out During MOVX (write) | $t_{RWLDV}$ | 20 | | ns |
| 51 | Valid Data Out Hold Time from $\overline{CE1}$–4, $\overline{PE1}$–4, or $\overline{CE1N}$ High | $t_{CEHDV}$ | $1t_{CLK}$–15 | | ns |
| 52 | Valid Data Out Hold Time from R/$\overline{W}$ High | $t_{RWHDV}$ | 0 | | ns |
| 53 | Write Pulse Width (R/$\overline{W}$ Low Time) | $t_{RWLPW}$ | $6t_{CLK}$–20 | | ns |

## BYTE-WIDE BUS TIMING






## RPC AC CHARACTERISTICS – DBB READ

($t_A$ = 0°C to70°C; $V_{CC}$ = 5V ± 10%)

| # | PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| 54 | $\overline{CS}$, $A_0$ Setup to $\overline{RD}$ | $t_{AR}$ | 0 | | ns |
| 55 | $\overline{CS}$, $A_0$ Hold After $\overline{RD}$ | $t_{RA}$ | 0 | | ns |
| 56 | $\overline{RD}$ Pulse Width | $t_{RR}$ | 160 | | ns |
| 57 | $\overline{CS}$, $A_0$ to Data Out Delay | $t_{AD}$ | | 130 | ns |
| 58 | $\overline{RD}$ to Data Out Delay | $t_{RD}$ | 0 | 130 | ns |
| 59 | $\overline{RD}$ to Data Float Delay | $t_{RDZ}$ | | 85 | ns |

## RPC AC CHARACTERISTICS – DBB WRITE

($t_A$ = 0°C to70°C; $V_{CC}$ = 5V ± 10%)

| # | PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| 60 | $\overline{CS}$, $A_0$ Setup to $\overline{WR}$ | $t_{AW}$ | 0 | | ns |
| 61A | $\overline{CS}$, Hold After $\overline{WR}$ | $t_{WA}$ | 0 | | ns |
| 61B | $A_0$, Hold After $\overline{WR}$ | $t_{WA}$ | 20 | | ns |
| 62 | $\overline{WR}$ Pulse Width | $t_{WW}$ | 20 | | ns |
| 63 | Data Setup to $\overline{WR}$ | $t_{DW}$ | 130 | | ns |
| 64 | Data Hold After $\overline{WR}$ | $t_{WD}$ | 20 | | ns |

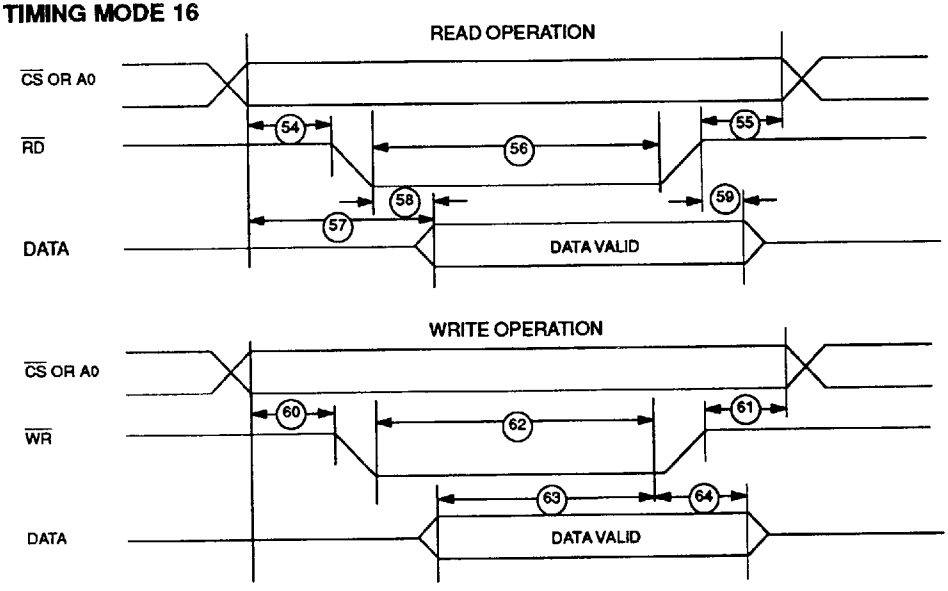
## AC CHARACTERISTICS – DMA

($t_A$ = 0°C to70°C; $V_{CC}$ = 5V ± 10%)

| # | PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| 65 | $\overline{DACK}$ to $\overline{WR}$ or $\overline{RD}$ | $t_{ACC}$ | 0 | | ns |
| 66 | $\overline{RD}$ or $\overline{WR}$ to $\overline{DACK}$ | $t_{CAC}$ | 0 | | ns |
| 67 | $\overline{DACK}$ to Data Valid | $t_{ACD}$ | 0 | 130 | ns |
| 68 | $\overline{RD}$ or $\overline{WR}$ to DRQ Cleared | $t_{CRQ}$ | | 110 | ns |



## RPC TIMING MODE 16

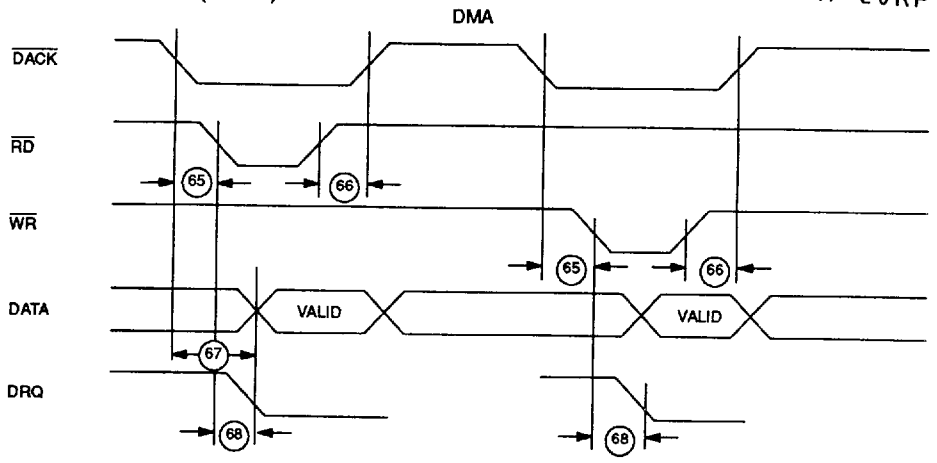



## AC CHARACTERISTICS – $\overline{PROG}$

($t_A$ = 0°C to70°C; $V_{CC}$ = 5V ± 10%)

| # | PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| 69 | $\overline{PROG}$ Low to Active | $t_{PRA}$ | 48 | | CLKS |
| 70 | $\overline{PROG}$ High to Inactive | $t_{PRI}$ | 48 | | CLKS |

**RPC TIMING MODE 16** (cont'd)

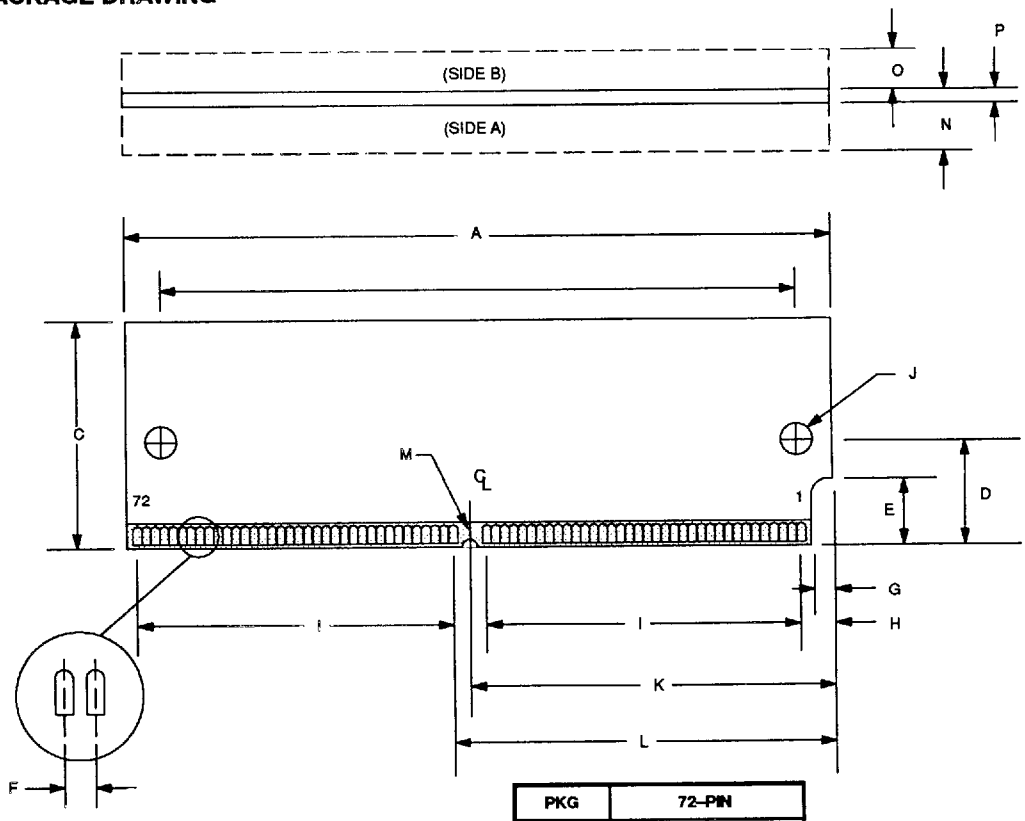



## NOTES:

1. All voltages are referenced to ground.
2. Maximum operating $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $t_{CLKR}$, $t_{CLKF}$=10 ns, $V_{IL}$ = 0.5V; XTAL2 disconnected; RST = PORT0 = $V_{CC}$.
3. Idle mode $I_{IDLE}$ is measured with all output pins disconnected; XTAL1 driven with $t_{CLKR}$, $t_{CLKF}$ = 10 ns, $V_{IL}$ = 0.5V; XTAL2 disconnected; PORT0 = $V_{CC}$, RST = $V_{SS}$.
4. Stop mode $I_{STOP}$ is measured with all output pins disconnected; PORT0 = $V_{CC}$; XTAL2 not connected; RST = XTAL1 = $V_{SS}$.
5. Pin capacitance is measured with a test frequency – 1 MHz, $t_A$ = 25°C.
6. Crystal start–up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on–chip oscillator. The user should check with the crystal vendor for a worst case specification on this time.

DALLAS SEMICONDUCTOR CORP

## PACKAGE DRAWING




| PKG | 72-PIN | |
|---|---|---|
| DIM | MIN | MAX |
| A | 4.245 | 4.255 |
| B | 3.979 | 3.989 |
| C | 0.995 | 1.005 |
| D | 0.395 | 0.405 |
| E | 0.245 | 0.255 |
| F | 0.050 BSC | |
| G | 0.075 | 0.085 |
| H | 0.245 | 0.255 |
| I | 1.750 BSC | |
| J | 0.120 | 0.130 |
| K | 2.120 | 2.130 |
| L | 2.245 | 2.255 |
| M | 0.057 | 0.067 |
| N | | 0.275 |
| O | | 0.145 |
| P | | 0.054 |