**DALLAS SEMICONDUCTOR**

# DS2264/DS2268 ADPCM Stik

T-75-11-37

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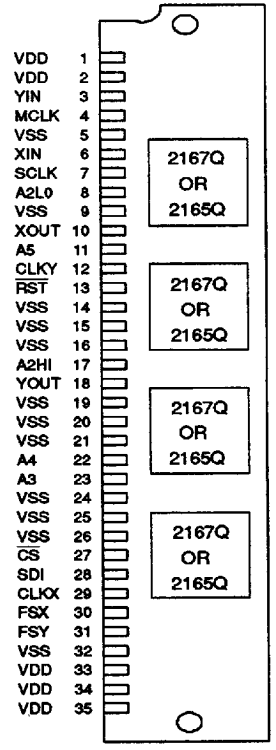
## FEATURES

- Provides four channels (DS2264) or eight channels (DS2268) of parallel full-duplex ADPCM processing in a pre-fabricated, snap-in module
- Based on the DS2167Q or DS2165Q ADPCM Processor Chip which implements the T1.301 and CCITT G.721 recommendations
- Occupies only 2 square inches of board space
- Conforms to popular JEDEC standard 35 position single in-line connector
- Easily cascadable up to 64 full-duplex channels in multiples of four or eight
- Both A-law and μ-law compatible
- Utilizes serial interface port for microprocessor control of timeslot assignments
- Includes onboard buffers for all critical signals

## ORDERING INFORMATION

| | |
|---|---|
| 4 channels with DS2167Q | DS2264 |
| 8 channels with DS2167Q | DS2268 |
| 4 channels with DS2165Q | DS2264 – EXP |
| 8 channels with DS2165Q | DS2268 – EXP |

## PIN ASSIGNMENT

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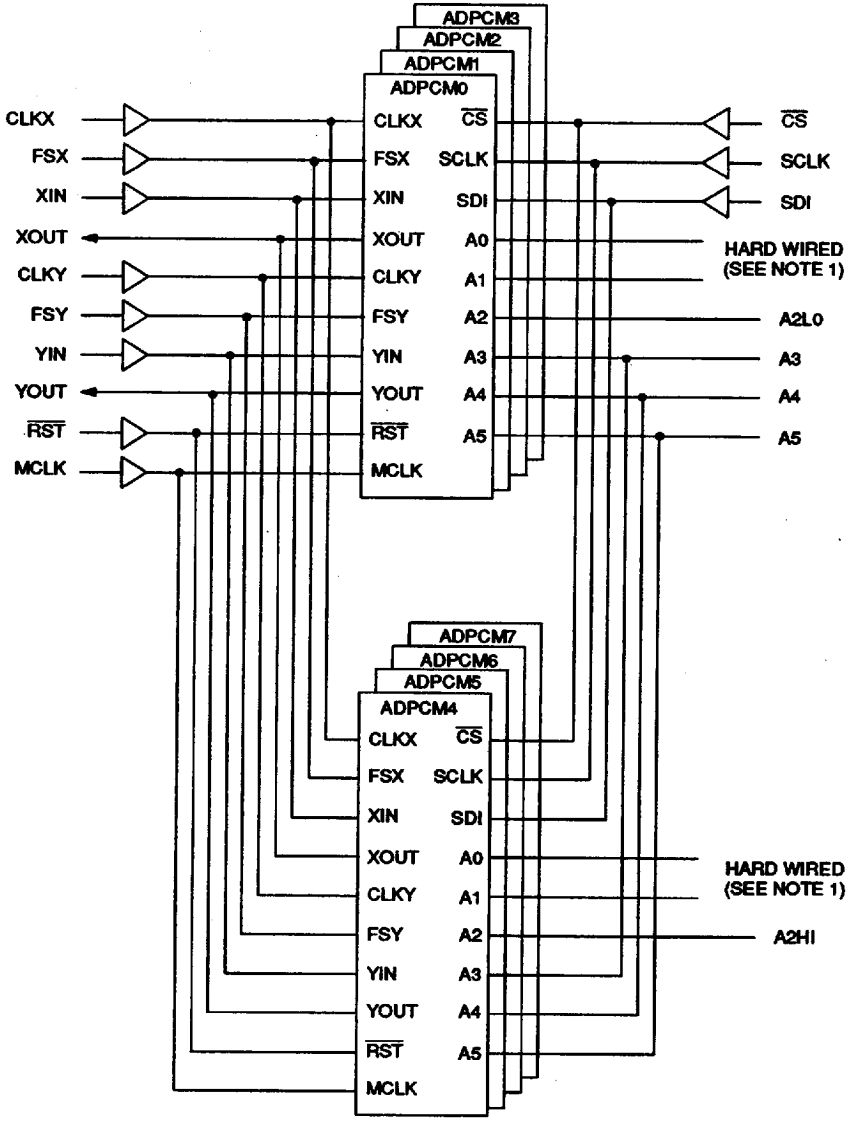
## DESCRIPTION

The DS2264 and DS2268 ADPCM Stiks are complete, pre-fabricated cards that perform either four or eight channels of full-duplex ADPCM processing. The ADPCM algorithm compresses 64Kbps voice data to either 32Kbps, 24Kbps, or 16Kbps. The DS2264 is only populated on one side and offers four channels while the DS2268 is populated on both sides of the Stik and offers eight channels. Control of the Stiks is handled by an external microcontroller via a serial port. Both Stiks are based on the DS2167Q or DS2165Q ADPCM Processor Chips. Specific details on the DS2167Q and DS2165Q can be found in their respective data sheets.

**DS2264/DS2268 BLOCK DIAGRAM** Figure 1




**NOTES:**

1. Pins A0 and A1 are configured as follows:

| Processor | A1 | A0 |
|---|---|---|
| 0 and 4 | 0 | 0 |
| 1 and 5 | 0 | 1 |
| 2 and 6 | 1 | 0 |
| 3 and 7 | 1 | 1 |

2. For the DS2264, processors 4 to 7 are not included and signal A2HI should be left open.

**PIN DESCRIPTION** Table 1

| PIN | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| 1<br>2 | $V_{DD}$ | – | **Positive Supply.** 5.0 volts. |
| 3 | YIN | I | **Y Data In.** Sampled on falling edge of CLKY during selected time slots. |
| 4 | MCLK | I | **Master Clock.** 10 MHz clock for the ADPCM processing engine; may be asynchronous to SCLK, CLKX, and CLKY. |
| 5 | $V_{SS}$ | – | **Signal Ground.** 0.0 volts. |
| 6 | XIN | I | **X Data In.** Sampled on falling edge of CLKX during selected time slots. |
| 7 | SCLK | I | **Serial Data Clock.** Used to write to the serial port. |
| 8 | A2LO | I | **Address Bit 2.** Defines address selection for the lower four channels. May be tied either high or low on the DS2264. Must be tied low on the DS2268. |
| 9 | VSS | – | **Signal Ground.** 0.0 volts. |
| 10 | XOUT | O | **X Data Output.** Updated on rising edge of CLKX during selected time slots. |
| 11 | A5 | I | **Address Bit 5.** Defines value for address bit 5. |
| 12 | CLKY | I | **Y Data Clock.** Data clock for the Y side PCM interface; must be synchronous with FSY. |
| 13 | $\overline{RST}$ | I | **Reset.** Active low. A high-low-high transition clears all internal registers, resets the algorithms, and idles the outputs of all the channels. |
| 14<br>15<br>16 | $V_{SS}$ | – | **Signal Ground.** 0.0 volts. |
| 17 | A2HI | I | **Address Bit 2.** Defines address selection for upper four channels. Must be left open on the DS2264 and tied high on the DS2268. |
| 18 | YOUT | O | **Y Data Output.** Updated on rising edge of CLKY during selected time slots. |
| 19<br>20<br>21 | $V_{SS}$ | – | **Signal Ground.** 0.0 volts. |
| 22 | A4 | I | **Address Bit 4.** Defines value for address bit 4. |
| 23 | A3 | I | **Address Bit 3.** Defines value for address bit 3. |
| 24<br>25<br>26 | $V_{SS}$ | – | **Signal Ground.** 0.0 volts. |
| 27 | $\overline{CS}$ | I | **Chip Select.** Active low. Serial port select; must be low to write to the serial port. |
| 28 | SDI | I | **Serial Data In.** Data for onboard control registers; sampled on the rising edge of SCLK. LSB sent first. |
| 29 | CLKX | I | **X Data Clock.** Data clock for the X side PCM interface; must be synchronous with FSX. |
| 30 | FSX | I | **X Frame Sync.** 8 KHz frame sync for the X side PCM interface. |
| 31 | FSY | I | **Y Frame Sync.** 8 KHz frame sync for the Y side PCM interface. |
| 32 | $V_{SS}$ | – | **Signal Ground.** 0.0 volts. |
| 33<br>34<br>35 | $V_{DD}$ | – | **Positive Supply.** 5.0 volts. |

## SYSTEM INTERFACE AND CONTROL

Both the DS2264 and DS2268 are designed to operate with an external microcontroller such as a DS5000 or an 8051/31. The microcontroller communicates to the APDCM Stiks over a 3-wire serial port consisting of $\overline{CS}$, SCLK, and SDI. Data that is written to serial port can be either two or four bytes long. A 4-byte write consists of the Address/Command byte, the Control byte, the Input Time Slot byte, and the Output Time Slot byte. A 2-byte write only contains the Address/Command byte and the Control byte. Within the Address/Command byte, there is an address field. Each ADPCM processor on the Stik monitors the serial port and looks for a match between its address (set by the configuration of the A0 to A5 pins) and the address specified in the Address/Command byte. If a match occurs, then either the next one or three bytes are accepted as configuration data. Complete details on the operation of the serial port can be found in the DS2167 and DS2165 data sheets. Details on the four configuration registers are shown in Figures 2 through 5.

### ADDRESS/COMMAND BYTE Figure 2

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| – | X/Y | A5 | A4 | A3 | A2 | A1 | A0 |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| – | ACB.7 | Reserved; must be 0 for proper operation. |
| X/Y | ACB.6 | **X/Y Channel Select.**<br>0 = update channel Y characteristics<br>1 = update channel X characteristics |
| A5 | ACB.5 | MSB of Device Address. |
| A4 | ACB.4 | |
| A3 | ACB.3 | |
| A2 | ACB.2 | |
| A1 | ACB.1 | |
| A0 | ACB.0 | LSB of Device Address. |

**CONTROL REGISTER** Figure 3

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| AS0 | AS1 | IPD | ALRST | BYP | U/A | AS2 | CP/EX |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| AS0 | CR.7 | Algorithm Select 0. See table below. |
| AS1 | CR.6 | Algorithm Select 1. See table below. |
| IPD | CR.5 | **Idle and Power Down.**<br>0 = channel enabled<br>1 = channel disabled (output 3-stated) |
| ALRST | CR.4 | **Algorithm Reset.**<br>0 = normal operation<br>1 = reset algorithm for selected channel |
| BYP | CR.3 | **Bypass.**<br>0 = normal operation<br>1 = bypass selected channel |
| U/A | CR.2 | **Data Format.**<br>0 = A-law<br>1 = μ-law |
| AS2 | CR.1 | Algorithm Select 2. See table below. |
| CP/EX | CR.0 | **Channel Coding.**<br>0 = expand (decode) selected channel<br>1 = compress (encode) selected channel |

| ALGORITHM SELECTED | AS2 | AS1 | AS0 |
|---|---|---|---|
| 64Kbps to/from 32Kbps | 0 | 0 | 0 |
| 64Kbps to/from 24Kbps | 1 | 1 | 1 |
| 64Kbps to/from 16Kbps | 1 | 0 | 1 |

**INPUT TIME SLOT REGISTER** Figure 4

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| – | – | D5 | D4 | D3 | D2 | D1 | D0 |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| – | ITR.7 | Reserved; must be 0 for proper operation. |
| – | ITR.6 | Reserved; must be 0 for proper operation. |
| D5 | ITR.5 | MSB of input time slot register. |
| D4 | ITR.4 | |
| D3 | ITR.3 | |
| D2 | ITR.2 | |
| D1 | ITR.1 | |
| D0 | ITR.0 | LSB of input time slot register. |

**OUTPUT TIME SLOT REGISTER** Figure 5

| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| – | – | D5 | D4 | D3 | D2 | D1 | D0 |

| SYMBOL | POSITION | NAME AND DESCRIPTION |
|---|---|---|
| – | OTR.7 | Reserved; must be 0 for proper operation. |
| – | OTR.6 | Reserved; must be 0 for proper operation. |
| D5 | OTR.5 | MSB of output time slot register. |
| D4 | OTR.4 | |
| D3 | OTR.3 | |
| D2 | OTR.2 | |
| D1 | OTR.1 | |
| D0 | OTR.0 | LSB of output time slot register. |

## DATA BUSSING

The DS2264 and DS2268 can be cascaded to process up to 64 full-duplex ADPCM channels. For example, eight DS2268s can be combined in parallel to achieve 64 channels. All of the common PCM interface signals (CLKX, FSX, XIN, XOUT, CLKY, FSY, YIN, YOUT) should be tied together. Also, the serial interface signals (SCLK, $\overline{CS}$, SDI) should be tied together. Every processor will be assigned a unique address via the A0 to A5 pins on the processor. Address pins A0 and A1 are already assigned for each ADPCM processor; the user selects A2 through A5. The address range for the processors on a single module is defined by the strapping of the A5, A4, A3, A2LO, and A2HI address control pins.

Each DS2264 occupies four consecutive address locations. The exact placement of this 4-address block is defined by the user via the address control pins. (See Table 2.) On the DS2264, the A2HI pin should be left open. Each DS2268 occupies eight consecutive address locations. (See Table 3.) On the DS2268, the A2HI pin should be tied to $V_{DD}$ and the A2LO pin should be tied to $V_{SS}$. If the address control pins are tied so that each module in the stack has a unique range of addresses, then an external microcontroller will be able to select any processor in the group and configure it appropriately.

**DS2264 ADDRESS STRAPPING** Table 2

| | | | 4-Block Address Selected | |
|---|---|---|---|---|
| A5 | A4 | A3 | A2LO = 0 | A2LO = 1 |
| 0 | 0 | 0 | 0 through 3 | 4 through 7 |
| 0 | 0 | 1 | 8 through 11 | 12 through 15 |
| 0 | 1 | 0 | 16 through 19 | 20 through 23 |
| 0 | 1 | 1 | 24 through 27 | 28 through 31 |
| 1 | 0 | 0 | 32 through 35 | 36 through 39 |
| 1 | 0 | 1 | 40 through 43 | 44 through 47 |
| 1 | 1 | 0 | 48 through 51 | 52 through 55 |
| 1 | 1 | 1 | 56 through 59 | 60 through 63 |

**DS2268 ADDRESS STRAPPING** Table 3

| A5 | A4 | A3 | 8-Block Address Selected |
|---|---|---|---|
| 0 | 0 | 0 | 0 through 7 |
| 0 | 0 | 1 | 8 through 15 |
| 0 | 1 | 0 | 16 through 23 |
| 0 | 1 | 1 | 24 through 31 |
| 1 | 0 | 0 | 32 through 39 |
| 1 | 0 | 1 | 40 through 47 |
| 1 | 1 | 0 | 48 through 55 |
| 1 | 1 | 1 | 56 through 63 |



## SYSTEM RESET

A system reset may be initialized with a high-low-high transition on the $\overline{RST}$ pin. This action clears all of the internal registers, resets the ADPCM algorithms, and places the processors in idle (outputs 3-stated). On system power-up, the $\overline{RST}$ pin should be held low for at least 1 ms after the Master Clock (MCLK) has stabilized to assure proper initialization. Use of a DS1231 or DS1232 will automatically generate a reset when power is applied. Please see the Dallas Semiconductor Data Book for more information on the DS1231 and DS1232.

## STIK CONNECTORS

The DS2264 and DS2268 are designed to connect into a standard 35-pin SIMM connector with a pin spacing pitch of 0.100 inches. Both vertical and inclined connectors are available from connector vendors such as AMP and Molex. Table 4 lists two such connectors.

**35-PIN SIMM CONNECTORS FOR DS2264/DS2268** Table 4

| Description | Vendor | Part Number |
|---|---|---|
| Vertical upright | AMP | 821828-3 |
| Low profile, 25 degree angle | Molex | 15-46-0385 |

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on any Pin Relative to Ground | -1.0V to +7.0V |
| Operating Temperature | 0°C to 70°C |
| Storage Temperature | -55°C to +125°C |

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 | $V_{IH}$ | 2.0 | | $V_{CC}$+0.3 | V | |
| Logic 0 | $V_{IL}$ | -0.3 | | +0.8 | V | |
| Supply | $V_{DD}$ | 4.5 | | 5.5 | V | |

## CAPACITANCE

($t_A$=25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | | 20 | pF | |
| Output Capacitance | $C_{OUT}$ | | | 40<br>80 | pF<br>pF | 4<br>5 |

## DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; $V_{DD}$=5V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Operating Current | $I_{DDA}$ | | | 175<br>280 | mA<br>mA | 1,2,4<br>1,2,5 |
| Standby Current | $I_{DDPD}$ | | | 50<br>50 | mA<br>mA | 1,2,3,4<br>1,2,3,5 |
| Input Leakage | $I_I$ | -40.0 | | +40.0 | µA | |
| Output Leakage | $I_{IO}$ | -4.0<br>-8.0 | | +4.0<br>+8.0 | µA<br>µA | 4,6<br>5,6 |
| Output Current (2.4V) | $I_{OH}$ | -1.0 | | | mA | |
| Output Current (0.4V) | $I_{OL}$ | +4.0 | | | mA | |

## NOTES:

1. CLKX = CLKY = 1.544 MHz; MCLK = 10 MHz.
2. Outputs open; inputs swinging full supply levels.
3. All channels of all processors programmed to idle (IPD = 1).
4. For DS2264 only.
5. For DS2268 only.
6. XOUT and YOUT 3-stated.

## PCM INTERFACE AC ELECTRICAL CHARACTERISTICS

($0°C$ to $70°C$; $V_{DD}$=5V ±10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| CLKX, CLKY Period | $t_{PXY}$ | 244 | | 5208 | ns | 4 |
| CLKX, CLKY Pulse Width | $t_{WXYL}$ $t_{WXYH}$ | 100 | | | ns | |
| CLKX, CLKY Rise Fall Times | $t_{RXY}$ $t_{FXY}$ | | 10 | 20 | ns | |
| Hold Time from CLKX, CLKY to FSX, FSY | $t_{HOLD}$ | 0 | | | ns | 1 |
| Setup Time from FSX, FSY High to CLKX, CLKY Low | $t_{SF}$ | 50 | | | ns | 1 |
| Hold Time from CLKX, CLKY Low to FSX, FSY Low | $t_{HF}$ | 100 | | | ns | 1 |
| Setup Time for XIN, YIN to CLKX, CLKY Low | $t_{SD}$ | 50 | | | ns | 1 |
| Hold Time for XIN, YIN to CLKX, CLKY Low | $t_{HD}$ | 50 | | | ns | 1 |
| Delay Time from CLKX, CLKY to Valid XOUT, YOUT | $t_{DXYO}$ | 10 | | 150 | ns | 2 |
| Delay Time from CLKX, CLKY to XOUT, YOUT 3-stated | $t_{DXYZ}$ | | 150 | | ns | 1,2,3 |

**NOTES:**

1. Measured at $V_{IH}$ = 2.0V, $V_{IL}$ = 0.8V, and 10 ns maximum rise and fall times.
2. Load = 150 pF + 2 LSTTL loads.
3. For LSB of PCM or ADPCM byte.
4. Maximum width of FSX and FSY is one CLKX or CLKY period.

## MASTER CLOCK/RESET AC ELECTRICAL CHARACTERISTICS

($0°C$ to $70°C$; $V_{DD}$=5V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| MCLK Period | $t_{PM}$ | | 100 | | ns | 1 |
| MCLK Pulse Width | $t_{WMH}$ $t_{WML}$ | 45 | 50 | 55 | ns | |
| MCLK Rise/Fall Times | $t_{RM}$, $t_{FM}$ | | | 10 | ns | |
| $\overline{RST}$ Pulse Width | $t_{RST}$ | 1 | | | ms | |

**NOTE:**

1. MCLK = 10 MHz ± 500 ppm.

## SERIAL PORT AC ELECTRICAL CHARACTERISTICS

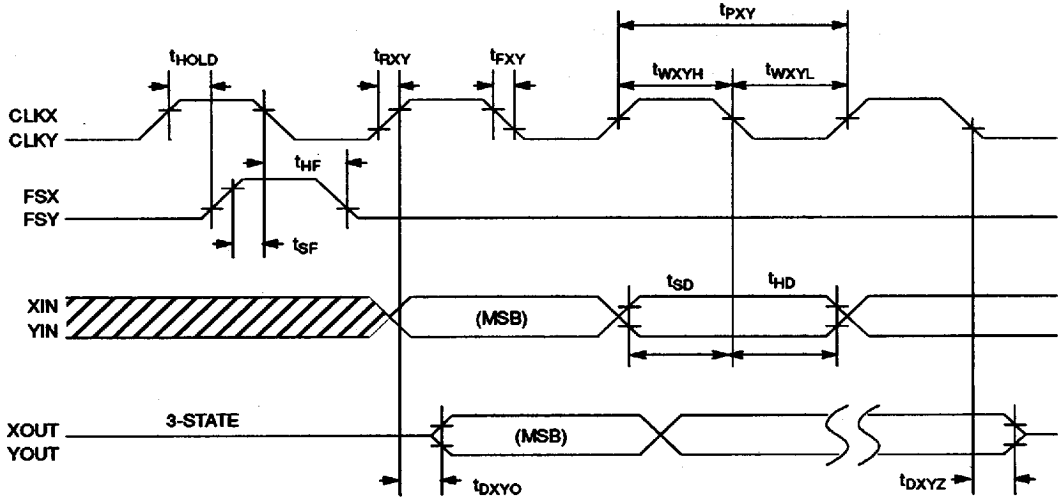
(0°C to 70°C; $V_{DD}$=5V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| SDI to SCLK Set Up | $t_{DC}$ | 55 | | | ns | 1 |
| SCLK to SDI Hold | $t_{CDH}$ | 55 | | | ns | 1 |
| SCLK Low Time | $t_{CL}$ | 250 | | | ns | 1 |
| SCLK High Time | $t_{CH}$ | 250 | | | ns | 1 |
| SCLK Rise and Fall Time | $t_R$, $t_F$ | | | 100 | ns | 1 |
| $\overline{CS}$ to SCLK Set Up | $t_{CC}$ | 50 | | | ns | 1 |
| SCLK to $\overline{CS}$ Hold | $t_{CCH}$ | 250 | | | ns | 1 |
| $\overline{CS}$ Inactive Time | $t_{CWH}$ | 250 | | | ns | 1 |
| SCLK Set Up to $\overline{CS}$ Falling | $t_{SCC}$ | 50 | | | ns | 1 |

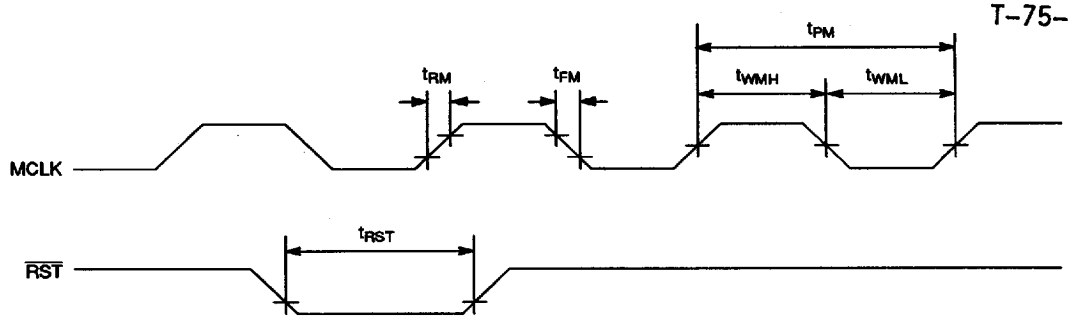
**NOTE:**

1. Measured at $V_{IH}$ = 2.0V, $V_{IL}$ = 0.8V, and 10ns maximum rise and fall times.

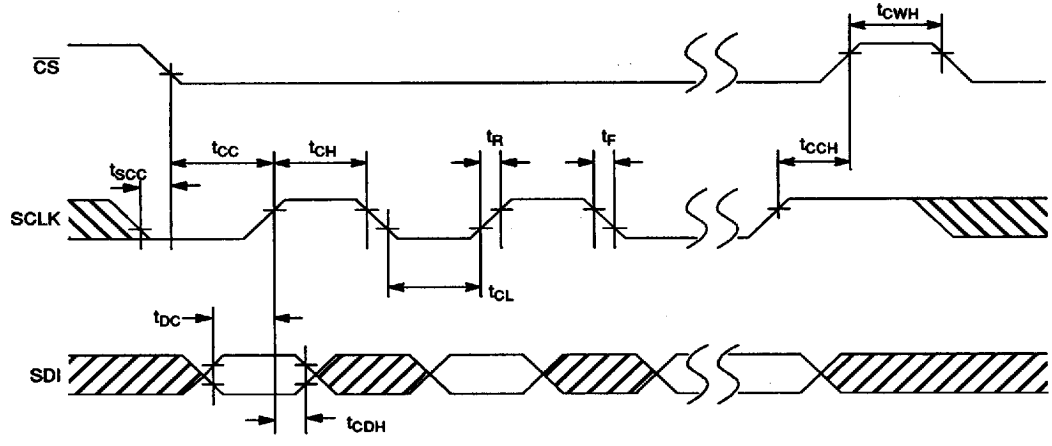
## PCM INTERFACE AC TIMING DIAGRAM Figure 6



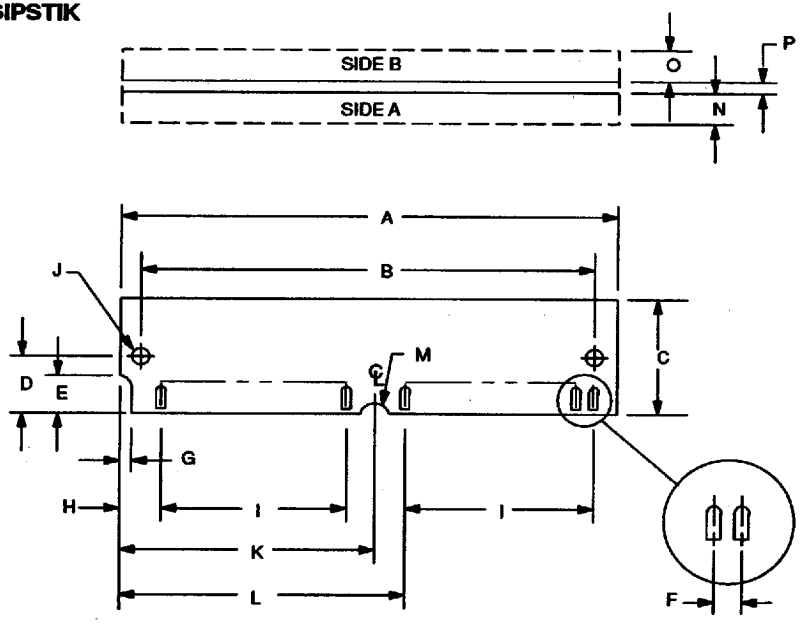
**MASTER CLOCK/RESET AC TIMING DIAGRAM** Figure 7




**SERIAL PORT AC TIMING DIAGRAM** Figure 8



## DS2264/DS2268 ADPCM STIK
## 35-PIN SIPSTIK




| PKG | 35-PIN | |
|---|---|---|
| DIM | MIN | MAX |
| A IN. | 3.995 | 4.005 |
| B IN. | 3.729 | 3.739 |
| C IN. | 0.795 | 0.805 |
| D IN. | 0.395 | 0.405 |
| E IN. | 0.245 | 0.255 |
| F IN. | 0.100 BSC | |
| G IN. | 0.075 | 0.085 |
| H IN. | 0.295 | 0.305 |
| I IN. | 2.900 BSC | |
| J IN. | 0.120 | 0.130 |
| K IN. | 0.000 | 0.000 |
| L IN. | 0.000 | 0.000 |
| M IN. | 0.000 | 0.000 |
| N IN. | | 0.230 |
| O IN. | | 0.230 |
| P IN. | | 0.054 |