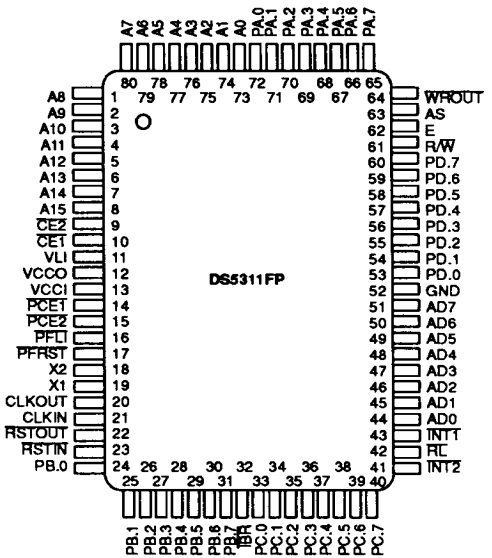
DALLAS SEMICONDUCTOR

DS5311FP
68HC11 Softener Chip

FEATURES

- Softens 68HC11-based systems
  - Converts up to 64K bytes of CMOS RAM into lithium-backed NV program/data storage
  - Serial bootstrap loading
  - In-system program changes adapt HC11 to task at hand
- Crashproof operation during transient conditions
  - NV storage for 10 years with no V_{CC}
  - Orderly shutdown/restart on power-up/down
  - Watchdog timer
  - CRC of memory on power-up
  - Call for Help via Modem
- Enhanced I/O
  - Provides four 8-bit parallel I/O ports to HC11
  - Dual port register file for Host bus interface
  - 4 decoded chip enables with write protection
  - Mates to HC11 Address/Data Bus

PACKAGE OUTLINE



DESCRIPTION

The DS5311FP 68HC11 Softener Chip is a member of the Softener family that is designed to provide the benefits of adaptability, crashproof operation, and enhanced parallel I/O capabilities, as discussed in the DS53xx Softener Family User's Guide, for systems based on the popular Motorola MC68HC11 microprocessor. The DS5311FP interfaces directly to the HC11's address/data bus and control signals, and converts up to 64K bytes of CMOS SRAM into nonvolatile read/write storage.

An embedded control system with the above attributes can be implemented using only the 68HC11, DS5311FP Softener Chip, CMOS static RAM, and a lithium cell. Additional peripheral functions, such as a permanently powered DS1283 Watchdog Timekeeper Chip, can be added to the system without the need for additional glue logic.

Also available from Dallas Semiconductor is the DS2311 Soft HC11 Stik, a complete implementation of the embedded control system described above. The Stik is implemented on a SIMM module that plugs into the industry-standard 72-pin SIMM connector scheme which supports redundant contacts, simple insertion/extraction, and low overall height profiles. The DS2311 can be used as a high-level building block in a system design, resulting in a quick time to market for a Softener-based HC11 system. Alternatively, it can be used for fast prototyping of a system that will ultimately incorporate the DS5311FP HC11 Softener Chip. The designer should consult the DS2311 data sheet for information on this application of the DS5311.

PIN DESCRIPTION

The table shown below summarizes the pin functions of the DS5311FP by function type.

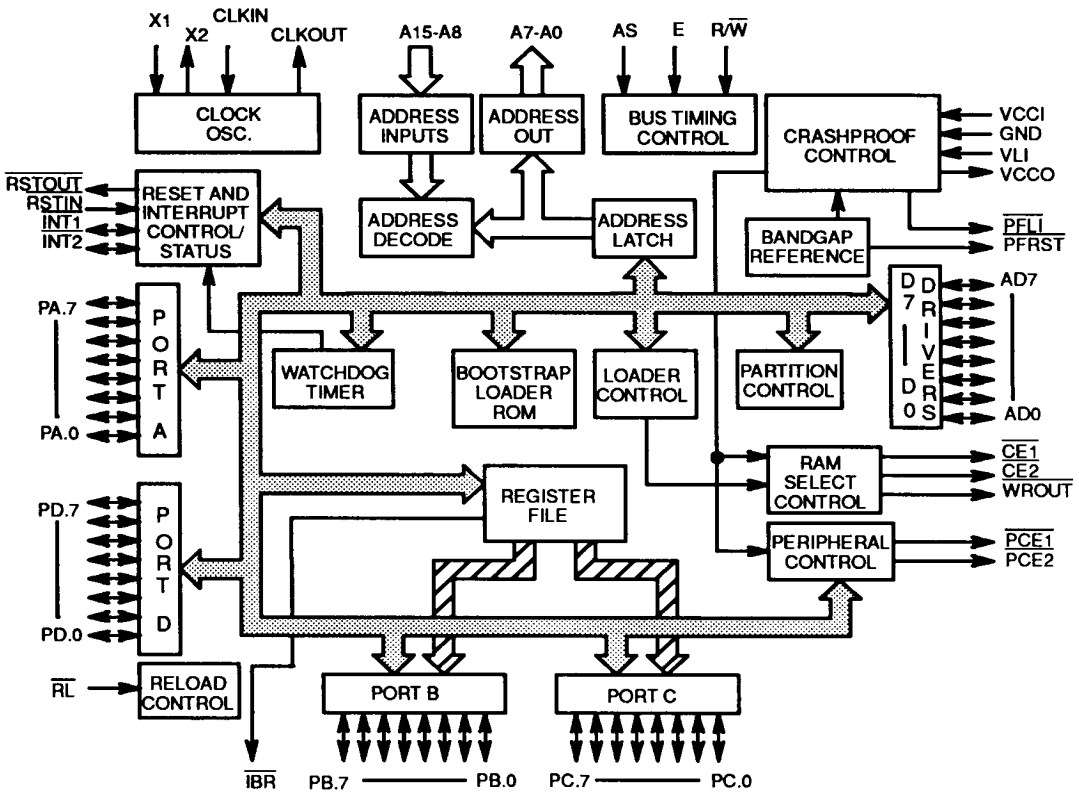
DS5311FP PIN DESCRIPTION Table 1

PIN	NAME	DESCRIPTION
13	VCCI	+5V Power Supply Input
52	GND	Ground
11	VLI	+3V Lithium Supply Input
12	VCCO	Lithium-Backed Power Supply Output
17	$\overline{\text{PFRST}}$	Power Fail Reset Threshold Output
16	$\overline{\text{PFLI}}$	Power Fail Lithium Threshold Output
19	X1	Crystal Oscillator Input
18	X2	Crystal Oscillator Output
42	$\overline{\text{RL}}$	Reload Input
21	CLKIN	Clock Monitor Input from HC11
20	CLKOUT	Clock Output to HC11
8 - 1	A15 - A8	Address Bus Inputs from HC11
80 - 73	A7 - A0	Demux Address Bus Outputs from DS5311
51 - 44	AD7 - AD0	Mux. Address/Data Bus to/from HC11; bidirectional
62	E	E-Clock Input from HC11
61	R/$\overline{\text{W}}$	Read/Write Input from HC11
63	AS	Address Strobe Input from HC11
10, 9	$\overline{\text{CE1}}$, $\overline{\text{CE2}}$	Chip Enable Outputs to RAM
14, 15	$\overline{\text{PCE1}}$, $\overline{\text{PCE2}}$	Peripheral Chip Enable Outputs
64	$\overline{\text{WROUT}}$	Write Output
23	$\overline{\text{RSTIN}}$	Reset Input
22	$\overline{\text{RSTOUT}}$	Reset Output to HC11
43	$\overline{\text{INT1}}$	Interrupt Input/Output 1 to HC11
41	$\overline{\text{INT2}}$	Interrupt Input/Output 2 to HC11
65 - 72	PA7 - PA0	Port A; Bidirectional
31 - 24	PB7 - PB0	Port B; Bidirectional
40 - 33	PC7 - PC0	Port C; Bidirectional
60 - 53	PD7 - PD0	Port D; Bidirectional
32	$\overline{\text{IBR}}$	Input Buffer Ready Status Output

BLOCK DIAGRAM

A conceptual block diagram of the DS5311FP is illustrated in Figure 1. The designer should consult the DS53xx Softener Family User's Guide for complete operational details which are common to all versions of the Softener. Features which are unique to the DS5311FP are described below:

DS5311FP SOFTENER BLOCK DIAGRAM Figure 1



MEMORY MAP

The DS5311FP interfaces directly to the Motorola MC68HC11's multiplexed address and data busses. All 16 address lines as well as the E and R/$\overline{W}$ control signals are monitored so that all external bus accesses performed by the processor are interpreted by the DS5311. The HC11 Softener decodes incoming addresses and controls access to its internal registers, to external CMOS SRAMs, and to external peripherals such as the DS1283 Watchdog Timekeeper Chip.

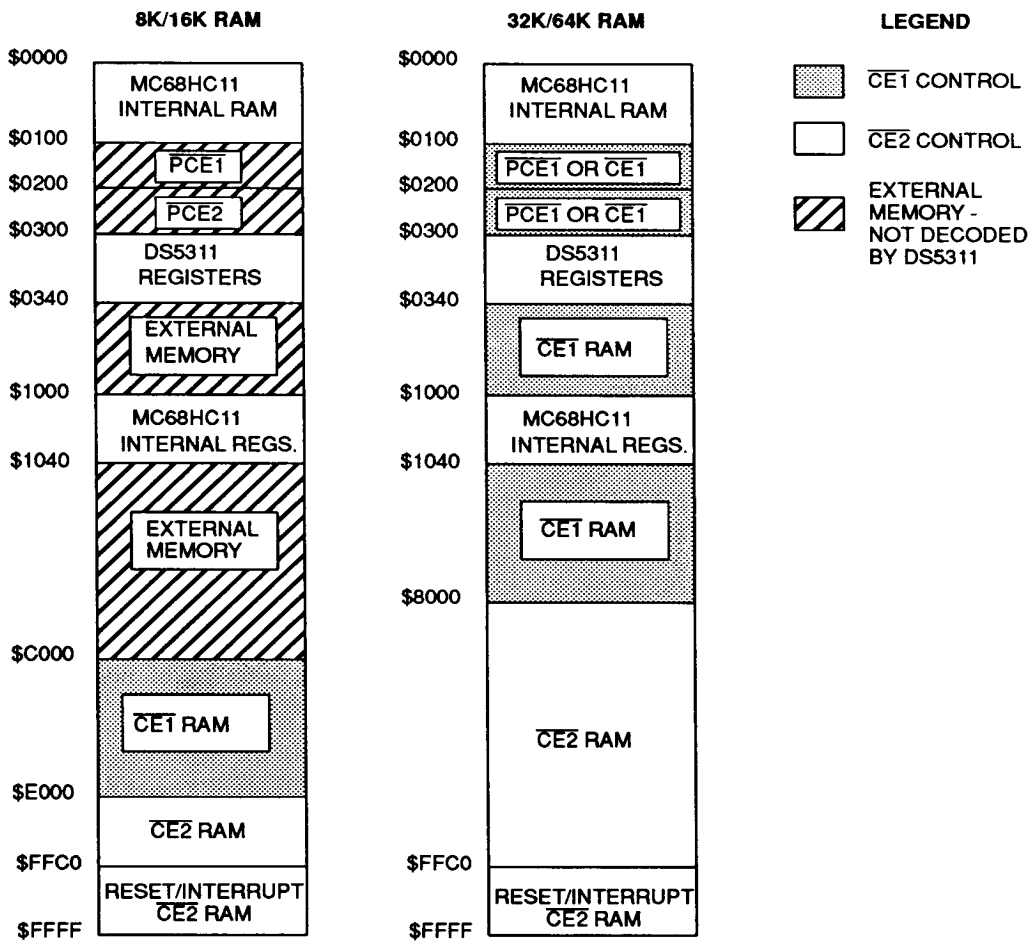
$\overline{CE1}$ and $\overline{CE2}$ are the chip enable signals used to control the external nonvolatile CMOS SRAMs. As illustrated in Figure 2, two different system memory maps can be selected by programming an internal Range Select bit during system initialization via the serial bootstrap loader. By programming this bit, the chip enable outputs can be assigned to each control either an 8K x 8 or a 32K x 8 CMOS static RAM. As a result, a minimum of 8K bytes up to a maximum of 64K bytes of nonvolatile storage is supported. This operating mode information is retained

in the absence of VCC. Programming of the Range Select bit is summarized in the "Register Summary" section of this data sheet.

The diagram shown in Figure 2 illustrates the resulting memory maps for a DS5311FP used with the MC68HC11A0 version. As shown in the figure, the MC68HC11A0 processor maps its internal registers in the region from $1000 - $103F and its internal RAM in the region from $0 to $FF. As a result, no accesses are performed on its external address and data busses when these internal locations are addressed, and the corresponding locations in NV SRAM under the control of $\overline{CE1}$ are not accessible when a 64K byte range is selected.

For accesses that are performed on the external bus, the DS5311FP performs the necessary decoding for its internal registers and the external NV SRAM and peripherals under its control. The DS5311FP registers are located in the 64-byte space from $300 to $33F. If a 32K byte SRAM is interfaced on the $\overline{CE1}$ signal, then the locations within that RAM which correspond to the register space will not be accessible from the processor. The DS5311FP can also be used with other versions of the 68HC11, with certain implications to the memory map.

DS5311FP MEMORY MAPS Figure 2



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The reset and interrupt vectors for the 68HC11 are stored in the region from $FFC0 - $FFFF. If a single SRAM (8K x 8 or 32K x 8) is used with the DS5311, then it should be interfaced on the $\overline{CE2}$ line in order to accommodate these vector locations.

The Softener MODE bits (MD2-0; MODES.4-2) serve no function on the DS5311. Setting or clearing these bits will have no effect on operation.

As described in the DS53xx Softener Family User's Guide, the $\overline{PCE1}$ and $\overline{PCE2}$ lines are available for the interface of peripheral devices. When enabled, each of these lines is used to access a 256-byte block of memory as shown for each of the two possible memory map modes shown in Figure 2.

MEMORY PARTITION

For the maximum amount of write protection of nonvolatile storage, the SRAM under the control of the DS5311FP can be partitioned into distinct areas which are accessible either as read-only or read/write by the application software. SRAM that is assigned by partitioning as a read-only area cannot be written directly by application software. Areas assigned as read/write storage can be written by the application software at any time.

Partitioning of the SRAM is controlled via the Softener's Partition Enable bit (PE; MODES.6), and the Softener's Partition Address bits (PA3-0; MCON.7-4). The PE bit can only be set or cleared via the bootstrap loader by using the Write MODES register command (W MO XX). Once PE is set, any SRAM from $0 to $FFF is always assigned as read/write storage by the application software. Write protection of the remainder of the SRAM is determined by the setting of PA3-0. PA3-0 may be written either through the bootstrap loader environment using the Write MCON register command (W MC XX) or from application software using a Timed Access write cycle. If PE is set to 1, PA3-0 is the high nibble of the address equal to and less than which is considered read/write memory and greater than which is considered read-only memory. The Partition addressing is summarized in Table 2.

PARALLEL I/O

The DS5311FP Softener incorporates a total of four additional 8-bit parallel I/O ports which are easily accessed by the microprocessor. The ports are designated as A, B, C and D. These port pins are in addition to the HC11 ports, and all are accessible without conflict. The port functions are described in the DS53xx Softener Family User's Guide.

OSCILLATOR

The DS5311FP provides an on-chip oscillator circuit which may be driven either by using an external crystal as a time base or from a CMOS-compatible clock signal. The oscillator circuitry provides the internal clocking signals to the DS5311FP Softener and a CMOS-compatible clock output signal on CLKOUT. The frequency of the signal on CLKOUT is the same as the input frequency to the DS5311's oscillator circuit.

Figure 3 illustrates the required connections when using the DS5311FP with a crystal. The typical values of C1 and C2 are 15 pF each. The oscillator is designed for use with a parallel resonant crystal. When the oscillator is driven from an external clock circuit, the CMOS-compatible waveform should be connected to X1, and X2 should be left open.

Also shown in Figure 3, the DS5311's CLKOUT pin should be used to drive the 68HC11 microprocessor's EXTAL pin in its external clock configuration. In turn, the 68HC11's E pin should be connected to the DS5311's CLKIN pin. This connection is used to monitor clock cessation from the 68HC11 when entering STOP mode, allowing the DS5311FP to enter a low power mode.

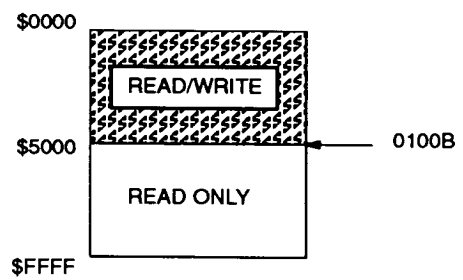
STOP MODE

The DS5311FP supports the 68HC11 STOP mode where all clocks are stopped to reduce power consumption to a few microamps. Recovery to active mode is accomplished by a reset or an interrupt. When an interrupt takes the HC11 out of STOP, the HC11's DLY bit in the OPTION register must be set to a 1. The DS5311FP will not go through a crystal startup wait period following an interrupt when no reset is issued.

DS5311FP PARTITION ADDRESS CONTROL Table 2

ADDRESS	EXPANDED MODE MEMORY	PARTITION BITS (PA3-PA0)
$0000		
$1000		0000B
$2000		0001B
$3000		0010B
$4000		0011B
$5000		0100B
$6000		0101B
$7000		0110B
$8000		0111B
$9000		1000B
$A000		1001B
$B000		1010B
$C000		1011B
$D000		1100B
$E000		1101B
$F000		1110B
$FFFF		1111B

Example:
If the partition address is 0100B ($4), then memory from $0 to $4FFF is read/write memory, and memory from $5000 to $FFFF is read-only memory. The partition function is enabled by the PE bit in the MODES register. As can be seen from the example above, when the partition is enabled, the minimum amount of read/write memory available is 4096 bytes (4K). If the partition is set to 1111B ($F) or the PE bit is cleared, then the entire memory is read/write.



DS5311FP BOOTSTRAP LOADER

The general function of the on-chip bootstrap loader is described in the DS53xx Softener Family User's Guide. Unique aspects of its implementation in the DS5311FP are documented in this section.

AUTO-BAUD DETECTION

Serial communication with the bootstrap loader requires an asynchronous communications format at one of the supported baud rates using eight data bits, no parity, and one or more stop bits. When the bootstrap loader is invoked, the firmware initializes the 68HC11's on-chip serial port and awaits an ASCII carriage return (<CR>) or $0D character to be received from the remote PC. The firmware will automatically attempt to establish communication at the correct baud rate by adjusting the 68HC11's Baud-Rate Prescale Selects and Baud-Rate Selects and writing one of the 26 unique divisors into the baud rate generator. As a result, the firmware selects the baud rate which is as close as possible to the baud rate from the sending terminal.

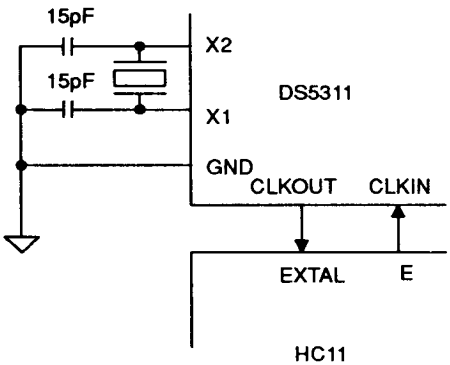
The baud rate selected by the firmware is given by the following equation:

[fosc / (64 x Divisor)]

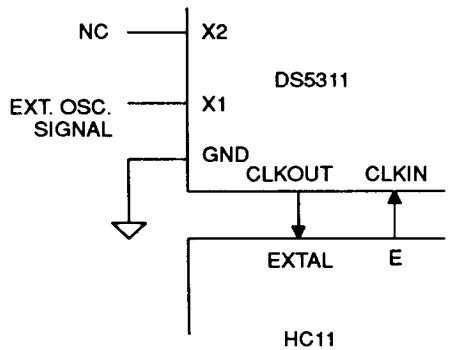
where the divisor value chosen is the one of 26 possible values shown in Table 3 which most closely matches the baud rate of the received carriage return character. Table 3 also gives resulting rates for three crystals which can be used with the 68HC11/DS5311.

CLOCK CONNECTION FOR DS5311FP Figure 3

DS5311FP CRYSTAL CONNECTION



DS5311FP EXTERNAL OSCILLATOR CONNECTI



DS5311FP AUTOBAUD FREQUENCIES & DIVISOR VALUES Table 3

DIVISOR	4.9152 MHZ	9.83 MHZ	11.0592 MHZ
1	76800	153600	172800
2	38400	76800	86400
3	25600	51200	57600
4	19200	38400	43200
6	12800	25600	28800
8	9600	19200	21600
12	6400	12800	14400
13	5908	11815	13292
16	4800	9600	10800
24	3200	6400	7200
26	2954	5908	6646
32	2400	4800	5400
48	1600	3200	3600
52	1477	2954	3323
64	1200	2400	2700
96	800	1600	1800
104	738	1477	1662
128	600	1200	1350
192	400	800	900
208	369	738	831
256	300	600	675
384	200	400	450
416	185	369	415
512	150	300	338
832	92	185	208
1664	46	92	104

DS5311FP BOOTSTRAP LOADER SERIAL COMMANDS

Commands will not be processed until an entire command line is entered and terminated with a <CR>. No command line can be longer than 14 bytes. Since a command line is not processed until a <CR> is entered, it can be edited with the delete key which does a destructive delete to the screen. Lines longer than 14 characters will cause an error message to be displayed and no action to be taken on the command line.

A command summary is given below:

^C (Abort)

Abort command. The bootstrap loader clears all of its internal buffers, issues a prompt, and waits for the next command. Anything in the type-ahead buffer is removed. All output is stopped. If trace was previously

enabled, it is returned to its default disabled state. Similarly, if XOFF was previously enabled, it is turned off.

C [Begin-Address [End-Address]] (CRC)
A CRC-16 is calculated and reported for the requested range. The range must be between $340 and $FFFF. Every CRC value calculated is pushed on the CRC stack of length two.

The CRC range and the calculated value can be seen with the R command. (See "Range Syntax" and K command.)

D [Begin-Address [End-Address]] (DUMP)
The requested range is dumped in Motorola S-Record format. All 64K bytes of memory can be dumped. (See "Range Syntax.")

E (EXIT)
The bootstrap loader is exited.

F Byte [Begin-Address [End-Address]] (FILL)
The requested value is filled into the memory range requested. Any range from $340 through $FFFF may be requested. (See "Range Syntax.")

G (GET)
The Softener registers for ports A, B, C, and D (addresses $317 to $32D) are dumped as Hex bytes.

K (KLEAR)
The CRC stack is cleared. (See C command.)

L (LOAD)
Motorola S-Records are loaded into the nonvolatile SRAM. The Softener registers and the 768 bytes prior to the Softener registers (memory area from $0 through $33F) may not be loaded. (See "Range Syntax.")

Record types S0, S1 and S9 are supported. Each line of the file is treated the same way. All characters are thrown away until the sync character "S" is read. The record is then processed as defined by the record type and record length. Control will return to the command prompt after a termination record (S9) is encountered. Every time a byte is put to memory, it is read back to verify that it is there. If the byte read back is different, an error is reported. All errors are reported immediately after the erroneous character is received. The program will then read characters until a sync character is found and then attempt to process the data input from the input stream. Note that all bytes are put to memory as they are encountered. This means that if a bad checksum is found, an error will be reported, but all the bytes on the line will have been put to memory.

M [Modem Address [P] [K]] (MODEM)
This command replies with AVAILABLE or UNAVAILABLE.

A modem can be mapped into the following address spaces - $100 to $1FF (with PCE1), $200 to $2FF (with PCE2), $340 to $FFF, and $1040 to $EFFF. The three least significant bits of the modem address are cleared, resulting in the modem being mapped on 8-byte boundaries. Whenever the modem is made available, the eight memory address spaces will be altered, and interrupts will be allowed on IRQ (vector $FFF2). Including the "P" in the modem command activates the peripheral chip enables for the appropriate memory locations. The "P" command requests that peripheral chip enables be used at addresses $100 to $2FF with the modem. Any valid character entered through the modem during a serial load will PREEMPT a serial communication and cause the serial loader to restart the dialog through the modem. "K" signifies that a DS1283 clock is present on PCE1 at address $1C0H.

N (NEW)
This command is used to set the "FRESHNESS". It is necessary that the reload pin be low to do this. If it isn't the error message "RELOAD PIN MUST BE ACTIVE TO ENABLE FRESHNESS" is displayed. If this condition is met, the serial loader will ask the user to confirm that freshness is to be set. This is done with the message "CONFIRM: ". At this point the user must enter "FRESH" without any errors to enable the part to go into freshness. The confirm word is echoed. If "FRESH" is entered correctly, the message "POWER DOWN TO MAINTAIN FRESHNESS" is displayed and NO more communication can be made with the serial loader until the Softener is reset.

P Port Byte (PUT)
Puts a byte into a Softener port register. The port value is a hex number between 17 and 2D.

R (READ)

The R command reads and displays the Softener registers, CRC ranges, and modem status. The Memory Control, WatchDog, MOdes and POwer registers are displayed in the following format:

MC:XX WD:XX MO:XX PO:XX

If the modem is available because the user executed the M command with the "P" or "K" options, then the message

MODEM AT:XXXX [USING PCE] [with CLOCK]

is displayed. If any CRC calculations have been done and not Kleared, then the following messages are displayed:

CRC 1 > Starting Address - Ending Address =
CRC value
CRC 2 > Starting Address - Ending Address =
CRC value

T (TRACE)

This command replies with ON or OFF. When on, incoming Motorola S-Records input to the load and verify commands are echoed. A control-C always turns this value to the off state.

V (VERIFY)

Motorola S-Records are read and compared to existing data in memory. Any time a difference is found, an error is reported and the rest of the current record is discarded. (See the T and L commands.)

W Reg Value (WRITE)

Any one of the four registers, MCon, WatchDog, MOdes or POwer, is altered. Examples of the W command with two character mnemonics:

W MC 12
W WD 34
W MO 56
W PO 78

RANGE SYNTAX

[start-segment] [end-segment]
What this means is that no values need be entered, and defaults will be taken. These defaults are $340 to $FFFF, except for the "D" command where the defaults are $0 to $FFFF. If only a starting value is given then the default ending value is used.

The starting value must be less than or equal to the ending value.

SERIAL LOADER BANNER

DS5311FP SERIAL LOADER Vn.n.n COPYRIGHT (C) 1990, DALLAS SEMICONDUCTOR
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ERROR MESSAGES:

E:ARGREQ - command requires an argument.
E:BADADR - illegal address specified. (See "Range Syntax.")
E:BADCKS - bad check sum encountered on a Motorola S-Record. Unfortunately the data has already been loaded.
E:BADCMD - an invalid command was requested.
E:BADLEN - illegal length for a Motorola S-Record.
E:BADREC - an illegal Motorola S-Record was encountered.
E:BADREG - an unrecognized register was requested.
E:BADRNG - beginning address is less than $340.
E:EXTARG - more arguments on the command line than necessary.
E:ILLOPT - bad range specified, ending address may be less than beginning address. (See "Range Syntax.")
E:NOTHEX - a non-hexadecimal character was encountered when it was not expected.
E:VERIFY - memory is not the same as the value being verified against it.

NOTES:

- Motorola S-Records S2 through S8 types are ignored.
- Tabs are made spaces, lower case is converted to upper case, deletes are made into back spaces.

DS5311FP INTERRUPT SUMMARY

The DS5311FP can be programmed to generate interrupts to the 68HC11 processor in response to a number of conditions, as shown below in Table 4.

DS5311FP RESET/INTERRUPT SOURCES Table 4

TYPE	PIN	BIT(S)	LOCATION	FUNCTION
RC	$\overline{\text{RSTOUT}}$			
$\overline{\text{RSTIN}}$	$\overline{\text{RSTOUT}}$			
Power Fail	$\overline{\text{RSTOUT}}$			
Power-on	$\overline{\text{RSTOUT}}$			
		CRC	WDOG.1	CRC Test Enable
		POR	RIST.4	Power-On Reset Status
Bootstrap Ldr	$\overline{\text{RSTOUT}}$	ROM	MODES.0	Invoke Bootstrap Loader
		ROMLTR	WDOG.0	ROM Later Enable
Watchdog	$\overline{\text{RSTOUT}}$	WDM	WDOG.4	Watchdog Timer Mask
		WD2-0	WDOG.7-5	Watchdog Timeout Select
		WDS	RIST.6	Watchdog Status Flag
Power Fail	$\overline{\text{INT1}}$	PFWM	POWER.3	Power Fail Warning Mask
		PFW	RIST.5	Power Fail Warning Status
Port A	$\overline{\text{INT2}}$	PAM7-0	PAM.7-0	Port A Interrupt Masks
		PAELS7-0	PAELS.7-0	Port A Edge/Level Select
		PAPNS7-0	PAPNS.7-0	Port A Pos./Neg. Select
		PAI	RIST.0	Port A Interrupt Status
Register File	$\overline{\text{INT2}}$	SIBM7-0	SIBM.7-0	Slave Input Buffer Masks
		SOBM7-0	SOBM.7-0	Slave Output Buffer Masks
		ITS	MCS.7	Interrupt To Slave
		IFMM	SCS.6	Interrupt From Master Mask
		RFSI	RIST.3	Register File Interrupt Status
		IBI	RIST.2	Input Buffer Interrupt Status
		OBI	RIST.1	Output Buffer Interrupt Status

DS5311FP REGISTER SUMMARY

Table 3 shown below summarizes the addresses for the registers within the DS5311.

DS5311FP REGISTER ADDRESSES Table 5

REGISTER	LABEL	LOCATION
Input Buffer Register (8)	IBR7-0	$300-$307
Output Buffer Register (8)	OBR7-0	$300-$307
Input Buffer Full Register	IBF	$308
Output Buffer Full Register	OBF	$309
Slave Input Buffer Mask Register	SIBM	$30A
Slave Output Buffer Mask Register	SOBM	$30B
Master Input Buffer Mask Register	MIBM	$30C
Master Output Buffer Mask Register	MOBM	$30D
Slave Control/Status Register	SCS	$30E
Master Control/Status Register	MCS	$30F
Timed Access Register	TAS	$310
Port A Interrupt Mask Register	PAM	$311
Memory Control Register	MCON	$312
Watchdog Timer Register	WDOG	$313
Modes Register	MODES	$314
Power Register	POWER	$315
Reset and Interrupt Status Register	RIST	$316
Port A Data Latch Register	PADL	$317
Port A Data Direction Register	PADDR	$318
Port A Motorola/Intel Select Register	PAMIS	$319
Port A Pin Level Register	PAPL	$31A
Port A Edge Detect Register	PAED	$31B
Port A Level Detect Register	PALD	$31C
Port A Edge/Level Select Register	PAELS	$31D
Port A Positive/Negative Select Register	PAPNS	$31E
Port B Data Latch	PBDL	$31F
Port B Data Direction Register	PBDDR	$320
Port B Motorola/Intel Select	PBMIS	$321
Port B Pin Level Register	PBPL	$322
Port B Edge Detect Register	PBED	$323
Port C Data Latch	PCDL	$324
Port C Data Direction Register	PCDDR	$325

REGISTER	LABEL	LOCATION
Port C Motorola/Intel Select	PCMIS	$326
Port C Pin Level Register	PCPL	$327
Port C Edge Detect Register	PCED	$328
Port D Data Latch	PDDL	$329
Port D Data Direction Register	PDDDR	$32A
Port D Motorola/Intel Select	PDMIS	$32B
Port D Pin Level Register	PDPL	$32C
Port D Edge Detect Register	PDED	$32D
CRC Registers	CRC1-2	$32E-$32F
Reserved for Bootstrap	N/A	$330-$33F

Below is a summary of operation of all control/status bits unique in function for the DS5311.

MEMORY CONTROL REGISTER

ADDR.	7	6	5	4	3	2	1	0	LABEL
$312	PA3	PA2	PA1	PA0			PCE2	PCE1	MCON

PA3-PA0 Partition Address:
Partitions the memory map between read-only and read/write areas if PE (MODES.6) is set. The partition address is the high nibble of the address equal to and less than which is considered read/write memory and greater than which is considered read-only memory.

For example, if PE is set and the partition address is 0100B, then read/write memory is from $0 to $4FFF and read-only memory from $5000 to $FFFF.

If the partition address is set to 1111B, then the entire memory map is partitioned as read/write memory and can be written without restriction by the application software. If PE is clear, then PA3-PA0 have no effect on operation and the entire memory is read/write memory.

Writable only via Timed Access.[3]

PCE2-1 Peripheral Chip Enable Controls:
PCEn = 0 causes external $\overline{\text{PCEn}}$ pin to remain at inactive high level.
PCEn = 1 causes external $\overline{\text{PCEn}}$ pin to pulse low when read or write access is performed in its associated block as follows:

When PCE1 = 1, the $\overline{\text{PCE1}}$ pin will be activated for any access within the range $100 to $1FF.

When PCE2 = 1, the $\overline{\text{PCE2}}$ pin will be activated for any access within the range $200 to $2FF.

MODES REGISTER

ADDR.	7	6	5	4	3	2	1	0	LABEL
$314	RG	PE	RFEN	MD2	MD1	MD0	IRL	ROM	MODES

RG Range select:
RG = 0; 8K Byte RAM
RG = 1; 32K Byte RAM
Writable only via bootstrap loader.[2]

PE Partition Enable:
PE = 0: Partition function disabled. (All memory is read/write)
PE = 1: Partition function enabled. (Separate read-only and read/write memory)

Writable only via bootstrap loader.[2]

RFEN Dual Port Register File Enable:
RFEN = 0 disables Register File
RFEN = 1 enables Register File

Writable only via timed access.[3]

MD2-0 Memory Map Mode Control:
Non-functional on DS5311

IRL Internal Reload Pin state:
Indicates current logic level being applied to Reload pin ($\overline{RL}$):
IRL = 0 means $\overline{RL}$ pin = 1.
IRL = 1 means $\overline{RL}$ pin = 0.

ROM Invoke Bootstrap Loader ROM:
The ROM bit can be used by the application software to invoke the bootstrap loader.
ROM = 0: Application software executes normally.
ROM = 1: Bootstrap loader invoked by application software.

Writable only via timed access.[3]

NOTES:

1. All registers and their control/status bits are read/write unless otherwise indicated.
2. Control bits which are designated as "Writable only via bootstrap loader" can only be altered via the Write command while the bootstrap loader is invoked. These bits can be read, but not written, while the application software is in execution.
3. Control bits which are designated as "Writable only via Timed Access" can be written using the timed access sequence while the application software is in execution. They can also be modified via the Write command when the bootstrap loader is invoked. The Write command firmware takes care of the timed access requirement.

ORDERING INFORMATION

The following versions of the DS5311FP are available as standard products from Dallas Semiconductor:

PART#	CLOCK	PACKAGE
DS5311FP	2.0MHz	80-pin QFP
DS5311FP-A	3.0MHz	80-pin QFP

DS5311FP ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to 7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to 125°C
Lead Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(t_A = 0°C to +70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage						
AS, $\overline{RL}$, CLKIN, ADn, A8-A15, E, R/$\overline{W}$	V_{IL}	-0.3		0.2 V_{CC}	V	1
All ports in edge/level detect mode	V_{IL}	-0.3		0.4	V	
All other pins	V_{IL}	-0.3		0.8	V	
Input High Voltage						
AS, $\overline{RL}$, CLKIN, ADn, E, R/$\overline{W}$, A8-A15	V_{IH}	0.7 V_{CC}		V_{CC} +0.3	V	1
XTAL1	V_{IH}	3.5		V_{CC} +0.3	V	
$\overline{RSTIN}$	V_{IH}	4.0		V_{CC} +0.3	V	
All ports in edge/level detect mode	V_{IH}	2.8		V_{CC} +0.3	V	
All other pins	V_{IH}	2.0		V_{CC} +0.3	V	
Output Low Voltage						
XTAL2 (I_{OL} = 1mA)	V_{OL}			0.4	V	1
All other pins (I_{OL} = 4mA)	V_{OL}			0.4	V	
Output High Voltage						
XTAL2 (I_{OH} = -100uA) $\overline{INT1}$, $\overline{INT2}$ (I_{OH} = -100uA) Ports A, B, C, D Intel mode (I_{OH} = -100uA)	V_{OH}	2.4			V	1, 7
All other pins and Ports A, B, C, D Motorola mode (I_{OH} = -1mA)	V_{OH}	2.4			V	
Transition Current						
1 to 0 Port A, B, C, D Intel mode (V_{PIN} = 2.0V)	I_{TL}			-500	µA	
1 to 0 Ports A, B, C, D Intel mode (pulsed) (V_{PIN} = 2.4V)	I_{TH}	-1			mA	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Current						
Ports A, B, C, D Intel mode (V_{PIN} = 0.4V)	I_{IL}			-50	µA	
$\overline{RL}$ Pull-up Resistor	R_{RL}	27		50	Kohms	
Power Fail Warning Voltage	V_{PFW}	4.25	4.37	4.50	V	1
Minimum Operating Voltage	V_{CCMIN}	4.00	4.12	4.25	V	1
Lithium Battery Voltage						
If not using STOP function	V_{LB}	2.5		4.0	V	1
If using STOP function	V_{LB}	2.9		3.3		
Output Supply Voltage						
(I_{CC0} = -100mA)	V_{CCO}	V_{CCI} -0.3			V	1, 2a
(I_{CC0} = -1uA)	V_{CCO}	V_{LB} -0.8		V_{LB} -0.2	V	1, 2b
Output Supply Current						
V_{CC0} = V_{CCI} -0.3V	I_{CCO}	100			mA	
Lithium Battery Current in Lithium-Backed Mode	I_{LB}		10	100	nA	3, 4
Operating Current	I_{CC}		7.0	15.0	mA	3
Stop Mode Current	I_{CCSTOP}		60	250	µA	
Battery Health Threshold Voltage	V_{BATH}	2.35		2.65	V	1
Input Leakage Current						
$\overline{INT1}$, $\overline{INT2}$ (V_{PIN} = 2.4V)	I_{IL}			-450	µA	
ADn, A8-A15, E, R/$\overline{W}$, AS, CLKIN: 0 < V_{IN} < 0.3V or V_{CC} -0.3 < V_{IN} < V_{CC}	I_{IL}			± 50	µA	
0.3V < V_{IN} < V_{CC} -0.3V	I_{IL}			±180	µA	
Input High Current						
Ports in Intel Mode, $\overline{RL}$ (V_{PIN} = V_{CCI})	I_{IHI}			-5	µA	
Input High Current						
Ports in Motorola Mode, $\overline{RSTIN}$	I_{IHM}			-1	µA	
Input Low Current						
Ports in Motorola Mode, $\overline{RSTIN}$	I_{ILM}			1	µA	

DS5311FP AC ELECTRICAL CHARACTERISTICS

NO.	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
1	Address, R/$\overline{W}$ setup to E rising	30			ns	
2	AS width	35			ns	
3	Address setup to AS falling	30			ns	
4	AS falling to address hold	10			ns	
5	Data input setup to E falling	20			ns	
6	E falling to data hold	0			ns	
7	E rising to $\overline{WROUT}$ falling			50	ns	
8	E falling to $\overline{WROUT}$ rising			40	ns	
9	E rising to data output valid			95	ns	
10	E falling to data output high-Z		30		ns	
11	E rising to $\overline{CEx}$ falling			40	ns	
12	E falling to $\overline{CEx}$ rising			40	ns	
13	E rising to $\overline{PCEx}$ falling			45	ns	
14	E falling to $\overline{PCEx}$ rising			45	ns	
15	Width of active "edge" (pulse)	20			ns	
16	Active edge to $\overline{INT2}$ falling			30	ns	
17	Active level setup to E rising	60			ns	
18	E rising (second time) to active level hold	10			ns	
19	E rising to $\overline{INT2}$ falling			50	ns	
20	E falling to $\overline{INT2}$ rising			50	ns	
21	E falling to port pin data valid		40		ns	
22	E falling to strong pull-up turn ON		25		ns	
23	E rising to strong pull-up turn OFF		25		ns	
24	Port pin data setup to E rising	0			ns	
25	E rising to port pin data hold	20			ns	
26	Master address setup to master $\overline{CS}$ falling (RF)	0			ns	
27	Master data setup to master $\overline{WR}$ rising (RF)	15			ns	Master $\overline{CS}$ is low
28	Master $\overline{WR}$ rising and master $\overline{CS}$ rising (simultaneously) to master data hold (RF)	0			ns	
28A	Master $\overline{WR}$ rising to master data hold (RF)	5			ns	Master $\overline{CS}$ is low

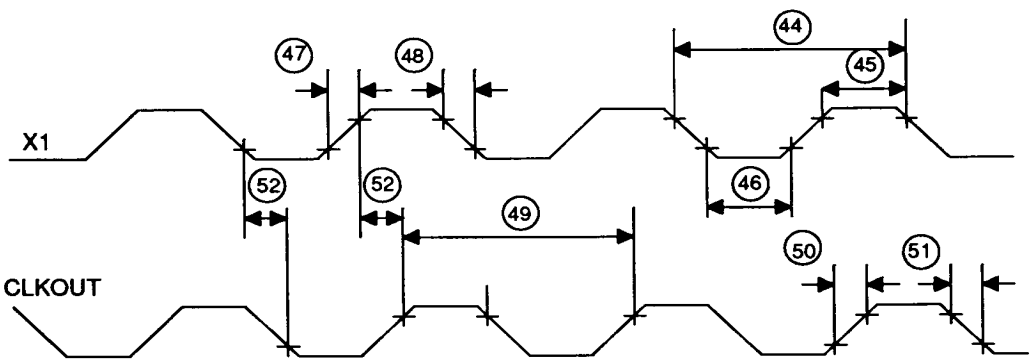
NO.	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
29	Master $\overline{RD}$ falling and master $\overline{CS}$ falling (simultaneously) to master data output valid (RF)			55	ns	
29A	Master $\overline{RD}$ falling to master data output valid (RF)			55	ns	Master $\overline{CS}$ is low
30	Master $\overline{RD}$ rising to master data output high-Z (RF)		25		ns	Master $\overline{CS}$ is low
31	(Read) E falling to $\overline{IBR}$ falling (RF) (Write) E falling to STS/OBR rising (RF)		70 100		ns	
32	Master $\overline{WR}$ rising to $\overline{IBR}$ rising (RF) Master $\overline{RD}$ rising to STS/OBR falling (RF)		70 70		ns	
33	AS rising to address output			65	ns	Address input is stable
34	Address input to address output			65	ns	AS is high
35	E falling to address hold	5			ns	
36	Master $\overline{WR}$ rising to master address hold (RF)	5			ns	Master $\overline{CS}$ is low
37	Master $\overline{RD}$ rising to master address hold (RF)	5			ns	Master $\overline{CS}$ is low
38	Master $\overline{CS}$ rising to master address hold (RF)	5			ns	Master $\overline{WR}$ or master $\overline{RD}$ is low
39	Master $\overline{WR}$ pulse width (RF)	50			ns	
40	Master $\overline{RD}$ pulse width (RF)	85			ns	
41	Master $\overline{CS}$ pulse width (RF)	50			ns	Write cycle
42	Master $\overline{CS}$ pulse width (RF)	85			ns	Read cycle
43	$\overline{RSTIN}$ pulse width	3			E cycles	
–	E rising to $\overline{RSTOUT}$ falling or rising			40	ns	
–	$\overline{RL}$ active	20			E cycles	
–	$\overline{RL}$ inactive	20			E cycles	

DS5311FP CLOCK TIMING AC CHARACTERISTICS

(t_A = 0°C to +70°C; V_{CC} = +5V ± 10%)

NO.	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
44	External clock input cycle time (t_{CLK})	60			ns	
45	External clock pulse width, high	TBD			ns	V_{X1} = 3.0V
46	External clock pulse width, low	TBD			ns	V_{X1} = 1.5V
47	External clock rise time (t_{XIR})			5	ns	1.5 to 3.0V
48	External clock fall time (t_{XIF})			5	ns	3.0 to 1.5V
49	CLKOUT cycle time	60			ns	
50	CLKOUT rise time			5	ns	1.5 to 3.0V
51	CLKOUT fall time			5	ns	3.0 to 1.5V
52	CLKOUT delay time from external clock			55	ns	

DS5311FP CLOCK TIMING DIAGRAM

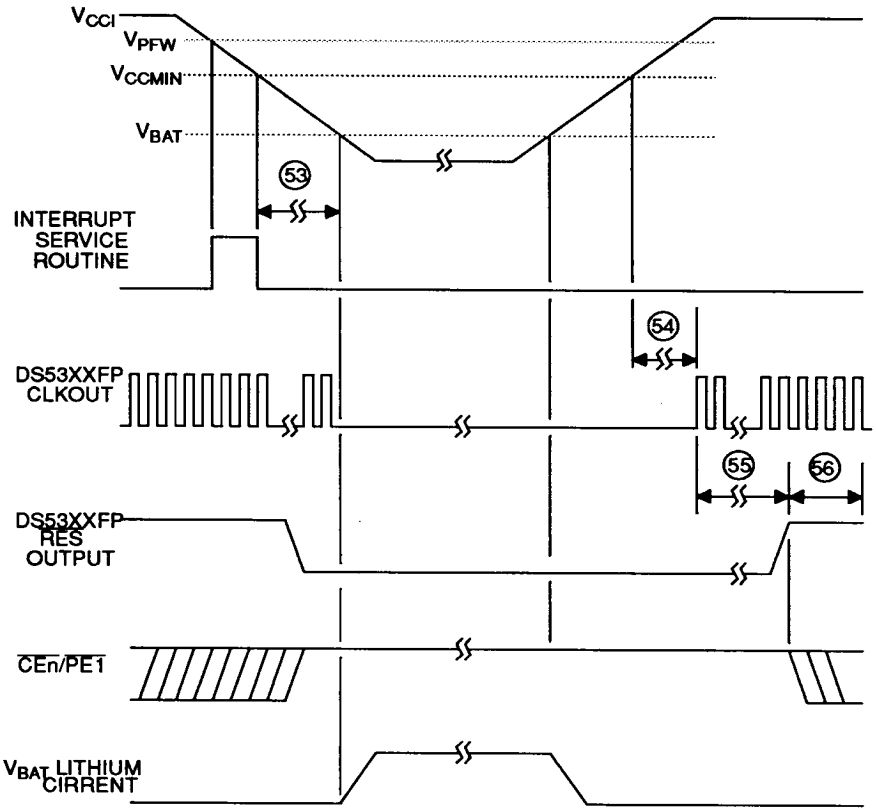


DS5311FP AC CHARACTERISTICS (CONT'D)
CRASHPROOF TIMING

(t_A = 0°C to 70°C; V_{CC} = 5V ± 10%)

NO.	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
53	Slew rate from V_{CCMIN} to V_{BAT}	100			t_{CLK} cycles	
54	Crystal start-up time		TBD			Note 5
55	Power-On Reset Delay			32,800	t_{CLK} cycles	
56	CRC Timing		TBD		t_{CLK} cycles	Note 6

CRASHPROOF OPERATION TIMING



NOTES:

1. All voltages are referenced to ground.

2(a). X1 low; $\overline{RSTIN}$ high, Ports A, C, and D in Intel input mode, Port B in Motorola input mode. All port pins open. All outputs open. CLKIN, AS, AD7 - AD0 low, E low, R/$\overline{W}$ high.

2(b). All pins low, except $\overline{CE1}$, $\overline{CE2}$, and $\overline{PCE1}$, which are open.

3. Maximum operating I_{CC} is measured with all output pins disconnected, X1 is driven @ 12 MHz with t_{X1R}, t_{X1F} = 10ns, V_{IL} = 0.5V, X2 disconnected; $\overline{RSTIN}$ = V_{CC}, Ports A, C, and D in Intel input mode, Port B in Motorola input mode, all port pins open. Write operations to internal registers in progress.

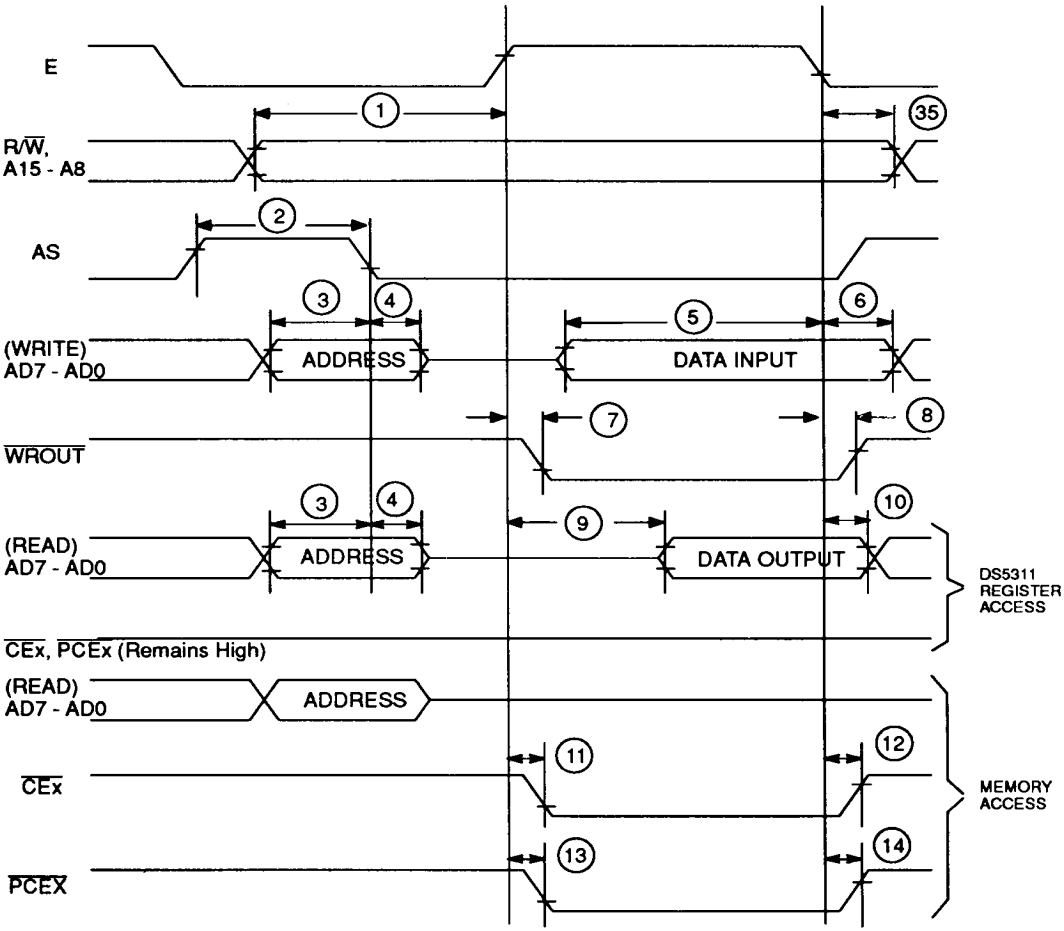
4. I_{LB} is measured with V_{CCI} = 0V; 2.5 < V_{BAT} < 4.0, all inputs and outputs low, except for V_{CCO}, $\overline{CE1}$, $\overline{CE2}$, and $\overline{PCE1}$, which are open.

5. Crystal start up time is required to get the mass of the crystal into vibrational motion measured from the time that power is first applied to the circuit until the first clock pulse is produced by the on-chip oscillator. The user should check with the crystal vendor for a worst case specification on this time.

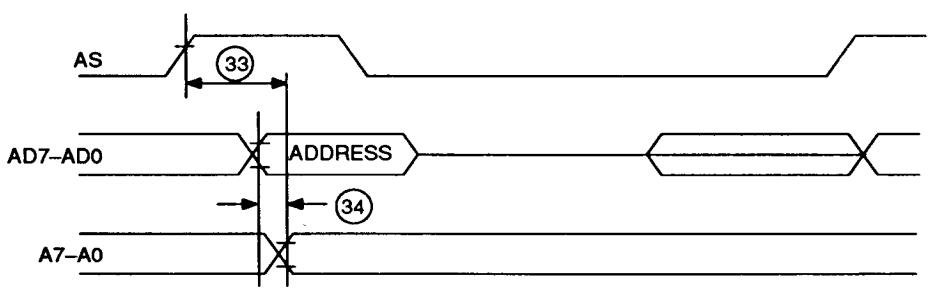
6. CRC time delay only applies if CRC testing has been enabled as described in the DS53xx User's Guide.

7. Because the pull-up current on pins $\overline{INT1}$ and $\overline{INT2}$ is low, the capacitance connected to these pins must be taken into account to avoid an unacceptably long rise time. In some cases an additional pull-up resistor may be needed.

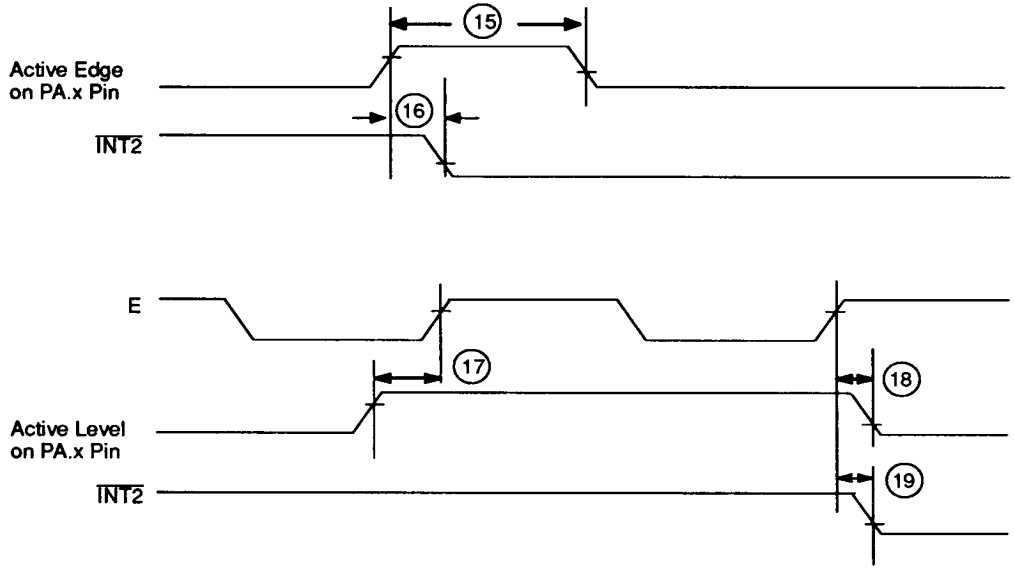
DS5311FP READ AND WRITE TIMING



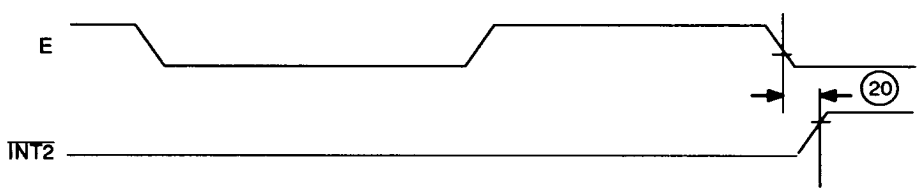
DS5311FP ADDRESS OUTPUT TIMING



DS5311FP INTERRUPT OUTPUT TIMING



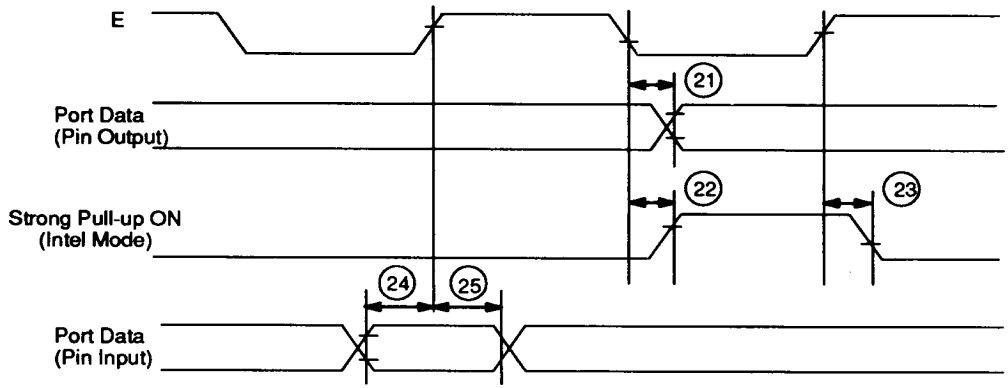
Level on PA.x pin must be active for two consecutive rising edges of E, with no transitions to the inactive level during that time, in order to generate an interrupt.



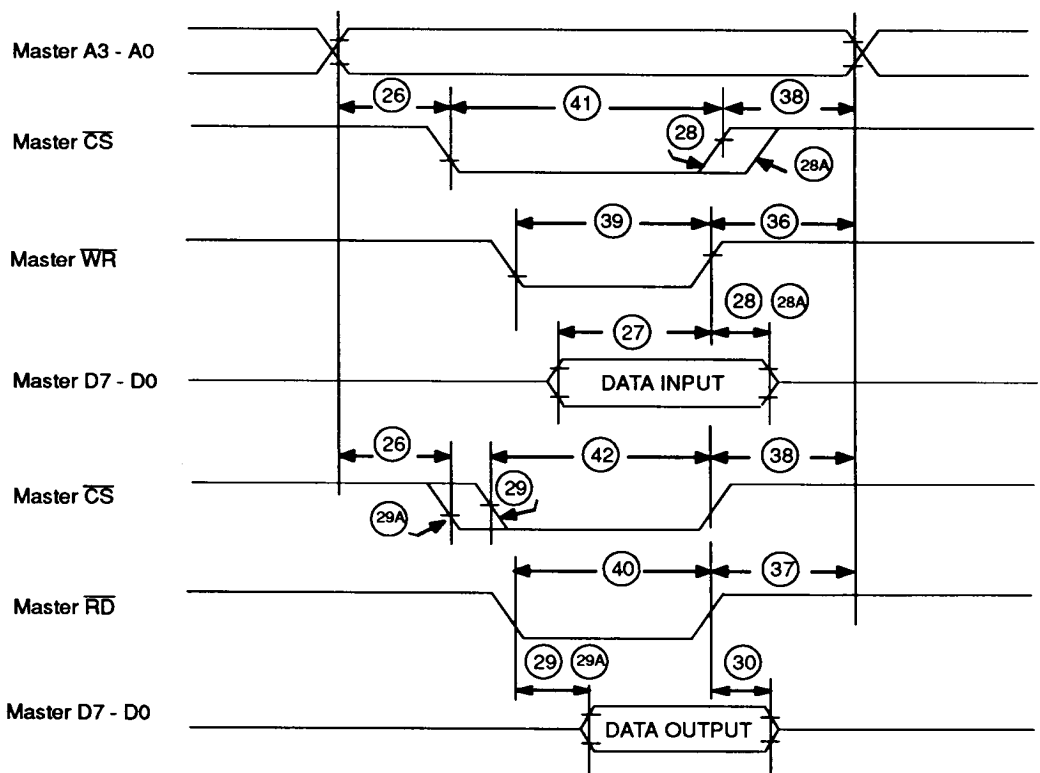
$\overline{INT2}$ can be cleared by the software doing one or more of the following (as appropriate):

- Read Port A Level Detect register
- Read Port A Edge Detect register
- Read one or more Input Buffer registers
- Write one or more Output Buffer registers
- Write the Master Control/Status register

DS5311FP PORT TIMING

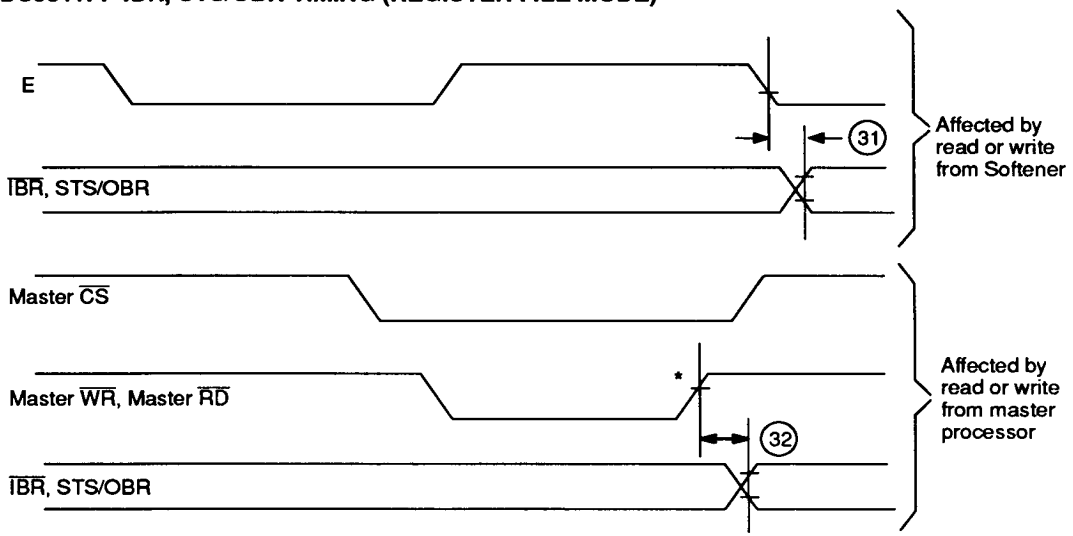


DS5311FP REGISTER FILE (RF) MASTER ACCESS TIMING



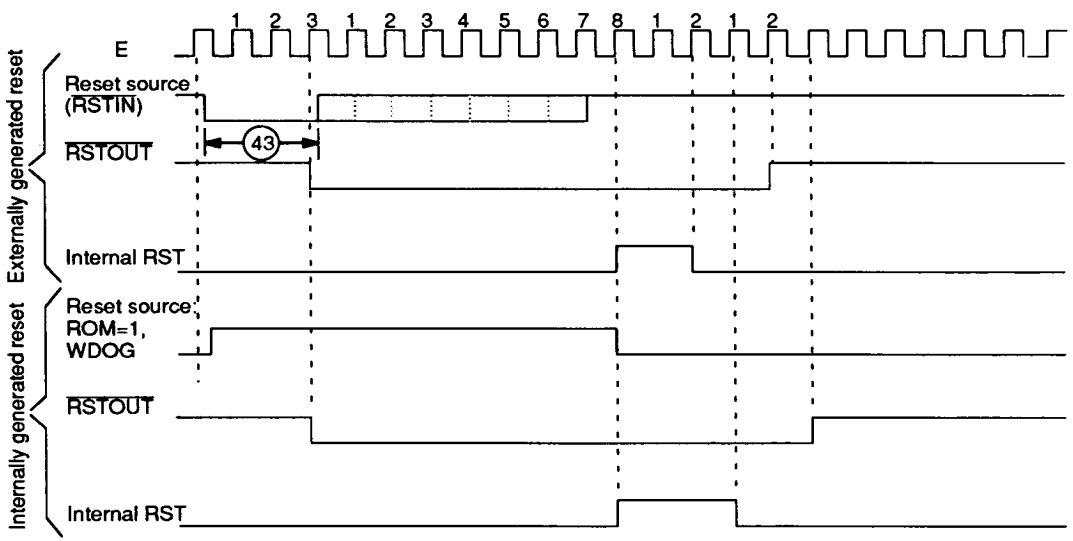
Master $\overline{CS}$ and master $\overline{WR}$ must both be low to write. The last one going low and the first one going high determine the write cycle width. The same holds true for the read cycle, using master $\overline{CS}$ and master $\overline{RD}$.

DS5311FP $\overline{IBR}$, STS/OBR TIMING (REGISTER FILE MODE)



* Assumes master $\overline{WR}$ or master $\overline{RD}$ goes high before master $\overline{CS}$ goes high.

DS5311FP RESET TIMING

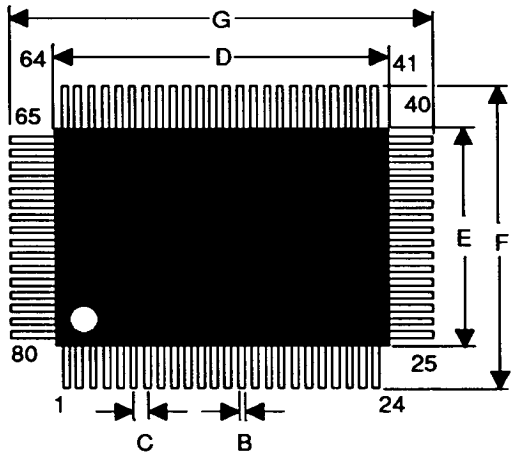


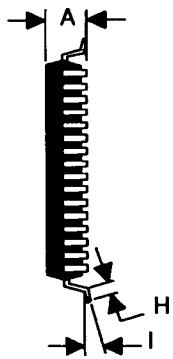
For a reset generated by power fail (PF) or crystal timeout (CRYTIM):

After the stimulus (PF, CRYTIM) is gone, the internal reset will be active for two E cycles more, starting from the first rising edge of E after the stimulus is gone. $\overline{RSTOUT}$ will be active for four E cycles more, starting from the same point.

The minimum active pulse width of $\overline{RSTOUT}$ is 12 E cycles. There is no maximum. If $\overline{RSTIN}$ is kept low for more than 11 E cycles, then $\overline{RSTOUT}$ will also stay low and not return high until four E cycles after $\overline{RSTIN}$ returns high.

DS5311FP MECHANICAL DRAWINGS





DIM	MIN	MAX
A IN.	0.115	0.124
MM	0.010	3.15
B IN	0.010	0.020
MM	0.25	0.45
C IN.	0.031	-
MM	0.80	-
D IN.	0.781	0.793
MM	19.85	20.15
E IN.	0.545	0.557
MM	13.85	14.15
F IN.	0.685	0.717
MM	17.40	18.20
G IN.	0.921	0.953
MM	23.40	24.30
H IN.	0.016	0.051
MM	0.40	1.30
I DEG.	0	10