DS75364 Dual MOS Clock Driver

General Description

The DS75364 is a dual MOS driver and interface circuit that operates with either current source or voltage source input signals. The device accepts signals from TTL levels or other logic systems and provides high current and high voltage output levels suitable for driving MOS circuits. It may be used to drive address, control and/or timing inputs for several types of MOS RAMs and MOS shift registers.

The DS75364 operates from standard MOS and bipolar supplies, and has been optimized for operation with V_{CC1} supply voltage from 12–20V positive with respect to V_{EE}, and with nominal V_{CC2} supply voltage from 3–4V more positive than V_{CC1}. However, it is designed so as to be useable over a much wider range of V_{CC1} and V_{CC2}. In some applications the V_{CC2} power supply can be eliminated by connecting the V_{CC2} pin to the V_{CC1} pin.

Inputs of the DS75364 are referenced to the V_{EE} terminal and contain a series current limiting resistor. The device will operate with either positive input current signals or input voltage signals which are positive with respect to V_{EE}. In many applications the V_{EE} terminal is connected to the MOS V_{DD} supply of −12V to −15V with the inputs to be driven from TTL levels or other positive voltage levels. The required negative level shifting may be done with an external PNP transistor current source or by use of capacitive coupling and appropriate input voltage pulse characteristics.

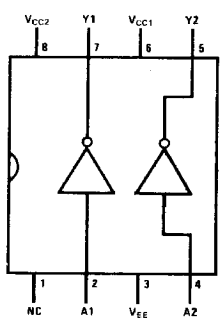
The DS75364 is characterized for operation over the 0°C to +70°C temperature range.

Features

- Versatile interface circuit for use between TTL levels and level shifted high current, high voltage systems
- Inputs may be level shifted by use of a current source or capacitive coupling or driven directly by a voltage source
- Capable of driving high capacitance loads
- Compatible with many popular MOS RAMs and MOS shift registers
- V_{CC1} supply voltage variable over wide range to 22V maximum with respect to V_{EE}
- V_{CC2} pull-up supply voltage pin available
- Operates from standard bipolar and/or MOS supply voltages
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS75364J-8 or DS75364N-8
See NS Package J08A or N08A

Absolute Maximum Ratings (Note 1)

Supply Voltage Range of V_{CC1}	-0.5V to 22V
Supply Voltage Range of V_{CC2}	-0.5V to 30V
Input Voltage	15V
Most Positive Voltage at Any Input with Respect to V_{CC2}	0.5V
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNIT
Supply Voltage			
V_{CC1}	4.75	22	V
V_{CC2}	V_{CC1}	28	V
Voltage Difference Between Supply Voltages	0	10	V
Input Voltage		V_{CC2}	
Temperature (T_A)	0	70	°C

Electrical Characteristics (Notes 2, 3, 4 and 5)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	Voltage Mode Input Logic Levels			5		10	V
V_{IL}	Low Level Input Voltage	Voltage Mode Input Logic Levels					1	V
I_{IH}	High Level Input Current	Current Mode Input Logic Levels			8		15	mA
I_{IL}	Low Level Input Current	Current Mode Input Logic Levels					0.7	mA
V_{OH}	High Level Output Voltage	$V_{CC2} = V_{CC1} + 3V$, (Note 4)	$I_{OH} = -100\mu A$	$V_{IL} = 1V$	$V_{CC1}-0.3$	$V_{CC1}-0.1$		V
				$I_{IL} = 0.7$ mA	$V_{CC1}-0.3$	$V_{CC1}-0.1$		V
			$I_{OH} = -10$ mA	$V_{IL} = 1V$	$V_{CC1}-1.2$	$V_{CC1}-0.9$		V
				$I_{IL} = 0.7$ mA	$V_{CC1}-1.2$	$V_{CC1}-0.9$		V
		$V_{CC2} = V_{CC1}$, (Note 4)	$I_{OH} = -50\mu A$	$V_{IL} = 1V$	$V_{CC1}-1$	$V_{CC1}-0.7$		V
				$I_{IL} = 0.7$ mA	$V_{CC1}-1$	$V_{CC1}-0.7$		V
			$I_{OH} = 10$ mA	$V_{IL} = 1V$	$V_{CC1}-2.3$	$V_{CC1}-1.8$		V
				$I_{IL} = 0.7$ mA	$V_{CC1}-2.3$	$V_{CC1}-1.8$		V
V_{OL}	Low Level Output Voltage	$I_{OL} = 10$ mA	$V_{IH} = 5V$			0.15	0.3	V
			$I_{IH} = 8$ mA			0.15	0.3	V
		$V_{CC2} = 15$ to 28V, $I_{OL} = 40$ mA	$V_{IH} = 5V$			0.25	0.5	V
			$I_{IH} = 8$ mA			0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA					$V_{CC1}+1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_{CC2} = 10V$ to 28V, $V_I = 10V$				17	26	mA
V_I	Input Voltage at Maximum Input Current	$V_{CC2} = 13.5V$ to 28V, $I_I = 15$ mA				9	13.5	V
I_{IH}	High Level Input Current	$V_I = 5V$				7	11	mA
V_{IH}	High Level Input Voltage	$I_I = 8$ mA				5.5	8	V
I_{IL}	Low Level Input Current	$V_I = 1V$				1.1	1.6	mA
V_{IL}	Low Level Input Voltage	$I_I = 0.7$ mA				0.7	1	V
$I_{CC1(H)}$	Supply Current From V_{CC1}, Both Outputs High	$V_{CC1} = 22V$, $V_{CC2} = 26V$, Both Inputs at 0V, No Load				1.1	1.6	mA
							0.25	mA
$I_{CC2(H)}$	Supply Current From V_{CC2}, Both Outputs High	$V_{CC1} = 22V$, $V_{CC2} = 26V$, Both Inputs at 0V, No Load				1.1	2	mA
$I_{CC1(L)}$	Supply Current From V_{CC1}, Both Outputs Low	$V_{CC1} = 22V$, $V_{CC2} = 28V$, Both Inputs at 7V, No Load				0.5	1	mA
$I_{CC2(L)}$	Supply Current From V_{CC2}, Both Outputs Low	$V_{CC1} = 22V$, $V_{CC2} = 28V$, Both Inputs at 7V, No Load				8	14	mA
$I_{CC1(H)}$	Supply Current From V_{CC1}, Both Outputs High	$V_{CC1} = 22V$, $V_{CC2} = 22V$, Both Inputs at 0V, No Load					0.25	mA
$I_{CC2(H)}$	Supply Current From V_{CC2}, Both Outputs High	$V_{CC1} = 22V$, $V_{CC2} = 22V$, Both Inputs at 0V, No Load					0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75364. All typical values are for $T_A = 25°C$, $V_{CC1} = 20V$, $V_{CC2} = 24V$ and $V_{EE} = 0V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

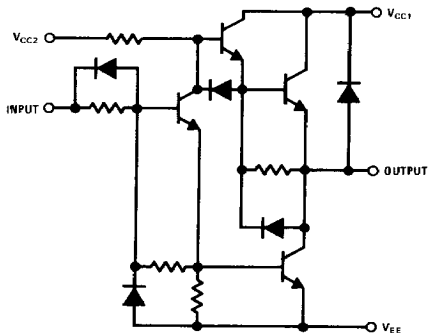
Note 4: Many of these parameters are specified independently for either voltage source or current source external forcing functions at the inputs. Use the appropriate set of specifications for each application.

Note 5: All parameters are specified with $V_{EE} = 0V$ and for input voltage no more positive than V_{CC2}.

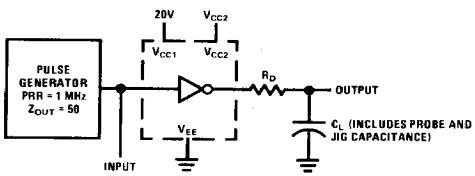
Switching Characteristics V_{CC1} = 20V, V_{EE} = 0V, T_A = 25°C

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		13		ns
			V_{CC2} = 20V		14		ns
t_{DHL}	Delay Time, High-to-Low Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		9		ns
			V_{CC2} = 20V		10		ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		21		ns
			V_{CC2} = 20V		21		ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		19		ns
			V_{CC2} = 20V		18		ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		34		ns
			V_{CC2} = 20V		35		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		28		ns
			V_{CC2} = 20V		28		ns

Schematic Diagram (1/2 shown)



AC Test Circuit and Switching Time Waveforms



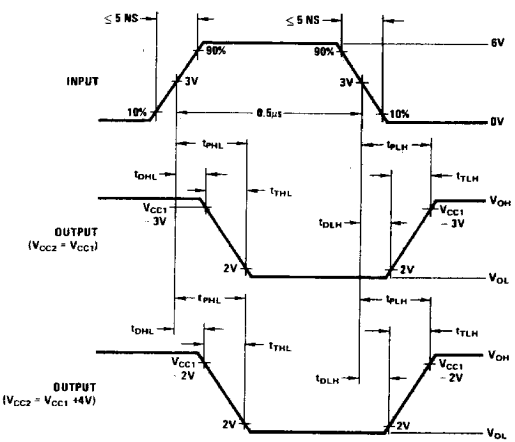


FIGURE 1. Switching Times, Each Driver

Typical Applications

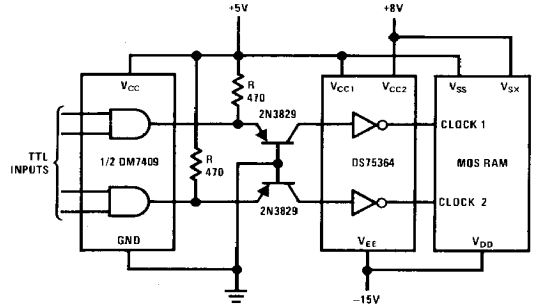


FIGURE 2. MOS RAM Clock Driver System with PNP Transistor Current Source used to Level-Shift to Inputs of DS75364

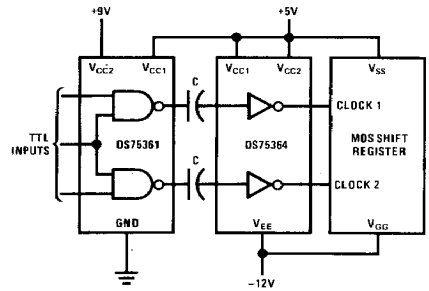


FIGURE 3. MOS Shift Register Clock Driver System with Capacitive Coupling used to Level-Shift to Inputs of DS75364

Application Hints

Applications of the DS75364 used as an interface device in systems converting TTL signals to negative polarity MOS clock signals are shown in *Figures 2 and 3*. In both applications the DS75364 V_{EE} pin is connected to a negative MOS supply voltage. The V_{CC2} supply pin may be connected to the V_{CC1} pin as shown in *Figure 3* or connected to a separate voltage more-positive than V_{CC1} as shown in *Figure 2*. The DS75364 may be used over a wide range of V_{CC1} and V_{CC2} supply voltages which are positive with respect to V_{EE}. However, for proper operation the voltage at the inputs of the DS75364 should not be more positive than the voltage at V_{CC2}.

Both applications shown require negative level shifting from positive voltage levels to the inputs of the DS75364 which are referenced to the V_{EE} terminal. A PNP transistor current source is used to level shift in *Figure 2*. Resistor R sets the current and an open-collector TTL gate is used to switch the PNP transistor. *Figure 3* shows capacitive coupling being used to level shift with the DS75361 TTL-to-MOS driver used as a low impedance voltage source driver. The value of coupling capacitor C depends on the frequency and characteristics of the signal applied to the capacitor.

The fast switching of the DS75364 may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10 and 30 ohms (*Figure 4*).

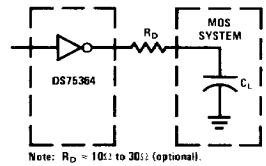


FIGURE 4. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75364 Applications