



## DS55451/2/3/4, DS75450/1/2/3/4 Series Dual Peripheral Drivers

### General Description

The DS75450 series of dual peripheral drivers is a family of versatile devices designed for use in systems that use TTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

The DS75450 is a general purpose device featuring two standard Series 54/74 TTL gates and two uncommitted, high current, high voltage NPN transistors. The device offers the system designer the flexibility of tailoring the circuit to the application.

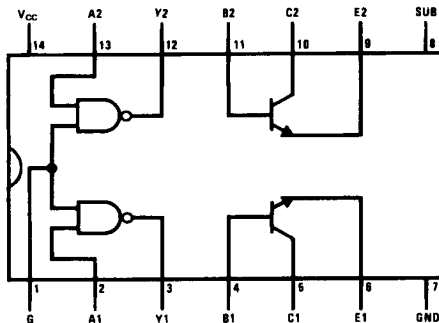
The DS55451/DS75451, DS55452/DS75452, DS55453/DS75453 and DS55454/DS75454 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic)

with the output of the logic gates internally connected to the bases of the NPN output transistors.

### Features

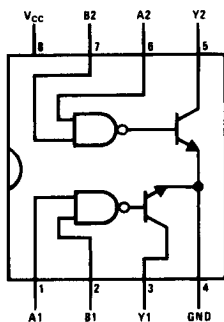
- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI "A" and "B" series

### Connection Diagrams (Dual-In-Line and Metal Can Packages)



TL/F/5824-1

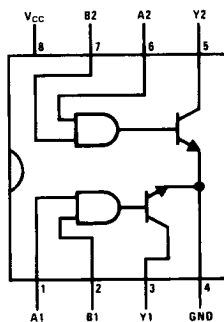
**Top View**  
**Order Number DS75450N**  
**See NS Package Number N14A**



TL/F/5824-2

**Top View**

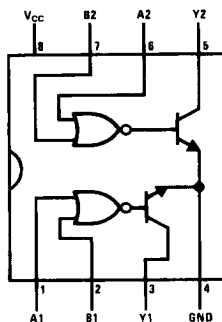
**Order Number DS55451J-8, DS75451M or DS75451N**



TL/F/5824-3

**Top View**

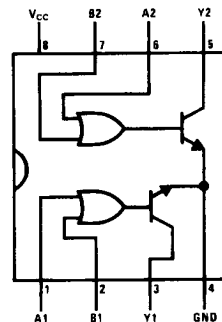
**Order Number DS55452J-8, DS75452M or DS75452N**



TL/F/5824-4

**Top View**

**Order Number DS55453J-8, DS75453M or DS75453N**



TL/F/5824-5

**Top View**

**Order Number DS55454J-8, DS75454M or DS75454N**

**See NS Package Numbers J08A, M08A\* or N08E**

\*See Note 6 and Appendix E regarding S.O. package power dissipation constraints.

DS55451/DS55452/DS55453/DS55454/DS75450/DS75451/DS75452/DS75453/DS75454

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                                                                                  |        |
|--------------------------------------------------------------------------------------------------|--------|
| Supply Voltage, ( $V_{CC}$ ) (Note 2)                                                            | 7.0V   |
| Input Voltage                                                                                    | 5.5V   |
| Inter-Emitter Voltage (Note 3)                                                                   | 5.5V   |
| $V_{CC}$ -to-Substrate Voltage<br>DS75450                                                        | 35V    |
| Collector-to-Substrate Voltage<br>DS75450                                                        | 35V    |
| Collector-Base Voltage<br>DS75450                                                                | 35V    |
| Collector-Emitter Voltage (Note 4)<br>DS75450                                                    | 30V    |
| Emitter-Base Voltage<br>DS75450                                                                  | 5.0V   |
| Output Voltage (Note 5)<br>DS55451/DS75451, DS55452/DS75452,<br>DS55453/DS75453, DS55454/DS75454 | 30V    |
| Collector Current (Note 6)<br>DS75450                                                            | 300 mA |
| Output Current (Note 6)<br>DS55451/DS75451, DS55452/DS75452,<br>DS55453/DS75453, DS55454/DS75454 | 300 mA |

## DS75450 Maximum Power (Note 6)

|                      |         |
|----------------------|---------|
| Dissipation* at 25°C |         |
| Cavity Package       | 1308 mW |
| Molded Package       | 1207 mW |

## DS75451/2/3/4 Maximum Power (Note 6)

|                      |         |
|----------------------|---------|
| Dissipation† at 25°C |         |
| Cavity Package       | 1090 mW |
| Molded DIP Package   | 957 mW  |
| TO-5 Package         | 760 mW  |
| SO Package           | 632 mW  |

|                                      |                 |
|--------------------------------------|-----------------|
| Storage Temperature Range            | -65°C to +150°C |
| Lead Temperature (Soldering, 4 sec.) | 260°C           |

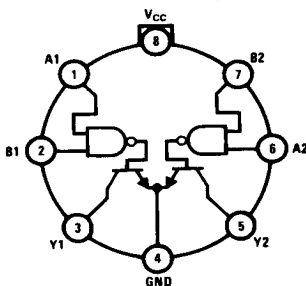
## Operating Conditions (Note 7)

|                              | Min  | Max  | Units |
|------------------------------|------|------|-------|
| Supply Voltage, ( $V_{CC}$ ) |      |      |       |
| DS5545X                      | 4.5  | 5.5  | V     |
| DS7545X                      | 4.75 | 5.25 | V     |
| Temperature, ( $T_A$ )       |      |      |       |
| DS5545X                      | -55  | +125 | °C    |
| DS7545X                      | 0    | +70  | °C    |

\*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

†Derate cavity package 7.3 mW/°C above 25°C; derate molded package 7.7 mW/°C above 25°C; derate TO-5 package 5.1 mW/°C above 25°C; derate SO package 7.56 mW/°C above 25°C.

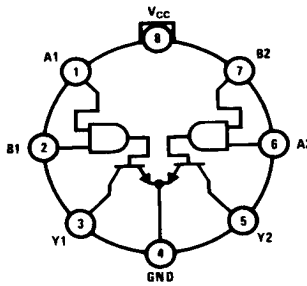
## Connection Diagrams (Dual-In-Line and Metal Can Packages) (Continued)



TL/F/5824-6

Top View

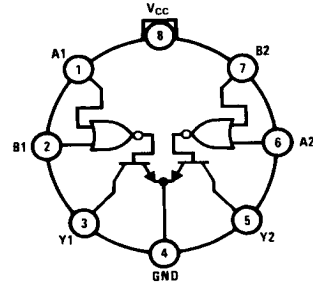
Order Number DS55451H



TL/F/5824-7

Top View

Order Number DS55452H



TL/F/5824-8

Top View

Order Number DS55453H

See NS Package Number H08C

## Electrical Characteristics DS75450 (Notes 8 and 9)

| Symbol           | Parameter                              | Conditions                                                                                  | Min | Typ  | Max  | Units |
|------------------|----------------------------------------|---------------------------------------------------------------------------------------------|-----|------|------|-------|
| <b>TTL GATES</b> |                                        |                                                                                             |     |      |      |       |
| $V_{IH}$         | High Level Input Voltage               | (Figure 1)                                                                                  | 2   |      |      | V     |
| $V_{IL}$         | Low Level Input Voltage                | (Figure 2)                                                                                  |     |      | 0.8  | V     |
| $V_I$            | Input Clamp Voltage                    | $V_{CC} = \text{Min}$ , $I_I = -12 \text{ mA}$ , (Figure 3)                                 |     |      | -1.5 | V     |
| $V_{OH}$         | High Level Output Voltage              | $V_{CC} = \text{Min}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = -400 \mu\text{A}$ , (Figure 2) | 2.4 | 3.3  |      | V     |
| $V_{OL}$         | Low Level Output Voltage               | $V_{CC} = \text{Min}$ , $V_{IH} = 2 \text{ V}$ , $I_{OL} = 16 \text{ mA}$ (Figure 1)        |     | 0.22 | 0.4  | V     |
| $I_I$            | Input Current at Maximum Input Voltage | $V_{CC} = \text{Max}$ , $V_I = 5.5 \text{ V}$ , (Figure 4)                                  |     |      |      |       |
|                  |                                        | Input A                                                                                     |     |      | 1    | mA    |
|                  |                                        | Input G                                                                                     |     |      | 2    | mA    |

**Electrical Characteristics** DS75450 (Notes 8 and 9) (Continued)

| Symbol                       | Parameter                    | Conditions                                                              | Min | Typ | Max  | Units   |
|------------------------------|------------------------------|-------------------------------------------------------------------------|-----|-----|------|---------|
| <b>TTL GATES</b> (Continued) |                              |                                                                         |     |     |      |         |
| $I_{IH}$                     | High Level Input Current     | $V_{CC} = \text{Max}, V_I = 2.4V, \text{(Figure 4)}$                    |     |     | 40   | $\mu A$ |
|                              |                              |                                                                         |     |     | 80   | $\mu A$ |
| $I_{IL}$                     | Low Level Input Current      | $V_{CC} = \text{Max}, V_I = 0.4V, \text{(Figure 3)}$                    |     |     | -1.6 | mA      |
|                              |                              |                                                                         |     |     | -3.2 | mA      |
| $I_{OS}$                     | Short Circuit Output Current | $V_{CC} = \text{Max}, \text{(Figure 5)}, \text{(Note 10)}$              | -18 |     | -55  | mA      |
| $I_{CCH}$                    | Supply Current               | $V_{CC} = \text{Max}, V_I = 0V, \text{Outputs High}, \text{(Figure 6)}$ |     | 2   | 4    | mA      |
| $I_{CCL}$                    | Supply Current               | $V_{CC} = \text{Max}, V_I = 5V, \text{Outputs Low}, \text{(Figure 6)}$  |     | 6   | 11   | mA      |

**OUTPUT TRANSISTORS**

|               |                                       |                                       |                     |                                             |      |     |   |
|---------------|---------------------------------------|---------------------------------------|---------------------|---------------------------------------------|------|-----|---|
| $V_{(BR)CBO}$ | Collector-Base Breakdown Voltage      | $I_C = 100 \mu A, I_E = 0 \mu A$      |                     | 35                                          |      |     | V |
| $V_{(BR)CER}$ | Collector-Emitter Breakdown Voltage   | $I_C = 100 \mu A, R_{BE} = 500\Omega$ |                     | 30                                          |      |     | V |
| $V_{(BR)EBO}$ | Emitter-Base Breakdown Voltage        | $I_E = 100 \mu A, I_C = 0 \mu A$      |                     | 5                                           |      |     | V |
| $h_{FE}$      | Static Forward Current Transfer Ratio | $V_{CE} = 3V, \text{(Note 11)}$       | $T_A = +25^\circ C$ | $I_C = 100 \text{ mA}$                      | 25   |     |   |
|               |                                       |                                       |                     | $I_C = 300 \text{ mA}$                      | 30   |     |   |
|               |                                       | $T_A = 0^\circ C$                     |                     | $I_C = 100 \text{ mA}$                      | 20   |     |   |
|               |                                       |                                       |                     | $I_C = 300 \text{ mA}$                      | 25   |     |   |
| $V_{BE}$      | Base-Emitter Voltage                  | $\text{(Note 11)}$                    |                     | $I_B = 10 \text{ mA}, I_C = 100 \text{ mA}$ | 0.85 | 1   | V |
|               |                                       |                                       |                     | $I_B = 30 \text{ mA}, I_C = 300 \text{ mA}$ | 1.05 | 1.2 | V |
| $V_{CE(SAT)}$ | Collector-Emitter Saturation Voltage  | $\text{(Note 11)}$                    |                     | $I_B = 10 \text{ mA}, I_C = 100 \text{ mA}$ | 0.25 | 0.4 | V |
|               |                                       |                                       |                     | $I_B = 30 \text{ mA}, I_C = 300 \text{ mA}$ | 0.5  | 0.7 | V |

**Electrical Characteristics** (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 8 and 9)

| Symbol          | Parameter                              | Conditions                                               |                        |                          |                  | Min | Typ  | Max  | Units |
|-----------------|----------------------------------------|----------------------------------------------------------|------------------------|--------------------------|------------------|-----|------|------|-------|
| V <sub>IH</sub> | High-Level Input Voltage               | (Figure 7)                                               |                        |                          |                  | 2   |      |      | V     |
| V <sub>IL</sub> | Low-Level Input Voltage                |                                                          |                        |                          |                  |     |      | 0.8  | V     |
| V <sub>I</sub>  | Input Clamp Voltage                    | V <sub>CC</sub> = Min, I <sub>I</sub> = −12 mA           |                        |                          |                  |     |      | −1.5 | V     |
| V <sub>OL</sub> | Low-Level Output Voltage               | V <sub>CC</sub> = Min,<br>(Figure 7)                     | V <sub>IL</sub> = 0.8V | I <sub>OL</sub> = 100 mA | DS55451, DS55453 |     | 0.25 | 0.5  | V     |
|                 |                                        |                                                          |                        |                          | DS75451, DS75453 |     | 0.25 | 0.4  | V     |
|                 |                                        |                                                          |                        | I <sub>OL</sub> = 300 mA | DS55451, DS55453 |     | 0.5  | 0.8  | V     |
|                 |                                        |                                                          |                        |                          | DS75451, DS75453 |     | 0.5  | 0.7  | V     |
|                 |                                        |                                                          | V <sub>IH</sub> = 2V   | I <sub>OL</sub> = 100 mA | DS55452, DS55454 |     | 0.25 | 0.5  | V     |
|                 |                                        |                                                          |                        |                          | DS75452, DS75454 |     | 0.25 | 0.4  | V     |
|                 |                                        |                                                          |                        | I <sub>OL</sub> = 300 mA | DS55452, DS55454 |     | 0.5  | 0.8  | V     |
|                 |                                        |                                                          |                        |                          | DS75452, DS75454 |     | 0.5  | 0.7  | V     |
| I <sub>OH</sub> | High-Level Output Current              | V <sub>CC</sub> = Min,<br>(Figure 7)                     | V <sub>OH</sub> = 30V  | V <sub>IH</sub> = 2V     | DS55451, DS55453 |     |      | 300  | μA    |
|                 |                                        |                                                          |                        |                          | DS75451, DS75453 |     |      | 100  | μA    |
|                 |                                        |                                                          |                        | V <sub>IL</sub> = 0.8V   | DS55452, DS55454 |     |      | 300  | μA    |
|                 |                                        |                                                          |                        |                          | DS75452, DS75454 |     |      | 100  | μA    |
|                 |                                        |                                                          |                        |                          |                  |     |      |      |       |
| I <sub>I</sub>  | Input Current at Maximum Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V, (Figure 9) |                        |                          |                  |     |      | 1    | mA    |

**Electrical Characteristics** (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 8 and 9) (Continued)

| Symbol    | Parameter                                   | Conditions                                               | Min             | Typ | Max  | Units         |
|-----------|---------------------------------------------|----------------------------------------------------------|-----------------|-----|------|---------------|
| $I_{IH}$  | High-Level Input Current                    | $V_{CC} = \text{Max}$ , $V_I = 2.4\text{V}$ , (Figure 9) |                 |     | 40   | $\mu\text{A}$ |
| $I_{IL}$  | Low-Level Input Current                     | $V_{CC} = \text{Max}$ , $V_I = 0.4\text{V}$ , (Figure 8) |                 | -1  | -1.6 | mA            |
| $I_{CCH}$ | Supply Current, Outputs High<br>(Figure 10) | $V_{CC} = \text{Max}$ ,<br>$V_I = 5\text{V}$             | DS55451/DS75451 | 7   | 11   | mA            |
|           |                                             | $V_I = 0\text{V}$                                        | DS55452/DS75452 | 11  | 14   | mA            |
|           |                                             | $V_I = 5\text{V}$                                        | DS55453/DS75453 | 8   | 11   | mA            |
|           |                                             | $V_I = 0\text{V}$                                        | DS55454/DS75454 | 13  | 17   | mA            |
| $I_{CCL}$ | Supply Current, Outputs Low<br>(Figure 10)  | $V_{CC} = \text{Max}$ ,<br>$V_I = 0\text{V}$             | DS55451/DS75451 | 52  | 65   | mA            |
|           |                                             | $V_I = 5\text{V}$                                        | DS55452/DS75452 | 56  | 71   | mA            |
|           |                                             | $V_I = 0\text{V}$                                        | DS55453/DS75453 | 54  | 68   | mA            |
|           |                                             | $V_I = 5\text{V}$                                        | DS55454/DS75454 | 61  | 79   | mA            |

**Switching Characteristics** DS75450 ( $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ )

| Symbol    | Parameter                                        | Conditions                                                                                                                                                                         | Min         | Typ | Max | Units |
|-----------|--------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-----|-----|-------|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_L = 15\text{ pF}$ , $R_L = 400\Omega$ , TTL Gates, (Figure 12)<br>$R_L = 50\Omega$ , $I_C \approx 200\text{ mA}$ , Gates and Transistors Combined, (Figure 14)                  |             | 12  | 22  | ns    |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | $C_L = 15\text{ pF}$ , $R_L = 400\Omega$ , TTL Gates, (Figure 12)<br>$R_L = 50\Omega$ , $I_C \approx 200\text{ mA}$ , Gates and Transistors Combined, (Figure 14)                  |             | 8   | 15  | ns    |
| $t_{TLH}$ | Transition Time, Low-to-High Level Output        | $C_L = 15\text{ pF}$ , $R_L = 50\Omega$ , $I_C \approx 200\text{ mA}$ , Gates and Transistors Combined, (Figure 14)                                                                |             | 7   | 12  | ns    |
| $t_{THL}$ | Transition Time, High-to-Low Level Output        | $C_L = 15\text{ pF}$ , $R_L = 50\Omega$ , $I_C \approx 200\text{ mA}$ , Gates and Transistors Combined, (Figure 14)                                                                |             | 9   | 15  | ns    |
| $V_{OH}$  | High-Level Output Voltage after Switching        | $V_S = 20\text{V}$ , $I_C \approx 300\text{ mA}$ , $R_{BE} = 500\Omega$ , (Figure 15)                                                                                              | $V_S - 6.5$ |     |     | mV    |
| $t_D$     | Delay Time                                       | $I_C = 200\text{ mA}$ , $I_{B(1)} = 20\text{ mA}$ ,<br>$I_B = -40\text{ mA}$ , $V_{BE(OFF)} = -1\text{V}$ ,<br>$C_L = 15\text{ pF}$ , $R_L = 50\Omega$ ,<br>(Figure 13), (Note 12) |             | 8   | 15  | ns    |
| $t_R$     | Rise Time                                        |                                                                                                                                                                                    |             | 12  | 20  | ns    |
| $t_S$     | Storage Time                                     |                                                                                                                                                                                    |             | 7   | 15  | ns    |
| $t_F$     | Full Time                                        |                                                                                                                                                                                    |             | 6   | 15  | ns    |

**Switching Characteristics** (Continued)DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 ( $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ )

| Symbol    | Parameter                                        | Conditions                                                                             | Min             | Typ | Max | Units |
|-----------|--------------------------------------------------|----------------------------------------------------------------------------------------|-----------------|-----|-----|-------|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_L = 15\text{ pF}$ , $R_L = 50\Omega$ ,<br>$I_O \approx 200\text{ mA}$ , (Figure 14) | DS55451/DS75451 | 18  | 25  | ns    |
|           |                                                  |                                                                                        | DS55452/DS75452 | 26  | 35  | ns    |
|           |                                                  |                                                                                        | DS55453/DS75453 | 18  | 25  | ns    |
|           |                                                  |                                                                                        | DS55454/DS75454 | 27  | 35  | ns    |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | $C_L = 15\text{ pF}$ , $R_L = 50\Omega$ ,<br>$I_O \approx 200\text{ mA}$ , (Figure 14) | DS55451/DS75451 | 18  | 25  | ns    |
|           |                                                  |                                                                                        | DS55452/DS75452 | 24  | 35  | ns    |
|           |                                                  |                                                                                        | DS55453/DS75453 | 16  | 25  | ns    |
|           |                                                  |                                                                                        | DS55454/DS75454 | 24  | 35  | ns    |
| $t_{TLH}$ | Transition Time, Low-to-High Level Output        | $C_L = 15\text{ pF}$ , $R_L = 50\Omega$ , $I_O \approx 200\text{ mA}$ ,<br>(Figure 14) |                 | 5   | 8   | ns    |
| $t_{THL}$ | Transition Time, High-to-Low Level Output        | $C_L = 15\text{ pF}$ , $R_L = 50\Omega$ , $I_O \approx 200\text{ mA}$ ,<br>(Figure 14) |                 | 7   | 12  | ns    |
| $V_{OH}$  | High-Level Output Voltage after Switching        | $V_S = 20\text{V}$ , $I_O \approx 300\text{ mA}$ , (Figure 15)                         | $V_S - 6.5$     |     |     | mV    |

## Switching Characteristics (Continued)

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Voltage values are with respect to network ground terminal unless otherwise specified.

**Note 3:** The voltage between two emitters of a multiple-emitter transistor.

**Note 4:** Value applies when the base-emitter resistance ( $R_{BE}$ ) is equal to or less than 500 $\Omega$ .

**Note 5:** The maximum voltage which should be applied to any output when it is in the "OFF" state.

**Note 6:** Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

**Note 7:** For the DS75450 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

**Note 8:** Unless otherwise specified min/max limits apply across the  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range for the DS55450 series and across the  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  range for the DS75450 series. All typicals are given for  $V_{CC} = +5\text{V}$  and  $T_A = 25^{\circ}\text{C}$ .

**Note 9:** All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

**Note 10:** Only one output at a time should be shorted.

**Note 11:** These parameters must be measured using pulse techniques.  $t_W = 300\text{ }\mu\text{s}$ , duty cycle  $< 2\%$ .

**Note 12:** Applies to output transistors only.

## Truth Tables (H = high level, L = low level)

DS55451/DS75451

| A | B | Y             |
|---|---|---------------|
| L | L | L (ON State)  |
| L | H | L (ON State)  |
| H | L | L (ON State)  |
| H | H | H (OFF State) |

DS55453/DS75453

| A | B | Y             |
|---|---|---------------|
| L | L | L (ON State)  |
| L | H | H (OFF State) |
| H | L | H (OFF State) |
| H | H | H (OFF State) |

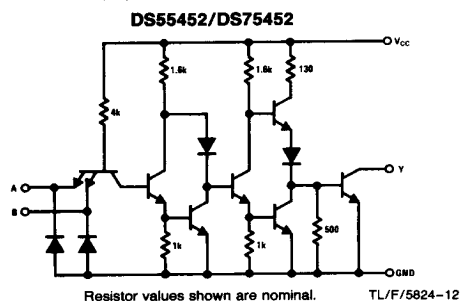
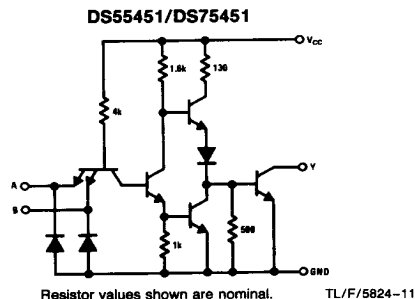
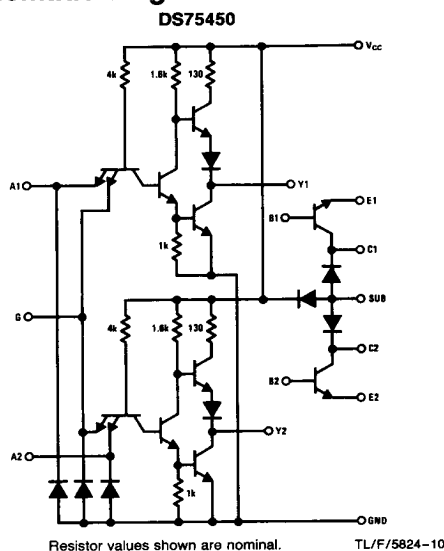
DS55452/DS75452

| A | B | Y             |
|---|---|---------------|
| L | L | H (OFF State) |
| L | H | H (OFF State) |
| H | L | H (OFF State) |
| H | H | L (ON State)  |

DS55454/DS75454

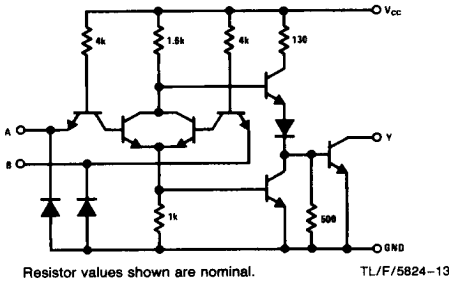
| A | B | Y             |
|---|---|---------------|
| L | L | H (OFF State) |
| L | H | L (ON State)  |
| H | L | L (ON State)  |
| H | H | L (ON State)  |

## Schematic Diagrams

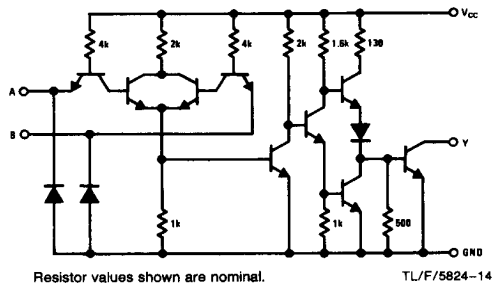


## Schematic Diagrams (Continued)

DS55453/DS75453



DS55454/DS75454



## DC Test Circuits

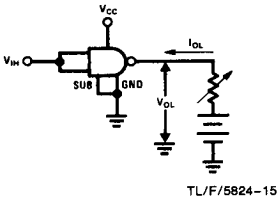


FIGURE 1.  $V_{IH}$ ,  $V_{OL}$

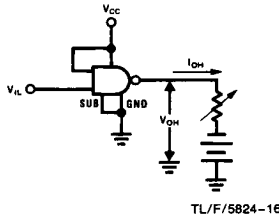


FIGURE 2.  $V_{IL}$ ,  $V_{OH}$

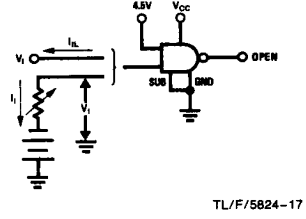


FIGURE 3.  $V_I$ ,  $I_{IL}$

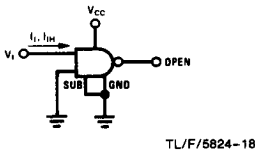


FIGURE 4.  $I_I$ ,  $I_{IH}$

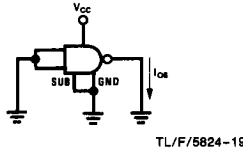


FIGURE 5.  $I_{OS}$

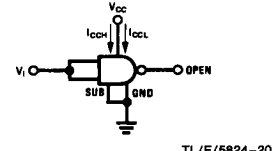


FIGURE 6.  $I_{CCH}$ ,  $I_{CCL}$

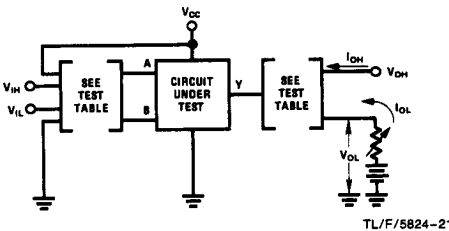
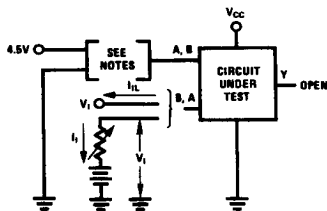


FIGURE 7.  $V_{IH}$ ,  $V_{IL}$ ,  $I_{OH}$ ,  $V_{OL}$

| Circuit | Input Under Test | Other Input | Output   |          |
|---------|------------------|-------------|----------|----------|
|         |                  |             | Apply    | Measure  |
| DS55451 | $V_{IH}$         | $V_{IH}$    | $V_{OH}$ | $I_{OH}$ |
|         | $V_{IL}$         | $V_{CC}$    | $I_{OL}$ | $V_{OL}$ |
| DS55452 | $V_{IH}$         | $V_{IH}$    | $I_{OL}$ | $V_{OL}$ |
|         | $V_{IL}$         | $V_{CC}$    | $V_{OH}$ | $I_{OH}$ |
| DS55453 | $V_{IH}$         | Gnd         | $V_{OH}$ | $I_{OH}$ |
|         | $V_{IL}$         | $V_{IL}$    | $I_{OL}$ | $V_{OH}$ |
| DS55454 | $V_{IH}$         | Gnd         | $I_{OL}$ | $V_{OL}$ |
|         | $V_{IL}$         | $V_{IL}$    | $V_{OH}$ | $I_{OH}$ |

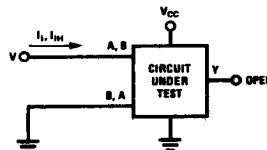
## DC Test Circuits (Continued)



**Note A:** Each input is tested separately.  
**Note B:** When testing DS55453/DS75453, DS55454/DS75454, input not under test is grounded.  
 For all other circuits it is at 4.5V.

TL/F/5824-22

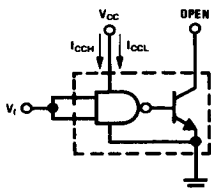
**FIGURE 8.  $V_I$ ,  $V_{IL}$**



Each input is tested separately.

TL/F/5824-23

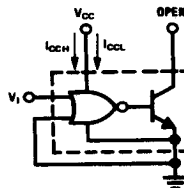
**FIGURE 9.  $I_I$ ,  $I_{IH}$**



Both gates are tested simultaneously.

TL/F/5824-24

**FIGURE 10.  $I_{OCH}$ ,  $I_{OCL}$  for AND, NAND Circuits**

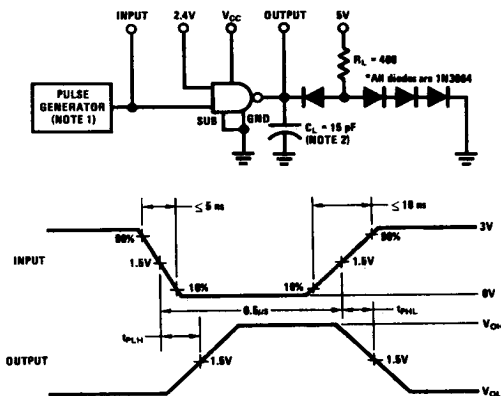


Both gates are tested simultaneously.

TL/F/5824-25

**FIGURE 11.  $I_{OCH}$ ,  $I_{OCL}$  for OR, NOR Circuits**

## AC Test Circuits and Switching Time Waveforms



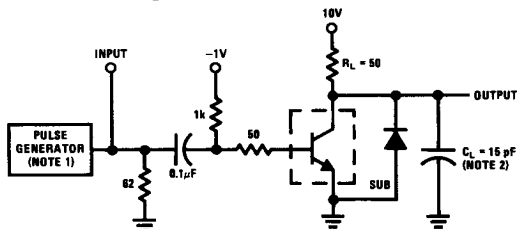
TL/F/5824-26

**Note 1:** The pulse generator has the following characteristics: PRR = 1 MHz,  $Z_{OUT} \approx 50\Omega$ .

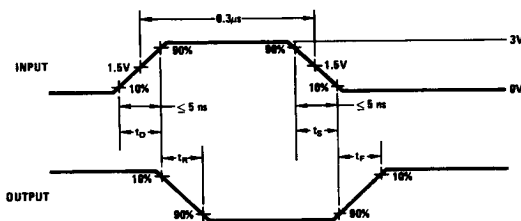
**Note 2:**  $C_L$  includes probe and jig capacitance.

**FIGURE 12. Propagation Delay Times, Each Gate (DS75450 Only)**

# AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5824-28

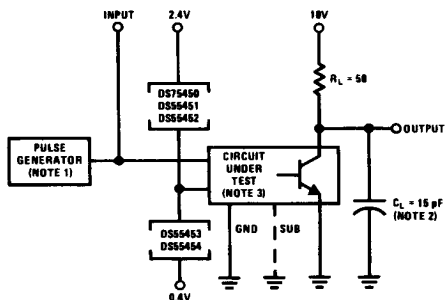


TL/F/5824-29

**Note 1:** The pulse generator has the following characteristics: duty cycle  $\leq 1\%$ ,  $Z_{OUT} \approx 50\Omega$ .

**Note 2:**  $C_L$  includes probe and jig capacitance.

**FIGURE 13. Switching Times, Each Transistor (DS75450 Only)**

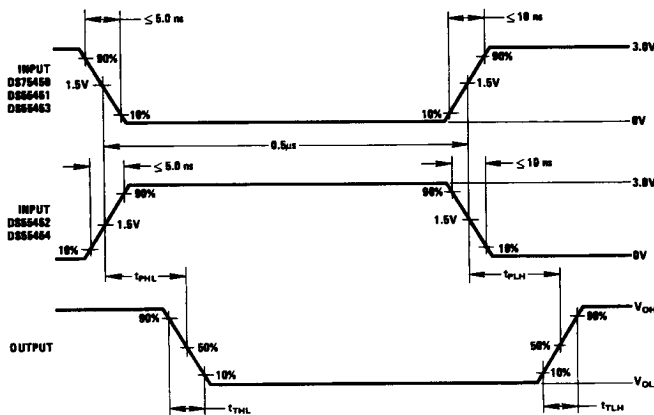


TL/F/5824-30

**Note 1:** The pulse generator has the following characteristics: PRR = 1.0 MHz,  $Z_{OUT} \approx 50\Omega$ .

**Note 2:**  $C_L$  includes probe and jig capacitance.

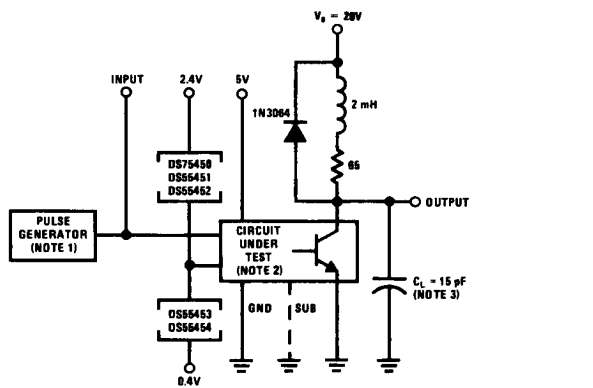
**Note 3:** When testing DS75450, connect output V to transistor base and ground the substrate terminal.



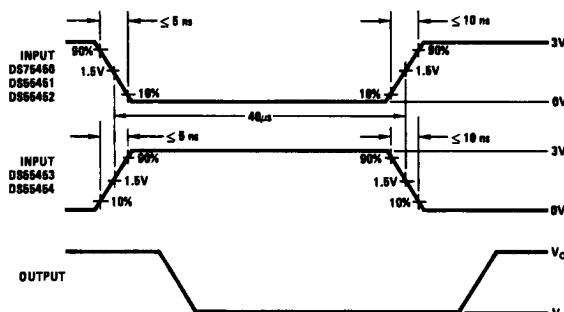
TL/F/5824-31

**FIGURE 14. Switching Times of Complete Drivers**

# AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5824-32



Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz,  $Z_{OUT} \approx 50\Omega$ .

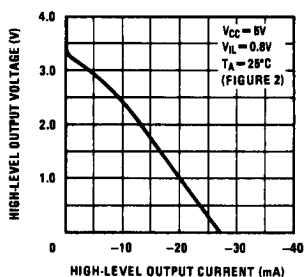
TL/F/5824-33

Note 2: When testing DS75450, connect output V to transistor base with a  $600\Omega$  resistor from there to ground and ground the substrate terminal.

Note 3:  $C_L$  includes probe and jig capacitance.

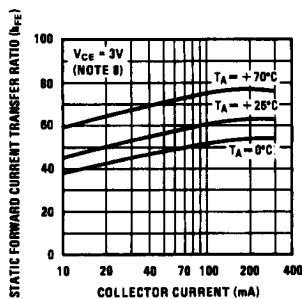
FIGURE 15. Latch-UP Test of Complete Drivers

## Typical Performance Characteristics



TL/F/5824-34

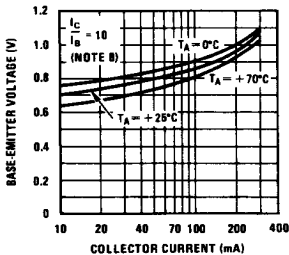
FIGURE 16. DS75450 TTL Gate High-Level Output Voltage vs High-Level Output Current



TL/F/5824-35

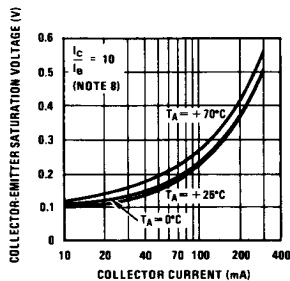
FIGURE 17. DS75450 Transistor Static Forward Current Transfer Ratio vs Collector Current

## Typical Performance Characteristics (Continued)



TL/F/5824-36

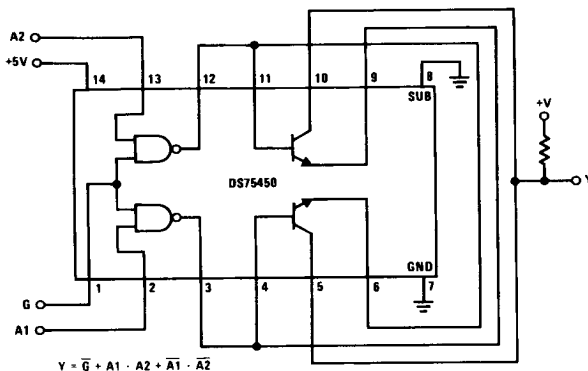
FIGURE 18. DS75450 Transistor Base-Emitter Voltage vs Collector Current



TL/F/5824-37

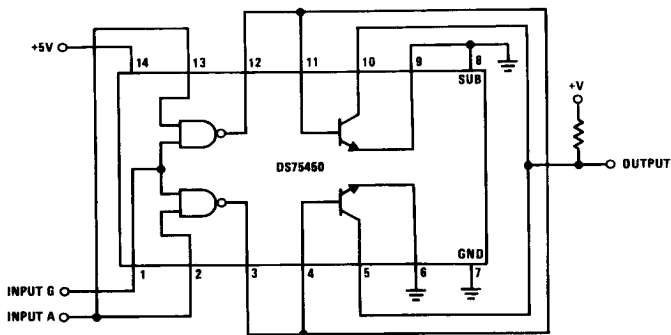
FIGURE 19. Transistor Collector-Emitter Saturation Voltage vs Collector Current

## Typical Applications



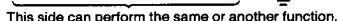
TL/F/5824-38

FIGURE 20. Gated Comparator

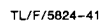


TL/F/5824-39

FIGURE 21. 500 mA Sink



TL/F/5824-40

[illegible]

TL/F/5824-42

# Typical Applications (Continued)

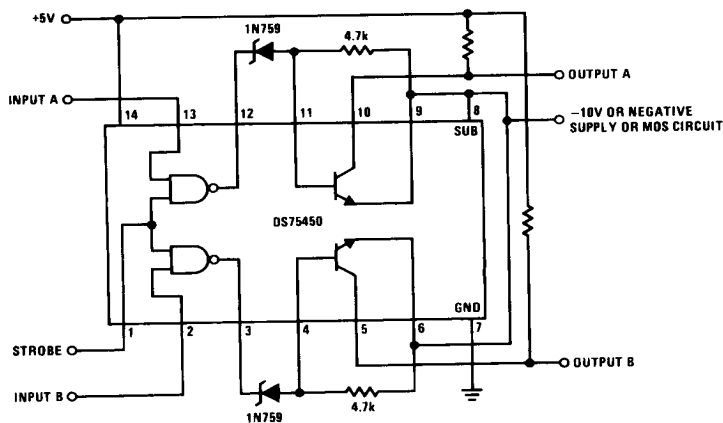


FIGURE 25. Dual TTL-to-MOS Driver

TL/F/5824-43

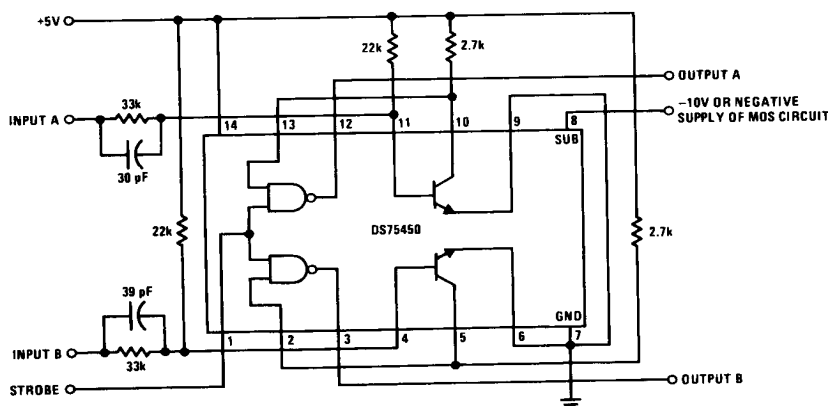


FIGURE 26. Dual MOS-to-TTL Driver

TL/F/5824-44

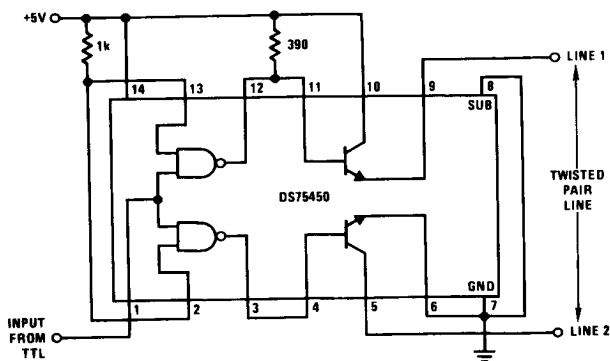


FIGURE 27. Balanced Line Driver

TL/F/5824-45

Termination is made at the receiving end as follows:  
 Line 1 is terminated to ground through  $Z_0/Z$ ;  
 Line 2 is terminated to +5V through  $Z_0/Z$ ;  
 where  $Z_0$  is the line impedance.

## Typical Applications (Continued)

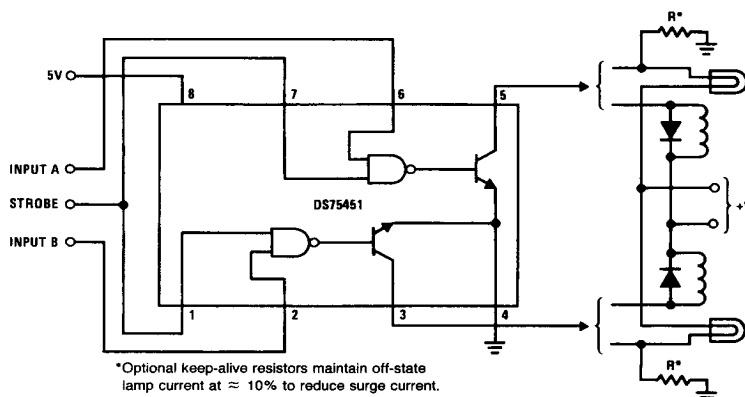


FIGURE 28. Dual Lamp or Relay Driver

TL/F/5824-46

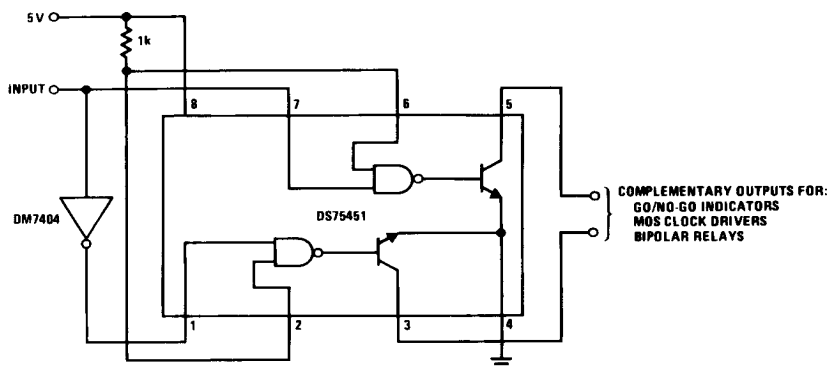


FIGURE 29. Complementary Driver

TL/F/5824-47

## Typical Applications (Continued)

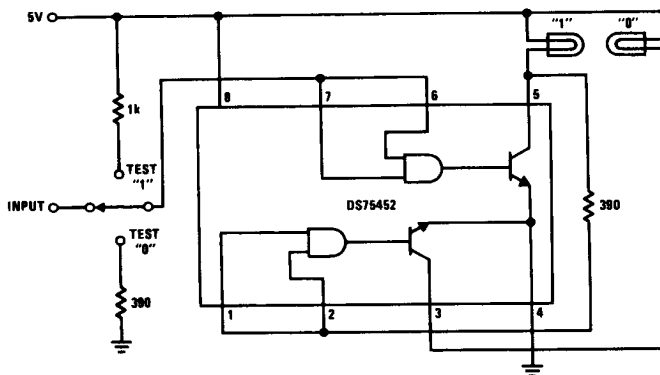
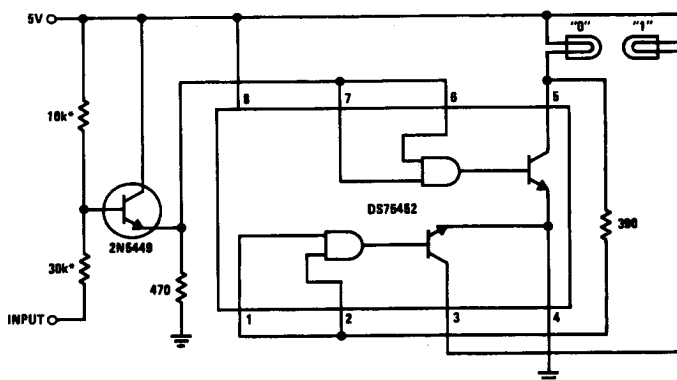


FIGURE 30. TTL or DTL Positive Logic-Level Detector

TL/F/5824-48



\*The two input resistors must be adjusted for the level of MOS input.

FIGURE 31. MOS Negative Logic-Level Detector

TL/F/5824-49

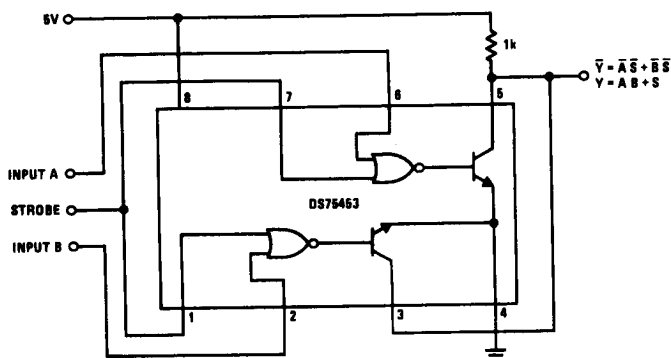
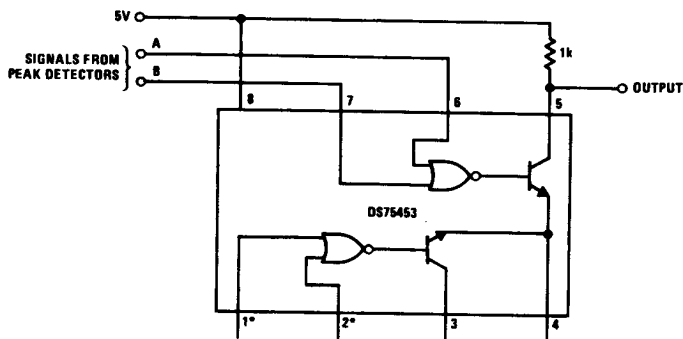


FIGURE 32. Logic Signal Comparator

TL/F/5824-50

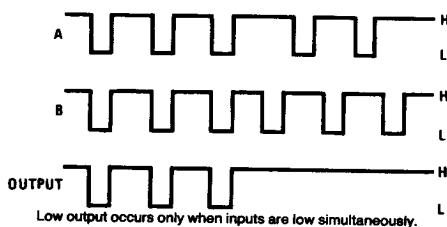
DS55451/DS55452/DS55453/DS55454/DS75450/DS75451/DS75452/DS75453/DS75454

# Typical Applications (Continued)



\*If inputs are unused, they should be connected to +5V through a 1k resistor.

TL/F/5824-51



TL/F/5824-52

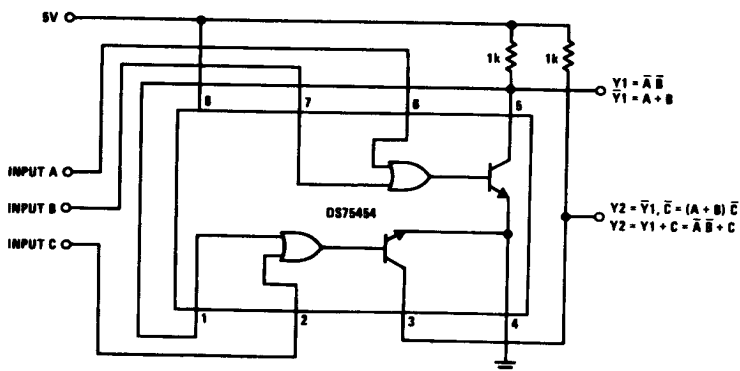


FIGURE 34. Multifunction Logic-Signal Comparator

TL/F/5824-53

