National Semiconductor

# DS55451/2/3/4, DS75451/2/3/4 Series Dual Peripheral Drivers

## General Description

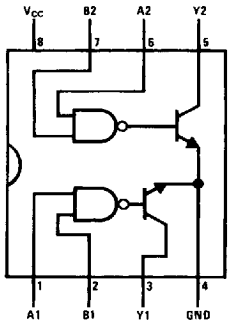
The DS7545X series of dual peripheral drivers is a family of versatile devices designed for use in systems that use TTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

The DS55451/DS75451, DS55452/DS75452, DS55453/DS75453 and DS55454/DS75454 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

## Features

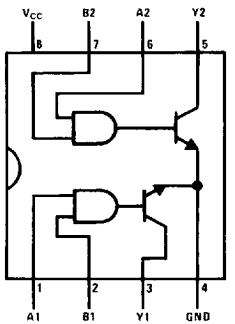
- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI "A" and "B" series

## Connection Diagrams (Dual-In-Line and Metal Can Packages)



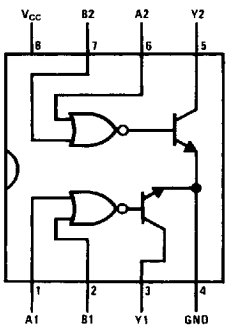

TL/F/5824–2

**Top View**
**Order Number DS55451J-8, DS75451M or DS75451N**



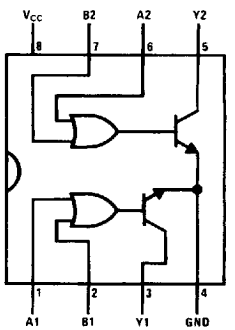

TL/F/5824–3

**Top View**
**Order Number DS55452J-8, DS75452M or DS75452N**




TL/F/5824–4

**Top View**
**Order Number DS55453J-8, DS75453M or DS75453N**

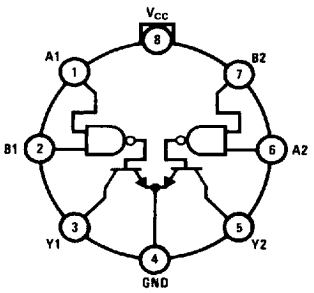



TL/F/5824–5

**Top View**
**Order Number DS55454J-8, DS75454M or DS75454N**

**See NS Package Numbers J08A, M08A* or N08E**

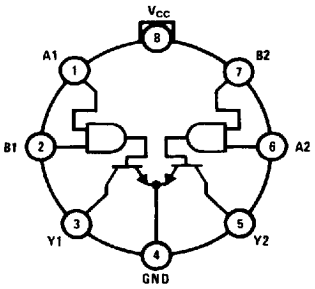
*See Note 5 and Appendix E regarding S.O. package power dissipation constraints.




TL/F/5824–6

**Top View**

**Order Number DS55451H**

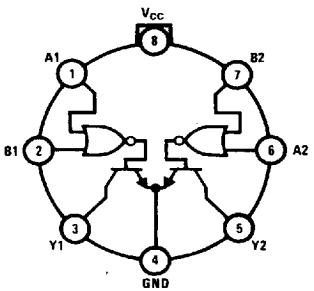



TL/F/5824–7

**Top View**

(Pin 4 is in Electrical Contact with the Case)

**Order Number DS55452H**




TL/F/5824–8

**Top View**

**Order Number DS55453H**

**See NS Package Number H08C**

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage, ($V_{CC}$) (Note 2) | 7.0V |
| Input Voltage | 5.5V |
| Inter-Emitter Voltage (Note 3) | 5.5V |
| Output Voltage (Note 4) DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 | 30V |
| Output Current (Note 5) DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 | 300 mA |
| DS75451/2/3/4 Maximum Power (Note 5) Dissipation† at 25°C | |
| Cavity Package | 1090 mW |
| Molded DIP Package | 957 mW |
| TO-5 Package | 760 mW |
| SO Package | 632 mW |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 4 sec.) | 260°C |

## Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage, ($V_{CC}$) | | | |
| DS5545X | 4.5 | 5.5 | V |
| DS7545X | 4.75 | 5.25 | V |
| Temperature, ($T_A$) | | | |
| DS5545X | −55 | +125 | °C |
| DS7545X | 0 | +70 | °C |

† Derate cavity package 7.3 mW/°C above 25°C; derate molded package 7.7 mW/°C above 25°C; derate TO-5 package 5.1 mW/°C above 25°C; derate SO package 7.56 mW/°C above 25°C.

## Electrical Characteristics

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 6 and 7)

| Symbol | Parameter | Conditions | | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-Level Input Voltage | *(Figure 7)* | | | | 2 | | | V |
| $V_{IL}$ | Low-Level Input Voltage | | | | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | | | −1.5 | V |
| $V_{OL}$ | Low-Level Output Voltage | $V_{CC}$ = Min, *(Figure 7)* | $V_{IL}$ = 0.8V | $I_{OL}$ = 100 mA | DS55451, DS55453 | | 0.25 | 0.5 | V |
| | | | | | DS75451, DS75453 | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$ = 300 mA | DS55451, DS55453 | | 0.5 | 0.8 | V |
| | | | | | DS75451, DS75453 | | 0.5 | 0.7 | V |
| | | | $V_{IH}$ = 2V | $I_{OL}$ = 100 mA | DS55452, DS55454 | | 0.25 | 0.5 | V |
| | | | | | DS75452, DS75454 | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$ = 300 mA | DS55452, DS55454 | | 0.5 | 0.8 | V |
| | | | | | DS75452, DS75454 | | 0.5 | 0.7 | V |
| $I_{OH}$ | High-Level Output Current | $V_{CC}$ = Min, *(Figure 7)* | $V_{OH}$ = 30V | $V_{IH}$ = 2V | DS55451, DS55453 | | | 300 | μA |
| | | | | | DS75451, DS75453 | | | 100 | μA |
| | | | | $V_{IL}$ = 0.8V | DS55452, DS55454 | | | 300 | μA |
| | | | | | DS75452, DS75454 | | | 100 | μA |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5V, *(Figure 9)* | | | | | | 1 | mA |
| $I_{IH}$ | High-Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4V, *(Figure 9)* | | | | | | 40 | μA |
| $I_{IL}$ | Low-Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4V, *(Figure 8)* | | | | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply Current, Outputs High | $V_{CC}$ = Max, *(Figure 10)* | $V_I$ = 5V | | DS55451/DS75451 | | 7 | 11 | mA |
| | | | $V_I$ = 0V | | DS55452/DS75452 | | 11 | 14 | mA |
| | | | $V_I$ = 5V | | DS55453/DS75453 | | 8 | 11 | mA |
| | | | $V_I$ = 0V | | DS55454/DS75454 | | 13 | 17 | mA |
| $I_{CCL}$ | Supply Current, Outputs Low | $V_{CC}$ = Max, *(Figure 10)* | $V_I$ = 0V | | DS55451/DS75451 | | 52 | 65 | mA |
| | | | $V_I$ = 5V | | DS55452/DS75452 | | 56 | 71 | mA |
| | | | $V_I$ = 0V | | DS55453/DS75453 | | 54 | 68 | mA |
| | | | $V_I$ = 5V | | DS55454/DS75454 | | 61 | 79 | mA |

## Switching Characteristics

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 ($V_{CC}$ = 5V, $T_A$ = 25°C)

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $C_L$ = 15 pF, $R_L$ = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)* | DS55451/DS75451 | | 18 | 25 | ns |
| | | | DS55452/DS75452 | | 26 | 35 | ns |
| | | | DS55453/DS75453 | | 18 | 25 | ns |
| | | | DS55454/DS75454 | | 27 | 35 | ns |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output | $C_L$ = 15 pF, $R_L$ = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)* | DS55451/DS75451 | | 18 | 25 | ns |
| | | | DS55452/DS75452 | | 24 | 35 | ns |
| | | | DS55453/DS75453 | | 16 | 25 | ns |
| | | | DS55454/DS75454 | | 24 | 35 | ns |
| $t_{TLH}$ | Transition Time, Low-to-High Level Output | $C_L$ = 15 pF, $R_L$ = 50Ω, $I_O \approx$ 200mA, *(Figure 14)* | | | 5 | 8 | ns |
| $t_{THL}$ | Transition Time, High-to-Low Level Output | $C_L$ = 15 pF, $R_L$ = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)* | | | 7 | 12 | ns |
| $V_{OH}$ | High-Level Output Voltage after Switching | $V_S$ = 20V, $I_O \approx$ 300 mA, *(Figure 15)* | | $V_S$ − 6.5 | | | mV |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Voltage values are with respect to network ground terminal unless otherwise specified.

**Note 3:** The voltage between two emitters of a multiple-emitter transistor.

**Note 4:** The maximum voltage which should be applied to any output when it is in the "OFF" state.

**Note 5:** Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

**Note 6:** Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55450 series and across the 0°C to +70°C range for the DS7545X series. All typicals are given for $V_{CC}$ = +5V and $T_A$ = 25°C.

**Note 7:** All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

## Truth Tables (H = high level, L = low level)

**DS55451/DS75451**

| A | B | Y |
|---|---|---|
| L | L | L (ON State) |
| L | H | L (ON State) |
| H | L | L (ON State) |
| H | H | H (OFF State) |

**DS55453/DS75453**

| A | B | Y |
|---|---|---|
| L | L | L (ON State) |
| L | H | H (OFF State) |
| H | L | H (OFF State) |
| H | H | H (OFF State) |

**DS55452/DS75452**

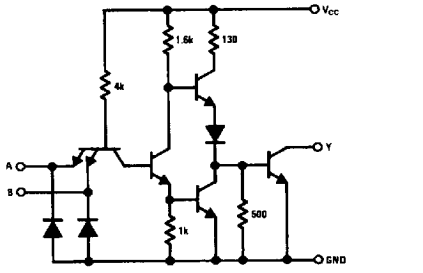
| A | B | Y |
|---|---|---|
| L | L | H (OFF State) |
| L | H | H (OFF State) |
| H | L | H (OFF State) |
| H | H | L (ON State) |

**DS55454/DS75454**

| A | B | Y |
|---|---|---|
| L | L | H (OFF State) |
| L | H | L (ON State) |
| H | L | L (ON State) |
| H | H | L (ON State) |

## Schematic Diagrams

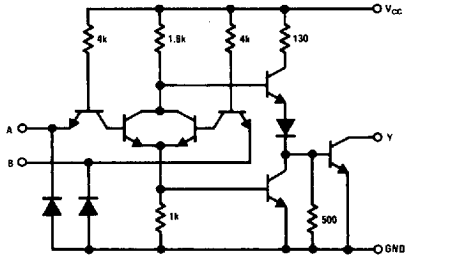
**DS55451/DS75451**




TL/F/5824–11

Resistor values shown are nominal.

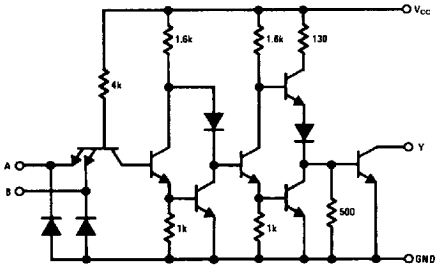
**DS55453/DS75453**




TL/F/5824–13

Resistor values shown are nominal.

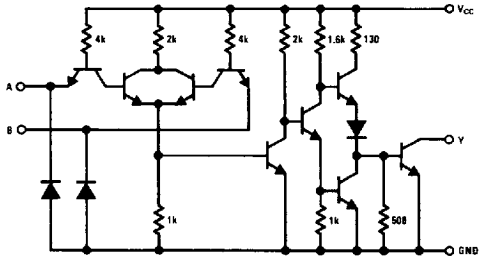
**DS55452/DS75452**




TL/F/5824–12

Resistor values shown are nominal.

**DS55454/DS75454**

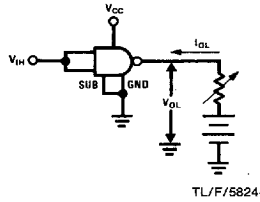



TL/F/5824–14

Resistor values shown are nominal.

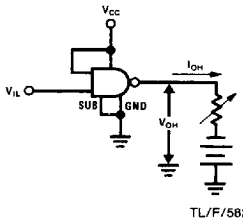
3

## DC Test Circuits



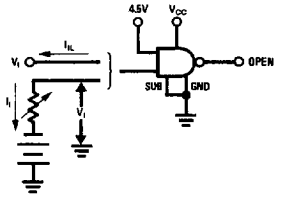

Both inputs are tested simultaneously.

**FIGURE 1. $V_{IH}$, $V_{OL}$**



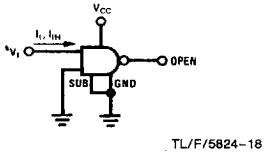

Each input is tested separately.

**FIGURE 2. $V_{IL}$, $V_{OH}$**



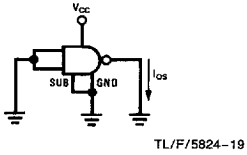

Each input is tested separately.

**FIGURE 3. $V_I$, $I_{IL}$**



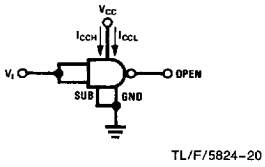

Each input is tested separately.

**FIGURE 4. $I_I$, $I_{IH}$**



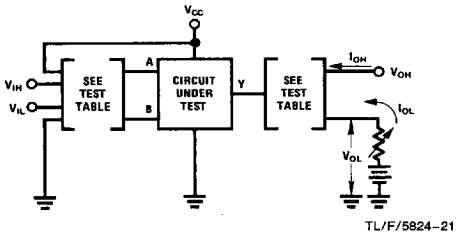

Each input is tested separately.

**FIGURE 5. $I_{OS}$**



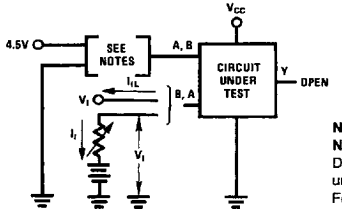

Both gates are tested simultaneously.

**FIGURE 6. $I_{CCH}$, $I_{CCL}$**



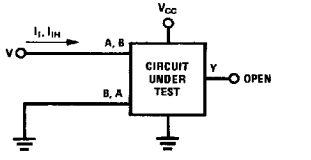

| Circuit | Input Under Test | Other Input | Output | |
|---|---|---|---|---|
| | | | Apply | Measure |
| DS55451 | $V_{IH}$ | $V_{IH}$ | $V_{OH}$ | $I_{OH}$ |
| | $V_{IL}$ | $V_{CC}$ | $I_{OL}$ | $V_{OL}$ |
| DS55452 | $V_{IH}$ | $V_{IH}$ | $I_{OL}$ | $V_{OL}$ |
| | $V_{IL}$ | $V_{CC}$ | $V_{OH}$ | $I_{OH}$ |
| DS55453 | $V_{IH}$ | Gnd | $V_{OH}$ | $I_{OH}$ |
| | $V_{IL}$ | $V_{IL}$ | $I_{OL}$ | $V_{OH}$ |
| DS55454 | $V_{IH}$ | Gnd | $I_{OL}$ | $V_{OL}$ |
| | $V_{IL}$ | $V_{IL}$ | $V_{OH}$ | $I_{OH}$ |

**FIGURE 7. $V_{IH}$, $V_{IL}$, $I_{OH}$, $V_{OL}$**



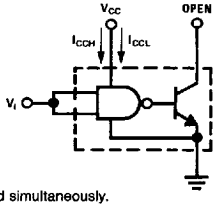

**Note A:** Each input is tested separately.
**Note B:** When testing DS55453/DS75453, DS55454/DS75454, input not under test is grounded. For all other circuits it is at 4.5V.

**FIGURE 8. $V_I$, $V_{IL}$**



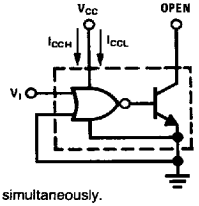

Each input is tested separately.

**FIGURE 9. $I_I$, $I_{IH}$**




Both gates are tested simultaneously.

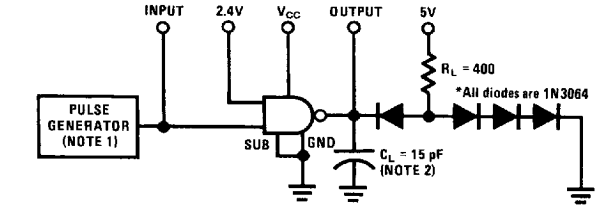
**FIGURE 10. $I_{CCH}$, $I_{CCL}$ for AND, NAND Circuits**



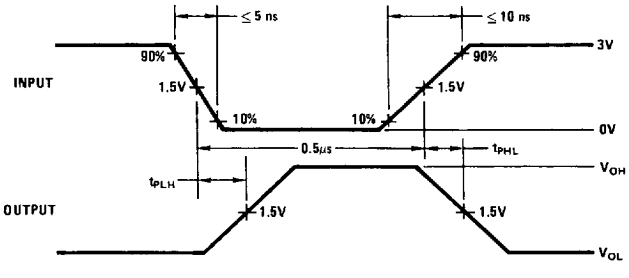

Both gates are tested simultaneously.

**FIGURE 11. $I_{CCH}$, $I_{CCL}$ for OR, NOR Circuits**

## AC Test Circuits and Switching Time Waveforms




TL/F/5824–26

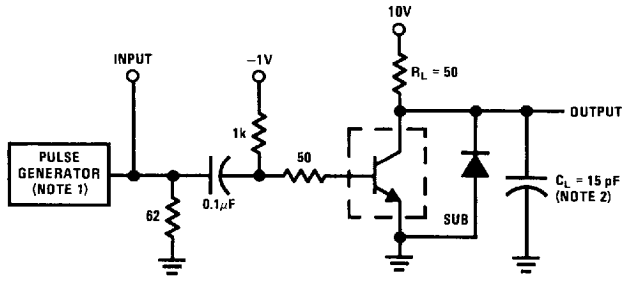



TL/F/5824–27

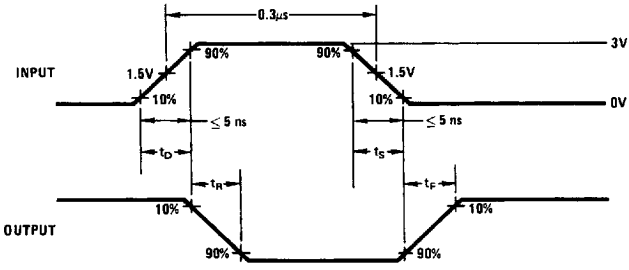
**Note 1:** The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.

**Note 2:** $C_L$ includes probe and jig capacitance.

**FIGURE 12. Propagation Delay Times, Each Gate**




TL/F/5824–28




TL/F/5824–29

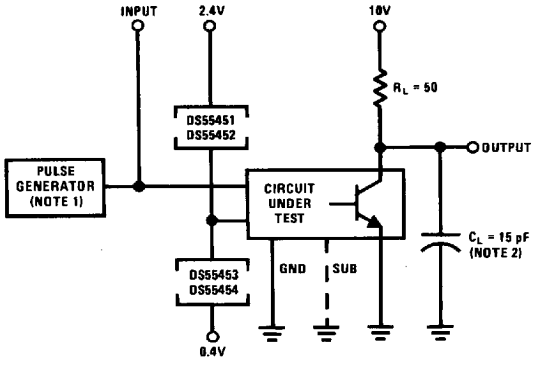
**Note 1:** The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{OUT} \approx 50\Omega$.

**Note 2:** $C_L$ includes probe and jig capacitance.

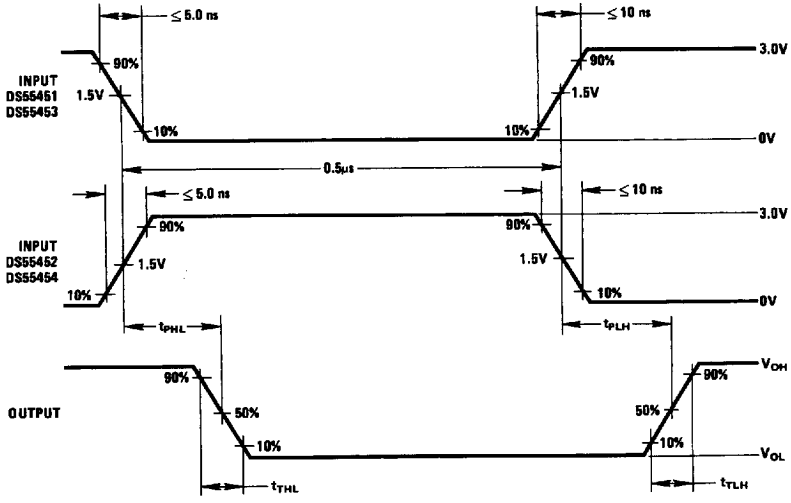
**FIGURE 13. Switching Times, Each Transistor**

3

## AC Test Circuits and Switching Time Waveforms (Continued)




TL/F/5824–30



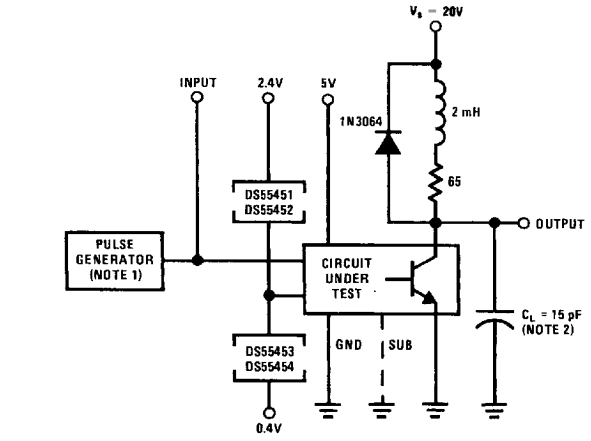

TL/F/5824–31

**Note 1:** The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$.

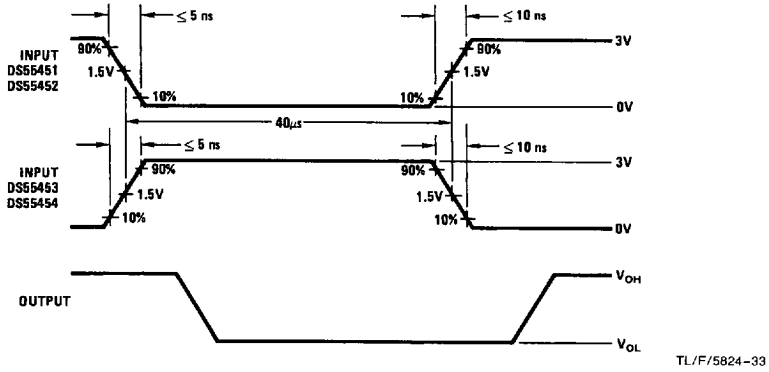
**Note 2:** $C_L$ includes probe and jig capacitance.

**FIGURE 14. Switching Times of Complete Drivers**

## AC Test Circuits and Switching Time Waveforms (Continued)




TL/F/5824–32



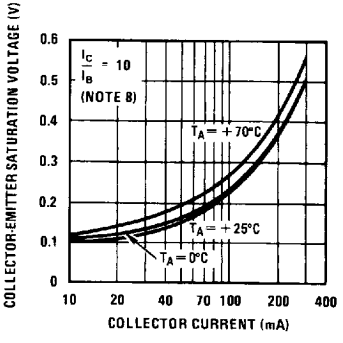

TL/F/5824–33

**Note 1:** The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{OUT} \approx 50\Omega$.

**Note 2:** $C_L$ includes probe and jig capacitance.

**FIGURE 15. Latch-UP Test of Complete Drivers**

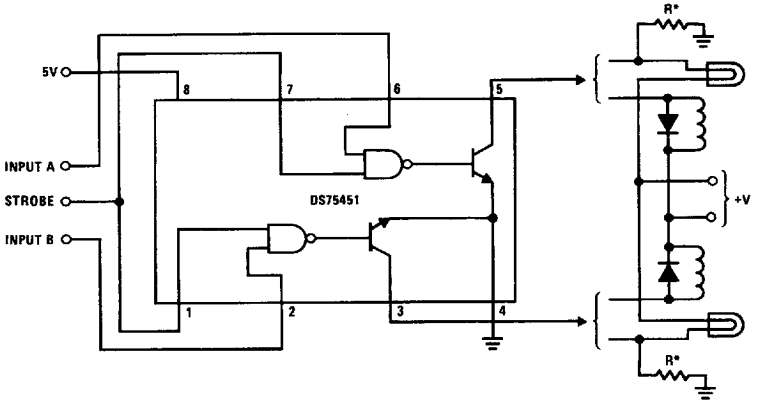
## Typical Performance Characteristics




TL/F/5824–37

**FIGURE 16. Transistor Collector-Emitter Saturation Voltage vs Collector Current**

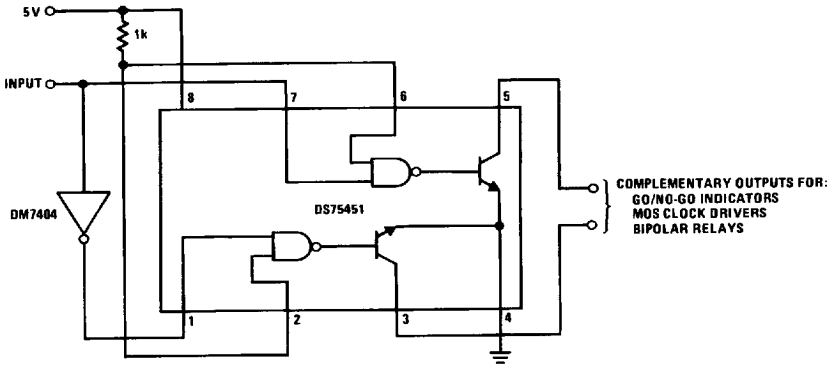
## Typical Applications




TL/F/5824–46

*Optional keep-alive resistors maintain off-state lamp current at ≈ 10% to reduce surge current.

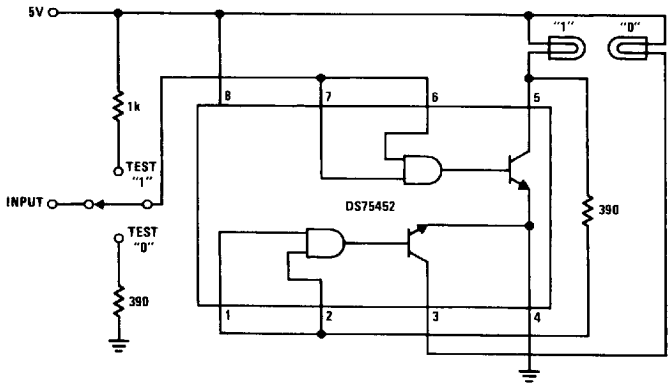
**FIGURE 17. Dual Lamp or Relay Driver**




TL/F/5824–47

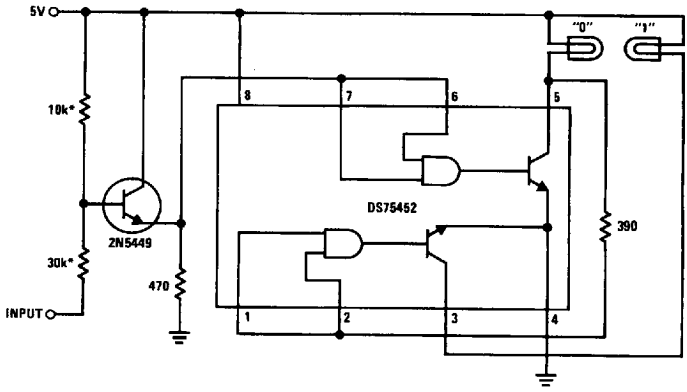
**FIGURE 18. Complementary Driver**

## Typical Applications (Continued)




TL/F/5824–48

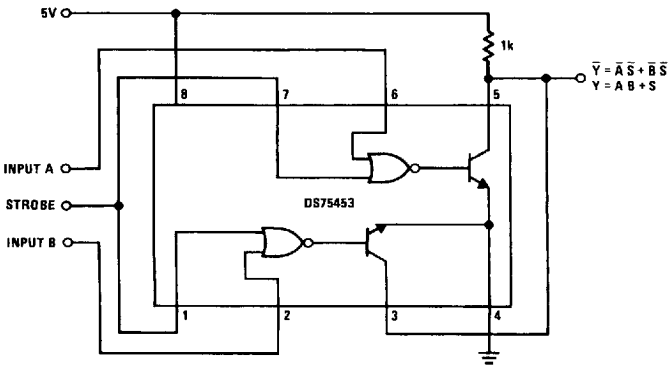
**FIGURE 19. TTL or DTL Positive Logic-Level Detector**




TL/F/5824–49

*The two input resistors must be adjusted for the level of MOS input.

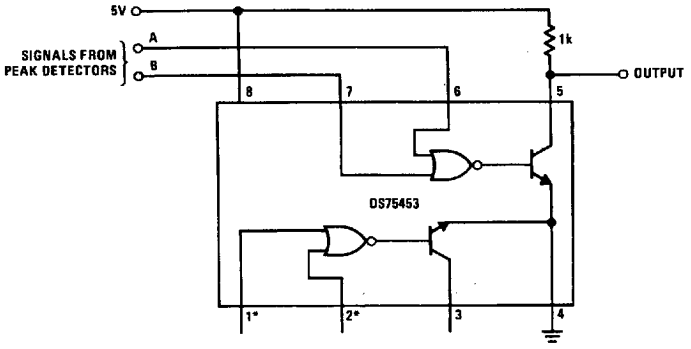
**FIGURE 20. MOS Negative Logic-Level Detector**




TL/F/5824–50

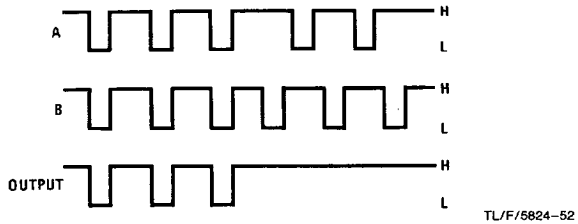
**FIGURE 21. Logic Signal Comparator**

## Typical Applications (Continued)




TL/F/5824–51

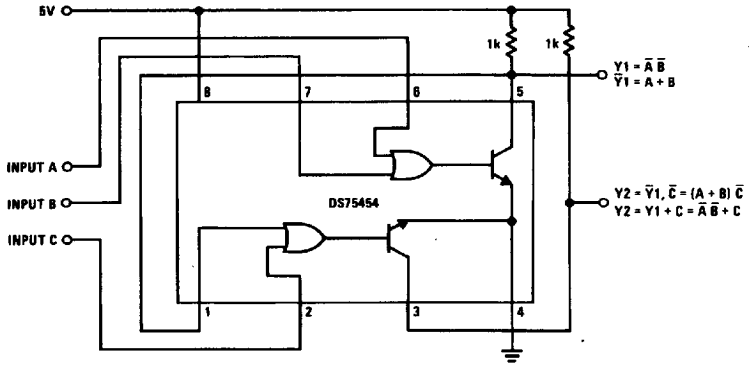
*If inputs are unused, they should be connected to +5V through a 1k resistor.




TL/F/5824–52

Low output occurs only when inputs are low simultaneously.

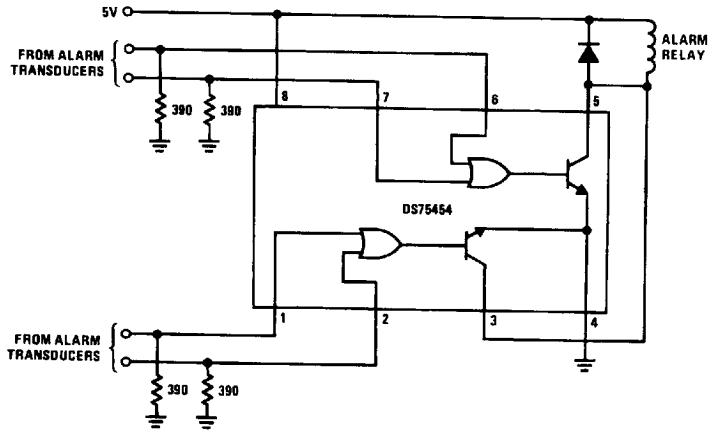
**FIGURE 22. In-Phase Detector**




TL/F/5824–53

**FIGURE 23. Multifunction Logic-Signal Comparator**

## Typical Applications (Continued)




TL/F/5824–54

**FIGURE 24. Alarm Detector**