LXT362

Integrated T1 LH/SH Transceiver for DS1/DSX-1 or PRI Applications

Datasheet

The LXT362 is a fully integrated, combination transceiver for T1 ISDN Primary Rate Interface and general T1 long and short haul applications. It operates over 22 AWG twisted-pair cables from 0 to 6 kft and offers Line Build Outs and pulse equalization settings for all T1 Line Interface Unit (LIU) applications.

LXT362 provides both a serial port for microprocessor control (Host mode) as well as stand-alone operation (Hardware mode). The device incorporates advanced crystal-less digital jitter attenuation in either the transmit or receive data path starting at 3 Hz. B8ZS encoding/decoding and unipolar or bipolar data I/O are selectable. Loss of signal monitoring and a variety of diagnostic loopback modes can also be selected.

Applications

- ISDN Primary Rate Interface (ISDN PRI)
- CSU/NTU interface to T1 Service
- Wireless Base Station interface
- T1 LAN/WAN bridge/routers
- T1 Mux; Channel Banks
- Digital Loop Carrier - Subscriber Carrier Systems

Product Features

- Fully integrated transceiver for Long or Short-Haul T1 interfaces
  - —Crystal-less digital jitter attenuation
  - —Select either transmit or receive path
- No crystal or high speed external clock required
- Meets or exceeds specifications in ANSI T1.102, T1.403 and T1.408; and AT&T Pub 62411
- Supports 100 Ω (T1 twisted-pair) applications
- Selectable receiver sensitivity – fully restores the received signal after transmission through a cable with attenuation of either 0 to 26 dB, or 0 to 36 dB @ 772 kHz
- Five Pulse Equalization Settings for T1 short-haul applications
- Four Line Build-Outs for T1 long-haul applications from 0 dB to -22.5 dB
- Transmit/receive performance monitors with Driver Fail Monitor Open and Loss of Signal outputs
- Selectable unipolar or bipolar data I/O and B8ZS encoding/decoding
- Line attenuation indication output in 2.9 dB steps
- QRSS generator/detector for testing or monitoring
- Local, remote, and analog loopback, plus in-band network loopback code generation and detection
- Multiple register serial interface for microprocessor control
- Available in 28-pin PLCC, 44-pin PQFP, and 44-pin LQFP packages

As of January 15, 2001, this document replaces the Level One document known as *LXT362 — Integrated T1 LH/SH Transceiver for DS1/DSX-1 or PRI Applications*.

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January 2001

Datasheet

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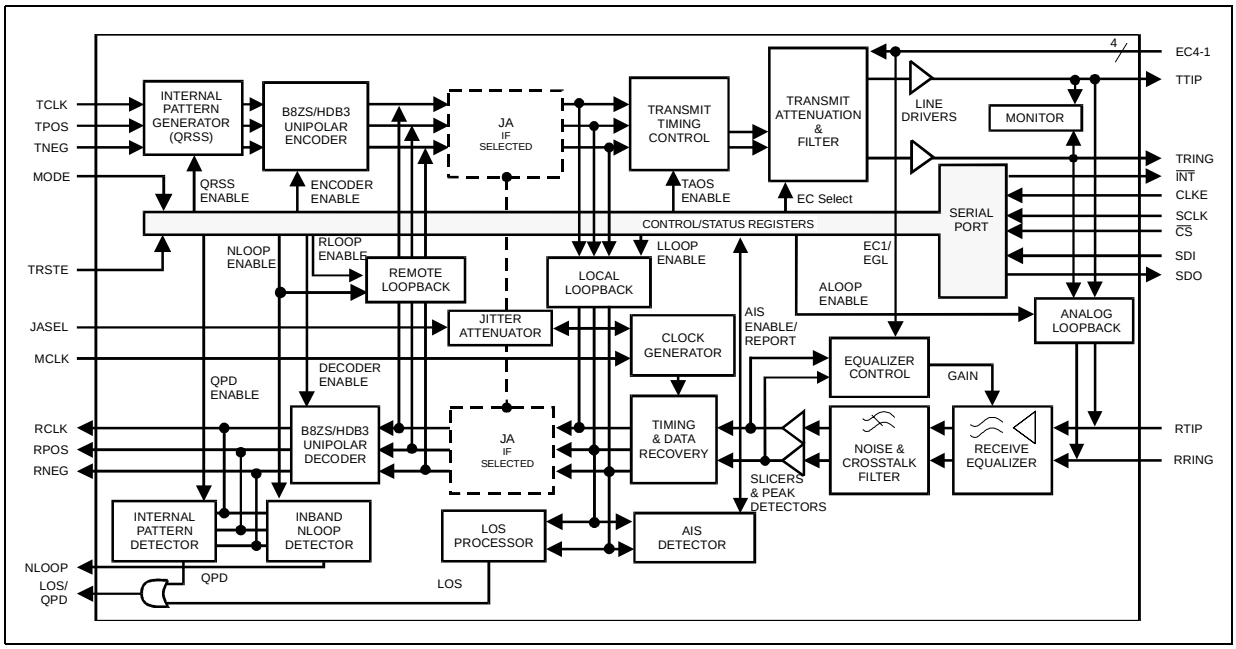
Revision History

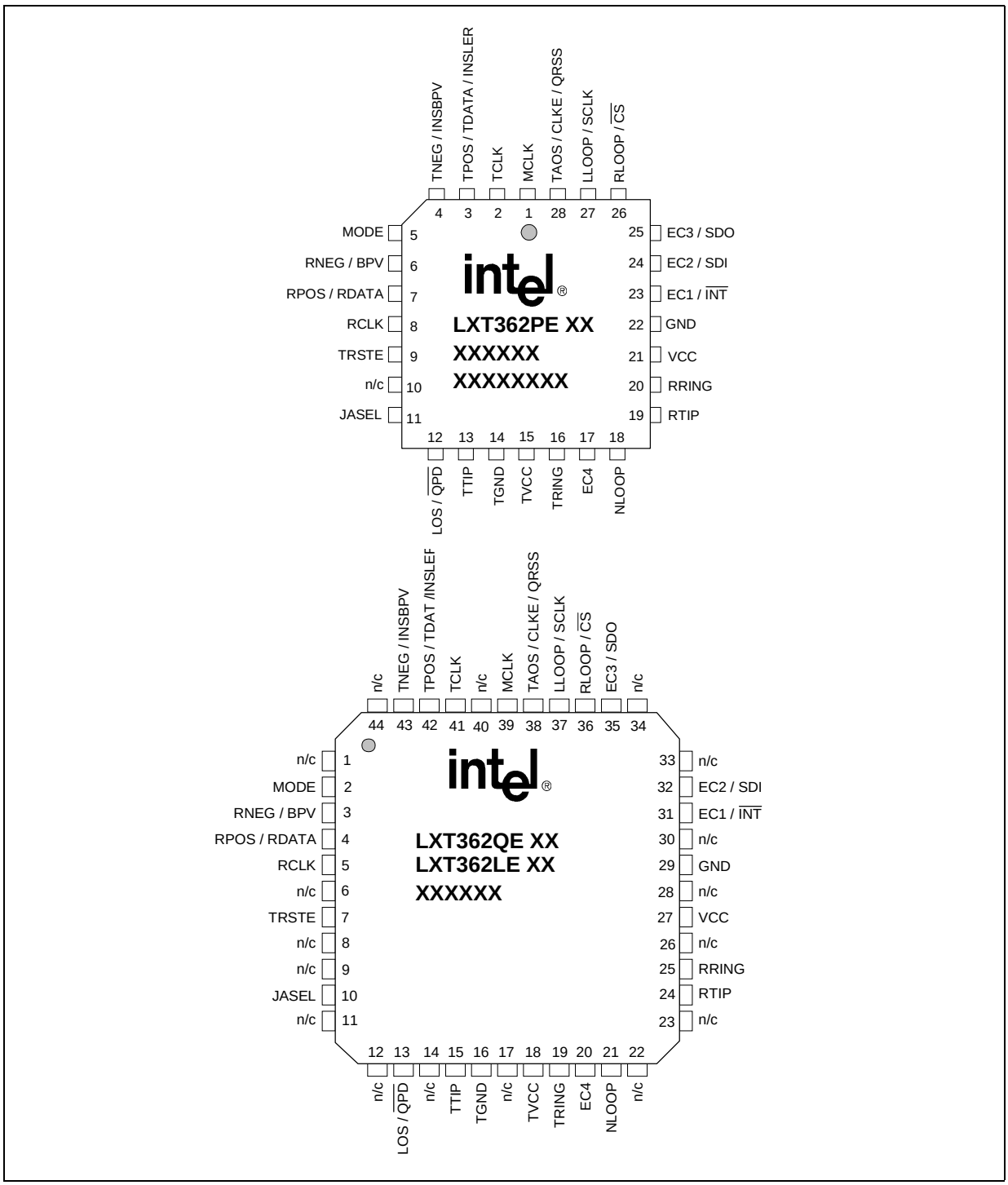
Revision	Date	Description

Figure 1. LXT362 Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 2. LXT362 Pin Assignments



1.1 Mode Dependent Signals

As shown in Figure 2, the LXT362 has various signal pins that change function (and name) according to the selected mode(s) of operation. These pins, associated signal names and operating modes are summarized in Table 1 and Table 2. LXT362 signals are described in Table 3.

Table 1. LXT362 Clock and Data Pins by Mode[1]

Pin #		External Data Modes		QRSS Modes	
PLCC	QFP	Bipolar Mode	Unipolar Mode	Bipolar Mode	Unipolar Mode
1	39	MCLK			
2	41	TCLK			
3	42	TPOS	TDATA	INSLER	
4	43	TNEG	INSBPV	INSBPV	
6	3	RNEG	BPV	RNEG	BPV
7	4	RPOS	RDATA	RPOS	RDATA
8	5	RCLK			
13	15	TTIP			
16	19	TRING			
19	24	RTIP			
20	25	RRING			

1. Data pins change based on whether external data or internal QRSS mode is active. Clock pins remain the same in both Hardware and Host modes.

Table 2. LXT362 Control Pins by Mode

Pin #		Hardware Modes		Host Modes		Pin #		Hardware Modes		Host Modes	
PLCC	QFP	Unipolar/ Bipolar	QRSS	Unipolar/ Bipolar	QRSS	PLCC	QFP	Unipolar/ Bipolar	QRSS	Unipolar/ Bipolar	QRSS
5	2	MODE		MODE		25	35	EC3		SDO	
9	7	TRSTE		TRSTE		17	20	EC4		Low	
11	10	JASEL		Low		18	21	NLOOP		NLOOP	
12	13	LOS	$\overline{\text{LOS}}$/ QPD	LOS	$\overline{\text{LOS}}$/ QPD	26	36	RLOOP		$\overline{\text{CS}}$	
23	31	EC1		$\overline{\text{INT}}$		27	37	LLOOP		SCLK	
24	32	EC2		SDI		28	38	TAOS	QRSS	CLKE	

Table 3. LXT362 Signal Descriptions

Pin #		Symbol	I/O[1]	Description
PLCC	QFP			
1	39	MCLK	DI	**Master Clock**. External, independent 1.544 MHz clock signal required to generate internal clocks. MCLK must be jitter-free and have an accuracy better than ± 50 ppm with a typical duty cycle of 50%. Upon Loss of Signal (LOS), RCLK is derived from MCLK.
2	41	TCLK	DI	**Transmit Clock**. A 1.544 MHz clock is required. The transceiver samples TPOS and TNEG on the **falling edge** of TCLK (or MCLK, if TCLK is not present).
3 4	42 43	TPOS / TDATA / INSLER TNEG / INSBPV	DI DI	**BIPOLAR MODES:** **Transmit – Positive and Negative**. TPOS and TNEG are the positive and negative sides of a bipolar input pair. Data to be transmitted onto the twisted-pair line is input at these pins. TPOS/TNEG are sampled on the falling edge of TCLK (or MCLK, if TCLK is not present). **UNIPOLAR MODES:** **Transmit Data**. TDATA carries unipolar data to be transmitted onto the twisted-pair line and is sampled on the falling edge of TCLK. Transmit Insert Logic Error. In *QRSS mode*, a Low-to-High transition on INSLER inserts a logic error into the transmitted QRSS data pattern. The inserted error follows the data flow of the active loopback mode. The LXT362 samples this pin on the falling edge of TCLK (or MCLK, if TCLK is not present). **Transmit Insert Bipolar Violation**. INSBPV is sampled on the falling edge of TCLK (or MCLK, if TCLK is not present) to control Bipolar Violation (BPV) insertions in the transmit data stream. A Low-to-High transition is required to insert each BPV. In ***QRSS mode***, the BPV is inserted into the transmitted QRSS pattern.
5	2	MODE	DI	**Mode Select**. Connect Low to select Hardware mode. Connect High to select Host mode. See Table 5 on page 19 for a complete list of operating modes.
6 7	3 4	RNEG / BPV RPOS / RDATA	DO DO	**BIPOLAR MODES:** **Receive – Negative and Positive**. RPOS and RNEG are the positive and negative sides of a bipolar output pair. Data recovered from the line interface is output on these pins. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS are Non-Return-to-Zero (NRZ). In ***Hardware mode***, RPOS/RNEG are stable and valid on the rising edge of RCLK. In ***Host mode***, the CLKE pin selects the RCLK clock edge when RPOS /RNEG are stable and valid as described in Table 4 on page 18. **UNIPOLAR MODES:** **Receive Bipolar Violation.** BPV goes High to indicate detection of a bipolar violation from the line. This is an NRZ output and is valid on the rising edge of RCLK. **Receive Data**. RDATA is the unipolar NRZ output of data recovered from the line interface. In ***Hardware mode***, RDATA is stable and valid on the rising edge of RCLK. In ***Host mode***, the CLKE pin selects the RCLK clock edge when RDATA is stable and valid as described in Table 4 on page 18.
8	5	RCLK	DO	**Receive Recovered Clock**. The clock recovered from the line input signal is output on this pin. Under LOS conditions, there is a smooth transition from the RCLK signal (derived from the recovered data) to the MCLK signal, which appears at the RCLK pin.

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
2. Midrange is a voltage level such that 2.3 V ≤ Midrange ≤ 2.7 V. Midrange may also be established by letting the pin float.

Table 3. LXT362 Signal Descriptions (Continued)

Pin #		Symbol	I/O[1]	Description
PLCC	QFP			
9	7	TRSTE	DI	**Tristate**. **HARDWARE MODES:** Connect TRSTE High to force all output pins to the high impedance state. TRSTE, in conjunction with the MODE pin, selects the operating modes listed in Table 5 on page 19. **HOST MODES:** Connect TRSTE High to force all output pins to the high-impedance state. Connect this pin Low for normal operation.
11	10	JASEL	DI	**HARDWARE MODES:** **Jitter Attenuation Select**. Selects jitter attenuation location: Setting JASEL High activates the jitter attenuator in the receive path. Setting JASEL Low activates the jitter attenuator in the transmit path. Setting JASEL to Midrange[2] disables jitter attenuation. **HOST MODES:** Connect Low in Host mode.
12	13	LOS / $\overline{\text{QPD}}$	DO	**Loss of Signal Indicator**. LOS goes High upon receipt of 175 consecutive spaces and returns Low when the received signal reaches a mark density of 12.5% (determined by receipt of 16 marks within a sliding window of 128 bits with fewer than 100 consecutive zeros). Note that the transceiver outputs received marks on RPOS and RNEG even when LOS is High. **QRSS Pattern Detect.** In ***QRSS mode***, $\overline{\text{QPD}}$ stays High until the transceiver detects a QRSS pattern. When a QRSS pattern is detected, the pin goes Low. Any bit errors cause $\overline{\text{QPD}}$ to go High for half a clock cycle. This output can be used to trigger an external error counter. Note that a LOS condition will cause $\overline{\text{QPD}}$ to remain High. See Figure 11.
13 16	15 19	TTIP TRING	AO	**Transmit Tip and Ring**. Differential driver output pair designed to drive a 50 - 200 Ω load. The transformer and line matching resistors should be selected to give the desired pulse height and return loss performance. See "Application Information" on page 34.
14	16	TGND	-	**Ground** return for the transmit driver power supply TVCC.
15	18	TVCC	-	**+5 VDC Power Supply** for the transmit drivers. TVCC must not vary from VCC by more than ± 0.3 V.
17	20	EC4	DI	**HARDWARE MODES:** **Equalization Control 4**. Used along with EC3, EC2 and EC1 pins to specify pulse equalization, line build out and equalizer gain limit settings. See Table 10 on page 30 for details. **HOST MODES:** Connect Low in Host mode.
18	21	NLOOP	DO	**Network Loopback Active**. Goes High to indicate that Network loopback (NLOOP) is active. NLOOP is activated by the reception of a 00001 pattern for five seconds. NLOOP is reset by reception of a 001 pattern for five seconds, or by activation of Remote loopback (RLOOP).
19 20	24 25	RTIP RRING	AI	**Receive Tip and Ring**. The Alternate Mark Inversion (AMI) signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock recovered from RTIP/RRING are output on the RPOS/RNEG (or RDATA in ***Unipolar mode***), and RCLK pins.
21	27	VCC	-	**+5 VDC Power Supply** for all circuits except the transmit drivers. Transmit drivers are supplied by TVCC.

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
2. Midrange is a voltage level such that 2.3 V ≤ Midrange ≤ 2.7 V. Midrange may also be established by letting the pin float.

Table 3. LXT362 Signal Descriptions (Continued)

Pin #		Symbol	I/O[1]	Description
PLCC	QFP			
22	29	GND	-	**Ground** return for power supply VCC.
23 24 25	31 32 35	EC1 / $\overline{INT}$ EC2 / SDI EC3 / SDO	DI DI DI/O	**HARDWARE MODES:** **Equalization Control 1-3**. EC1, EC2, and EC3 (along with the EC4 pin) specify the pulse equalization, line build out and equalizer gain limit settings. See Table 10 on page 30 for details. **HOST MODES:** **Interrupt**. $\overline{INT}$ goes Low to flag the host when LOS, AIS, NLOOP, QRSS, DFMS or DFMO bits changes state, or when an elastic store overflow or underflow occurs. To identify the specific interrupt, read the Performance Status Register (PSR). To clear or mask an interrupt, write a one to the appropriate bit in the Interrupt Clear Register (ICR). To re-enable the interrupt, write a zero. $\overline{INT}$ is an ***open drain output*** that must be connected to VCC through a pull-up resistor. **Serial Data Input**. SDI inputs the 16-bit serial address/command and data word. SDI is sampled on the rising edge of SCLK. Timing is shown in Figure 17 on page 43. **Serial Data Output**. SDO outputs the 8-bit serial data read from the selected LXT362 register. When the CLKE pin is High, SDO is valid on the rising edge of SCLK. When CLKE is Low, SDO is valid on the falling edge of SCLK. SDO goes to a high-impedance state when the serial port is being written to or when $\overline{CS}$ is High. Timing is shown in Figure 18 on page 43.
26	36	RLOOP / $\overline{CS}$	DI	**HARDWARE MODES:** **Remote Loopback.** When held High, the clock and data inputs from the framer (TPOS/TNEG or TDATA) are ignored and the data received from the twisted-pair line is transmitted back onto the line at the RCLK frequency. Connect to Midrange[2] to enable In-band Network loopback detection (NLOOP). **HOST MODES:** **Chip Select.** $\overline{CS}$ is used to access the serial interface. For each read or write operation, $\overline{CS}$ must transition from High to Low, and remain Low.

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
2. Midrange is a voltage level such that 2.3 V ≤ Midrange ≤ 2.7 V. Midrange may also be established by letting the pin float.

Table 3. LXT362 Signal Descriptions (Continued)

Pin #		Symbol	I/O[1]	Description
PLCC	QFP			
27	37	LLOOP / SCLK	DI	**HARDWARE MODES:** **Local Loopback**. When held High, the data on TPOS and TNEG loops back digitally to the RPOS and RNEG outputs (through the JA if enabled). Connecting this pin to Midrange[2] enables Analog loopback (TTIP and TRING are looped back to RTIP and RRING). **HOST MODES:** **Serial Clock**. SCLK synchronizes serial port read/write operations. The clock frequency can be any rate up to 2.048 MHz.
28	38	TAOS / QRSS / CLKE	DI	**HARDWARE MODES:** **Transmit All Ones**. When held High, the transmit data inputs are ignored and the LXT362 transmits a stream of 1's at the TCLK frequency. If TCLK is not supplied, MCLK becomes the transmit clock reference. Note that TAOS is inhibited during Remote loopback. **QRSS**. In ***QRSS mode***, setting this pin to Midrange[2], enables QRSS pattern generation and detection. The transceiver transmits the QRSS pattern at the TCLK rate (or MCLK, if TCLK is not present). **HOST MODES:** **Clock Edge Select**. When CLKE is High, RPOS/RNEG or RDATA are valid on the falling edge of RCLK, and SDO is valid on the rising edge of SCLK. When CLKE is Low, RPOS/RNEG or RDATA are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK. The operation of CLKE is summarized in Table 4 on page 18.
10	1, 6, 8, 9, 11, 12, 14, 17, 22, 23, 26, 28, 30, 33, 34, 40, 44	n/c	-	**Not Connected**

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
2. Midrange is a voltage level such that 2.3 V ≤ Midrange ≤ 2.7 V. Midrange may also be established by letting the pin float.

2.0 Functional Description

The LXT362 is a fully integrated, PCM transceiver for long- or short-haul, 1.544 Mbps (T1) applications allowing full-duplex transmission of digital data over existing twisted-pair installations. It interfaces with two twisted-pair lines (one pair each for transmit and receive) through standard pulse transformers and appropriate resistors.

The figure on the front page of this data sheet shows a block diagram of the LXT362. The designer can configure the device for either Host or Hardware control. In Host mode, control is via the serial microprocessor port. In Hardware mode, individual pin settings allow stand-alone operation.

The transceiver provides a high-precision, crystal-less jitter attenuator. The user may place it in the transmit or receive path, or bypass it completely.

The LXT362 meets or exceeds FCC, ANSI T1 and AT&T specifications for CSU and DSX-1 applications.

2.1 Initialization

During power up, the transceiver remains static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the Phase Lock Loops (PLL). The transceiver uses a reference clock to calibrate the PLLs: the transmitter reference is TCLK, and the receiver reference clock is MCLK. MCLK is mandatory for chip operation and must be an independent free running jitter free reference clock.

2.1.1 Reset Operation

A reset operation initializes the status and state machines for the LOS, AIS, NLOOP, and QRSS blocks. In Hardware mode, holding pins RLOOP, LLOOP and TAOS High for at least one clock cycle resets the device. In Host mode, writing a 1 to the bit CR2.RESET commands a reset which clears all registers to 0. Allow 32 ms for the device to settle after removing all reset conditions.

2.2 Transmitter

2.2.1 Transmit Digital Data Interface

Input data for transmission onto the line is clocked serially into the device at the TCLK rate. TPOS and TNEG are the bipolar data inputs. In Unipolar mode, the TDATA pin accepts unipolar data.

Input data may pass through either the Jitter Attenuator or B8ZS the encoder or both. In Host mode, setting CR1.ENCENB = 1 enables B8ZS encoding. In Hardware mode, connecting the MODE pin to Midrange selects zero suppression coding. With zero suppression enabled, the EC1 through EC4 inputs determine the coding scheme as listed in Table 10 on page 30.

TCLK supplies input synchronization. See the Figure 15 on page 41 for the transmit timing requirements for TCLK and the Master Clock (MCLK).

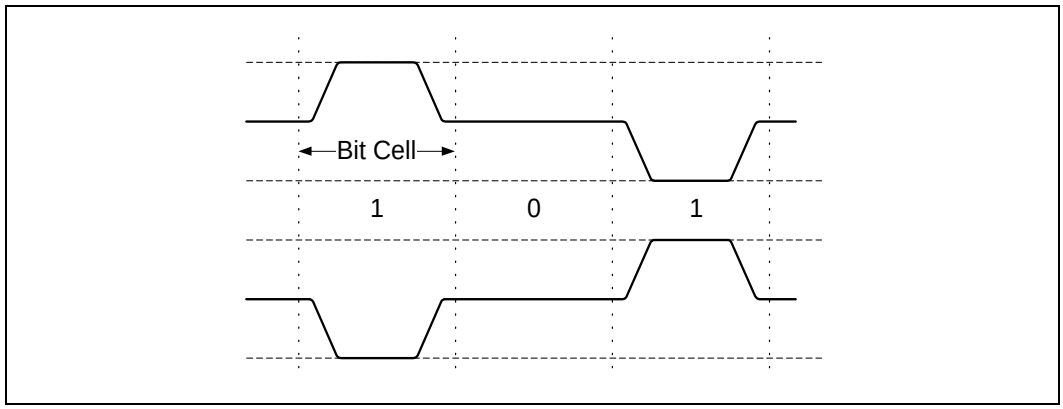
2.2.2 Transmit Monitoring

In Host mode, the Performance Status Register flags open circuits in bit PSR.DFMO. A transition on DFMO will provide an interrupt, and its transition sets bit TSR.DFMO = 1. Writing a 1 in bit ICR.CDFMO clears the interrupt; leaving a 1 in the bit masks that interrupt.

2.2.3 Transmit Drivers

The transceiver transmits data as a 50% line code as shown in Figure 3. To reduce power consumption, the line driver is active only during transmission of marks, and is disabled during transmission of spaces. Biasing of the transmit DC level is on-chip.

Figure 3. 50% Duty Cycle Coding



2.2.4 Transmit Idle Mode

Transmit Idle mode allows multiple transceivers to be connected to a single line for redundant applications. When TCLK is not present, Transmit Idle mode becomes active, and TTIP and TRING change to the high impedance state. Remote loopback, Dual loopback, TAOS, or detection of Network Loop Up code in the receive direction will temporarily disable the high impedance state.

2.2.5 Transmit Pulse Shape

As shown in Table 10 on page 30, Equalizer Control inputs (EC1 through EC4) determine the transmitted pulse shape. In Host mode, EC1 through 4 are established by bits 0 through 3 of Control Register #1 (CR1), respectively. In Hardware mode, pins EC1, EC2, EC3, and EC4 specify pulse shape.

Shaped pulses meeting the various T1, DS1, and DSX-1 specifications are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The transceiver produces DSX-1 pulses for short-haul T1 applications (settings from 0 dB to +6.0 dB of cable), DS1 pulses for long-haul T1 applications (settings from 0 dB to -22.5 dB). Refer to Figure 14 on page 40 for pulse mask specifications.

2.3 Receiver

A 1:1 transformer provides the interface to the twisted-pair line (RTIP/RING). Recovered data is output at RPOS/RNEG (RDATA in Unipolar mode), and the recovered clock is output at RCLK. Refer to Table 27 on page 41 for receiver timing specifications.

2.3.1 Receive Equalizer

The receive equalizer processes the signal received at RTIP and RRING. The equalizer gain is up 36 dB. As shown in Table 10, Equalizer Control inputs (EC1 through EC4) determine the maximum gain applied to the equalizer. In Host mode, EC1 through 4 are established by bits 0 through 3 of Control Register #1 (CR1), respectively. In Hardware mode, pins EC1, EC2, EC3, and EC4 specify equalizer gain setting. With EC1 Low, up to 36 dB of gain may be applied. When EC1 is High, 26 dB is the gain limit to provide an increased noise margin in shorter loop operations.

2.3.2 Receive Data Recovery

The transceiver filters the equalized signal and applies it to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. The data slicers are set at 50% of the peak value to ensure optimum signal-to-noise performance.

After processing through the data slicers, the received signal goes to the data and timing recovery section, then to the B8ZS decoder (if selected) and to the receive monitor. The data and timing recovery circuits provide input jitter tolerance significantly better than required by AT&T Pub 62411. See “Test Specifications” on page 38 for details.

2.3.3 Receive Digital Data Interface

Recovered data is routed to the Loss of Signal (LOS) Monitor. In Host mode, it also goes through the Alarm Indication Signal (AIS, Blue Alarm) Monitor. The jitter attenuator (JA) may be enabled or disabled in the receive data path or the transmit path. Received data can be routed to the B8ZS decoder or bypassed. Finally, the device may send the digital data to the framer as either unipolar or bipolar data.

2.3.4 Receiver Monitor Mode

The receive equalizer can be used in Monitor mode applications. Monitor mode applications require 20 dB to 30 dB resistive attenuation of the signal, plus a small amount of cable attenuation (less than 6 dB). In Host mode, setting bit CR3.EQZMON = 1 configures the device to operate in Monitor mode. Note that the LXT362 must be in long-haul receiver mode (set bits CR1.EC4:1 = 0xx0, 1001, or 1010) to enable Monitor mode. Note that the Monitor mode feature is not available in Hardware mode.

2.4 Jitter Attenuation

A Jitter Attenuation Loop (JAL) with an Elastic Store (ES) provides the jitter attenuation function. The JAL requires no special circuitry, such as an external quartz crystal or high-frequency clock (higher than the line rate). Rather, its timing reference is MCLK.

In Hardware mode, the ES is a 32 x 2-bit register. Setting the JASEL pin High places the JA circuitry in the receive data path; setting JASEL Low places the JA in the transmit data path; setting it to Midrange disables the JA.

In Host mode, bit CR1.JASEL0 enables or disables the JA circuit while bit CR1.JASEL1 controls the JA circuit placement as specified in Table 9 on page 30. The ES can be either a 32 x 2-bit or 64 x 2-bit register depending on the value of bit CR3.ES64 (see Table 12).

The device clocks data into the ES using either TCLK or RCLK depending on whether the JA circuitry is in the transmit or receive data path, respectively. Data is shifted out of the elastic store using the dejittered clock from the JAL. When the FIFO is within two bits of overflowing or underflowing, the ES adjusts the output clock by $^1/_8$ of a bit period. The ES produces an average delay of 16 bits in the data path. An average delay of 32 bits occurs when the 64-bit ES option selected (Host mode only). In the event of a LOS condition, with the Jitter Attenuator in the receive path, RCLK will be derived from MCLK.

Transition Status Register bits TSR.ESOVR and TSR.ESUNF indicate an elastic store overflow or underflow, respectively. Note that these are “sticky bits”, that is, once set to 1, they remain set until the host reads the register. An ES overflow or underflow condition will generate a maskable interrupt.

2.5 Hardware Mode

The LXT362 operates in Hardware mode when the MODE pin is set to Low or Midrange. In Hardware mode individual pins are used to access and control the transceiver. In Hardware mode, RPOS/RNEG or RDATA are valid on the rising edge of RCLK.

Note that some functions, such as interrupt ($\overline{\text{INT}}$), clock edge selection (CLKE), and various diagnostic modes, are provided only in Host mode.

2.6 Host Mode

The LXT362 operates in Host mode when the MODE pin is set High. In Host mode a microprocessor controls the LXT362 and reads its status via the serial port which provides access to the LXT362’s internal registers.

The host microprocessor can completely configure the device, as well as get a full diagnostic/status report, via the serial port. However, in Unipolar mode, bipolar violation (BPV) insertions and logic error insertions are controlled by the BPV and INSLER pins, respectively. Similarly, the recovered clock, data, and BPV detection are available only at output pins. All other mode settings and diagnostic information are available via the serial port. See “Register Definitions” on page 29 for details.

Figure 4 shows the serial port data structure. The registers are accessible through a 16-bit word composed of an 8-bit Command/Address byte (bits R/$\overline{\text{W}}$ and A1-A7) and a subsequent 8-bit data byte (bits D0-7). The R/$\overline{\text{W}}$ bit commands a read or a write operation, i.e., the direction of the following byte. Bits A1 through A6, of the command/address byte, point to a specific register. Note that the LXT362 address decoder ignores bits A0 and A7. Refer to Table 28 on page 42 for timing specifications.

Host mode also allows control of data output timing. The CLKE pin determines when SDO is valid, relative to the Serial Clock (SCLK) as shown in Table 4.

2.6.1 Interrupt Handling

In Host mode, the LXT362 provides a latched interrupt output pin ($\overline{INT}$). When enabled, a change in any of the Performance Status Register bits will generate an interrupt. An interrupt can also be generated when the elastic store overflows (TSR.ESOVR) or underflows (TSR.ESUNF). When an interrupt occurs, the $\overline{INT}$ output pin is pulled Low. Note that the output stage of the $\overline{INT}$ pin has internal pull-down only. Therefore, each device that shares the $\overline{INT}$ line ***requires an external pull-up resistor***.

The interrupt is cleared when the interrupt condition no longer exists, and the host processor writes a 1 to the respective interrupt causing bit(s) in the Interrupt Clear Register (ICR). Leaving a 1 in any of the ICR bits masks that interrupt. To re-enable an interrupt bit, write a 0.

Table 4. CLKE Pin Settings[1]

CLKE Pin	Output	Valid Clock Edge
Low	RPOS	Rising RCLK
	RNEG	
	RDATA	
	SDO	Falling SCLK
High	RPOS	Falling RCLK
	RNEG	
	RDATA	
	SDO	Rising SCLK

1. The clock edge selection feature is not available in Hardware mode.

Figure 4. Serial Port Data Structure

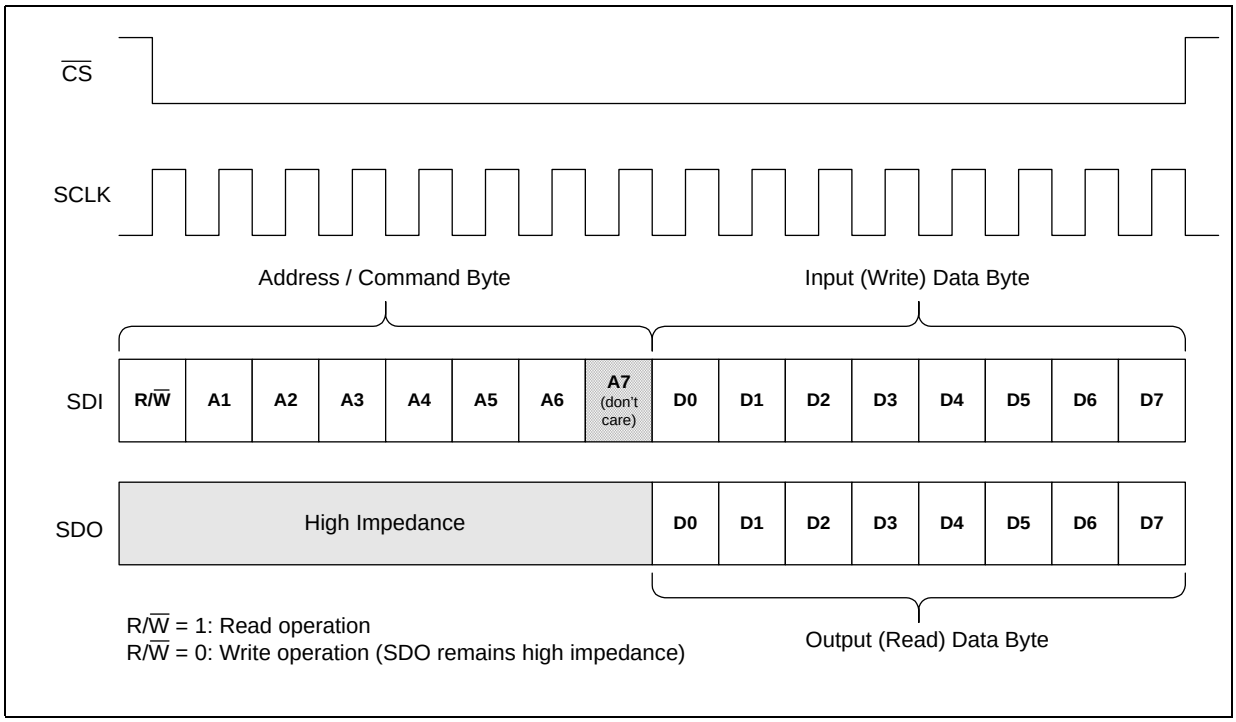


Table 5. Control and Operational Mode Selection

Input to Pin[1]		Mode of Operation						
Mode	**TRSTE**	**Hardware**	**Host[2]**	**Unipolar**	**Bipolar**	**AMI Enc/Dec**	**B8ZS Encoder/Decoder**	**All Outputs Tristated**
Low	Low	On	Off	Off	On	Off[3]	Off	No
Low	High	On	Off	Off	On	Off[3]	Off	Yes
Low	Open	On	Off	On	Off	On	Off	No
High	Low	Off	On	x	x	x	x	No
High	High	Off	On	x	x	x	x	Yes
High	Open	Off	On	x	x	x	x	No
Open	Low	On	Off	On	Off	Off	On	No
Open	High	On	Off	On	Off	Off	On	Yes
Open	Open	On	Off	On	Off	Off	On	No

1. Open is either a midrange voltage or the pin is floating.
2. In Host mode, the contents of register CR1 determine the operation mode.
3. Encoding is done externally.

2.7 Diagnostic Mode Operation

The LXT362 offers multiple diagnostic modes as listed in Table 6. Note that various diagnostic modes are only available in Host mode. In Hardware mode, the diagnostic modes are selected by a combination of pin settings. In Host mode, the diagnostic modes are selected by writing appropriate bits in the Diagnostic Control Register (DCR). The following paragraphs provide details of the diagnostic modes.

Table 6. Diagnostic Mode Availability

Diagnostic Mode	Availability[1]		Host Mode Maskable[2]
	Hardware	Host	
Loopback Modes			
Local Loopback (LLOOP)	Yes	Yes	No
Analog Loopback (ALOOP)	Yes	Yes	No
Remote Loopback (RLOOP)	Yes	Yes	No
In-band Network Loopback (NLOOP)	Yes	Yes	Yes
Dual Loopback (DLOOP)	Yes	Yes	No
Internal Data Pattern Generation and Detection			
Transmit All Ones (TAOS)	Yes	Yes	No
Quasi-Random Signal Source (QRSS)	Yes	Yes	Yes
In-band Loop up/down Code Generator	No	Yes	No
Error Insertion and Detection			
Bipolar Violation Insertion (INSBPV)	Yes	Yes	No
Logic Error Insertion (INSLER)	Yes	Yes	No
Bipolar Violation Detection (BPV)	Yes	Yes	No
Logic Error Detection, QRSS (QPD)	Yes	Yes	No
Alarm Condition Monitoring			
Receive Loss of Signal (LOS) Monitoring	Yes	Yes	Yes
Receive Alarm Indication Signal (AIS) Monitoring	No	Yes	Yes
Transmit Driver Failure Monitoring—Open (DFMO)	No	Yes	Yes
Elastic Store Overflow and Underflow Monitoring	No	Yes	Yes
Other Diagnostic Reports			
Receive Line Attenuation Indicator (LATN)	No	Yes	No
Built-In Self Test (BIST)	No	Yes	Yes

1. In Hardware mode, a combination of pin settings selects the Diagnostics Modes. In Host mode, writing appropriate bits in the Control Registers selects the Diagnostic Modes.
2. Host mode allows interrupt masking by writing a “1” to the corresponding bit in the Interrupt Clear Register.

2.7.1 Loopback Modes

2.7.1.1 Local Loopback (LLOOP)

See Figure 5 and Figure 6. LLOOP inhibits the receiver circuits. The transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) loop back through the jitter attenuator (if enabled) and appear at RCLK and RPOS/RNEG or RDATA. Note that during LLOOP, the JASEL input is strictly an enable/disable control, i.e. it does not affect the placement of the JA. If the JA is enabled, it is active in the loopback circuit. If the JA is bypassed, it is not active in the loopback circuit.

The transmitter circuits are unaffected by LLOOP and the LXT362 continues to transmit the TPOS/TNEG or TDATA inputs (or a stream of 1's if TAOS is asserted). When used in this mode, the transceiver can function as a stand-alone jitter attenuator.

In Hardware mode, Local loopback (LLOOP) is selected by setting LLOOP High; in Host mode, by setting bit CR2.ELLOOP = 1.

Figure 5. TAOS with LLOOP

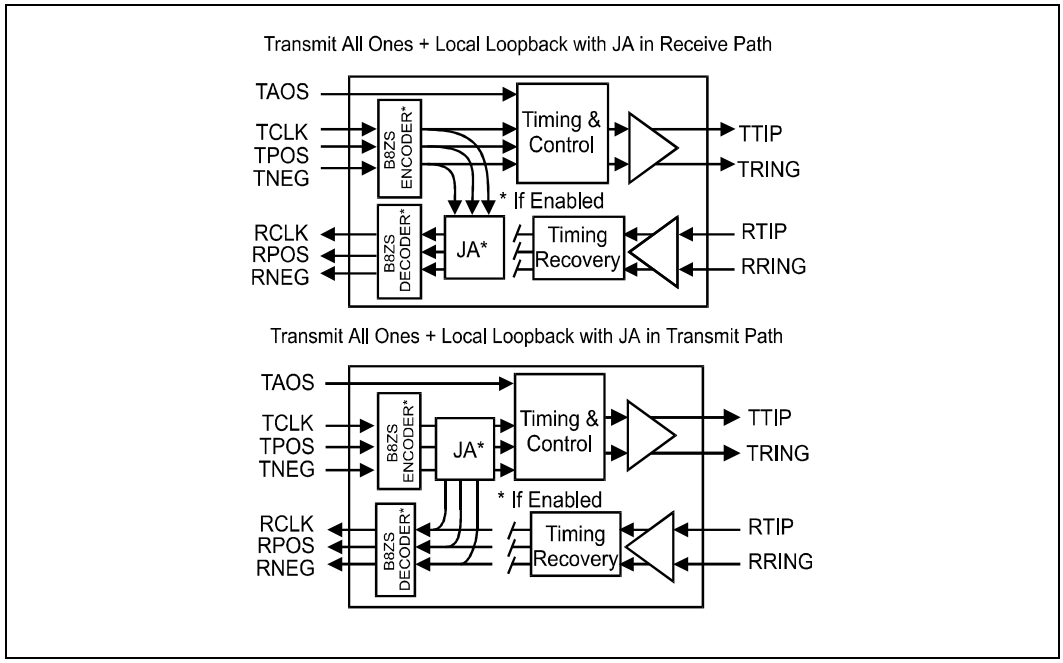
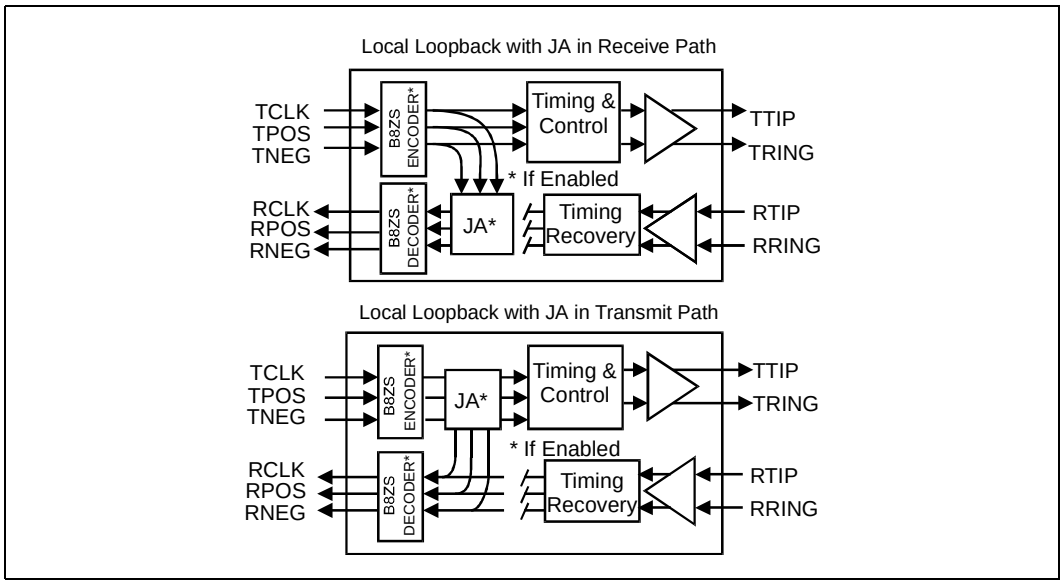


Figure 6. Local Loopback

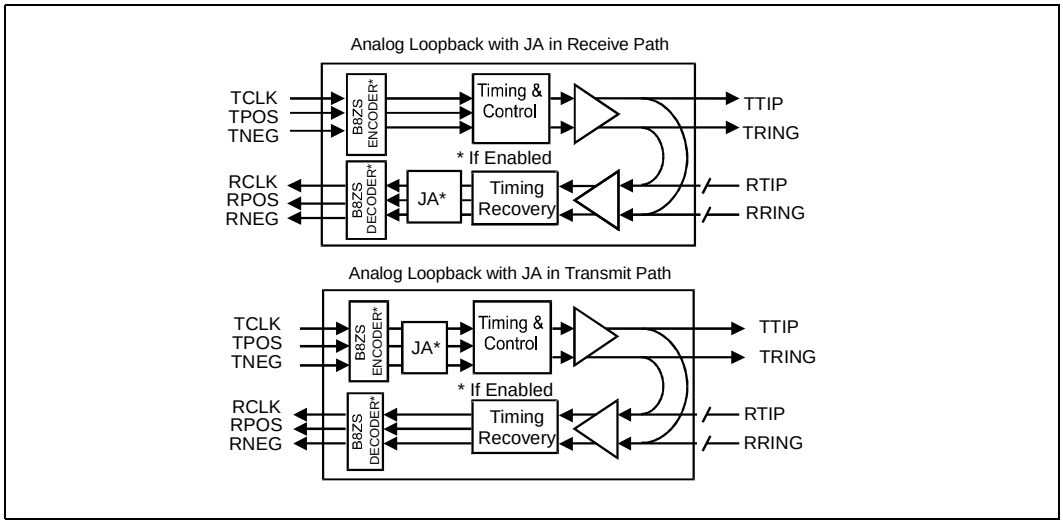


2.7.1.2 Analog Loopback (ALOOP)

See Figure 7. Analog loopback (ALOOP) exercises the maximum number of functional blocks. ALOOP operation disconnects the RTIP/RRING inputs from the line and routes the transmit outputs back into the receive inputs. This tests the encoders/decoders, jitter attenuator, transmitter, receiver and timing recovery sections.

In Hardware mode, ALOOP becomes active when the LLOOP pin is floating (i.e. Midrange). In Host mode, setting bit CR2.EALOOP = 1 commands ALOOP. Note that ALOOP overrides all other loopback modes.

Figure 7. Analog Loopback



2.7.1.3 Remote Loopback (RLOOP)

See Figure 8. When RLOOP is active, the device ignores the transmit data and clock inputs (TCLK and TPOS/TNEG or TDATA), and bypasses the in-line encoders/decoders. The RPOS/RNEG or RDATA outputs loop back through the transmit circuits to TTIP and TRING at the RCLK frequency. The RLOOP command does not affect the receiver circuits which continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line.

In Host mode, command RLOOP by writing a 1 to bit CR2.ERLOOP. In Hardware mode, RLOOP is commanded by setting the RLOOP pin High.

2.7.1.4 Network Loopback (NLOOP)

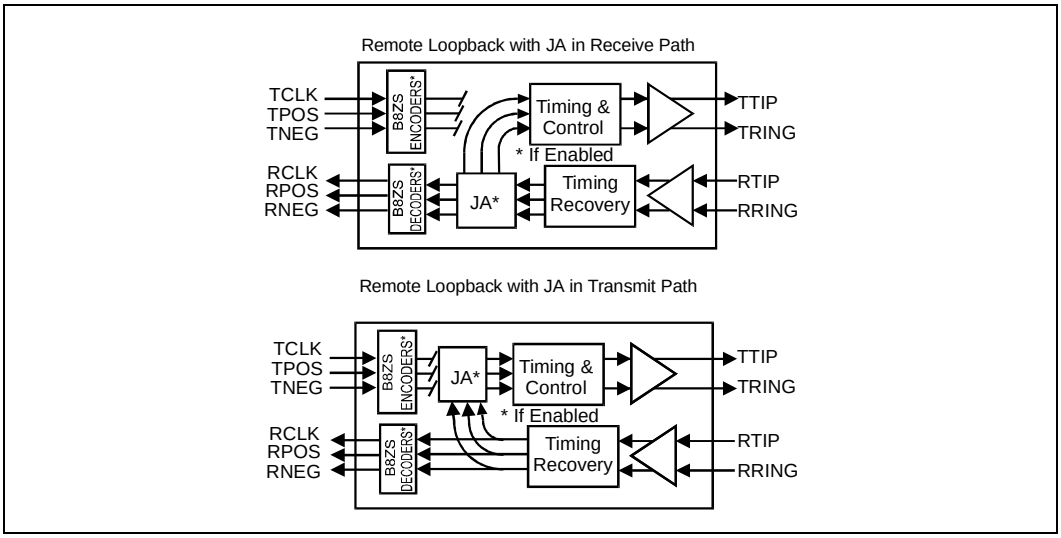
NLOOP can be initiated only when the Network loopback detect function is enabled. With NLOOP detection enabled, the receiver looks for the NLOOP data patterns (00001 = enable, 001 = disable) in the input data stream. The LXT362 responds to both framed and unframed NLOOP patterns.

When the receiver detects the NLOOP enable data pattern repeated for a minimum of five seconds, loopback is activated. Once activated, operation is identical to Remote loopback (RLOOP).

In Host mode, setting bit CR2.ENLOOP = 1 enables NLOOP detection. In Hardware mode, setting the RLOOP pin to Midrange enables NLOOP detection.

NLOOP is disabled upon reception of the 001 pattern for five seconds, or by activating RLOOP or ALOOP, or by disabling NLOOP detection. Note that the LXT362 enters Dual loopback mode (DLOOP) when both NLOOP and LLOOP functions are selected.

Figure 8. Remote Loopback

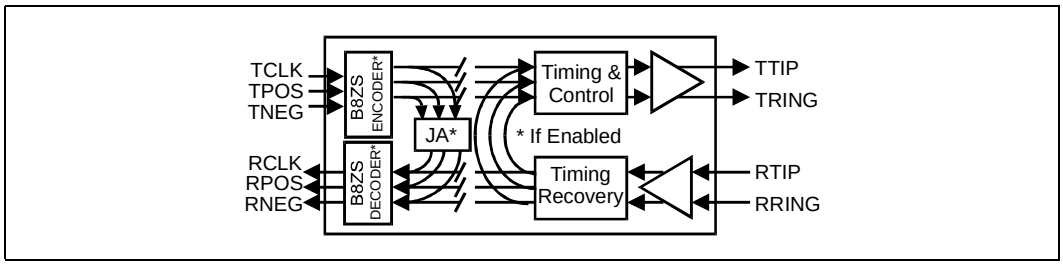


2.7.1.5 Dual Loopback (DLOOP)

See Figure 9. In Hardware mode, DLOOP is selected by setting both the RLOOP and LLOOP pins High. In Host mode set bits CR2.ERLOOP = 1 and CR2.ELLOOP = 1. In DLOOP mode, the transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) loop back through the Jitter

Attenuator (unless disabled) to RCLK and RPOS/RNEG or RDATA. The data and clock recovered from the twisted-pair line loop back through the transmit circuits to TTIP and TRING without jitter attenuation.

Figure 9. Dual Loopback



2.7.2 Internal Pattern Generation and Detection

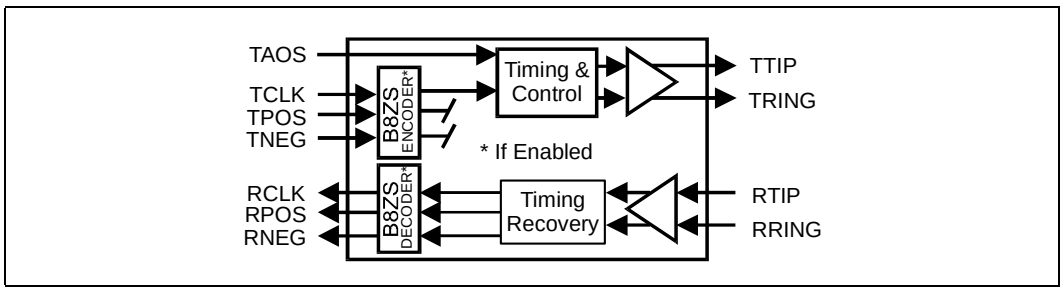
2.7.2.1 Transmit All Ones (TAOS)

See Figure 10. When TAOS is active, the transceiver ignores the TPOS and TNEG inputs and transmits a continuous stream of 1's at the TCLK frequency. When TCLK is not supplied, TAOS timing is derived from MCLK. This can be used as the Alarm Indication Signal (AIS–also called the Blue Alarm).

Both TAOS and LLOOP can operate simultaneously as shown in Figure 5, however, RLOOP inhibits TAOS. When both TAOS and LLOOP are active, TCLK and TPOS/TNEG loop back to RCLK and RPOS/RNEG (through the jitter attenuator if enabled), and the all ones pattern is also routed to TTIP/TRING.

In Host mode, TAOS is activated when bit CR2.ETAOS = 1. In Hardware mode, setting the TAOS pin High activates TAOS.

Figure 10. TAOS Data Path



2.7.2.2 Quasi-Random Signal Source (QRSS)

See Figure 11. The Quasi-Random Signal Source (QRSS) is a 2^{20}-1 pseudo-random bit sequence (PRBS) with no more than 14 consecutive zeros.

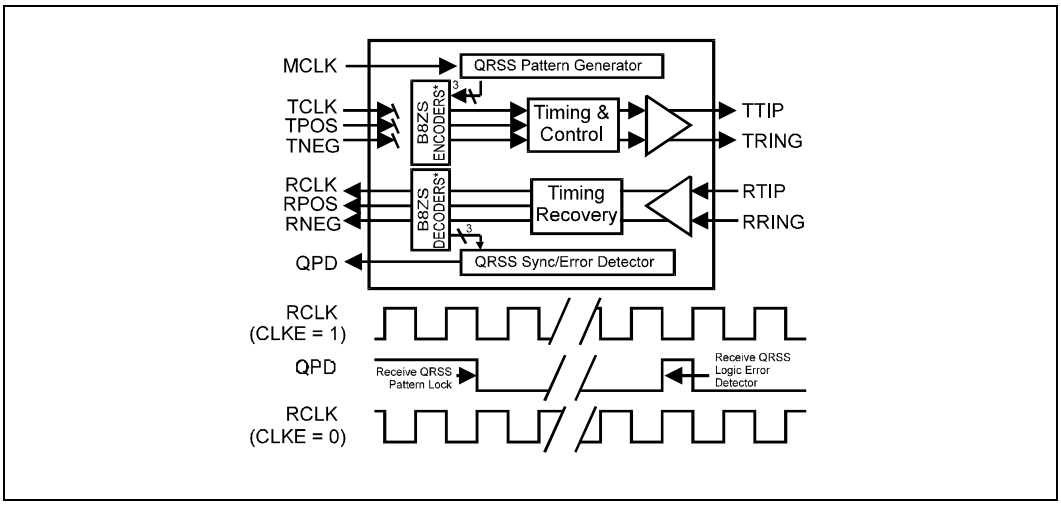
Both Hardware and Host Modes allow QRSS mode. The QRSS pattern is normally locked to TCLK, however, if there is no TCLK, MCLK is the clock source. Bellcore Pub 62411 defines the T1 QRSS transmit format.

With QRSS transmission enabled, it is possible to insert a logic error into the transmit data stream by causing a Low-to-High transition on the INSLER pin. However, if no logic or bit errors are to be inserted into the QRSS pattern, INSLER must remain Low. Logic Error insertion waits until the next bit if the current bit is “jammed”. When there are more than 14 consecutive 0s, the output is jammed to a 1.

A Low-to-High transition on the INSBPV pin will insert a bipolar violation in the QRSS pattern. Note that the BPV insertion occurs regardless of whether the device is in Bipolar or Unipolar operating mode.

In Hardware mode, connecting the TAOS pin to Midrange enables QRSS transmission. In Host mode, setting bits CR2.EPAT0 = 0 and CR2.EPAT1=1 enables QRSS.

Figure 11. QRSS Mode



Selecting QRSS mode also enables QRSS Pattern Detection (QPD) in the receive path. The QRSS pattern is synchronized when there are fewer than four errors in 128 bits. After achieving synchronization the device drives the $\overline{\text{QPD}}$ pin Low. In the QRSS mode, any subsequent bit error in the QRSS pattern causes $\overline{\text{QPD}}$ to go High for half an RCLK clock cycle. Note that in Host mode, the precise relationship between $\overline{\text{QPD}}$ and RCLK depends on the CLKE pin. When CLKE is Low, $\overline{\text{QPD}}$ goes High while RCLK is High; when CLKE is High, $\overline{\text{QPD}}$ goes High while RCLK is Low. The edge of $\overline{\text{QPD}}$ can serve as a trigger for an external bit-error counter. A LOS condition or a loss of QRSS synchronization will cause $\overline{\text{QPD}}$ to go High continuously. In this case, and with either Unipolar mode or the encoders/decoders enabled, the BPV pin indicates BPVs, CODEVs or ZEROVs.

Host mode can generate an interrupt to indicate that QRSS detection has occurred, or that synchronization is lost. This interrupt is enabled when bit ICR.CQRSS = 0. If the $\overline{\text{QPD}}$ signal is used to trigger a bit error counter, the interrupt could be used to start or reset the error counter.

The PSR.QRSS bit provides an indication of QRSS pattern synchronization. This bit goes to 0 when the QRSS pattern is not detected (*i.e.*, when there are more than four errors in 128 bits). The TQRSS bit in the Transition Status Register indicates that QRSS status has changed since the last QRSS Interrupt Clear command.

2.7.2.3 In-Band Network Loop Up or Down Code Generator

In-band Network Loop Up or Loop Down code transmission is available in Host mode only. The Loop Up code is 00001; Loop Down code is 001. A Loop Up code transmission occurs when bits CR2.EPAT0 = 1 and CR2.EPAT1 = 0. A Loop Down code transmission occurs when CR2.EPAT0 = 1 and CR2.EPAT1 = 1.

With this mode is active, logic errors and bipolar violations can be inserted into the transmit data stream. Inserting a logic error requires a Low-to-High transition of the INSLER pin. If no logic or bit errors are to be inserted, INSLER must remain Low. A Low-to-High transition on the INSBPV pin will insert a bipolar violation, regardless of whether the device is in the Unipolar or Bipolar mode of operation.

2.7.3 Error Insertion and Detection

2.7.3.1 Bipolar Violation Insertion (INSBPV)

The INSBPV function is available in Unipolar mode. Sampling occurs on the falling edge of TCLK. A Low-to-High transition on the INSBPV pin inserts a BPV on the next available mark, except in the four following situations:

- When zero suppression (B8ZS) is not violated
- When LLOOP and TAOS are both active. In this case, the BPV is looped back to the BPV pin and the line driver transmits all ones with no violation.
- When RLOOP is active
- When NLOOP is active

Note that when the LXT362 is configured to transmit internally generated data patterns (QRSS or NLOOP), a BPV can be inserted on the transmit pattern regardless of whether the device is in the Unipolar or Bipolar mode of operation.

2.7.3.2 Logic Error Insertion (INSLER)

When transmission of QRSS or NLOOP Up/Down codes are active, a logic error is inserted into the transmit data pattern when a Low-to-High transition occurs on the INSLER pin. Note that in QRSS mode, logic error insertion is inhibited on a jammed bit (i.e. a bit forced to one to suppress transmission of more than 14 consecutive zeros).

The transceiver treats data patterns the same way it treats data applied to TPOS/TNEG. Therefore, the inserted logic error will follow the data flow path as defined by the active loopback mode

2.7.3.3 Logic Error Detection (QPD)

After pattern synchronization is detected in QRSS mode, subsequent logic errors are reported on the $\overline{\text{QPD}}$ pin. If a logic error occurs, the $\overline{\text{QPD}}$ pin goes High for half an RCLK cycle. Note that in Host mode, the precise relationship between $\overline{\text{QPD}}$ and RCLK depends on the value of the CLKE pin. When CLKE is Low, $\overline{\text{QPD}}$ goes High while RCLK is High; when CLKE is High, $\overline{\text{QPD}}$ goes High while RCLK is Low. To tally logic errors, connect an error counter to $\overline{\text{QPD}}$. A continuous High on this pin indicates loss of either the QRSS pattern lock or a LOS condition. “Quasi-Random Signal Source (QRSS)” on page 24 provides additional details on QRSS pattern lock criteria.

2.7.3.4 Bipolar Violation Detection (BPV)

When the internal encoders/decoders are disabled or when configured in Unipolar mode, bipolar violations are reported at the BPV pin. BPV goes High for a full clock cycle to indicate receipt of a BPV. When the encoders/decoders are enabled, the LXT362 does not report bipolar violations due to the line coding scheme.

2.7.4 Alarm Condition Monitoring

2.7.4.1 Loss of Signal (LOS)

The receiver LOS monitor loads a digital counter at the RCLK frequency. The count increments with each received 0 and the counter resets to 0 on receipt of a 1. When the count reaches “n” 0s, the LOS flag goes High, and the MCLK replaces the recovered clock at the RCLK output in a smooth transition. For Hardware mode, the number of 0s, n = 175. In Host mode, either 175 or 2048 may be selected by setting bit CR4.LOS2048.

When the received signal has 12.5% 1’s density (16 marks in a sliding 128-bit period, with fewer than 100 consecutive 0s), the LOS flag returns Low and the recovered clock replaces MCLK at the RCLK output in another smooth transition.

During LOS, the device sends received data to the RPOS/RNEG pins (or RDATA in Unipolar mode). In Hardware and Host modes, the LOS pin goes High when a LOS condition occurs. In Host mode, bit PSR.LOS =1 indicates a LOS condition, and will generate an interrupt if enabled.

2.7.4.2 Alarm Indication Signal Detection (AIS)

This function is only available in Host mode. The receiver detects an AIS pattern when it receives fewer than three 0s in any string of 2048 bits. The device clears the AIS condition when it receives three or more 0s in a string of 2048 bits.

The AIS bit in the Performance Status Register indicates AIS detection. Whenever the AIS status changes, bit TSR.TAIS =1. Unless masked, a change of AIS status generates an interrupt.

2.7.4.3 Driver Failure Monitor Open (DFMO)

This function is only available in Host mode. The DFMO bit is available in the Performance Status Register to indicate an open condition on the lines. DFMO can generate an interrupt to the host controller. The Transition Status Register bit TDFMO indicates a transition in the status of the bit. Writing a 1 to ICR.CDFMO will clear or mask the interrupt.

2.7.4.4 Elastic Store Overflow/Underflow (ESOVR and ESUNF)

This function is only available in Host mode. When the bit count in the Elastic Store (ES) is within two bits of overflowing or underflowing the ES adjusts the output clock by $^{1}/_{8}$ of a bit period. The ES provides an indication of overflow and underflow via bits TRS.ESOVR and TSR.ESUNF. These are “sticky bits” and will stay set to 1 until the host controller reads the register. These interrupts can be cleared or masked by writing a 1 to the bits ICR.CESO and ICR.CESU, respectively.

2.7.5 Other Diagnostic Reports

2.7.5.1 Receive Line Attenuation Indication

This function is only available in Host mode. The Equalizer Status Register (ESR) provides an approximation of the line attenuation encountered by the device. The four MSBs of the register (ESR.LATN7:4) indicate line attenuation in approximately 2.9 dB steps for the receive equalizer. For instance, if ESR.LATN7:4 is 10 (decimal), then the receiver is seeing a signal attenuated by approximately 29 dB (2.9 dB x 10) of cable loss.

2.7.5.2 Built-In Self Test (BIST)

The BIST function in only available in Host mode. The BIST exercises the internal circuits by providing an internal QRSS pattern, running it through the encoders and the transmit drivers then looping it back through the receive equalizer, jitter attenuator and decoders to the QRSS pattern detection circuitry. The BIST is initiated by setting bit CR3.SBIST = 1. If all the blocks in this data path operate correctly, the receive pattern detector locks onto the pattern. It then pulls $\overline{\text{INT}}$ Low and sets the following bits:

- TSR.TQRSS = 1
- PSR.QRSS = 1
- PSR.BIST = 1

The $\overline{\text{QPD}}$ pin also indicates completion status of the test. Initiating the BIST forces $\overline{\text{QPD}}$ High. During the test, it remains High until the test finishes successfully, at which time it goes Low.

The most reliable test will result when a separate TCLK and MCLK are applied and the Line Build-Out (LBO) is set to -22.5 dB (CR1.EC4:1 = 011x).

3.0 Register Definitions

The LXT362 contains five read/write and three read-only registers that are accessible in Host mode via the serial I/O port. Table 7 lists the LXT362 register addresses. Only bits A6 through A1 of the address byte are valid (the address decoder ignores bits A7 and A0) while A0 functions as the read/write (R/$\overline{W}$) bit. Table 8 identifies the name of each register bit. Table 9 through Table 17 describe the function of the bits in each register.

Note that upon power-up or reset, all registers are cleared to 0.

Table 7. Register Addresses

Register		Address[1, 2] A7 - A1
Name	Abbr	
Control #1	CR1	x010000
Control #2	CR2	x010001
Control #3	CR3	x010010
Interrupt Clear	ICR	x010011
Transition Status	TSR	x010100
Performance Status	PSR	x010101
Equalizer Status	ESR	x010110
Control #4	CR4	x010111

1. x = don't care
2. Address A0 is the read/write (R/$\overline{W}$) bit.

Table 8. Register and Bit Summary

Register			Bit							
Name		Type	7	6	5	4	3	2	1	0
Control #1	CR1	R/W	JASEL1	JASEL0	ENCENB	UNIENB	EC4	EC3	EC2	EC1
Control #2	CR2	R/W	RESET	EPAT1	EPAT0	ETAOS	ENLOOP	EALOOP	ELLOOP	ERLOOP
Control #3	CR3	R/W	JA6HZ	reserved[1]	SBIST	EQZMON	reserved[1]	ES64	ESCEN	ESJAM
Interrupt Clear	ICR	R/W	CESU	CESO	CDFMO	*reserved*[2]	CQRSS	CAIS	CNLOOP	CLOS
Transition Status	TSR	R	ESUNF	ESOVR	TDFMO	reserved[1]	TQRSS	TAIS	TNLOOP	TLOS
Performance Status	PSR	R	reserved[1]	BIST	DFMO	reserved[1]	QRSS	AIS	NLOOP	LOS
Equalizer Status	ESR	R	LATN7	LATN6	LATN5	LATN4	reserved[1]	reserved[1]	reserved[1]	reserved[1]
Control #4	CR4	R/W	reserved[1]	reserved[1]	reserved[1]	reserved[1]	reserved[1]	LOS2048	reserved[1]	reserved[1]

1. In writable registers, bits labeled *reserved* should be set to 0 (except as in note 2 below) for normal operation and ignored in read only registers.
2. Write a 1 to this bit for normal operation.

Table 9. Control Register #1 Read/Write, Address (A7-A0) = x010000x

Bit	Name	Function	Jitter Attenuator		
			JASEL0	JASEL1	Position
0	EC1	Sets T1 mode and equalizer (see Table 10 below for control codes).	1	0	Transmit
1	EC2		1	1	Receive
2	EC3		0	X	Disabled
3	EC4				
4	UNIENB	1 = Enable Unipolar I/O mode and allow insertion/detection of BPVs. 0 = Enable Bipolar I/O mode			
5	ENCENB	1 = Enable B8ZS encoders/decoders and force Unipolar I/O mode. 0 = Disable B8ZS encoders/decoders			
6	JASEL0	Select jitter attenuation circuitry position in data path or disables the JA. See right hand section of table for codes. ↗			
7	JASEL1				

Table 10. Equalizer Control Input Settings

EC4	EC3	EC2	EC1[1]	Function	Pulse	Cable	Gain
0	0	0	0	T1 Long Haul	0.0 dB pulse	100 Ω TP	36 dB
0	0	1	0	T1 Long Haul	-7.5 dB pulse	100 Ω TP	36 dB
0	1	0	0	T1 Long Haul	-15.0 dB pulse	100 Ω TP	36 dB
0	1	1	0	T1 Long Haul	-22.5 dB pulse	100 Ω TP	36 dB
0	0	0	1	T1 Long Haul	0.0 dB pulse	100 Ω TP	26 dB
0	0	1	1	T1 Long Haul	-7.5 dB pulse	100 Ω TP	26 dB
0	1	0	1	T1 Long Haul	-15.0 dB pulse	100 Ω TP	26 dB
0	1	1	1	T1 Long Haul	-22.5 dB pulse	100 Ω TP	26 dB
1	0	0	1	D4 Short Haul	6 V pulse	100 Ω TP	12 dB
1	0	1	1	T1 Short Haul	0-133 ft / 0.6 dB	100 Ω TP	12 dB
1	1	0	0	T1 Short Haul	133-266 ft / 1.2 dB	100 Ω TP	12 dB
1	1	0	1	T1 Short Haul	266-399 ft / 1.8 dB	100 Ω TP	12 dB
1	1	1	0	T1 Short Haul	399-533 ft / 2.4 dB	100 Ω TP	12 dB
1	1	1	1	T1 Short Haul	533-655 ft / 3.0 dB	100 Ω TP	12 dB

1. EC1 sets the receive equalizer gain (EGL) for T1 long-haul operation.

Table 11. Control Register #2 Read/Write, Address (A7-A0) = x010001x

Bit	Name	Function	Pattern		
			EPAT0	EPAT1	Selected
0	ERLOOP[1]	1 = Enable Remote loopback mode 0 = Disable Remote loopback mode	0	0	Transmit TPOS/TNEG
1	ELLOOP[1]	1 = Enable Local loopback mode 0 = Disable Local loopback mode	0	1	Detect and transmit QRSS
2	EALOOP	1 = Enable Analog loopback mode 0 = Disable Analog loopback mode	1	0	In-band Loop Up Code 00001
3	ENLOOP	1 = Enable Network loopback detection 0 = Disable Network loopback detection	1	1	In-band Loop Down Code 001
4	ETAOS	1 = Enable Transmit All Ones 0 = Disable Transmit All Ones			
5	EPAT0	Selects internal data pattern transmission. See right hand section of table for codes. ↗			
6	EPAT1				
7	RESET	1 = Reset device states and clear all registers. 0 = Reset complete.			

1. To enable Dual loopback (DLOOP), set both ERLOOP = 1 and ELLOOP = 1.

Table 12. Control Register #3 Read/Write, Address (A7-A0) = x010010x

Bit	Name	Description
0	ESJAM	1 = Disable jamming of Elastic Store read out clock ($^1/_8$ bit-time adjustment for over/underflow). 0 = Enable jamming of Elastic Store read out clock
1	ESCEN	1 = Center ES pointer for a difference of 16 or 32, depending on depth (clears automatically). 0 = Centering completed
2	ES64	1 = Set elastic store depth to 64 bits. 0 = Set elastic store depth to 32 bits.
3	-	Reserved. Set to 0 for normal operation.
4	EQZMON	1 = Configure receiver equalizer for monitor mode application (DSX-1 monitor). 0 = Configure receiver equalizer for normal mode application
5	SBIST	1 = Start Built-In Self Test. 0 = Built-In Self Test complete.
6	-	Reserved. Set to 0 for normal operation.
7	JA6HZ	1 = Set bandwidth of jitter attenuation loop to 6 Hz. 0 = Set bandwidth of jitter attenuation loop to 3 Hz.

Table 13. Interrupt Clear Register Read/Write, Address (A7-A0) = x010011x

Bit	Name	Function[1]
0	CLOS	1 = Clear/Mask Loss of Signal interrupt. 0 = Enable Loss of Signal interrupt.
1	CNLOOP	1 = Clear/Mask Network loopback interrupt. 0 = Enable Network loopback interrupt.
2	CAIS	1 = Clear/Mask Alarm Indication Signal interrupt. 0 = Enable Alarm Indication Signal interrupt.
3	CQRSS	1 = Clear/Mask Quasi-Random Signal Source interrupt. 0 = Enable Quasi-Random Signal Source interrupt.
4	-	Reserved. Set to 1 for normal operation.
5	CDFMO	1 = Clear/Mask Driver Failure Monitor Open interrupt. 0 = Enable Driver Failure Monitor Open interrupt.
6	CESO	1 = Clear/Mask Elastic Store Overflow interrupt. 0 = Enable Elastic Store Overflow interrupt.
7	CESU	1 = Clear/Mask Elastic Store Underflow interrupt. 0 = Enable Elastic Store Underflow interrupt.

1. Leaving a 1 of in any of these bits masks the associated interrupt.

Table 14. Transition Status Register Read Only, Address (A7-A0) = x010100x

Bit	Name	Function
0	TLOS	1 = Loss of Signal (LOS) has changed since last clear LOS interrupt occurred. 0 = No change in status.
1	TNLOOP	1 = NLOOP has changed since last clear NLOOP interrupt occurred. 0 = No change in status.
2	TAIS	1 = AIS has changed since last clear AIS interrupt occurred. 0 = No change in status.
3	TQRSS	1 = QRSS has changed since last clear QRSS interrupt occurred[1]. 0 = No change in status.
4	-	Reserved. Ignore.
5	TDFMO	1 = DFMO has changed since last clear DFMS interrupt occurred. 0 = No change in status.
6	ESOVR	1 = ES overflow status sticky bit[2]. 0 = No change in status.
7	ESUNF	1 = ES underflow status sticky bit[2]. 0 = No change in status.

1. A QRSS transition indicates receive QRSS pattern sync or loss. A simple error in QRSS pattern is not reported as a transition.
2. Tripping the overflow or underflow indicator in the ES sets the ESOVR/ESUNF status bit(s). Reading the Transition Status Register clears these bits. Setting CESO and CESU in the Interrupt Clear Register masks these interrupts.

Table 15. Performance Status Register Read Only, Address (A7-A0) = x010101x

Bit	Name	Function
0	LOS	1 = Loss of Signal occurred. 0 = Loss of Signal did not occur.
1	NLOOP	1 = Network loopback active. 0 = Network loopback not active.
2	AIS	1 = Alarm Indicator Signal detected. 0 = Alarm Indicator Signal not detected.
3	QRSS	1 = Quasi-Random Signal Source pattern detected. 0 = Quasi-Random Signal Source pattern not detected.
4	-	Reserved. Ignore.
5	DFMO	1 = Driver Failure Monitor Open detected. 0 = Driver Failure Monitor Open not detected.
6	BIST	1 = Built-In Self Test passed. 0 = Built-In Self Test did not pass (or was not run).
7	-	Reserved. Ignore.

Table 16. Equalizer Status Register Read Only, Address (A7-A0) = x010110x

Bit	Name	Function
0	-	Reserved. Ignore.
1	-	Reserved. Ignore.
2	-	Reserved. Ignore.
3	-	Reserved. Ignore.
4	LATN4	Receive Line Attenuation Indicators. Convert this binary output to a decimal number and multiply by 2.9 dB to determine the approximate cable attenuation as seen by the receiver. For example, if LATN7:4 = 1010 $_{BIN}$ (= 10 $_{DEC}$), then the receiver is seeing a signal attenuated by approximately 29 dB (2.9 dB x 10) of cable. This approximation assumes that a 3 V pulse was transmitted.
5	LATN5	
6	LATN6	
7	LATN7	

Table 17. Control Register #4 Read/Write, Address (A7-A0) = x010111x

Bit	Name	Function
0	-	Reserved. Set to 0 for normal operation, ignore when reading
1	-	Reserved. Set to 0 for normal operation, ignore when reading
2	LOS2048	1 = Set LOS detection threshold to 2048 consecutive zeros. 0 = Set LOS detection threshold to 175 consecutive zeros.
3	-	Reserved. Set to 0 for normal operation, ignore when reading
4	-	Reserved. Set to 0 for normal operation, ignore when reading
5	-	Reserved. Set to 0 for normal operation, ignore when reading
6	-	Reserved. Set to 0 for normal operation, ignore when reading
7	-	Reserved. Set to 0 for normal operation, ignore when reading

4.0 Application Information

4.1 Transmit Return Loss

Table 18 shows the transmit return loss values for T1 applications. Table 24 on page 39 specifies the receive return loss values.

4.2 Transformer Data

Specifications for transformers are listed in Table 19. A list of transformers recommended for use with the LXT362 are specified in Table 20.

4.3 Application Circuits

Figure 12 and Figure 13 show typical LXT362 applications for Hardware and Host modes of operation.

Table 18. Transmit Return Loss

EC4:1	Xfrmr/Rt	R_L (Ω)	C_L (pF)	Return Loss (dB)
Refer to Table 10	1:2 / 9.1 Ω	100	0	16
			470	17
	1:1.15[1] / 0 Ω	100	0	2
			470	2
1001 (D4 Mode)	1:2[2] / 0 Ω	100	0	1
			470	1

1. A 1:1.15 transmit transformer keeps the total transceiver power dissipation at a low level, a 0.47 µF DC blocking capacitor must be placed on TTIP or TRING.
2. A 0.47 µF DC blocking capacitor must be placed on TTIP or TRING.

Table 19. Transformer Specifications for LXT362

Tx/Rx	Frequency MHz	Turns Ratio	Primary Inductance µH (minimum)	Leakage Inductance µH (max)	Interwinding Capacitance pF (max)	DCR Ω (maximum)	Dielectric Breakdown V (minimum)
Tx	1.544	1:1.15	600	0.80	60	0.90 pri, 1.70 sec	1500 V_{RMS}[1]
	1.544	1:2	600	0.80	60	0.70 pri, 1.20 sec	1500 V_{RMS}[1]
Rx	1.544	1:1	600	1.10	60	1.10 pri, 1.10 sec	1500 V_{RMS}[1]

1. Some applications require transformers with a center tap (Long-Haul applications with DC current in the T1 loop).

Table 20. Recommended Transformers for LXT362

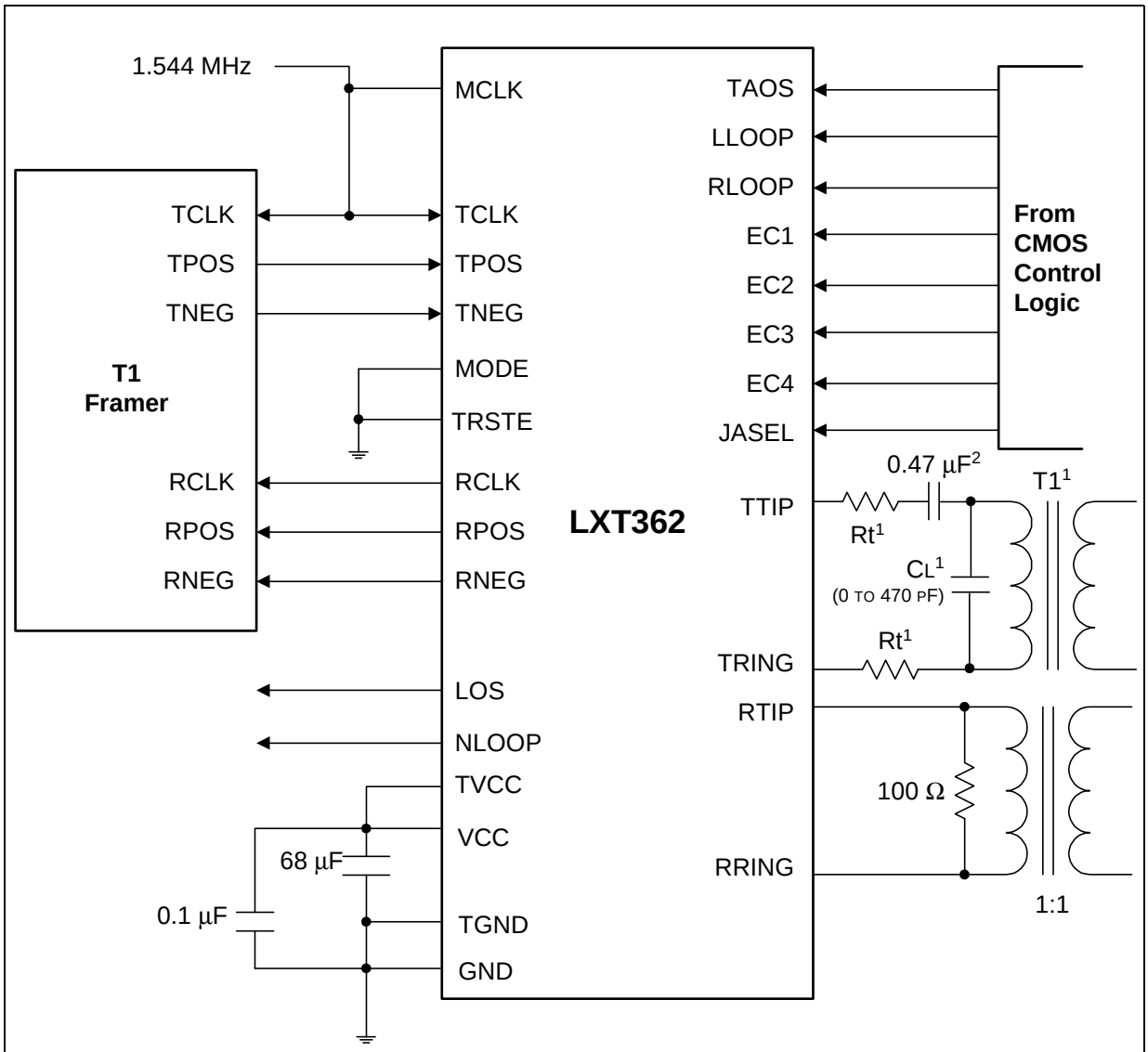
Tx/Rx	Turns Ratio	Part Number	Manufacturer
Tx	1:1.15	PE-65388	Pulse Engineering
		PE-65770	
		16Z5952	Vitec
	1:2	PE-65351	Pulse Engineering
		PE-65771	
		0553-5006-IC	Bell-Fuse
		66Z-1308	Fil-Mag
		671-5832	Midcom
		67127370	Schott Corp
		67130850	
		TD61-1205D	HALO (combination Tx/Rx set)
		TG26-1205NI	HALO (surface mount dual transformer 1CT:2CT & 1CT:2CT)
		TG48-1205NI	HALO (surface mount dual transformer 1CT:2CT & 1:1)
		16Z5946	Vitec
Rx	1:1	FE 8006-155	Fil-Mag
		671-5792	Midcom
		PE-64936	Pulse Engineering
		PE-65778	
		67130840	Schott Corp
		67109510	
		TD61-1205D	HALO (combination Tx/Rx set)
		16Z5936	Vitec
		16Z5934	

4.3.1 Hardware Mode Circuit

Figure 12 shows a typical LXT362 Hardware mode application. See Table 18 through Table 20 to select the transformers (T1 and T2), resistors (Rt and RL) and capacitor (CL) needed for this application.

Note that if the application includes surge protection, such as a varistor or sidactor on the TTIP/TRING lines, it may be necessary to reduce the value of the capacitor CL or eliminate it completely. Excessive capacitance at CL will distort the transmitted signals.

Figure 12. Typical Hardware Mode Application



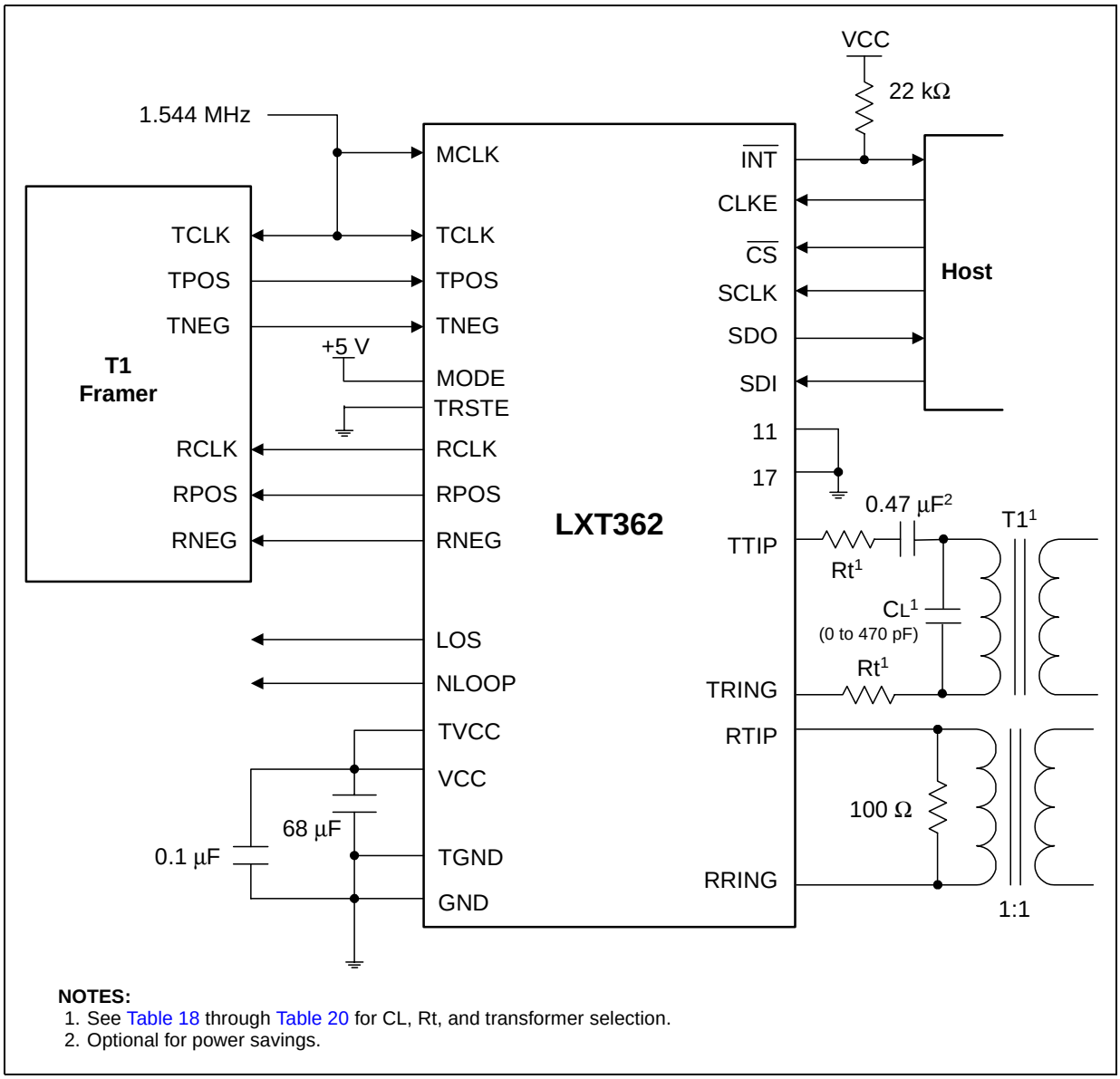
NOTES:
1. See Table 18 through Table 20 for CL, Rt, and transformer selection.
2. Optional for power savings.

4.3.2 Host Mode Circuit

Figure 13 shows an application using the LXT362 in Host mode. See Table 18 through Table 20 to select the transformers (T1 and T2), resistors (Rt and RL) and capacitor (CL) needed for this application.

Note that if the application includes surge protection, such as a varistor or sidactor on the TTIP/TRING lines, it may be necessary to reduce the value of the capacitor CL or eliminate it completely. Excessive capacitance at CL will distort the transmitted signals.

Figure 13. Typical Host Mode Application



NOTES:
1. See Table 18 through Table 20 for CL, Rt, and transformer selection.
2. Optional for power savings.

5.0 Test Specifications

Note: Table 21 through Table 28 and Figure 14 through Figure 20 represent the performance specifications of the LXT362 and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Table 23 through Table 28 are guaranteed over the recommended operating conditions specified in Table 22.

Table 21. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Unit
DC supply (reference to GND)	VCC, TVCC	–	6.0	V
Input voltage, any pin [1]	VIN	GND - 0.3 V	VCC + 0.3 V	V
Input current, any pin [2]	IIN	- 10	10	mA
Storage Temperature	TSTG	-65	150	° C

Caution: Exceeding these values may cause permanent damage.

Caution: Functional operation under these conditions is not implied.

Caution: Exposure to maximum rating conditions for extended periods may affect device reliability.

1. TVCC and VCC must not differ by more than 0.3 V during operation. TGND and GND must not differ by more than 0.3 V during operation.
2. Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TVCC, and TGND can withstand continuous currents of up to 100 mA.

Table 22. Recommended Operating Conditions

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Conditions
DC Supply [2]		VCC, TVCC	4.75	5.0	5.25	V	
Ambient Operating Temperature		TA	-40	–	85	° C	
Total Power Dissipation[3]	Short Haul	PD	–	450	540	mW	100% mark density
		PD	–	300	360	mW	50% mark density
	Long Haul	PD	–	350	425	mW	100% mark density
		PD	–	250	300	mW	50% mark density
	D4	PD	–	400	485	mW	100% mark density
		PD	–	275	330	mW	50% mark density

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. TVCC and VCC must not differ by more than 0.3 V.
3. Power dissipation while driving 100 Ω load over operating range. Includes power dissipation on device and load. Digital levels are within 10% of the supply rails and digital outputs driving a 50 pF capacity load, R_L=9.1, T1=1:2.

Table 23. Digital Characteristics

Parameter		Sym	Min	Typ	Max	Unit	Test Conditions
High level input voltage [1,2] (pins 1-4, 17, 23-25)[4]		VIH	2.0	–	–	V	
Low level input voltage [1,2] (pins 1-4, 17, 23-25)[4]		VIL	–	–	0.8	V	
High level output voltage [1,2] (pins 6-8, 10, 12, 23, 25)[4]		VOH	2.4	–	–	V	IOUT = 400 µA
Low level output voltage [1,2] (pins 6-8, 10, 12, 23, 25)[4]		VOL	–	–	0.4	V	IOUT = 1.6 mA
High level input voltage [3] (pins 5, 9, 11, 26-28)[4]		VIH	3.5	–	–	V	
Midrange input voltage [3] (pins 5, 9, 11, 26-28)[4]		VIM	2.3	–	2.7	V	
Low level input voltage [3] (pins 5, 9, 11, 26-28)[4]	Host mode Hardware mode	VIL VIL	– –	– –	0.8 1.5	V V	
Input leakage current		ILL	0	–	±50	µA	
Three-state leakage current [1] (all outputs)		I3L	0	–	±10	µA	
TTIP/TRING leakage current (pins 13, 16)[4]		ITR	–	–	±1.2	mA	in Idle and Power Down

1. Functionality of pins 23 and 25 depend on mode. See Host mode and Hardware mode description.
2. Output drivers will output CMOS logic levels into CMOS loads.
3. As an alternative to supplying 2.3 - 2.7 V (Midrange logic level) to these pins, they may be left open.
4. Referenced pin numbers are for the PLCC package. Refer to Figure 2 on page 8 for the corresponding QFP pins.

Table 24. Analog Characteristics

Parameter		Min	Typ[1]	Max	Unit	Test Conditions
Recommended output load on TTIP/TRING		50	–	200	Ω	
AMI Output Pulse Amplitudes	DSX-1, DS1	2.4	3.0	3.6	V	RL = 100 Ω
Jitter added by the transmitter[2]	10 Hz - 8 kHz [3]	–	–	0.02	UI	
	8 kHz - 40 kHz [3]	–	–	0.025	UI	
	10 Hz - 40 kHz[3]	–	–	0.025	UI	
	Broad Band	–	–	0.05	UI	
Receiver sensitivity @ 772 kHz	Mode 1 (EC1 = 1) (Long-Haul)	0	–	26	dB	See Table 10 for Gain Setting
	Mode 2 (EC1 = 0) (Long-Haul)	0	–	36	dB	
	Mode 3 (EC4 = 1) (Short-Haul)	0	–	13.6	dB	
Allowable consecutive zeros before LOS		160	175	190	–	
Input jitter tolerance	10 kHz - 100 kHz	0.4	–	–	UI	0 dB line AT&T Pub 62411
	1 Hz [3]	138	–	–	UI	
Jitter attenuation curve corner frequency [4]		–	3	–	Hz	selectable in data port

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter-free. The Jitter Attenuator is in the receive path or disabled.
3. Guaranteed by characterization; not subject to production testing.
4. Circuit attenuates jitter at 20 dB/decade above the corner frequency.

Figure 14. 1.544 MHz T1 Pulse (DS1 and DSX-1) (See Table 25)

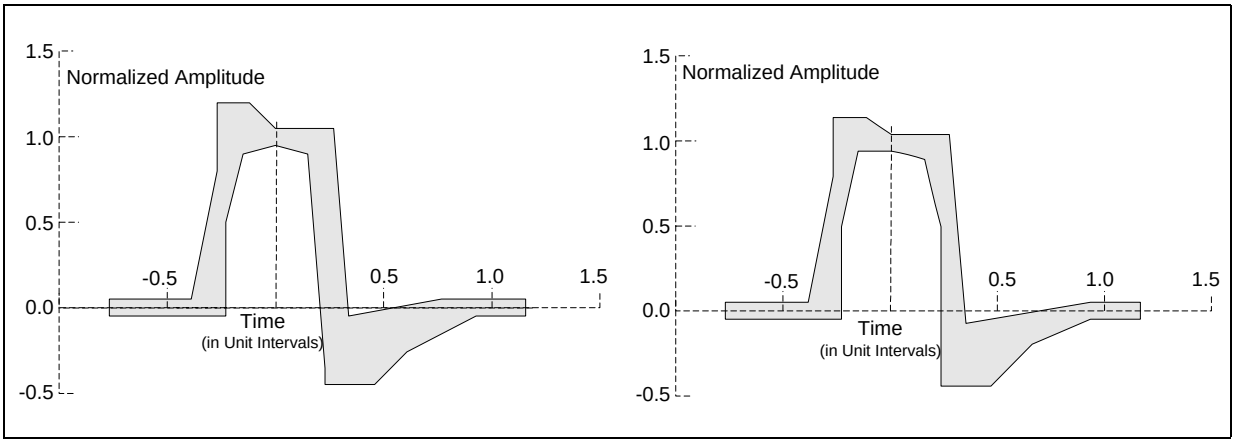


Table 25. 1.544 MHz T1 Pulse Mask Corner Point Specifications

DS1 Template (per ANSI T1. 403-1995)				DSX-1 Template (per ANSI T1. 102-1993)			
Minimum Curve		Maximum Curve		Minimum Curve		Maximum Curve	
Time (UI)	Amplitude	Time (UI)	Amplitude	Time (UI)	Amplitude	Time (UI)	Amplitude
-0.77	-0.05	-0.77	0.05	-0.77	-0.05	-0.77	0.05
-0.23	-0.05	-0.39	0.05	-0.23	-0.05	-0.39	0.05
-0.23	0.50	-0.27	0.80	-0.23	0.50	-0.27	0.80
-0.15	0.90	-0.27	1.20	-0.15	0.95	-0.27	1.15
0.0	0.95	-0.12	1.20	0.0	0.95	-0.12	1.15
0.15	0.90	0.0	1.05	0.15	0.90	0.0	1.05
0.23	0.50	0.27	1.05	0.23	0.50	0.27	1.05
0.23	-0.45	0.34	-0.05	0.23	-0.45	0.35	-0.07
0.46	-0.45	0.77	0.05	0.46	-0.45	0.93	0.05
0.61	-0.26	1.16	0.05	0.66	-0.20	1.16	0.05
0.93	-0.05			0.93	-0.05		
1.16	-0.05			1.16	-0.05		

Table 26. Master and Transmit Clock Timing Characteristics (See Figure 15)

Parameter	Sym	Min	Typ[1]	Max	Unit	Notes
Master clock frequency	MCLK	–	1.544	–	MHz	must be supplied
Master clock tolerance	MCLKt	–	±50	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
Transmit clock frequency	TCLK	–	1.544	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±100	ppm	
1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Table 26. Master and Transmit Clock Timing Characteristics (See Figure 15)

Parameter	Sym	Min	Typ[1]	Max	Unit	Notes
Transmit clock duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	t_{SUT}	50	–	–	ns	
TCLK to TPOS/TNEG hold time	t_{HT}	50	–	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 15. Transmit Clock Timing

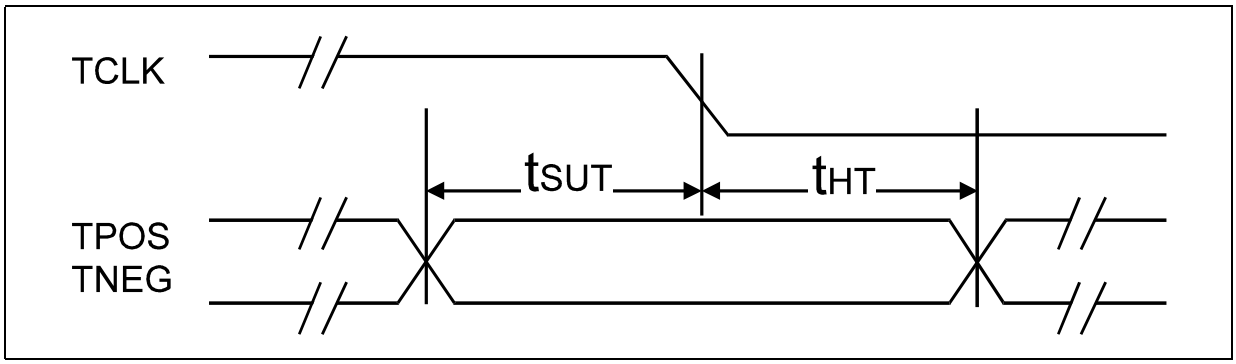


Table 27. Receive Timing Characteristics (See Figure 16)

Parameter	Sym	Min	Typ[1]	Max	Unit
Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
Receive clock pulse width [2, 3]	t_{PW}	–	648	–	ns
Receive clock pulse width high	t_{PWH}	–	324	–	ns
Receive clock pulse width low[1,3]	t_{PWL}	260	324	388	ns
RPOS/RNEG to RCLK rising time	t_{SUR}	–	274	–	ns
RCLK rising to RPOS/RNEG hold time	t_{HR}	–	274	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions.
3. Worst case conditions guaranteed by design only.

Figure 16. Receive Clock Timing

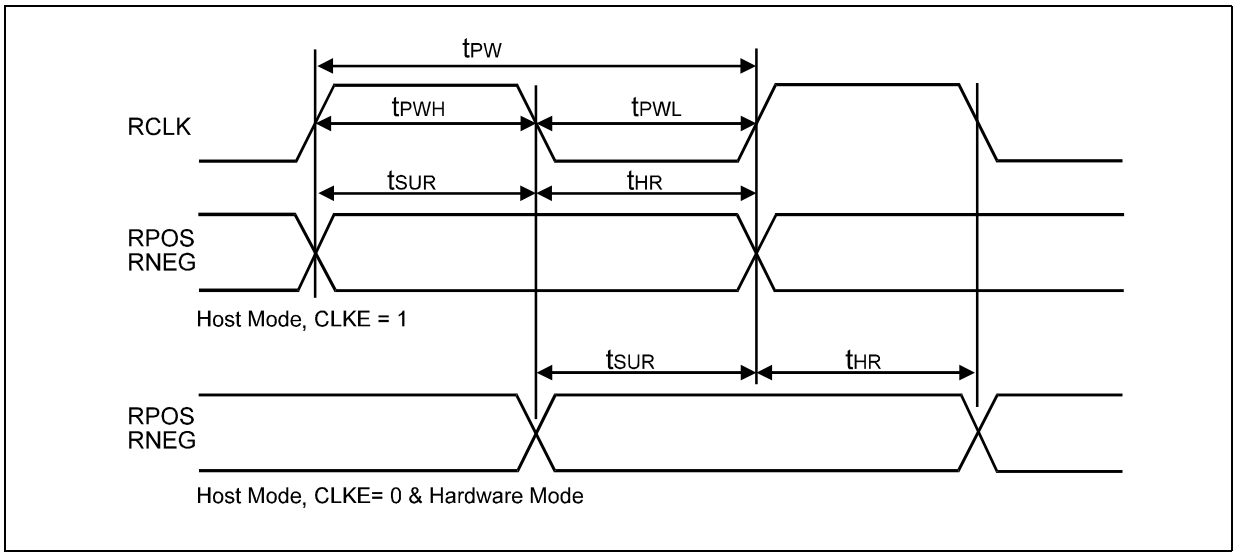


Table 28. Serial I/O Timing Characteristics (See Figure 17 and Figure 18)

Parameter	Sym	Min	Typ[1]	Max	Unit	Parameter
Rise/fall time—any digital output	t_{RF}	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	t_{DC}	50	–	–	ns	
SCLK to SDI hold time	t_{CDH}	50	–	–	ns	
SCLK low time	t_{CL}	240	–	–	ns	
SCLK high time	t_{CH}	240	–	–	ns	
SCLK rise and fall time	t_R, t_F	–	–	50	ns	
$\overline{CS}$ falling edge to SCLK rising edge	t_{CC}	50	–	–	ns	
Last SCLK edge to $\overline{CS}$ rising edge	t_{CCH}	50	–	–	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	–	–	ns	
SCLK to SDO valid time	t_{CDV}	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high-Z	t_{CDZ}	–	100	–	ns	

1. Typical figures are at 25 ℃ and are for design aid only; not guaranteed and not subject to production testing.

Figure 17. Serial Data Input Timing Diagram

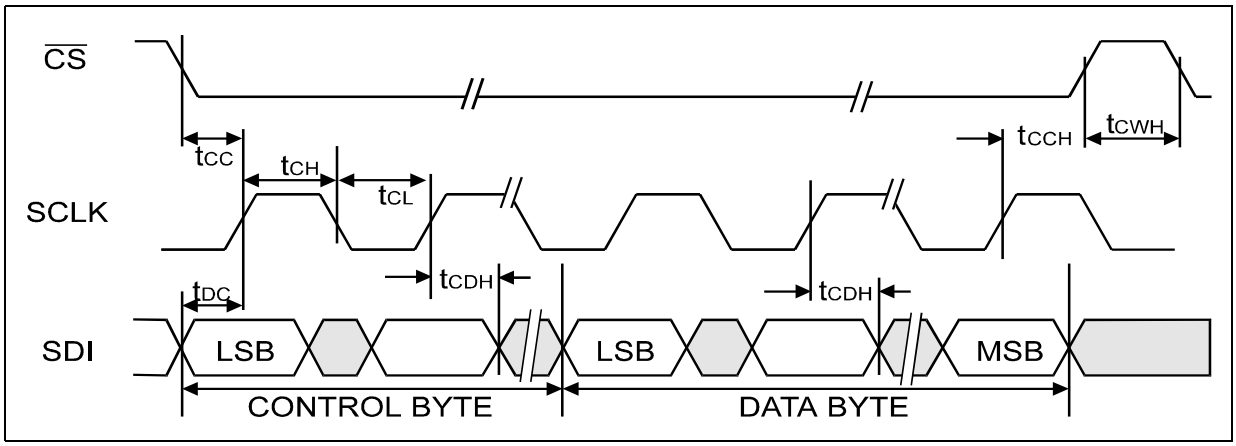


Figure 18. Serial Data Output Timing Diagram

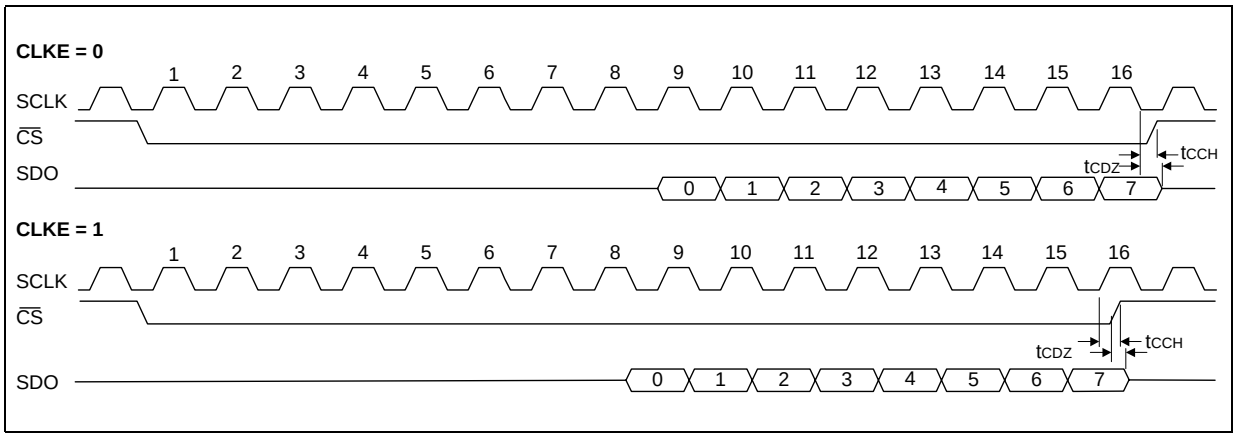


Figure 19. Typical T1 Jitter Tolerance at 36 dB

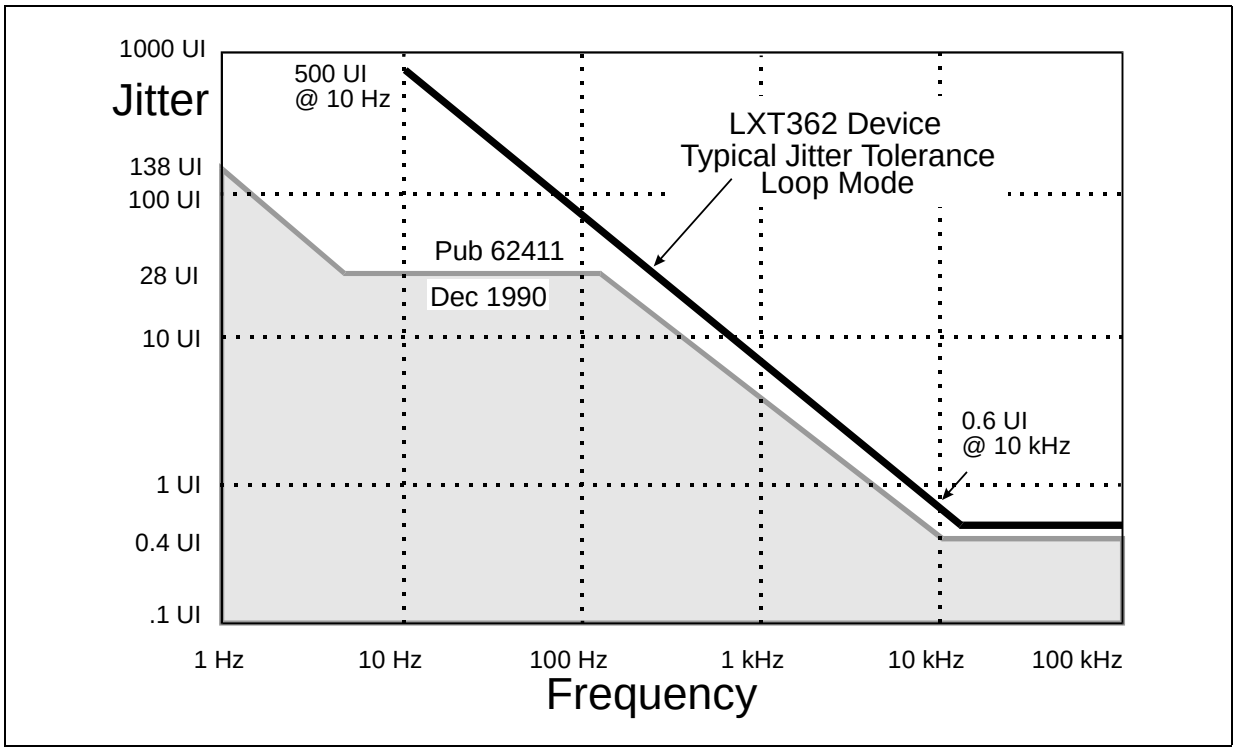
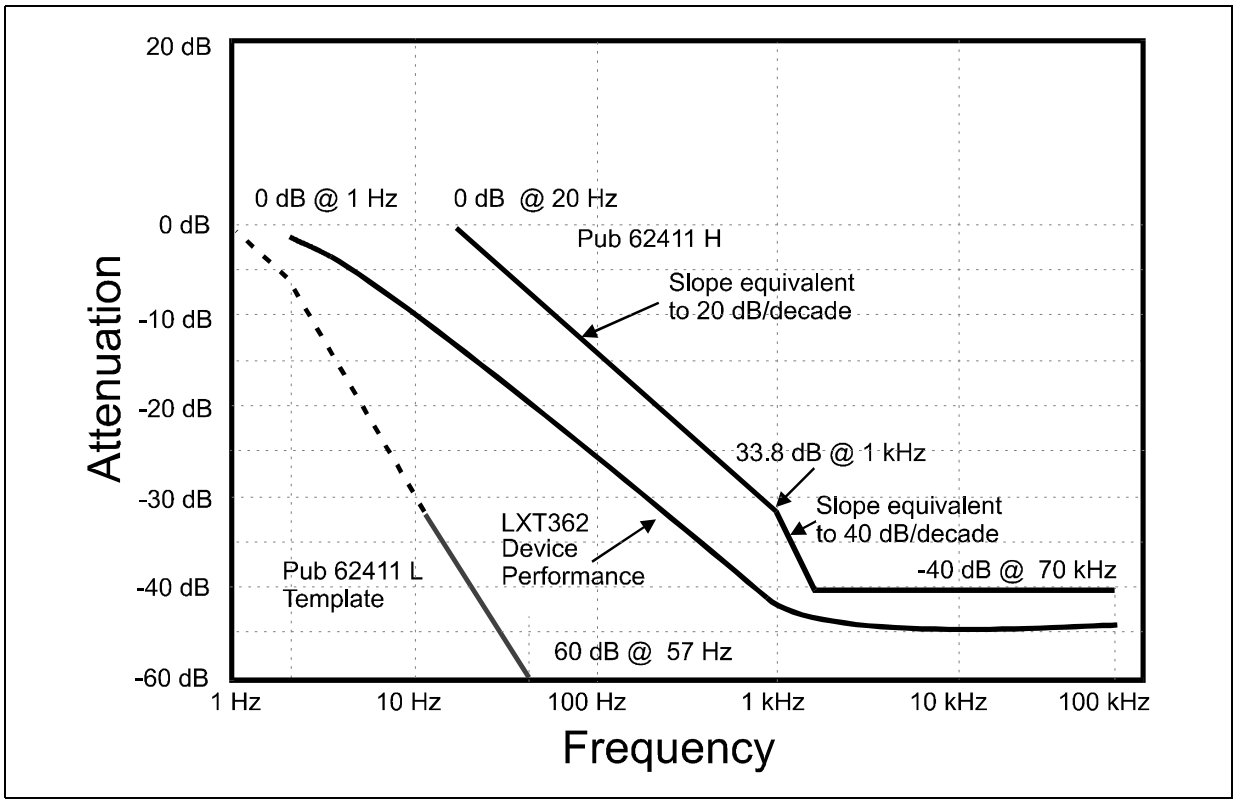


Figure 20. T1 Jitter Attenuation

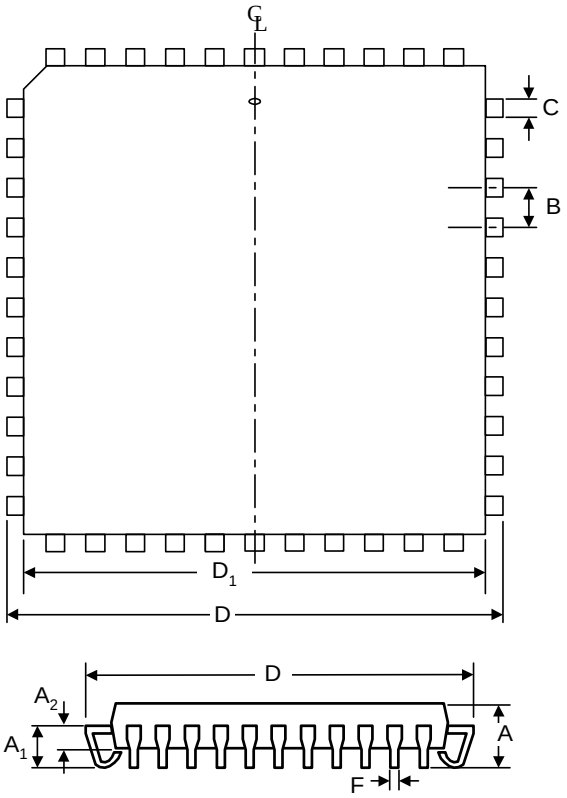


6.0 Mechanical Specifications

Figure 21. Plastic Leaded Chip Carrier Package Specifications

28-Pin PLCC

- Part Number LXT362PE
- Extended Temperature Range (-40 °C to 85 °C)



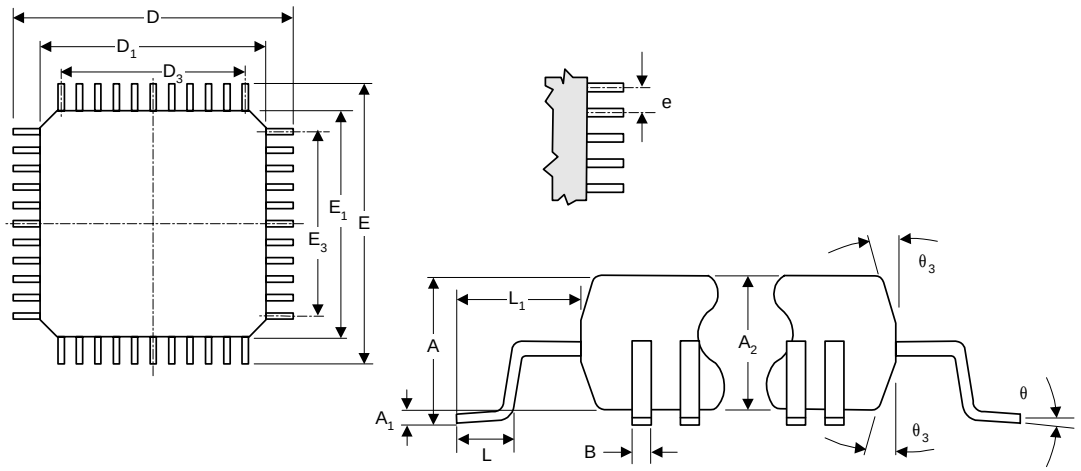
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	.050 BSC[1] (nominal)		1.27 BSC[1] (nominal)	
C	0.026	0.032	0.660	0.813
D	0.485	0.495	12.319	12.573
D1	0.450	0.456	11.430	11.582
F	0.013	0.021	0.330	0.533

1. BSC—Basic Spacing between Centers.

Figure 22. Plastic Quad Flat Package Specifications

44-Pin PQFP

- Part Number LXT362QE
- Extended Temperature Range (-40 °C to 85 °C)



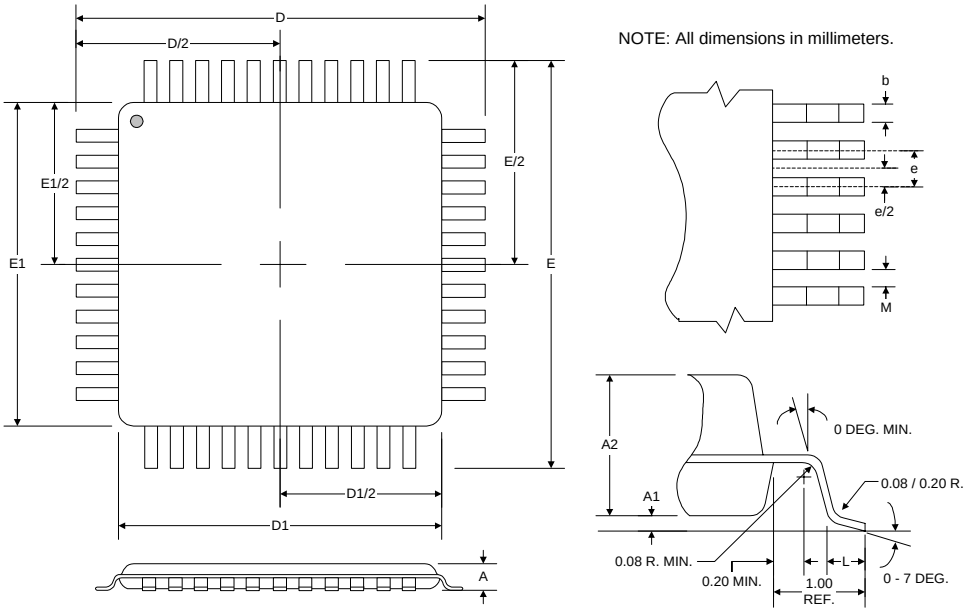
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.096	–	2.45
A1	0.010	–	0.25	–
A2	0.077	0.083	1.95	2.10
B	0.012	0.018	0.30	0.45
D	0.510	0.530	12.95	13.45
D1	0.390	0.398	9.90	10.10
D3	0.315 BSC[1] (nominal)		8.00 BSC[1] (nominal)	
E	0.510	0.530	12.95	13.45
E1	0.390	0.398	9.90	10.10
E3	0.315 BSC[1] (nominal)		8.00 BSC[1] (nominal)	
e	0.031 BSC[1] (nominal)		0.80 BSC[1] (nominal)	
L	0.029	0.041	0.73	1.03
L1	0.063 BSC[1] (nominal)		1.60 BSC[1] (nominal)	
q3	5°	16°	5°	16°
q	0°	7°	0°	7°

1. BSC—Basic Spacing between Centers.

Figure 23. Low-Profile Quad Flat Package Specifications

44-Pin LQFP

- Part Number LXT362LE
- Extended Temperature Range (-40 °C to 85 °C)



Dimension[1]	Millimeters		
	Minimum	Nominal	Maximum
A	-	-	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D	12.00 (basic spacing between centers)		
D1	10.00 (basic spacing between centers)		
E	12.00 (basic spacing between centers)		
E1	10.00 (basic spacing between centers)		
e	0.80 (basic spacing between centers)		
L	0.45	0.60	0.75
M	0.15	-	-

1. See JEDEC Publication for additional specifications.