

**LXT400****All Rate, Extended Range Switched 56 / DDS Transceiver****General Description**

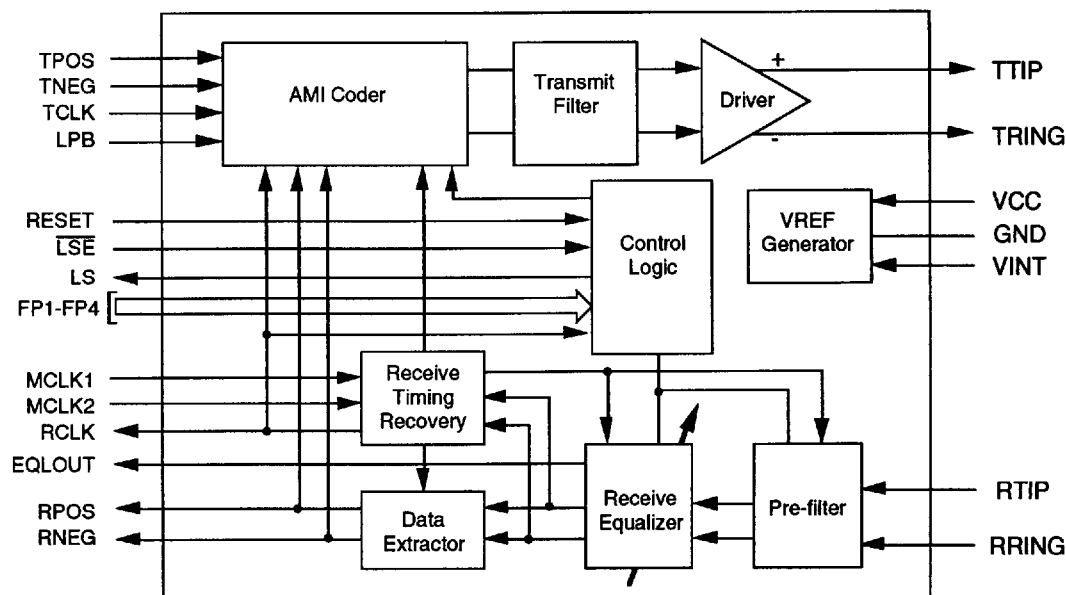
The LXT400 is an integrated line interface circuit for Switched 56 (SW 56) and Digital Data Service (DDS), compatible with any combination of 19 to 26 AWG cable. The LXT400 operates at any of 14 preset data rates from 2.4 kbps to 72.0 kbps, providing appropriate transmit pulse shaping, receive signal detection and timing recovery at the metallic interface between the carrier and the customer installation. The LXT400 diagnostic features including loopback, line status and equalizer monitor outputs, while conforming to AT&T, ANSI and Bellcore specifications.

The LXT400 transmit section includes switched capacitor filters, continuous reconstruction filters, and a 50% AMI encoder. The AMI pulse is synchronized with the transmit clock.

The LXT400 receive section performs line equalization, data extraction and timing recovery. The LXT400 has a BER of less than  $10^{-7}$  with up to 49 dB of cable attenuation at the Nyquist frequency for 56 and 72 kbps, and 40 dB at the lower rates. The LXT400 is an advanced CMOS device which requires only a single +5V power supply.

**Features**

- Integrated transmitter, receiver and timing recovery on a single CMOS chip
- Transparent to framing and coding
- Receive equalizer filters allow data recovery from signals with up to 40 dB of attenuation at the Nyquist frequency, at line rates below 56 kbps, and up to 49 dB at the 56 and 72 kbps line rates
- Single 4.096 MHz crystal or master clock input
- Digital back-end loopback
- Equalizer output monitor pin
- Line status (loop length, RLOS, etc.) available for customer maintenance purposes
- Low power consumption (200 mW typical)
- Available in 28-pin DIP
- Single 5 V only CMOS technology

**Figure 1: LXT400 Block Diagram**

VINT	1	28	EQLOUT
RTIP	2	27	TEST2
RRING	3	26	LSE
TEST1	4	25	FP4
FP2	5	24	TTIP
LPBK	6	23	DGND
AGND	7	22	DVCC
RCLK	8	21	TRING
RPOS	9	20	AVCC
RNEG	10	19	FP1
FP3	11	18	RESET
LS	12	17	TCLK
MCLK1	13	16	TPOS
MCLK2	14	15	TNEG

**Table 1: Data Rate Programming**

FP4	FP3	FP2	FP1	Data Rate <sup>1</sup>
0	0	0	0	2.4 kbps
0	0	0	1	3.2 kbps
0	0	1	0	4.8 kbps
0	0	1	1	6.4 kbps
0	1	0	0	9.6 kbps
0	1	0	1	12.8 kbps
0	1	1	0	19.2 kbps
0	1	1	1	25.6 kbps
1	0	0	0	56.0 kbps
1	0	0	1	72.0 kbps
1	0	1	0	3.5 kbps
1	0	1	1	7.0 kbps
1	1	0	0	14.0 kbps
1	1	0	1	28.0 kbps

**Table 2: Pin Descriptions**

Pin	Sym	I/O	Name	Description
1	VINT	I	Intermediate Voltage Reference	Reference voltage used for internal analog circuits. This pin must be connected through a 1 k $\Omega$ resistor (R <sub>v</sub> ) to the center node between the two termination resistors, R <sub>r</sub> , as shown in Figure 12.
2 3	RTIP RRING	I	Receive Tip Receive Ring	Receive data input pair. RTIP and RRING are a fully differential input for the receive line interface.
4	TEST1	I	Test 1	Factory Test Pin. Leave unconnected.
5 19 11 25	FP2 FP1 FP3 FP4	I I I I	Frequency Programming Inputs 1 thru 4	The LXT400 data rate is set by the logic levels present at the FP1 through FP4 inputs as shown in Table 1, above. For operation at 64 kbps and other alternate data rates, refer to Application Note AN-30.
6	LPBK	I	Loopback	When set to logic 1, activates digital back-end loopback.
7	AGND	-	IC Ground	IC ground for all circuits except the transmit driver.
8	RCLK	O	Recovered Clock	Clock recovered from signal input at RTIP and RRING.
9 10	RPOS RNEG	O O	Receive Data Positive and Negative	Receive data outputs. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. A signal on RNEG corresponds to a negative pulse on RTIP and RRING. Both outputs are stable and valid on the falling edge of RCLK, and are never high simultaneously.
12	LS	O	Line Status Output	An 8-bit serial word indicating loop length, line loss, loss of signal (LOS), etc. LS is <u>valid</u> on the rising edge of RCLK and goes to a high impedance state when LSE is high. If LSE is tied low, the LS output represents LOS only.
13 14	MCLK1 MCLK2	I I	Master Clock 1 Master Clock 2	The required 4.096 MHz input may be provided by a crystal connected across these pins, or by a digital clock connected to MCLK1. If a clock is provided on MCLK1, MCLK2 must be left unconnected.

Note 1. For information on 64 kbps operation and other alternate data rates, refer to Application Note AN-30.

Table 2: Pin Descriptions continued

Pin	Sym	I/O	Name	Description															
15	TNEG	I	Transmit Data Negative and Positive	Inputs are sampled at the halfway point between rising edges of TCLK. AMI pulses are encoded as follows: <table><tr><td>TPOS</td><td>TNEG</td><td>Transmit Signal</td></tr><tr><td>0</td><td>0</td><td>Space</td></tr><tr><td>0</td><td>1</td><td>Negative Pulse</td></tr><tr><td>1</td><td>0</td><td>Positive Pulse</td></tr><tr><td>1</td><td>1</td><td>Space</td></tr></table>	TPOS	TNEG	Transmit Signal	0	0	Space	0	1	Negative Pulse	1	0	Positive Pulse	1	1	Space
TPOS	TNEG	Transmit Signal																	
0	0	Space																	
0	1	Negative Pulse																	
1	0	Positive Pulse																	
1	1	Space																	
16	TPOS	I																	
17	TCLK	I	Transmit Clock	Transmit clock. TPOS and TNEG transitions must be coincident with the rising edges of TCLK.															
18	RESET	I	Reset	Hardware reset pin. Must be pulsed low on power-up to initialize all internal circuits. Must also be pulsed low after changing the baud rate and after forcing or releasing any loopback condition.															
20	AVCC	I	IC Power	IC power supply for all circuits except the transmit driver. +5 V (±5%).															
21	TRING	O	Transmit Ring	Differential driver outputs. Designed to drive the 135 Ω twisted-pair cable through transmit line interface shown in application diagram, Figure 7.															
24	TTIP	O	Transmit Tip																
22	DVCC	I	Driver Power	Transmit driver power supply. +5 V (±5%).															
23	DGND	-	Driver Ground	Transmit driver ground.															
26	LSE	I	Line Status Enable	Active low enable for the LS serial port. This pin must transition from high to low to read LS serial data. LSE is sampled on the rising edge of RCLK.															
27	TEST2	I	Test 2	Analog test pin. Must be tied to ground.															
28	EQLOUT	O	Equalizer Output Monitor	Monitors Equalizer. Must be left open when not used.															

Table 3: Absolute Maximum Ratings

Parameter	Min	Max	Units
DC supply - AVCC referenced to AGND	- 0.3	+ 6.0	V
DVCC referenced to DGND	- 0.3	+ 6.0	V
DVCC referenced to AVCC	- 0.3	+ 0.3	V
DGND referenced to AGND	- 0.3	+ 0.3	V
Input voltage, any pin <sup>1,2</sup>	AGND - 0.3	AVCC + 0.3	V
Input or output diode current, any pin <sup>2</sup>	-	$\pm 20$	mA
Continuous output current, any pin <sup>2</sup>	-	$\pm 25$	mA
Continuous current, VCC or GND pins	-	$\pm 50$	mA
Storage temperature	- 40	+ 150	$^{\circ}\text{C}$

<sup>1</sup> TTIP and TRING are referenced to DVCC and DGND.<sup>2</sup> Except supply pins.

Table 4: Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
DC supply	AVCC/DVCC	4.75	5.0	5.25	V
Ambient operating temperature	T <sub>A</sub>	-40	-	+85	$^{\circ}\text{C}$

**Table 5: AC Electrical Characteristics**

Parameter	Symbol	Min	Typ <sup>1</sup>	Max	Units	Notes
<b>Receive Timing (Figure 2)</b>						
RCLK period	$t_{PR}$	–	$1/f_b$	–	ns	
RCLK pulse width high	$t_{RWH}$	$1/(2 f_b) - 150$	$1/(2 f_b)$	$1/(2 f_b) + 150$	ns	
RPOS/RNEG delay from RCLK rising edge	$t_{DP}$	–	–	200	ns	2
Transition time on any digital output	$t_{TO}$	–	10	20	ns	2
<b>Transmit Timing (Figure 3)</b>						
TCLK period	$t_{PT}$	–	$1/f_b$	–	μs	
TCLK pulse width high	$t_{TWH}$	400	–	–	ns	
TPOS/TNEG setup to TCLK rising edge	$t_{TSU}$	–400	–	400	ns	
TPOS/TNEG hold time from the next rising edge of TCLK	$t_{TH}$	–400	–	400	ns	
Transition time on any digital input	$t_{TI}$	–	–	40	ns	
<b>LS Serial Port Timing (Figure 4)</b>						
LS delay from RCLK falling edge	$t_{LSP}$	–	–	200	ns	2
LSE setup to RCLK rising edge	$t_{LSU}$	200	–	–	ns	
LSE hold time from RCLK falling edge	$t_{LSH}$	0	–	–	ns	
LSE low to low Z state	$t_{LZ}$	–	–	100	ns	
LSE high to high Z state	$t_{HZ}$	–	–	100	ns	
<b>MCLK and Reset Timing (Figure 5)</b>						
MCLK1 input frequency	$f_{MCLK}$	–	4.096	–	MHz	
MCLK1 frequency tolerance - at OCU	$f_{TOCU}$	–	–	± 50	ppm	
- at DSU @ 2400 bps	$f_{TDSU}$	–	–	± 80	ppm	
- at DSU @ all other rates	$f_{TDSU}$	–	–	± 100	ppm	
MCLK pulse width high	$t_{MWH}$	98	122	146	ns	
RESET pulse width low	$t_{RWL}$	1000	–	–	ns	
<b>General</b>						
Input capacitance	$C_{IN}$	–	7	–	pF	
TCLK jitter at DSU with respect to RCLK	$t_{JIT}$	–	–	2	% $t_{PR}$ at DSU	
RCLK isochronous distortion at DSU	$r_{JIT}$	–	–	5	% $t_{PT}$ at OCU	
Transmit output jitter with respect to TCLK	$o_{JIT}$	–	–	3	% $t_{PT}$ at DSU	
Transmit pulse amplitude at TTIP/TRING						
- at 9.6 and 12.8 kbps	$A_T$	1.44	1.55	1.75	V	3
- at all other rates	$A_T$	2.56	2.74	2.92	V	3

<sup>1</sup>Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

<sup>2</sup>Measured with 15 pF load.

<sup>3</sup>The instantaneous peak amplitude of an isolated pulse (i.e.: a mark between two spaces) into a 270 Ω resistive load.

Table 6: DC Electrical Characteristics

Parameter	Sym	Min	Typ <sup>1</sup>	Max	Units	Test Conditions
Supply current (transmitting spaces)	$I_{CC}$	–	40	60	mA	270 $\Omega$ resistor across TTIP and TRING
Supply current (transmitting all marks)	$I_{CC}$	–	47.5	60	mA	270 $\Omega$ resistor across TTIP and TRING
Input low voltage	$V_{IL}$	–	–	0.8	V	Digital inputs
Input high voltage	$V_{IH}$	2.0	–	–	V	Digital inputs
Output low voltage	$V_{OL}$	–	–	0.4	V	$I_{OL} = 1.6$ mA
Output low voltage	$V_{OL}$	–	0.2	–	V	$I_{OL} < 10$ $\mu$ A
Output high voltage	$V_{OH}$	2.4	–	–	V	$I_{OH} = 0.4$ mA
Output high voltage	$V_{OH}$	–	4.5	–	V	$I_{OH} < 10$ $\mu$ A
Input leakage current	$I_{IL}$	-40	–	40	$\mu$ A	$0 < V_{IN} < V_{CC}$

<sup>1</sup> Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 2: Receive Digital Timing

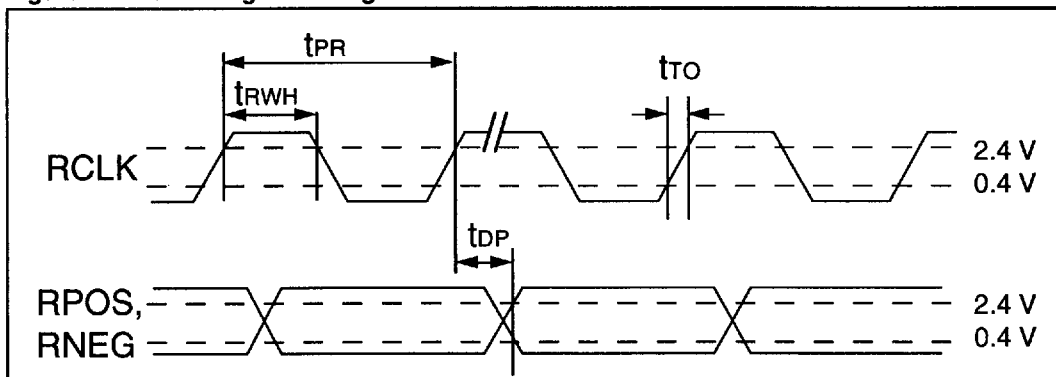
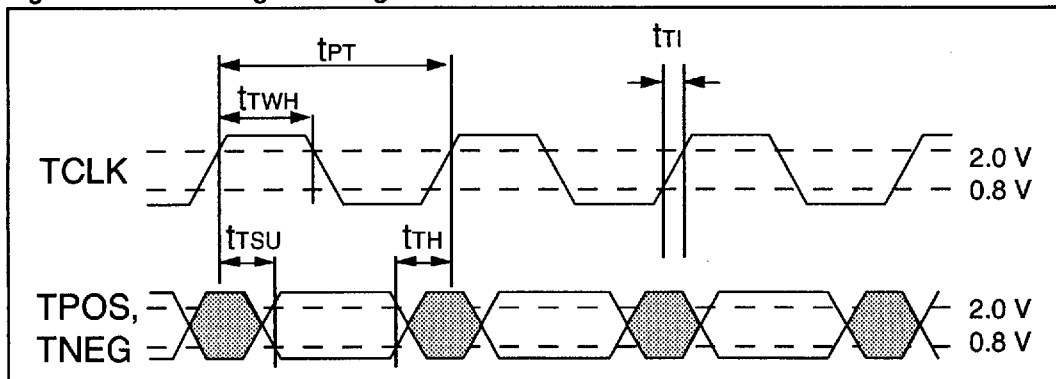


Figure 3: Transmit Digital Timing



## General Description

The LXT400 comprises three basic sections: transmit, receive and control logic.

The transmit section includes a 50% AMI encoder, a programmable switched-capacitor low-pass filter, a low-pass notch filter, a transmit timing resynchronizer and a continuous reconstruction filter. An on-chip CMOS driver is also incorporated to drive a 135  $\Omega$  line through a transformer.

The receive section includes pre-filters and line equalizers, and the timing recovery and data extraction blocks. An internal digital phase-locked loop (DPLL) is used in conjunction with the MCLK input to synchronize the recovered clock and data.

The control logic block initializes the transceiver, selects receive filters and reports status information on the serial port. Control logic inputs FP1 through FP4 determine the data rate in accordance with Table 1. The control logic

executes the initialization procedure upon automatic re-synchronization or external RESET. Filter selection optimizes the receive signal-to-noise ratio (SNR) by matching the filter in the equalizer section to the strength of the received signal (a function of loop length/line loss). The control logic block also reports receiver status, estimated line length (as indicated by filter selection) and a receive loss of signal (RLOS) alarm on the serial port.

## Functional Description

### Initialization

Upon power-up, or after changing the baud rate or loopback condition of the line interface, a RESET pulse is required to initialize the LXT400. On receipt of the RESET pulse, the LXT400 executes an iterative cycle of level detection and offset cancellation to select the appropriate equalizer settings for the received signal. Receiver initialization can be monitored on the serial channel. When received data has a 50% ones density, full operation is achieved within one

Figure 4: LS Serial Port Timing

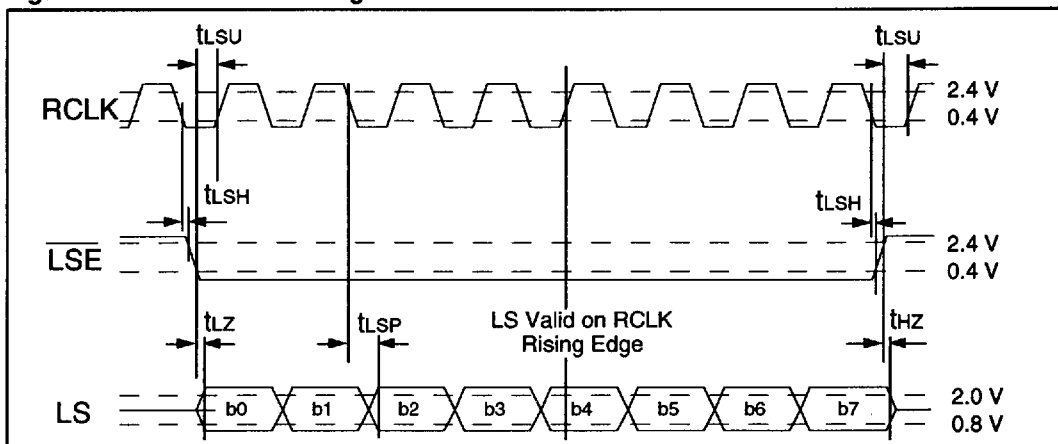
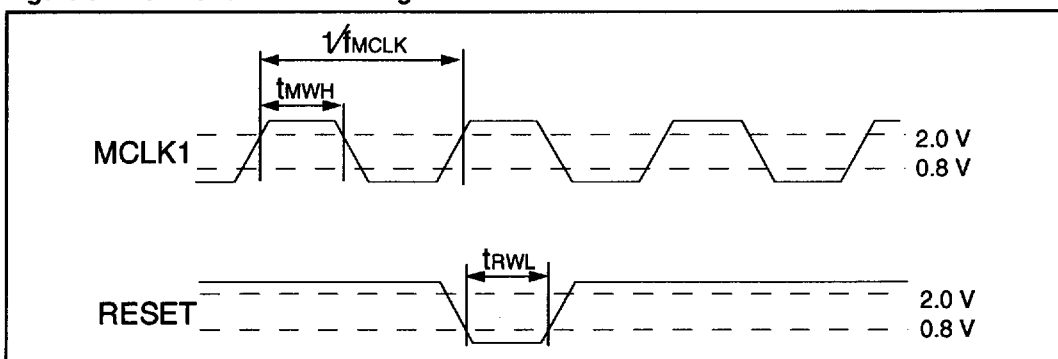


Figure 5: MCLK and RESET Timing



second after **RESET**. Under the minimum ones density condition specified in Table 7, full operation is achieved within eight seconds after **RESET**. Correct initialization assumes the presence of an AMI-coded signal at the RTIP and RRING inputs. The LXT400 will not correctly initialize unless a stable signal which meets the network interface specifications of AT&T Pub 62310 is present at the RTIP and RRING inputs during the entire initialization process. The RPOS/RNEG outputs are not valid until full operation is achieved. During offset cancellation, the RPOS/RNEG outputs do not adhere to the AMI rule. However, once initialized (assuming that a proper baud rate is selected), RPOS and RNEG never simultaneously output a logic 1.

A hardware reset is required after any of the following changes in transceiver configuration:

1. A change in Baud Rate
2. A change in the local analog loopback configuration
3. A local change in the line upon which the transceiver is communicating (for example, configurations for changing lines in a "1 for n" redundancy scheme).

Automatic re-initialization may be triggered by changes in received signal strength as follows:

- If received signal strength increases by more than about 6 dB after full operation is achieved, automatic re-initialization occurs.
- If received signal strength decreases by more than about 4 dB, re-initialization occurs. If the decrease in received signal strength exceeds 6 dB, the LXT400 reports an LOS condition and performs an automatic re-initialization.

**Table 7: Ones Density Requirements**

Data Rate (kbps)	Minimum Average Ones Density
2.4, 4.8, 9.6, 19.2	1 / 12
3.2, 6.4, 12.8, 25.6	1 / 16
56.0	1 / 14
72.0	1 / 18
3.5, 7.0, 14.0, 28.0	≈ 1 / 16

**Table 8: Notch Filter Attenuation**

OCU/Loop Data Rate (kbps)	Customer (Primary Channel) Data Rate (kbps)	Rejection Band	
		24 - 32 kHz	72 - 80 kHz
2.4 or 3.2	2.4	5 dB	1 dB
4.8 or 6.4	4.8	13 dB	9 dB
9.6 or 12.8	9.6	17 dB	8 dB

The time required to achieve full operation after reinitialization, is the same as required for power-on initialization (i.e., 1 second max with 50% ones density, 8 seconds under minimum ones density conditions). Reinitialization is not triggered by impulse noise events.

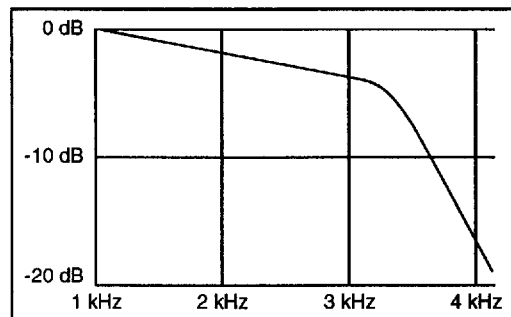
## Transmission

TPOS and TNEG must have transitions coincident with the rising edges of TCLK. The transmit section generates a 50% AMI pulse according to the pulse encoding rules, which is synchronized with the TCLK input. In DSU applications, RCLK is typically routed back into the TCLK input. The instantaneous baud period varies with the receive DPLL phase adjustments, however, the pulse duty cycle is maintained at 50% of the nominal baud period by internal re-synchronization to TCLK. The AMI pulse is then processed through a set of frequency dependent filters.

Initial filtering at all rates is accomplished by a programmable, switched-capacitor, low-pass filter. This filter is a single-pole type with the pole set at 1.3 times the bit rate (as determined by inputs FP1 - FP4).

For data rates of 2.4, 3.2, 4.8, 6.4, 9.6 and 12.8 kbps, the filtered pulses go through an additional low-pass notch filter. The notch filter is required to protect other DDS services with specific band requirements, and provides the attenuation listed in Table 8. The additional rejection requirement is weighted within each band by "C-Message" weighting over double speech sidebands around a carrier in the middle of each band (28 kHz and 78 kHz). The C-Message weighting function is graphed in Figure 6.

**Figure 6: C-Message Weighting**



Depending on the data rate, the frequency template extends to different limits as shown in Table 9. (An alternate notch filter is used for data rates of 3.5 and 7.0 kbps.) The single pole, low-pass filter would maintain the frequency within  $\pm 5\%$ . The notch filter attenuation is added to this.

A continuous filter, common to all data rates, is the final stage. The continuous filter removes high frequency components which remain after processing by the low-pass filter stages. The pulse is then applied to the line driver for transmission onto the twisted-pair line.

**Table 9: Frequency Limits per Data Rate**

Data Rate (kbps)	Upper Frequency Limit (kHz)
2.4 (3.2)	100
4.8 (6.4)	150
9.6 (12.8)	150
19.2 (25.6)	300
56.0 (72.0)	1750
3.5	100
7.0	150
14.0	150
28.0	1200

## Reception

RTIP and RRING inputs are differentially detected, then processed through the pre-filters and equalizer section. The continuous pre-filter removes high frequency noise and prevents aliasing problems for the switched capacitor (SC) line equalizers which follow. Pulse reshaping is achieved by the receive equalizer, which consists of an SC step equalizer and an adaptive decision feedback equalizer (DFE). The DFE eliminates residual inter-symbol interference (ISI) due to echoing by multiple bridged tap connections and the quantized frequency responses of the SC step filters. The DFE is continuously adapted to compensate for ISI due to time varying line characteristics such as temperature, humidity and age. Nine different filter selections based on signal strength are available.

## Changes in Received Signal Strength

During initialization, the LXT400 selects filters appropriate to the strength of the received signal. After initialization, the LXT400 continually monitors the receive signal strength to ensure the optimum signal/filter match. Data reception is not affected by impulsive noise events or by slow changes in signal amplitude, such as may be caused by temperature and humidity changes on the line. (The maximum constant rate of change which the LXT400 can track is 6 dB per minute.) However, instantaneous "step" changes (see Figure 7) may temporarily interfere with data reception. Step changes may be due to sudden changes in loop loss, far end transmitter output, etc.

After normal operation has been established, an instantaneous single-step change may cause one of three conditions, as shown in Figure 8.

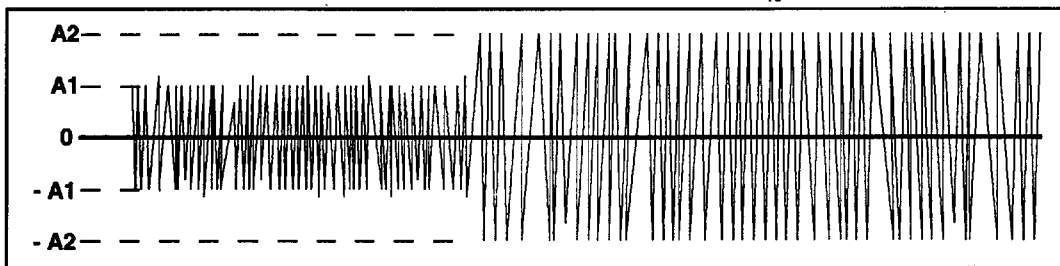
Under Condition 1, the LXT400 automatically adapts to minor step changes in signal strength (assuming that the new input is a valid DDS signal).

Under Condition 3, the LXT400 responds to significant step changes by re-initializing.

Condition 2, while unlikely to occur in an actual DDS implementation, may be observed in the laboratory due to artificial line simulators. Condition 2, which results from a 6 - 20 dB step increase in received signal strength, may result in a signal/filter mismatch. This condition is characterized by excessive bipolar violations (BPVs) which can be observed on RPOS and RNEG. External signal quality detection circuitry can be used to detect excessive BPVs that are not recognized as standard DDS BPV code words. Upon detection of unrecognized BPVs, the user may force a reset on the LXT400 to resume error-free operation.

Under normal operating conditions, step changes in received signal strength are all under local control. Thus, the user can reset the LXT400 once the new receive signal has stabilized at the chip inputs. Remote changes typically involve disconnecting one line and re-connecting another line of

**Figure 7: Step Changes in Received Signal Strength =  $20 \log_{10} (A^2/A_1)$  dB**





different length. These changes trigger the RLOS report and automatic re-initialization. Any remote changes in line length or transceiver configuration are beyond the local user's control. Remote changes in baud rate are not detected.

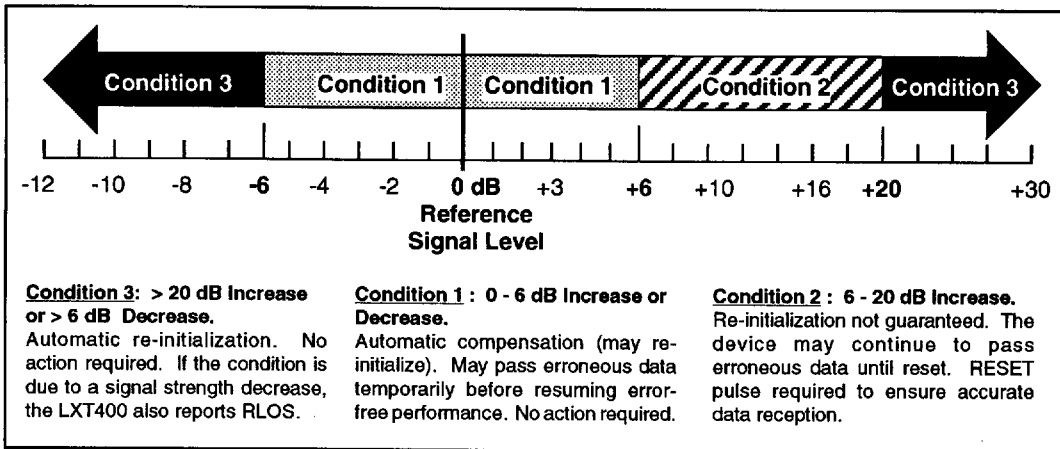
## Receive Loss of Signal

RLOS goes high when more than 32 consecutive zeros are received, caused either by a true loss of signal, or a signal strength drop greater than 6 dB. The LXT400 automatically re-initializes when RLOS goes high. Figure 9 shows the

RTIP/RRING input and RLOS output timing relationships for a true loss of signal. When signal energy returns to the chip input, the LXT400 executes one full activation cycle in the presence of this signal. The result is that RLOS will remain high for a period of time ( $0.13 \text{ s} < t_H < 16 \text{ s}$ ) after signal energy reappears.

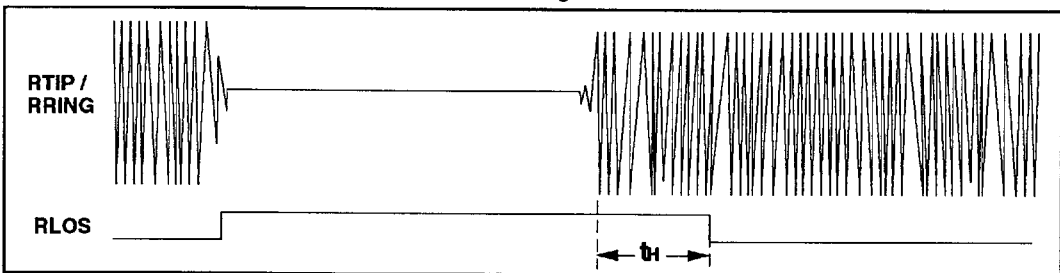
Figure 10 shows the RTIP/RRING input timing and RLOS output timing relationship for a signal strength decrease greater than 6 dB. In this case, RLOS will go high for a time  $0.26 \text{ s} < t_P < 16 \text{ s}$ .

**Figure 8: Conditions Based on Changes in Received Signal Strength**

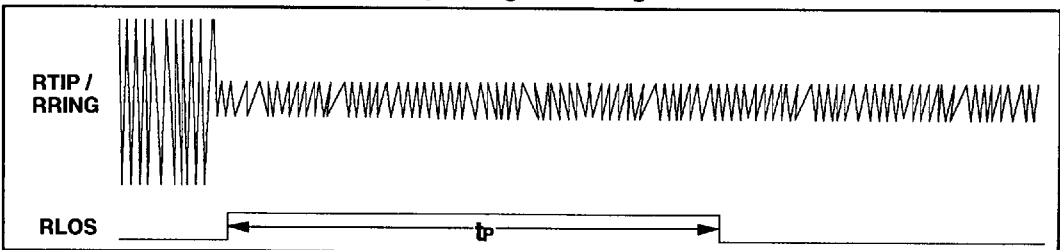


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**Figure 9: RLOS Timing for a True Loss of Signal**



**Figure 10: RLOS Timing for a Drop in Signal Strength > 6 dB**



## Timing Recovery

The timing recovery circuit uses a rate synchronizer to generate a high frequency internal clock from the MCLK input. A DPLL is used to synchronize this internal clock to the received data pulses. The output clock from the DPLL is divided down to generate RCLK and all other required clocks (except TCLK which is an external input).

## Data Extraction

The data extraction block provides RPOS and RNEG outputs. A positive differential pulse received between RTIP and RRING results in a logic 1 on RPOS. A negative differential pulse between RTIP and RRING results in a logic 1 on RNEG. RPOS and RNEG are output at the received data rate and are valid on the falling edge of RCLK.

Receiver operation is not affected by the data patterns, provided the ones density requirements of Table 7 are met with no more than 26 consecutive zeros. RLOS is declared after 32 consecutive zeros. However, the RCLK output remains synchronized to the RTIP/RRING input for more than 40 consecutive zeros. Bipolar violations are received properly. The bipolar violation coding rule that successive violations be of alternating polarity must be followed. However, if this rule is temporarily broken (due to channel noise, etc.), long term LXT400 data reception will not be adversely affected.

## Loopback Operation

When the LPBK pin is set to a logic 1, the recovered data and clock are sent back through the transmit section and onto the line interface, as well as being output on the RPOS/RNEG and RCLK pins. TPOS/TNEG and TCLK inputs are ignored in the loopback mode.

## Serial Port Operation

The line status (LS) output is an 8-bit serial word enabled by pulling LSE low for 8 bit-periods as shown in Figure 4. Bit assignments are listed in Table 10. Approximate line loss and loop length (based on received signal strength/filter selection, assuming far-end pulse transmission compliant with AT&T Pub 62310 or T1E1/90-051) are reported via bits b0 through b3 as listed in Table 11. Bits b4 through b6 indicate the receiver activation state. Bit b7 is the RLOS alarm.

Figure 11 shows the serial output for a typical LXT400 initialization sequence. Bits b0 - b3 report filter selection and bits b4 - b6 report receiver status. Bit b6 toggles to indicate that the receiver is alternating between offset cancellation ( $b6 - b4 = 100$ ) and receive level detection ( $b6 - b4 = 000$ ). The receiver starts with the highest-gain filter ( $b3 - b0 = 0111$ ), cancels systematic voltage offset at the filter output, and then detects the receive signal level at the filter output. If the signal exceeds the threshold for that filter, the LXT400 steps down to the filter with the next-highest gain ( $b3 - b0 = 1000$ ). This process is repeated until the receive signal level does not exceed the filter threshold.

Once the appropriate filter is selected, the receiver phase-locked loop (PLL) and slicer levels converge to match the receive signal for optimum SNR. During receiver convergence ( $b6 - b4 = 001$ ), the PLL adapts to sample the peak of the receive pulses and the slicer level adapts to the midway point between zero and the pulse peak voltage. Once convergence is complete, the LXT400 begins full operation ( $b6 - b4 = 010$ ).

**Table 10: LS Word Bit Assignments**

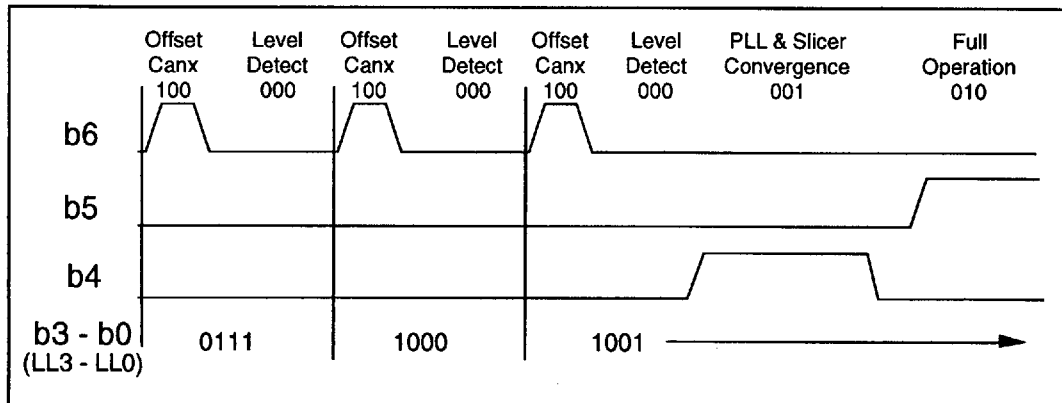
Bit #	Name	Description
b0	LL0	Loop Length Indication, bit 0
b1	LL1	Loop Length Indication, bit 1
b2	LL2	Loop Length Indication, bit 2
b3	LL3	Loop Length Indication, bit 3
b4	S1	Receiver Converging when high
b5	S2	Full Operation when high
b6	S0	Level Detection when high
b7	RLOS	Receive Loss of Signal when high

**Table 11: LS Loop Length Bits**

Rate kbps	Insertion Loss in dB / Line Range in km (24 AWG PIC, no bridged taps) for LL3 - LL0								
	0111	1000	1001	1010	1011	1100	1101	1110	1111
2.4	N/A	> 38 / > 21.0	38 / 21.0	33 / 17.3	27 / 13.4	22 / 9.6	18 / 6.2	13 / 3.5	7 / 1.8
3.2	N/A	> 38 / > 18.6	38 / 18.6	33 / 15.6	28 / 12.6	22.5 / 9.6	17.5 / 6.5	12.5 / 3.7	7 / 1.8
4.8	N/A	> 38.5 / > 15.8	38.5 / 15.8	33 / 13.2	27 / 10.6	22 / 8.0	16 / 5.3	12 / 2.8	7 / 1.3
6.4	N/A	> 38.5 / > 14.1	38.5 / 14.1	33 / 11.9	27.5 / 9.8	22 / 7.5	17 / 5.3	12.5 / 3.2	7 / 1.5
9.6	N/A	> 37 / > 11.4	37 / 11.4	32 / 9.6	27 / 7.9	22 / 6.2	16 / 4.3	11 / 2.6	5 / 1.1
12.8	N/A	> 39 / > 10.8	39 / 10.8	33 / 9.1	27.5 / 7.4	22 / 5.8	16 / 4.1	11 / 2.9	5 / 1.0
19.2	N/A	> 39 / > 9.2	39 / 9.2	33 / 7.8	27.5 / 6.4	22 / 5.0	16 / 3.5	11 / 2.1	4 / 0.8
25.6	N/A	> 38 / > 8.3	38 / 8.3	33 / 7.0	27.5 / 5.8	22 / 4.5	16 / 3.2	10.5 / 1.9	4 / 0.7
56.0	> 47.5 / > 8.0	47.5 / 8.0	41.5 / 6.9	35 / 5.8	29 / 4.8	22.5 / 3.8	17 / 2.7	10.5 / 1.6	4 / 0.5
72.0	> 48 / > 7.5	48 / 7.5	42 / 6.5	35.5 / 5.5	29 / 4.5	23 / 3.5	17 / 2.5	10.5 / 1.5	3 / 0.5
3.5	N/A	> 39 / > 18.4	39 / 18.4	34 / 15.4	28 / 12.5	23 / 9.6	17.5 / 6.6	12.5 / 3.8	7 / 1.8
7.0	N/A	> 39 / > 13.8	39 / 13.8	34 / 11.7	28 / 9.6	22.5 / 7.5	17.5 / 5.4	12.5 / 3.4	7 / 1.6
14.0	N/A	> 39 / > 10.5	39 / 10.5	34 / 8.9	28 / 7.3	22.5 / 5.7	16.5 / 4.1	11.5 / 2.6	5 / 1.0
28.0	N/A	> 39 / > 8.0	39 / 8.0	33 / 6.8	27.5 / 5.6	22 / 4.3	16 / 3.1	10 / 1.8	4 / 0.7

NOTE: The insertion loss/line range values are defined as being less than or equal to the listed numbers, but greater than the numbers to the immediate right, or zero for LL3 - LL0 = 1111.

**Figure 11: Typical Serial Port Output for Receive Activation @ 72 kbps**



## Design Considerations

Figure 12 shows a typical LXT400 application circuit. A DSU crystal (4.096 MHz) is connected across MCLK1 and MCLK2, with two grounded loading capacitors. The line interface consists of a pair of 1:1 transformers, center-tapped on the line side, with appropriate load resistors. The  $R_s/C_s$  shunt network provides high frequency compensation for the transmit driver. The input signal is developed across the  $R_r/R_{in}$  network.  $R_v$  limits current into the low-impedance VINT driver during over-voltage conditions on the line. Table 12 lists external component recommendations.

## Crosstalk

It is important to prevent crosstalk between the transmitter and receiver circuits. Steps were taken to reduce this interference inside the LXT400, but precautions must be taken with the line interface circuitry outside the chip as well. Crosstalk is especially high when the idle pattern (alternate positive and negative pulses) is being transmitted because the transmit power is concentrated around the Nyquist frequency (half the baud rate).

## PCB Layout

The external line interface circuit must be laid out to minimize coupling of other digital and analog signals into RTIP and RRING (see Figure 13.) These inputs, pins 2 and 3, are high impedance nodes which can pick up interference from adjacent PCB traces. The line interface circuit must be designed for loops with up to 50 dB of loss at the Nyquist frequency, even if the product will never be used on such long lines. When no receive signal is present, the LXT400 will switch to the highest gain filter, which at 56 and 72 kbit/s produces an internal gain of about 50 dB. Unless precautions are taken, substantial interference coupling into RTIP and RRING could exceed the internal slicer levels and prevent the RLOS report. Layout considerations for LXT400 application circuits include:

1. Minimum PCB trace lengths between the LXT400 and the 4.096 MHz crystal and loading capacitors.
2. Minimum PCB trace lengths between resistors  $R_{in}$  and the RTIP and RRING pins. Shield these connections with ground traces.
3. Minimum PCB trace lengths between the receive transformer and the receive termination network.

**Figure 12: Typical LXT400 Application Circuit for 72 kbps Operation**

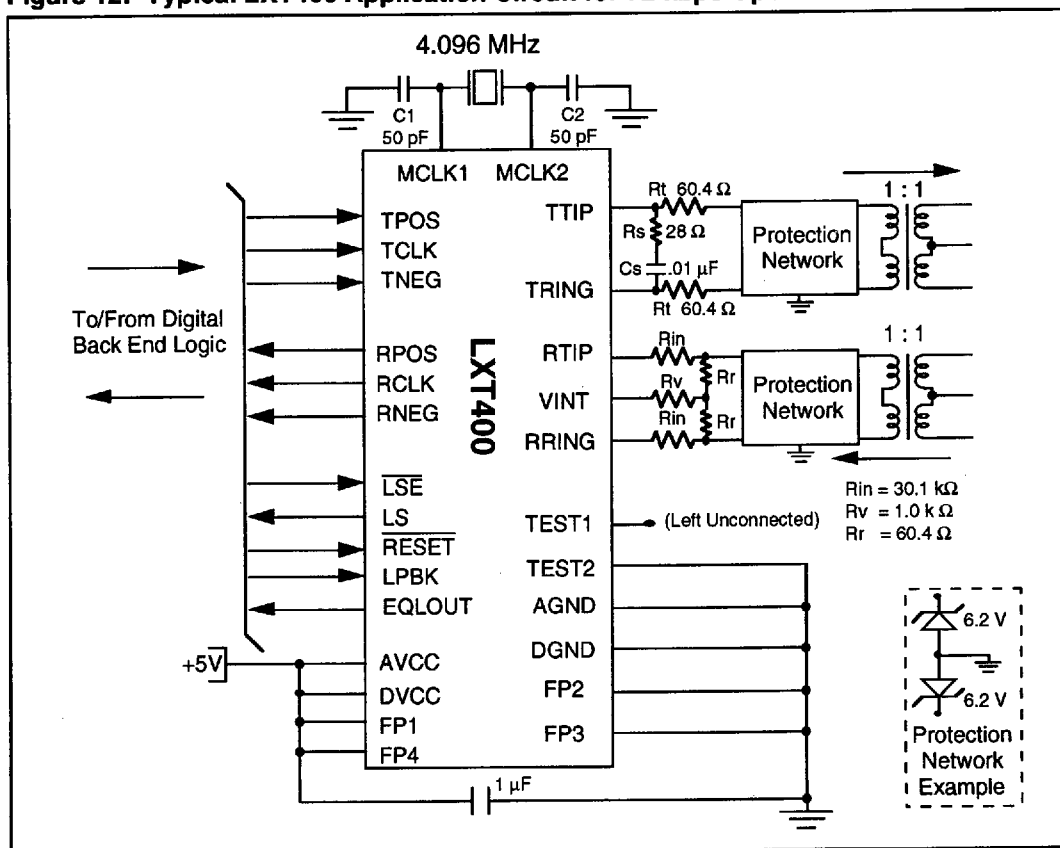


Table 12: External Component Recommendations

Component	Parameter	Recommended Value
<b>Line Transformer</b>  Suggested Manufacturers: Midcom - Phone 800/643-2661 Schott - Phone 615/889-8800	Turns ratio	1:1, $\pm 1\%$
	Structure	Center tapped (for line side)
	Primary Inductance	200 mH minimum
	Leakage Inductance	22 to 43 $\mu$ H maximum
	Interwinding Capacitance	350 pF maximum
	DC Resistance (Primary, Rwp)	7 $\Omega \pm 1 \Omega$
	DC Resistance (Secondary, Rws)	7 $\Omega \pm 1 \Omega$
<b>Rin</b>	Resistance, Tolerance, Rating	30.1 k $\Omega$ , $\pm 1\%$ , 1/4 W
<b>Rt, Rr</b>	Resistance, Tolerance, Rating	(135 $\Omega$ - Rwp - Rws) / 2, $\pm 1\%$ , 1/4 W
<b>Rv</b>	Resistance, Tolerance, Rating	1 k $\Omega$ , $\pm 5\%$ , 1/4 W
<b>DSU Crystal</b>  Suggested Manufacturers: Fox - Phone 813/693-0099 Monitor - Phone 815/432-5296	Nominal frequency	4.096 MHz
	Holder style	HC-49/U
	Operating Mode	Fundamental, parallel resonant
	Load Capacitance	28 pF nominal
	Tolerance	$\pm 25$ ppm @ 25 $^{\circ}$ C
	Range	$\pm 40$ ppm, 0 to 70 $^{\circ}$ C
	Aging	3 ppm per year maximum
	Maximum ESR	50 $\Omega$
	Drive Level	2 mW maximum
<b>DSU Crystal Loading Capacitors</b>	Capacitance, Tolerance, Rating	50 pF, $\pm 5\%$ , 10 V
	Construction	NPO ceramic or equivalent
<b>Transmit Shunt Network</b>		
<b>Rs</b>	Resistance, Tolerance, Rating	28 $\Omega$ , $\pm 5\%$ , 1/4 W
<b>Cs</b>	Capacitance, Tolerance, Rating	0.01 $\mu$ F, $\pm 20\%$ , 10 V

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Figure 13: Suggested LXT400 PCB Layout

