T-41-55

LZ2112J CCD Area Sensor for 1/2" EIA B/W

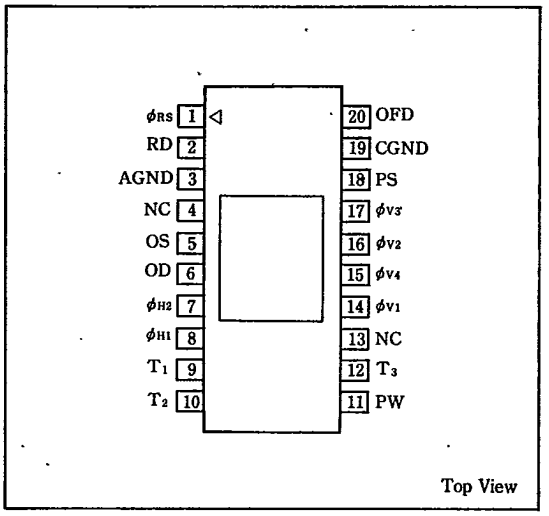
■ Description

The LZ2112J is a 1/2 inch solid-state image sensor comprised of PN-junction photodiodes and CCDs (charge-coupled device). Having approximately 270,000 (542 horizontal×492 vertical) pixels, the sensor provides a high-resolution stable monochrome image.

■ Features

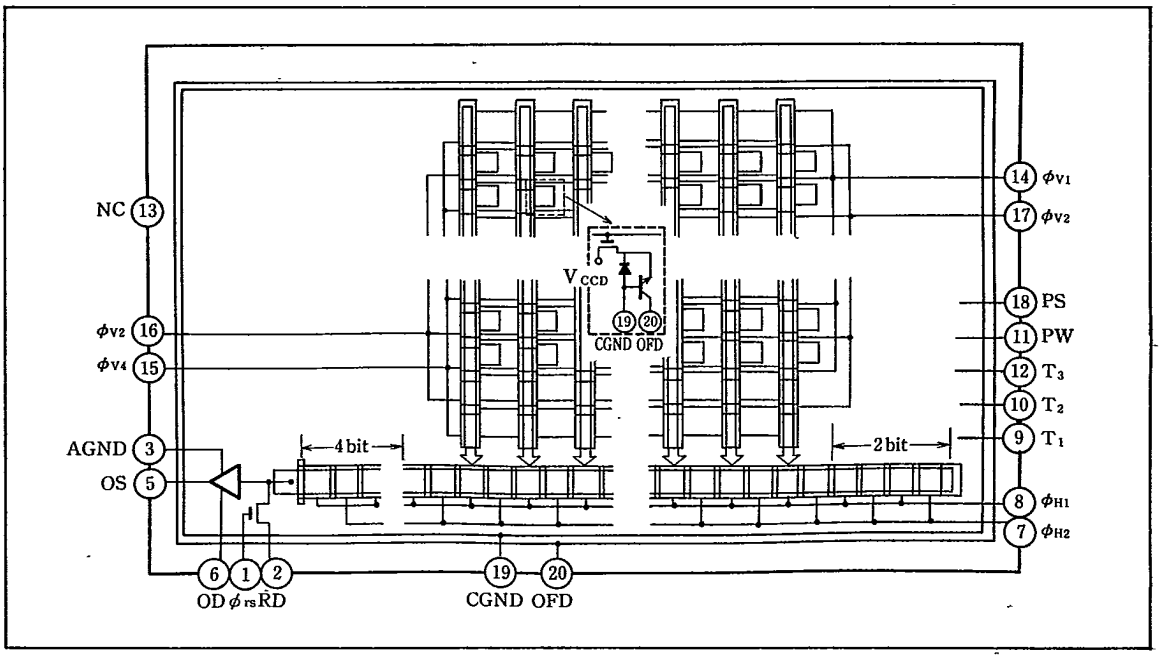
1. Number of effective pixels : 512 (H)×492 (V)
   Pixel pitch : 12.8 μm (H)×10.0 μm (V)
   The 542 horizontal pixels consist of 512 effective pixels, 2 optical black reference pixels at the left end and 28 optical black reference at the right end (See color filter array)
2. Low fixed pattern noise and lag
3. No geometric distortion and burn-in
4. Anti-blooming structure
5. Built-in output amplifier
6. Electronic shutter (1/1000 sec, 1/2000 sec)
7. 20-pin shrink dual-in-line package (CERDIP)

■ Pin Connections



Note : Great care must be taken not to be damaged by ESD. It comprises a CCD camera system used in combination with the timing IC (LZ92E62, LZ93N25), the SSG (LZ93N19), V driver IC (LR36682) and S/H IC (IR3P68, IR3P66).

■ Block Diagram



T-41-55

■ Pin Description

Symbol	Pin name
RD	Reset transistor drain
OD	Output transistor drain
OS	Video output
ϕ_{RS}	Reset transistor gate clock
ϕ_{V_1}, ϕ_{V_2}, ϕ_{V_3}, ϕ_{V_4}	Vertical shift register clock
ϕ_{H_1}, ϕ_{H_2}	Horizontal shift register clock
OFD	Overflow drain
PS	Photoshield
PW	P-well
AGND	Analog ground
CGND	Clock ground
T_1, T_2, T_3	Test pin
NC	Non connection

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Output transistor drain voltage	V_{OD}	0 to +18	V
Reset transistor drain voltage	V_{RD}	0 to +18	V
Overflow drain voltage	V_{OFD}	0 to +22	V
Photoshield voltage	V_{PS}	0 to V_{OD}	V
P-well voltage	V_{PW}	−8.5 to 0	V
Test pin voltage (T_1,T_3)	V_{T_1}, V_{T_3}	0 to V_{OD}	V
Test pin voltage (T_2)	V_{T_2}	0 to V_{OD}	V
Reset gate clock voltage	$V_{\phi RS}$	−0.3 to V_{OD}	V
Vertical shift register clock voltage	$V_{\phi V}$	V_{PW} to V_{OD}	V
Horizontal shift register clock voltage	$V_{\phi H}$	−0.3 to V_{OD}	V
Storage temperature	T_{stg}	−40 to +100	°C
Operating temperature	T_{opr}	−10 to +55	°C

■ Recommended Operating Conditions

Parameter		Symbol	MIN.	TYP.	MAX.	Unit
Operating temperature		T_{opr}	0	25.0	45.0	°C
Output transistor drain voltage		V_{OD}	14.5	15.0	15.5	V
Reset transistor drain voltage		V_{RD}	$V_{OD}-0.2$	V_{OD}	V_{OD}	V
Overflow drain voltage		V_{OFD}	5.0		18.0	V
Photoshield voltage		V_{PS}	1.0	1.25	1.5	V
P-well voltage		V_{PW}	−8.5	$V_{\phi VL}-1.0$	$V_{\phi VL}-0.7$	V
Analog ground voltage		V_{AGND}		0		V
Clock ground voltage		V_{CGND}		0		V
Test pin voltage	T_1, T_3 pin	V_{T1}, V_{T3}		0		V
	T_2 pin	V_{T2}	$V_{OD}-3.0$	V_{OD}	V_{OD}	V
Vertical shift register clock voltage	Low level	$V_{\phi V1L}$, $V_{\phi V3L}$ $V_{\phi V2L}$, $V_{\phi V4L}$	−7.5	−7.0	−6.8	V
	Intermediate level	$V_{\phi V1I}$, $V_{\phi V3I}$		0		V
		$V_{\phi V2I}$, $V_{\phi V4I}$	1.5	2.0	2.5	
	High level	$V_{\phi V1H}$, $V_{\phi V3H}$	13.5	14.0	14.5	V
Horizontal shift register clock voltage	Low level	$V_{\phi H1L}$, $V_{\phi H2L}$	0		0.7	V
	High level	$V_{\phi H1H}$, $V_{\phi H2H}$	4.7	5.0	6.0	V
Reset gate clock voltage	Low level	$V_{\phi RSL}$	0		$V_{RD}-8.0$	V
	High level	$V_{\phi RSH}$	$V_{RD}-3.5$		13.0	V
Vertical shift register clock frequency		$f_{\phi V1}$, $f_{\phi V2}$ $f_{\phi V3}$, $f_{\phi V4}$		15.73		kHz
Horizontal shift register clock frequency		$f_{\phi H1}$, $f_{\phi H2}$		9.53		MHz
Reset gate clock frequency		$f_{\phi RS}$		9.53		MHz

T-41-55

Electrical Characteristics (Field Integration Mode)

(Ta=25°C, Operating Conditions : Using typical values for the recommended operating conditions)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Standard output voltage	V_O		250		mV	2
Photo response non-uniformity	PRNU			10	%	3
Saturation output voltage	V_{sat}	650			mV	4
Dark output voltage	V_{dark}			15	mV	1, 5
Dark signal non-uniformity	DSNU			7	mV	1, 6
Responsivity	R	180	230		mV	7
Gamma	γ		1			
Smear Ratio	SMR			−60	dB	8, 9
Lag	AI			3	%	10
Antiblooming	ABL		100			11
Overflow drain voltage	V_{OFD}	5.0		18.0	V	12

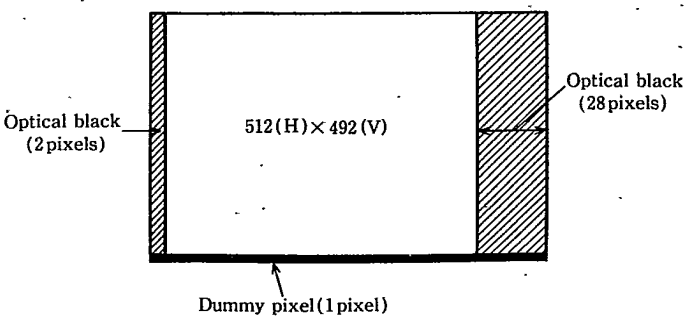
Notes

1. Ta=55°C
2. The average output voltage under standard condition that allows the voltage to be 250 mV.
3. The image area is sectioned into 10×10 small areas. The small-area voltage is the average of output voltages from all the pixels within the small area. PRNU is defined by $(V_{MAX}-V_{MIN}) / V_O$, where V_{MAX} and V_{MIN} are the maximum and the minimum respectively of the small-area voltages when the average output voltage V_O is 85 mV.
4. The average output voltage at a point where photo responsivity starts saturating.
5. The average output voltage under a non-exposure condition.
6. Defind by $(V_{DMAX}-V_{DMIN})$ under the non-exposure condition where V_{DMAX} and V_{DMIN} are the maximum and the minimum respectively of the pixel voltages in a central area of 50×50 pixels.
7. The average output voltage when a 1000 lux light source with a 90% reflector is imaged by a lens of F4, f50mm through the IR-absorbing filter (CM-500 1mmt).
8. The sensor is exposed only in the central area of V/10 square where V is the vertical length of the image area. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the pixel voltage in the V/10 square.
9. The light source is 3200°K halogen illumination through a 1mm thick CM-500 IR-absorbing filter.
10. The sensor is exposed at the exposure level corresponding to the standard condition. AI is defined by the ratio between the output voltage during the non-exposure measured at the 1st field.
11. The sensor is exposed only in the central area of the V/10 square. ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed extending from the exposed area to the non-exposed area.
12. The minimum voltage at the OFD under which the condition of 100 ABL is achieved.

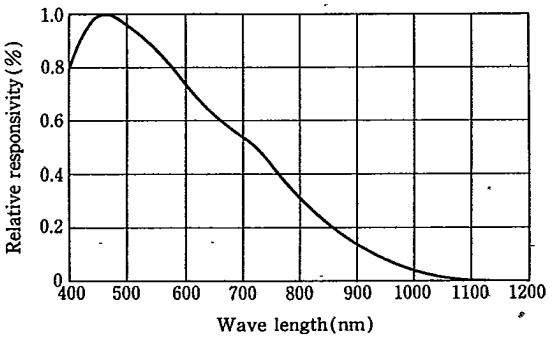
5

T-41-55

Pixel Structure

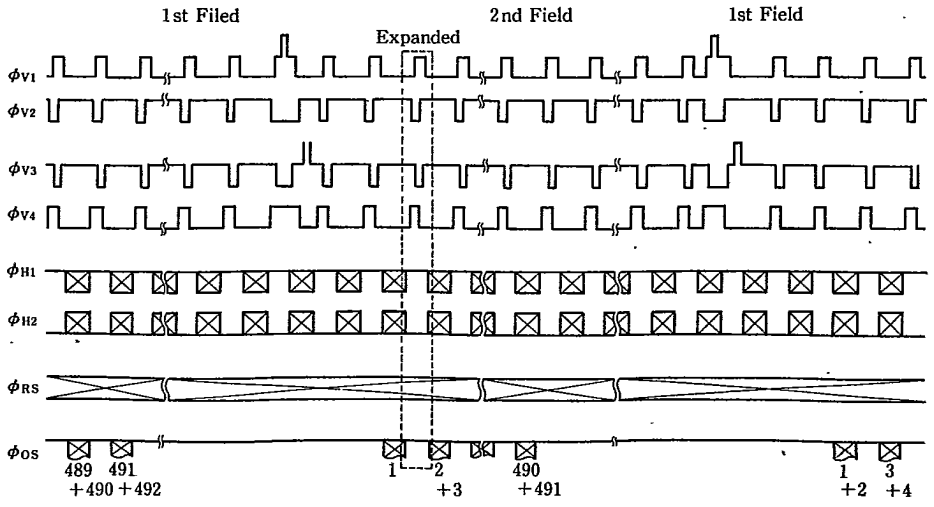


Spectral Response



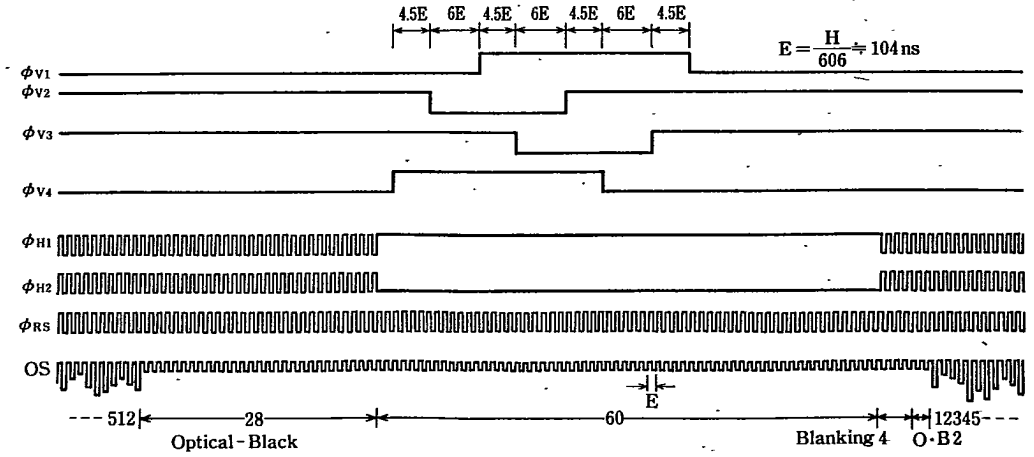
Timing Diagram

(1) V frequency timing

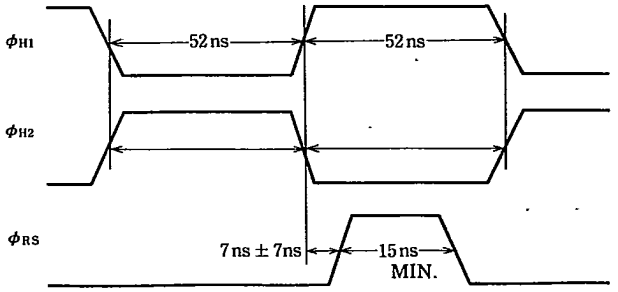


T-41-55

(2) H frequency timing



(3) H shift register clock



■ Precautions

1. Care must be taken not to damage the lid by mechanical stress because the lid is made of glass material.
2. Protect CCDs from destruction due to ESD by using conductive materials when storage, just as the same manner with the LSIs.
3. Ground human body and tools to discharge the static electricity when handling devices. A human body must be grounded through a resistor of approx. 1MΩ. Great care must be taken when handling because anti-ESD voltage of CCDs is lower than that of other LSIs.
4. Keep away from touching the glass surface. Stain or dust on the glass surface may cause faulty operation to CCDs. It is recommended to clean the glass surface of the device as below.
   . Use a cotton-tipped pick with a small amount of isopropyl alcohol on the tip, and wipe the glass surface gently in one direction.
5. Do not expose the device to the intensive light excepting in operation when mounting it to a camera.

■ System Configuration Example

T-41-55

(B/W video camera for NTSC TV in the field-integration mode)