



T-52-31

DS7833/DS8833/DS7835/DS8835 Quad TRI-STATE® Bus Transceivers

General Description

This family of TRI-STATE bus transceivers offers extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated DC or AC, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when $V_{CC} = 0V$. The receiver incorporates hysteresis to provide greater noise immunity. All devices utilize a high current TRI-STATE output driver. The DS7833/DS8833 and DS7835/DS8835 employ TRI-STATE outputs on the receiver also.

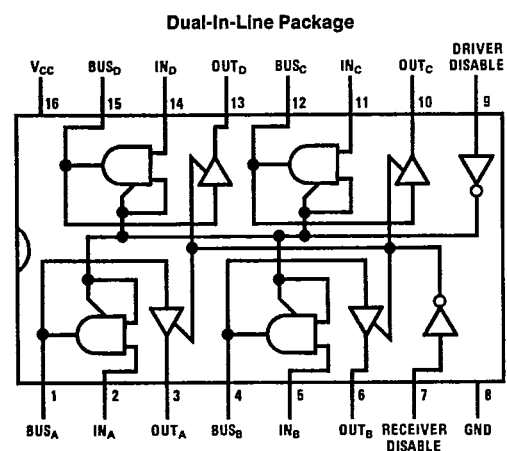
The DS7833/DS8833 are non-inverting quad transceivers with a common inverter driver disable control and common inverter receiver disable control.

The DS7835/DS8835 are inverting quad transceivers with a common inverter driver disable control and a common inverter receiver disable control.

Features

- Receiver hysteresis 400 mV typ
- Receiver noise immunity 1.4V typ
- Bus terminal current for normal V_{CC} or $V_{CC} = 0V$ 80 μA max
- Receivers
 - Sink 16 mA at 0.4V max
 - Source 2.0 mA (Mil) at 2.4V min
 - 5.2 mA (Com) at 2.4V min
- Drivers
 - Sink 50 mA at 0.5V max
 - Source 32 mA at 0.4V max
 - 10.4 mA (Com) at 2.4V min
 - 5.2 mA (Mil) at 2.4V min
- Drivers have TRI-STATE outputs
- DS7833/DS8833, DS7835/DS8835 receivers have TRI-STATE outputs
- Capable of driving 100 Ω DC-terminated buses
- Compatible with Series 54/74

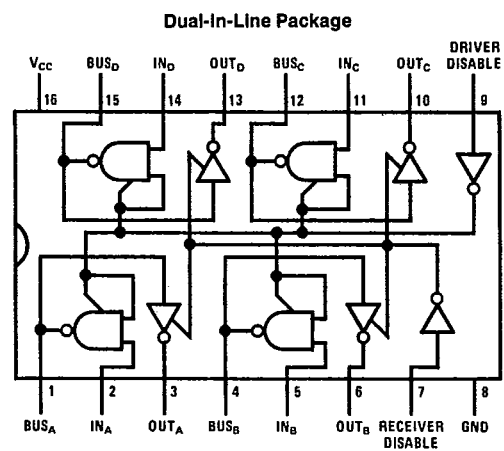
Connection Diagram



Top View

Order Number DS7833J, DS8833J
or DS8833N
See NS Package Number J16A or N16A

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Top View

Order Number DS7835J, DS8835J
or DS8835N
See NS Package Number J16A or N16A

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	-65°C to +150°C

Maximum Power Dissipation* at 25°C

Cavity Package	1509 mW
Molded Package	1476 mW

Lead Temperature (Soldering, 4 sec.) 260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions T-52-31

	Min	Max	Units
Supply Voltage, V_{CC}			
DS7833/DS7835	4.5	5.5	V
DS8833/DS8835	4.75	5.25	V
Temperature (T_A)			
DS7833/DS7835	-55	+125	°C
DS8833/DS8835	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units	
DISABLE/DRIVER INPUT								
V _{IH}	High Level Input Voltages	V _{CC} = Min		2.0			V	
V _{IL}	Low Level Input Voltage	V _{CC} = Min	DS7833, DS8833, DS8835			0.8	V	
			DS7835			0.7		
I _{IH}	High Level Input Current	V _{CC} = Max	V _{IN} = 2.4V			40	μA	
			V _{IN} = 5.5V			1.0	mA	
I _{IL}	Low Level Input Current	V _{CC} = Max, V _{IN} = 0.4V			−1.0	−1.6	mA	
V _{CL}	Input Clamp Diode	V _{CC} = 5.0V, I _{IN} = −12 mA, T _A = 25°C			−0.8	−1.5	V	
I _{IT}	Driver Low Level Disabled Input Current	Driver Disable Input = 2.0V, V _{IN} = 0.4V				−40	μA	
RECEIVER INPUT/BUS OUTPUT								
V _{TH}	High Level Threshold Voltage			DS7833, DS7835	1.4	1.75	2.1	V
				DS8833, DS8835	1.5	1.75	2.0	V
V _{TL}	Low Level Threshold Voltage			DS7833, DS7835	0.8	1.35	1.6	V
				DS8833, DS8835	0.8	1.35	1.5	V
I _S	Bus Current, Output Disabled or High	V _{BUS} = 4.0V	V _{CC} = Max		25	80	μA	
			V _{CC} = 0V		5.0	80	μA	
		V _{CC} = Max, V _{BUS} = 0.4V			−2.0	−40	μA	
V _{OH}	Logic “1” Output Voltage	V _{CC} = Min	I _{OUT} = −5.2 mA	DS7833, DS7835	2.4	2.75	V	
			I _{OUT} = −10.4 mA	DS8833, DS8835	2.4	2.75	V	
V _{OL}	Logic “0” Output Voltage	V _{CC} = Min	I _{OUT} = 50 mA		0.28	0.5	V	
			I _{OUT} = 32 mA			0.4	V	
I _{OS}	Output Short Circuit Current	V _{CC} = Max, (Note 4)		−40	−62	−120	mA	
RECEIVER OUTPUT								
V _{OH}	Logic “1” Output Voltage	V _{CC} = Min	I _{OUT} = −2.0 mA	DS7833, DS7835	2.4	3.0	V	
			I _{OUT} = −5.2 mA	DS8833, DS8835	2.4	2.9	V	
V _{OL}	Logic “0” Output Voltage	V _{CC} = Min, I _{OUT} = 16 mA			0.22	0.4	V	
I _{OT}	Output Disabled Current	V _{CC} = Max, Disable Inputs = 2.0V	V _{OUT} = 2.4V			40	μA	
			V _{OUT} = 0.4V			−40	μA	

Electrical Characteristics (Notes 2 and 3) (Continued)

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Symbol	Parameter	Conditions	Min	Typ	Max	Units	
RECEIVER OUTPUT (Continued)							
I _{OS}	Output Short Circuit Current	V _{CC} = Max, (Note 4)	DS7833, DS7835	28	−40	−70	mA
			DS8833, DS8835	−30		−70	mA
I _{CC}	Supply Current	V _{CC} = Max	DS7833, DS8833		84	116	mA
			DS7835, DS8835		75	95	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the -55°C to $+125^{\circ}\text{C}$ temperature range for the DS7833, DS7835 and across the 0°C to $+70^{\circ}\text{C}$ range for the DS8833, DS8835. All typicals are given for $V_{CC} = 5.0\text{V}$ and $T_A = 25^{\circ}\text{C}$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics $V_{CC} = 5.0\text{V}$, $T_A = 25^{\circ}\text{C}$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logic "0" from Input to Bus	(Figure 1) DS7833/DS8833		14	30	ns
		DS7835/DS8835		10	20	ns
t_{pd1}	Propagation Delay to a Logic "1" from Input to Bus	(Figure 1) DS7833/DS8833		14	30	ns
		DS7835/DS8835		11	30	ns
t_{pd0}	Propagation Delay to a Logic "0" from Bus to Input	(Figure 2) DS7833/DS8833		24	45	ns
		DS7835/DS8835		16	35	ns
t_{pd1}	Propagation Delay to a Logic "1" from Bus to Input	(Figure 2) DS7833/DS8833		12	30	ns
		DS7835/DS8835		18	30	ns
t_{PHZ}	Delay from Disable Input to High Impedance State (from Logic "1" Level)	$C_L = 5.0\text{ pF}$, (Figures 1 and 2) Driver		8.0	20	ns
		Receiver		6.0	15	ns
t_{PLZ}	Delay from Disable Input to High Impedance State (from Logic "0" Level)	$C_L = 5.0\text{ pF}$, (Figures 1 and 2) Driver		20	35	ns
		Receiver		13	25	ns
t_{PZH}	Delay from Disable Input to Logic "1" Level (from High Impedance State)	$C_L = 5.0\text{ pF}$, (Figures 1 and 2) Driver		24	40	ns
		Receiver		16	35	ns
t_{PZL}	Delay from Disable Input to Logic "0" Level (from High Impedance State)	$C_L = 5.0\text{ pF}$, (Figures 1 and 2) Driver		19	35	ns
		Receiver DS7833/DS8833		15	30	ns
		Receiver DS7835/DS8835		33	50	ns

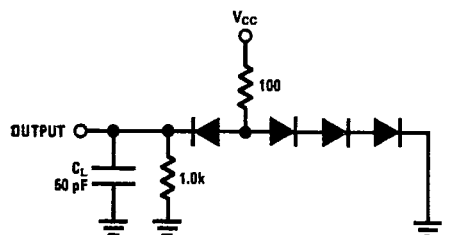
AC Test Circuits

FIGURE 1. Driver Output Load

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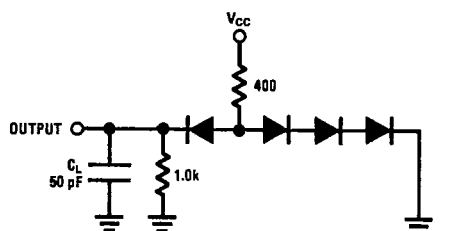
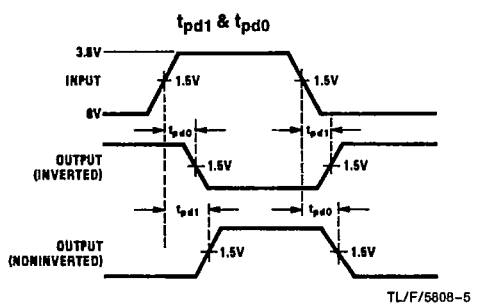


FIGURE 2. Receiver Output Load

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Switching Time Waveforms

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$f = 1 \text{ MHz}$
 $t_r = t_f \leq 10 \text{ ns}$ (10% to 90%)
 DUTY CYCLE = 50%

