National Semiconductor

ADVANCE INFORMATION

DS90C031
LVDS Quad CMOS Differential Line Driver

General Description

The DS90C031 is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 65 MHz utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90C031 accepts TTL/CMOS input levels and translates them to low voltage (330 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 7.5 mW typical.

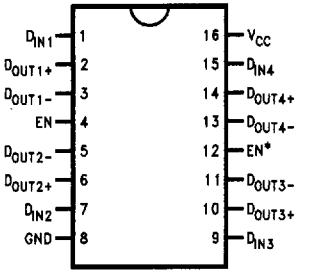
The DS90C031 and companion line receiver (DS90C032) provide a new alternative to high power psuedo-ECL devices for high speed point to point interfaces.

Features

- >65 MHz switching rates
- ±330 mV differential signaling
- Ultra low power dissipation
- 500 ps maximum differential skew
- 1.8 ns maximum chip to chip skew
- Industrial operating temperature range
- Available in surface mount packaging (SOIC)
- Pin compatible with DS26C31, MB571 and 41LG
- Compatible with IEEE P1596.3 SCI LVDS draft standard

Connection Diagram

Dual-In-Line



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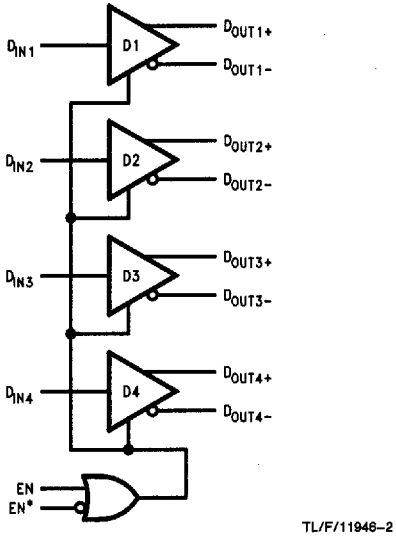
Order Number
DS90C031M or DS90C031N
See NS Package Number
M16A or N16E

Functional Diagram and Truth Tables



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DRIVER

Enables		Input	Outputs	
EN	EN*	D_{IN}	$D_{OUT}+$	$D_{OUT}-$
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
Input Voltage (D_{IN})	−0.3V to (V_{CC} + 0.3V)
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage ($D_{OUT}+$, $D_{OUT}-$)	−0.3V to (V_{CC} + 0.3V)
Short Circuit Duration ($D_{OUT}+$, $D_{OUT}-$)	Continuous
Maximum Package Power Dissipation @ +25°C	
M Package	TBDW
N Package	TBDW
Derate M Package	TBD mW/°C above +25°C
Derate N Package	TBD mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)	+260°C
Maximum Junction Temperature	+150°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	5.5	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified (Note 2).

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Output Voltage	R_L = 100Ω (*Figure 1*)	$D_{OUT}-$, $D_{OUT}+$	250	330	400	mV
ΔV_{OD1}	Change in Magnitude of V_{OD1} for Complementary Output States				TBD	25	|mV|
V_{OS}	Offset Voltage			1.125	1.2	1.275	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				TBD	25	|mV|
V_{OH}	Output Voltage High	R_L = 100Ω			1.365	1.4	V
V_{OL}	Output Voltage Low			1.0	1.035		V
V_{IH}	Input Voltage High		D_{IN}, EN, EN*	2.0		V_{CC}	V
V_{IL}	Input Voltage Low			GND		0.8	V
I_I	Input Current	V_{IN} = V_{CC}, GND, 2.5V, or 0.4V		−10		+10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5			V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	$D_{OUT}-$, $D_{OUT}+$		TBD	6.0	mA
I_{OZ}	Output TRI-STATE Current	EN = 0.8V and EN* = 2.0V, V_{OUT} = 0V or V_{CC}		−10		+10	μA
I_{CC}	No Load Supply Current Drivers Enabled	D_{IN} = V_{CC} or GND	V_{CC}		1.5	2.5	mA
		D_{IN} = 2.5V or 0.4V			TBD	TBD	mA
I_{CCL}	Loaded Supply Current Drivers Enabled	R_L = 100Ω All Channels V_{IN} = V_{CC} or GND (all inputs)			1.47	TBD	mA
I_{CCZ}	No Load Supply Current Drivers Disabled	D_{IN} = V_{CC} or GND EN = GND, EN* = V_{CC}			TBD	TBD	mA

Switching Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	$R_L = 100\Omega$, $C_L = 5$ pF (*Figures 2* and *3*)	0.6	1.3	2.4	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.6	1.3	2.4	ns
t_{SKD} $\lvert t_{PHLD} - t_{PLHD} \rvert$	Differential Skew		0	100	500	ps
t_{SK1}	Channel to Channel Skew			TBD	TBD	ns
t_{SK2}	Chip to Chip Skew	Note 4		TBD	1.8	ns
t_{TLH}	Rise Time	$R_L = 100\Omega$, $C_L = 5$ pF (*Figures 2* and *3*)	0.7	1.2	1.5	ns
t_{THL}	Fall Time		0.7	1.2	1.5	ns
t_{PHZ}	Disable Time High to Z			5	10	ns
t_{PLZ}	Disable Time Low to Z			5	10	ns
t_{PZH}	Enable Time Z to High			5	10	ns
t_{PZL}	Enable Time Z to Low			5	10	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.

Note 3: All typicals are given for: $V_{CC} = +5.0V$, $T_A = +25°C$.

Note 4: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

Parameter Measurement Information

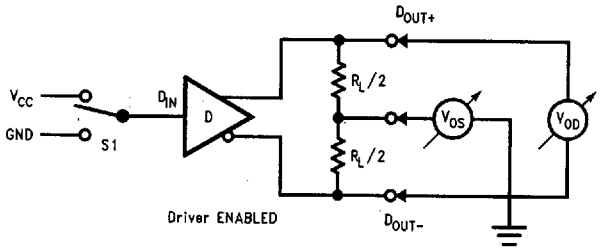

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FIGURE 1. Driver V_{OD} and V_{OS} Test Circuit

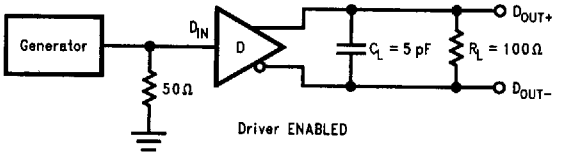

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FIGURE 2. Driver Propagation Delay and Transition Time Test Circuit

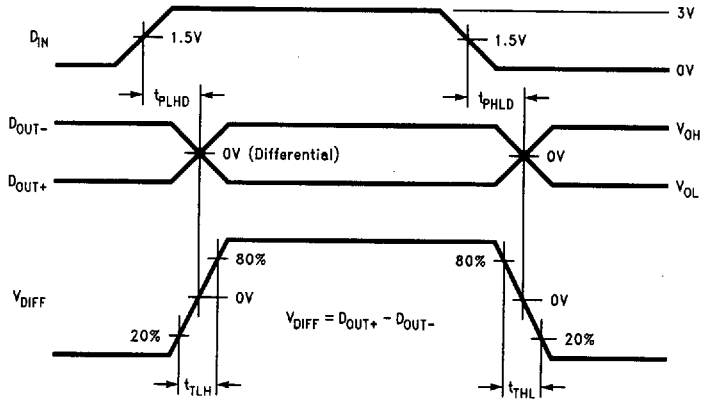

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FIGURE 3. Driver Propagation Delay and Transition Time Waveforms

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