National Semiconductor

T-75-45-05

DS96173/μA96173/DS96175/μA96175
RS-485/RS-422 Quad Differential Line Receivers

General Description

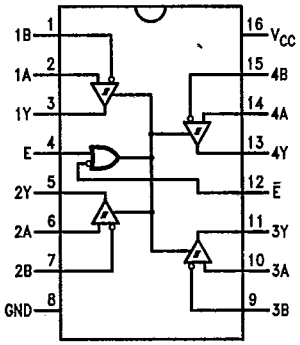
The DS96173/μA96173 and DS96175/μA96175 are high speed quad differential line receivers designed to meet EIA Standard RS-485. The devices have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −12V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96173/μA96173 features an active high and active low Enable, common to all four receivers. The DS96175/μA96175 features separate active high Enables for each receiver pair. Compatible RS-485 drivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96172/μA96172, DS96174/μA96174, DS96176/μA96176, DS96177/μA96177 and DS96178/μA96178.

Features

- Meets EIA Standard RS-485, RS-422A, RS-423A
- Designed for multipoint bus applications
- TRI-STATE Outputs
- Common mode input voltage range: −7V to +12V
- Operates from single +5V supply
- Input sensitivity of ±200 mV over common mode range
- Input hysteresis of 50 mV typical
- High input impedance
- Fail-safe input/output features drive output HIGH when input is open
- DS96173/μA96173/DS96175/μA96175 are lead and function compatible with SN75173/75175 or the AM26LS32/MC3486 respectively.

Connection Diagrams

16-Lead DIP
DS96173/μA96173



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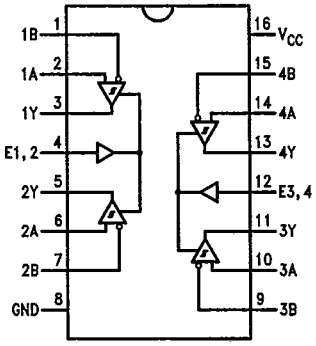
16-Lead DIP
DS96175/μA96175



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Order Number DS96173J, μA96173DC, DS96175J, μA96175DC
See NS Package Number J16A*

Order Number DS96173N, μA96173PC, DS96175N, μA96175PC
See NS Package Number N16A

*For most current package information, contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec.)	300°C
Molded DIP (soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Molded Package	1040 mW
Supply Voltage	7V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7V
Low Level Output Current	50 mA

*Derate cavity package 10 mW/°C above 25°C; derate molded DIP package 8.3 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5	5.25	V
Common Mode Input Voltage (V_{CM})	−7		+12	V
Differential Input Voltage (V_{ID})	−7		+12	V
Output Current High (I_{OH})			−400	μA
Output Current LOW (I_{OL})			16	mA
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.7V, I_O = − 0.4 mA				0.2	V
V_{TL}	Differential Input (Note 4) Low Threshold Voltage	V_O = 0.5V, I_O = 16 mA		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 5)	V_{CM} = 0V			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.5	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV, I_{OH} = −400 μA				2.7	V
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High Impedance State Output	V_O = 0.4V to 2.4V				±20	μA
I_I	Line Input Current (Note 6)	Other Input = 0V	V_I = 12V			1.0	mA
			V_I = −7V			−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−100	μA
R_I	Input Resistance			12	15		kΩ
I_{OS}	Short Circuit Output Current	(Note 7)		−15		−85	mA
I_{CC}	Supply Current	Outputs Disabled				75	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the 0°C to +70°C range for the DS96173/μA96173/DS96175/μA96175. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 5: Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 6: Refer to EIA Standards RS-485 for exact conditions.

Note 7: Only one output at a time should be shorted.

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	$V_{ID} = -2.5V$ to 2.5V, $C_L = 15$ pF, *Figure 1*		15	25	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			15	25	ns
t_{PZH}	Output Enable Time to High Level	$C_L = 15$ pF, *Figure 2*		15	22	ns
t_{PZL}	Output Enable Time to Low Level	$C_L = 15$ pF, *Figure 3*		15	22	ns
t_{PHZ}	Output Disable Time from High Level	$C_L = 5$ pF, *Figure 2*		14	30	ns
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5$ pF, *Figure 3*		24	40	ns

Function Tables

(Each Receiver) DS96173/μA96173

Differential Inputs	Enables		Outputs
A–B	E	$\overline{E}$	V
$V_{ID} > 0.2V$	H	X	H
	X	L	H
$V_{ID} < -0.2V$	H	X	L
	X	L	L
X	L	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

(Each Receiver) DS96175/μA96175

Differential Inputs A–B	Enable	Output Y
$V_{ID} \geq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

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Parameter Measurement Information

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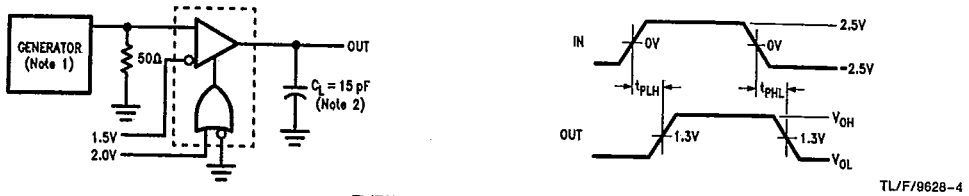

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FIGURE 1. t_{PLH}, t_{PHL} (Note 3)

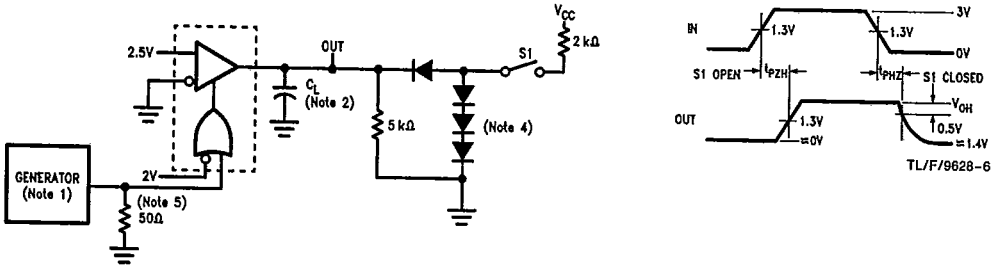

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FIGURE 2. t_{PHZ}, t_{PZH} (Note 3)

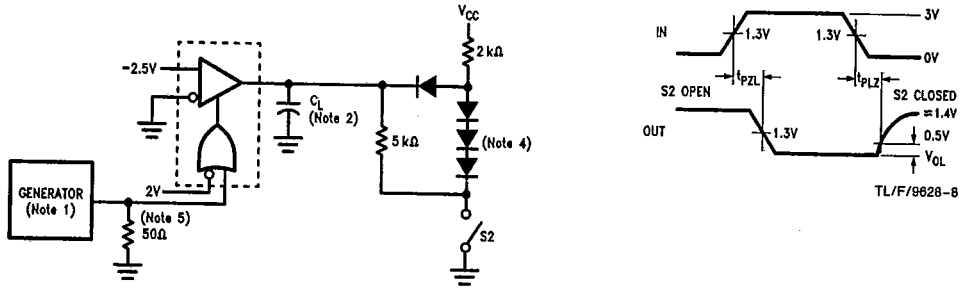

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FIGURE 3. t_{PZL}, t_{PLZ} (Note 3)

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and stray capacitance.

Note 3: DS96173/μA96173 with active high and active low Enables is shown here. DS96175/μA96175 has active high Enable only.

Note 4: All diodes are 1N916 or equivalent.

Note 5: To test the active low Enable $\overline{E}$ of DS96173/μA96173, ground E and apply an inverted input waveform to $\overline{E}$. DS96175/μA96175 has active high Enable only.

Typical Application

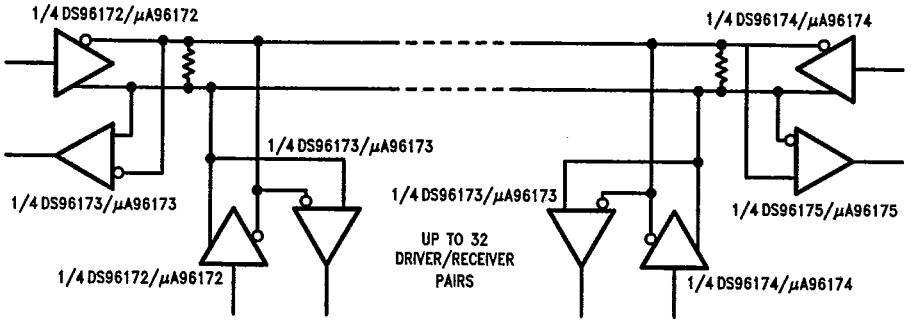

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FIGURE 4

Note: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.