National Semiconductor

PRELIMINARY
T-75-45-05

DS96F173/DS96F175
RS-485/RS-422 Quad Differential Receivers

General Description

The DS96F173 and the DS96F175 are high speed quad differential line receivers designed to meet EIA Standard RS-485. The DS96F173 and the DS96F175 offer improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS96F173 and the DS96F175 feature lower power, extended temperature range, improved RS-485 specifications, and meet SCSI specifications.

The DS96F173 and the DS96F175 have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input volage range of −12V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96F173 features an active high and active low Enable, common to all four receivers. The DS96F175 features separate active high Enables for each receiver pair.

Compatible RS-485 drivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96F172/DS96F174, DS36F95 and DS96F177/DS96F178.

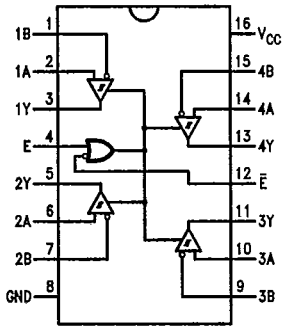
Features

- Meets EIA Standard RS-485, RS-422A, RS-423A
- Meets SCSI specifications
- Designed for multipoint bus applications
- TRI-STATE outputs
- Common mode input voltage range: −7V to +12V
- Operates from single +5.0V supply
- Extended temperature range available
- Lower power version
- Input sensitivity of ±200 mV over common mode range
- Input hysteresis of 50 mV typical
- High input impedance
- Fail-safe input/output features drive output HIGH when input is open
- DS96F173 and DS96F175 are lead and function compatible with SN75173/75175 or the AM26LS32/MC3486 respectively

Connection Diagrams

16-Lead DIP and SO-16 Package

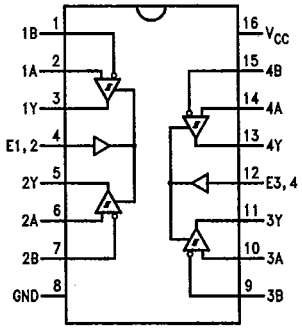
DS96F173



TL/F/9627–1

Top View

DS96F175



TL/F/9627–2

Top View

Order Number DS96F173CJ, DS96F173MJ, DS96F175CJ or DS96F175MJ
See NS Package Number J16A*

Order Number DS96F173CM or DS96F175CM
See NS Package Number M16A

Order Number DS96F173CN or DS96F175CN
See NS Package Number N16A

*For most current package information, contact product marketing.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP and SO-16: −65°C to +150°C

Lead Temperature
- Ceramic DIP (Soldering, 60 sec.): 300°C
- Molded DIP and SO-16 (Soldering, 10 sec.): 265°C

Maximum Power Dissipation* at 25°C
- Cavity Package: 1500 mW
- Molded Package: 1040 mW
- SO Package: 960 mW

Supply Voltage: 7.0V

Input Voltage, A or B Inputs: ±25V

Differential Input Voltage: ±25V

Enable Input Voltage: 7.0V

Low Level Output Current: 50 mA

*Derate cavity package 10 mW/°C above 25°C; derate molded DIP package 8.3 mW/°C above 25°C; derate SO package 7.7 mW°C above 25°C.

Recommended Operating Conditions T-75-45-05

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS96F173C/DS96F175C	4.75	5.0	5.25	V
DS96F173M/DS96F175M	4.50	5.0	5.50	
Common Mode Input Voltage V_{CM}	−7		+12	V
Differential Input Voltage (Note 2) (V_{ID})	−7		+12	V
Output Current HIGH (I_{OH})			−400	μA
Output Current LOW (I_{OL})			16	mA
Operating Temperature (T_A)				
DS96F173C/DS96F175C	0	25	70	°C
DS96F173M/DS96F175M	−55	25	125	

Electrical Characteristics over recommended operating conditions, unless otherwise specified (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential-Input High Threshold Voltage	$V_O = V_{OH}$				0.2	V
V_{TL}	Differential-Input (Note 4) Low Threshold Voltage	$V_O = V_{OL}$		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 5)	$V_{CM} = 0V$			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	Output Voltage HIGH	$V_{ID} = 200$ mV, $I_{OH} = -400$ μA	0°C to +70°C	2.8			V
			−55°C to +125°C	2.5			
V_{OL}	Output Voltage LOW	$V_{ID} = -200$ mV	$I_{OL} = 8.0$ mA			0.45	V
			$I_{OL} = 16$ mA			0.50	
I_{OZ}	High-Impedance State Output	$V_O = 0.4V$ to 2.4V				±20	μA
I_I	Line Input Current (Note 6)	Other Input = 0V	$V_I = 12V$			1.0	mA
			$V_I = -7.0V$			−0.8	
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7V$				20	μA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4V$				−100	μA
R_I	Input Resistance			14	18	22	kΩ
I_{OS}	Short Circuit Output Current	(Note 7)		−15		−85	mA
I_{CC}	Supply Current	No Load	Outputs Enabled			50	mA
I_{CCX}			Outputs Disabled			50	

1

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

T-75-45-05

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{ID} = −2.5V to +2.5V, C_L = 15 pF, *Figure 1*	5.0	15	22	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		5.0	15	22	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 2*		12	16	ns
t_{ZL}	Output Enable Time to Low Level	C_L = 15 pF, *Figure 3*		13	18	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 2*		14	20	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0 pF, *Figure 3*		14	18	ns
$\|t_{PLH}-t_{PHL}\|$	Pulse Width Distortion (SKEW)	*Figure 1*		1.0	3.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range the DS96F173M/DS96F175M and across the 0°C to +70°C range for the DS96F173C/DS96F175C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 5: Hysteresis is the difference between the positive-going input threshold voltage. V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 6: Refer to EIA Standards RS-485 for exact conditions.

Note 7: Only one output at a time should be shorted.

Function Tables

(Each Receiver) DS96F173

Differential Inputs	Enables		Outputs
A−B	E	$\overline{E}$	V
V_{ID} > 0.2V	H	X	H
	X	L	H
V_{ID} < −0.2V	H	X	L
	X	L	L
X	L	H	Z

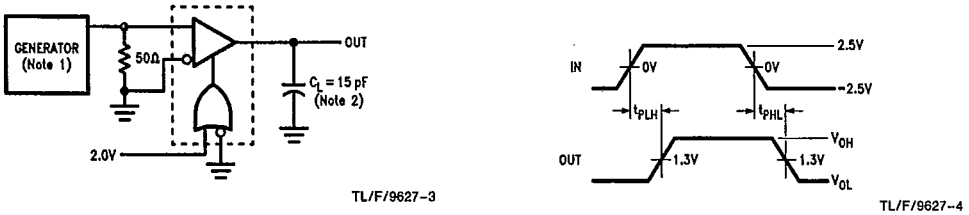
H = High Level
L = Low Level
Z = High Impedance (off)
X = Immaterial

(Each Receiver) DS96F175

Differential Inputs A−B	Enable	Output Y
$V_{ID} \geq$ 0.2V	H	H
$V_{ID} \leq$ −0.2V	H	L
X	L	Z

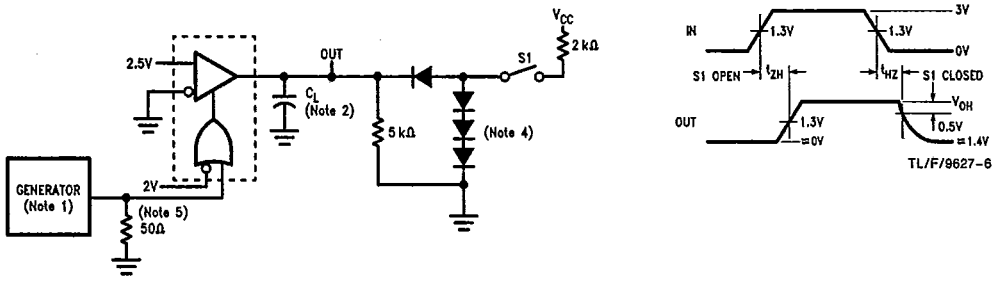
Parameter Measurement Information

T-75-45-05



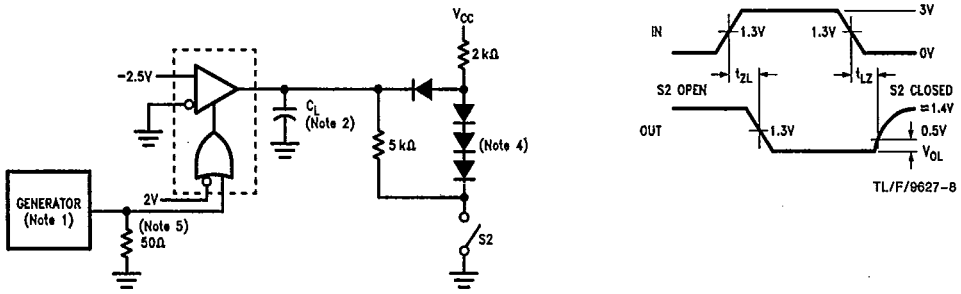
TL/F/9627–3 TL/F/9627–4

FIGURE 1. t_{PLH}, t_{PHL} (Note 3)



TL/F/9627–5 TL/F/9627–6

FIGURE 2. t_{HZ}, t_{ZH} (Note 3)



TL/F/9627–7 TL/F/9627–8

FIGURE 3. t_{ZL}, t_{LZ} (Note 3)

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and stray capacitance.

Note 3: DS96F173 with active high and active low Enables is shown here. DS96F175 has active high Enable only.

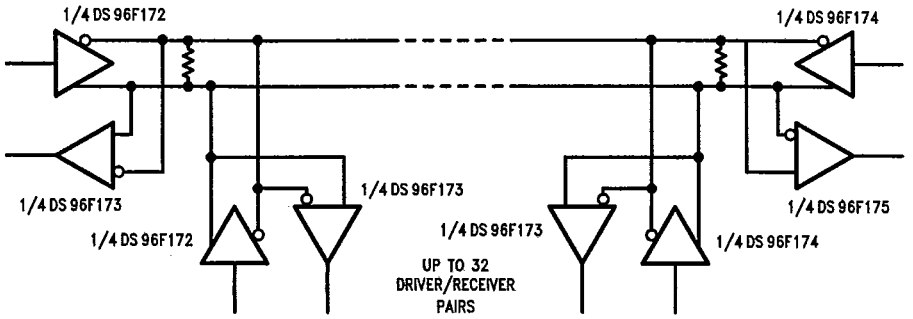
Note 4: All diodes are 1N916 or equivalent.

Note 5: To test the active low Enable $\overline{E}$ of DS96F173, ground E and apply an inverted input waveform to $\overline{E}$. DS96F175 has active high enable only.

1

Typical Application

T-75-45-05



TL/F/9627–9

FIGURE 4

Note: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.