SECTION 2

SPECIFICATIONS

INTRODUCTION

The DSP56011 is fabricated in high density CMOS with Transistor-Transistor Logic (TTL) compatible inputs and outputs. The DSP56011 specifications are preliminary and are from design simulations, and may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after full characterization and device qualifications are complete.

MAXIMUM RATINGS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification will never occur in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1 Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CC}	–0.3 to +7.0	V
All input voltages	V_{IN}	GND – 0.5 to V_{CC} + 0.5	V
Current drain per pin excluding V_{CC} and GND	I	10	mA
Operating temperature range	T_J	–40 to +125	°C
Storage temperature	T_{STG}	–55 to +150	°C

Notes: 1. GND = 0 V, V_{CC} = 5.0 V ± 5%, T_J = –40°C to +125°C, CL = 50 pF + 2 TTL Loads
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.

THERMAL CHARACTERISTICS

Table 2-2 Thermal Characteristics

Characteristic	Symbol	TQFP Value	Unit
Junction-to-ambient thermal resistance[1]	$R_{\theta JA}$ or θ_{JA}	50	°C/W
Junction-to-case thermal resistance[2]	$R_{\theta JC}$ or θ_{JC}	5	°C/W
Thermal characterization parameter	Ψ_{JT}	1.7	°C/W

Notes: 1. Junction-to-ambient thermal resistance is based on measurements on a horizontal-single-sided printed circuit board per SEMI G38-87 in natural convection.(SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111)
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.

DC ELECTRICAL CHARACTERISTICS

Table 2-3 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input high voltage					
• EXTAL	V_{IHC}	4.0	—	V_{CC}	V
• $\overline{\text{RESET}}$	V_{IHR}	2.5	—	V_{CC}	V
• MODA, MODB, MODC	V_{IHM}	3.5	—	V_{CC}	V
• ACI, SHI inputs[1]	V_{IHS}	$0.7 \times V_{CC}$	—	V_{CC}	V
• All other inputs	V_{IH}	2.0	—	V_{CC}	V
Input low voltage					
• EXTAL	V_{ILC}	–0.5	—	0.6	V
• MODA, MODB, MODC	V_{ILM}	–0.5	—	2.0	V
• ACI, SHI inputs[1]	V_{ILS}	–0.5	—	$0.3 \times V_{CC}$	V
• All other inputs	V_{IL}	–0.5	—	0.8	V
Input leakage current	I_{IN}				
• EXTAL, $\overline{\text{RESET}}$, MODA, MODB, MODC, $\overline{\text{DR}}$		–1	—	1	µA
• Other Input Pins (@ 2.4 V/0.4 V)		–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage (I_{OH} = –0.4 mA)	V_{OH}	2.4	—	—	V
Output low voltage (I_{OL} = 3.2 mA) SCK/SCL I_{OL} = 6.7 mA MISO/SDA I_{OL} = 6.7 mA $\overline{\text{HOREQ}}$ I_{OL} = 6.7 mA	V_{OL}	—	—	0.4	V
Internal Supply Current @ 81 MHz					
• Normal mode	I_{CCI}	—	135	TBD	mA
• Wait mode	I_{CCW}	—	22	TBD	mA
• Stop mode[2]	I_{CCS}	—	5	TBD	µA
PLL supply current @ 81 MHz		—	1.2	2.0	mA
Input capacitance[3]	C_{IN}	—	10	—	pF

Notes:
1. The SHI inputs are: MOSI/HA0, $\overline{\text{SS}}$/HA2, MISO/SDA, SCK/SCL, and $\overline{\text{HREQ}}$.
2. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). PLL signals are disabled during Stop state.
3. Periodically sampled and not 100% tested

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all inputs, except EXTAL, $\overline{\text{RESET}}$, MODA, MODB, $\overline{\text{MODC}}$, ACI, and SHI inputs (MOSI/HA0, $\overline{\text{SS}}$/HA2, MISO/SDA, SCK/SCL, $\overline{\text{HREQ}}$). These inputs are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56011 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.

All output delays are given for a 50 pF load unless otherwise specified. For load capacitance greater than 50 pF, the drive capability of the output pins typically decreases linearly:

1. At 1.5 ns per 10 pF of additional capacitance at all output pins except MOSI/HA0, MISO/SDA, SCK/SCL, $\overline{\text{HREQ}}$
2. At 1.0 ns per 10 pF of additional capacitance at output pins MOSI/HA0, MISO/SDA, SCK/SCL, $\overline{\text{HREQ}}$ (in SPI mode only)

INTERNAL CLOCKS

Table 2-4 Internal Clocks

Characteristics	Symbol	Expression	
		Minimum	Maximum
Internal operation frequency	f	0	81 MHz
Internal clock high period • with PLL disabled[1] • with PLL enabled and MF ≤ 4 • with PLL enabled and MF > 4	Th	 $ETh_{minimum}$ $0.48 \times Tc$ $0.467 \times Tc$	 $ETh_{maximum}$ $0.52 \times Tc$ $0.533 \times Tc$
Internal clock low period • with PLL disabled[1] • with PLL enabled and MF ≤ 4 • with PLL enabled and MF > 4	Tl	 $ETl_{minimum}$ $0.48 \times Tc$ $0.467 \times Tc$	 $ETl_{maximum}$ $0.52 \times Tc$ $0.533 \times Tc$
Internal clock cycle time	Tc	(DF × ETc)/MF	
Instruction cycle time	I_{cyc}	2 × Tc	

Notes: 1. See **Table 2-5** on page 2-5 for External Clock (ET) specifications.

EXTERNAL CLOCK OPERATION

The DSP56011 system clock is externally supplied via the EXTAL pin. Timings shown in this document are valid for clock rise and fall times of 3 ns maximum. The 81 MHz speed allows the DSP56011 to take advantage of the 27 MHz system clock in DVD applications.

Table 2-5 External Clock (EXTAL Pin)

No.	Characteristics	Sym.	81 MHz Min	81 MHz Max	Unit
	Frequency of external clock (EXTAL)	Ef	0	81	MHz
1	External clock input high—EXTAL[1]	ETh			
	• with PLL disabled (46.7%–53.3% duty cycle)		5.8	∞	ns
	• with PLL enabled (42.5%–57.5% duty cycle)		5.2	235500	ns
2	External clock input low—EXTAL Pin[1]	ETl			
	• with PLL disabled (46.7%–53.3% duty cycle)		5.8	∞	ns
	• with PLL enabled (42.5%–57.5% duty cycle)		5.2	235500	ns
3	External clock cycle time[1] • with PLL disabled • with PLL enabled	ETc	12.3 12.3	∞ 409600	ns
4	Instruction cycle time $= I_{cyc} = 2 \times Tc$[1] • with PLL disabled • with PLL enabled	I_{cyc}	24.7 24.7	∞ 819200	ns

Note: 1. EXTAL input high and input low are measured at 50% of the input transition.

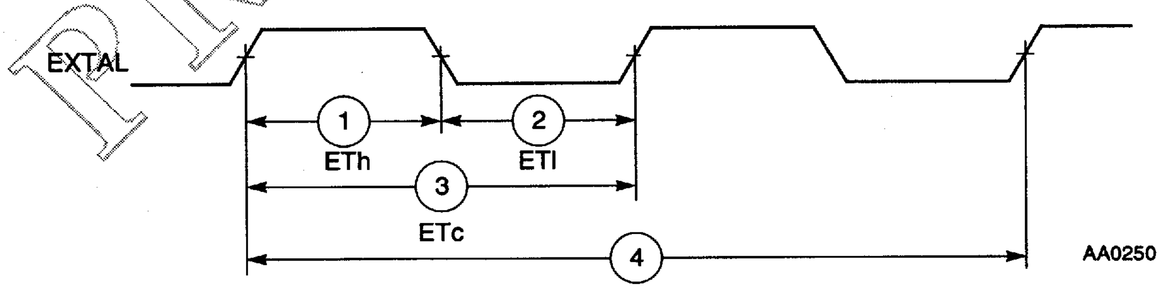


Figure 2-1 External Clock Timing

PHASE LOCK LOOP (PLL) CHARACTERISTICS

Table 2-6 Phase Lock Loop (PLL) Characteristics

Characteristics	Expression	Min	Max	Unit
VCO frequency when PLL enabled	MF × Ef	10	f	MHz
PLL external capacitor (PCAP pin to V_{CCP})	MF × Cpcap @ MF ≤ 4 @ MF > 4	 MF × 340 MF × 380	 MF × 480 MF × 970	 pF pF
Note: Cpcap is the value of the PLL capacitor (connected between PCAP pin and V_{CCP}) for MF = 1. The recommended value for Cpcap is 400 pF for MF ≤ 4 and 540 pF for MF > 4. The maximum VCO frequency is limited to the internal operation frequency, defined in **Table 2-4**.				

RESET, STOP, MODE SELECT, AND INTERRUPT TIMING

(V_{CC} = 5.0 V ± 5%; T_J = 125°C; C_L = 50 pF + 2 TTL Loads)

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing

No.	Characteristics	81 MHz		Unit
		Min	Max	
10	Minimum $\overline{RESET}$ assertion width: • PLL disabled • PLL enabled[1]	 25 × Tc 2500 × ETc	 — —	 ns ns
14	Mode select setup time	21	—	ns
15	Mode select hold time	0	—	ns
16	Minimum edge-triggered interrupt request assertion width	13	—	ns
16a	Minimum edge-triggered interrupt request deassertation width	13	—	ns
18	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{NMI}$ assertion to GPIO valid caused by first interrupt instruction execution • GPIO0–GPIO7 • PB14–PB0	 12 × Tc + Th 11 × Tc + Th	 — —	 ns ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing (Continued)

No.	Characteristics	81 MHz		Unit
		Min	Max	
22	Delay from General Purpose Output valid to interrupt request deassertion for level sensitive fast interrupts—if second interrupt instruction is:[2] • Single cycle • Two cycles		 Tl – 31 (2 × Tc) + Tl – 31	 ns ns
25	Duration of $\overline{\text{IRQA}}$ assertion for recovery from stop state	12	—	ns
27	Duration for level-sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop mode) • Stable external clock, OMR bit 6 = 1 • Stable external clock, PCTL bit 17 = 1	 6 × Tc + Tl 12	 — —	 ns ns

Note:
1. This timing requirement is sensitive to the quality of the external PLL capacitor connected to the PCAP pin. For capacitor values *less than or equal to* 2 nF, asserting RESET according to this timing requirement will ensure proper processor initialization for capacitors with a delta C/C *less than* 0.5%. (This is typical for ceramic capacitors.) For capacitor values *greater than* 2 nF, asserting RESET according to this timing requirement will ensure proper processor initialization for capacitors with a delta C/C *less than* 0.01%. (This is typical for Teflon, polystyrene, and polypropylene capacitors.) However, capacitors with values *greater than* 2 nF with a delta C/C *greater than* 0.01% may require longer RESET assertion to ensure proper initialization.
2. When using fast interrupts and IRQA and IRQB are defined as level-sensitive, timing 22 applies to prevent multiple interrupt service. To avoid these timing restrictions, negative-edge-triggered configuration is recommended when using fast interrupts. Long interrupts are recommended when using level-sensitive configuration.

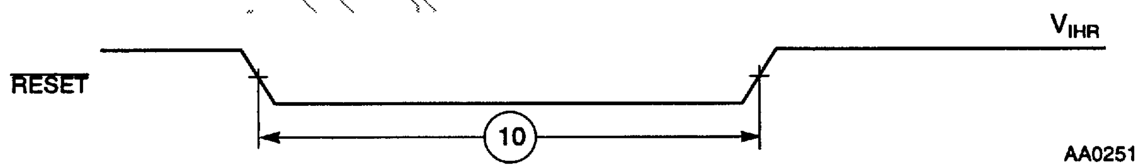


Figure 2-2 Reset Timing

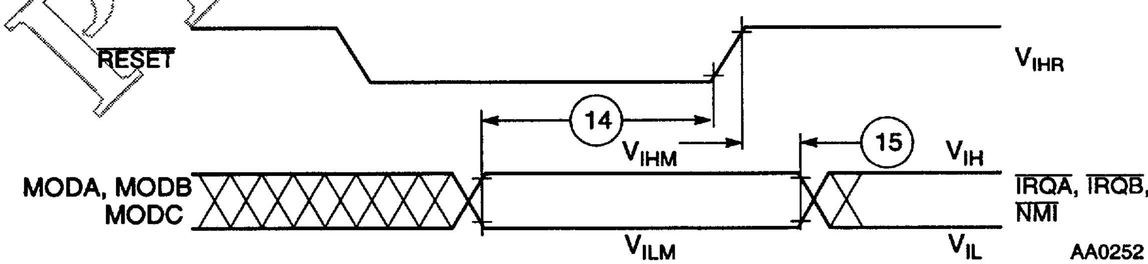


Figure 2-3 Operating Mode Select Timing

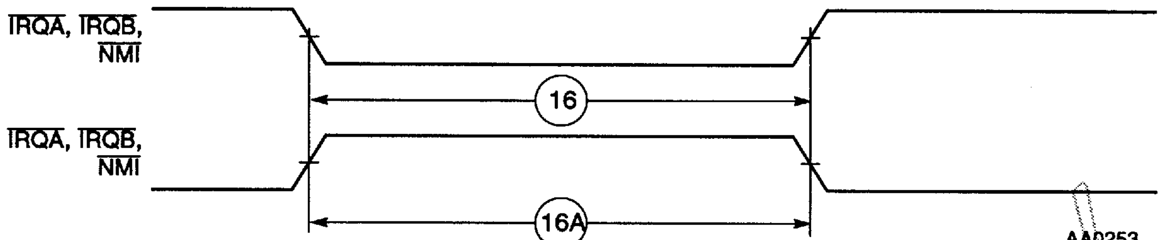


Figure 2-4 External Interrupt Timing (Negative Edge-triggered)

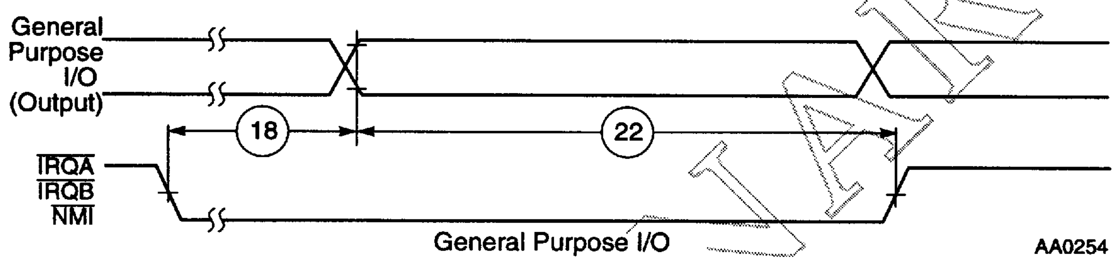


Figure 2-5 External Level-sensitive Fast Interrupt Timing

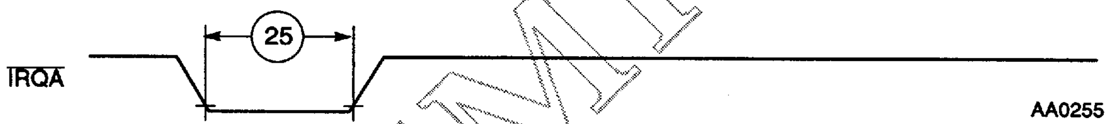


Figure 2-6 Recovery from Stop State Using $\overline{IRQA}$

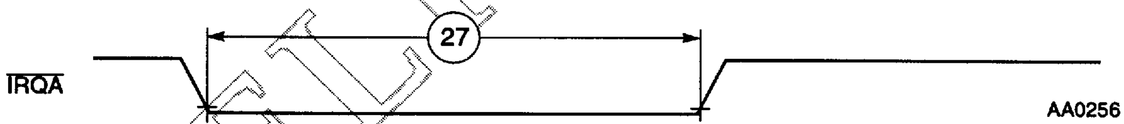


Figure 2-7 Recovery from Stop State Using $\overline{IRQA}$ Interrupt Service

HOST INTERFACE (HI) TIMING

V_{CC} = 5.0 V ± 5%; T_J = 125° C; C_L = 50 pF + 2 TTL loads

Note: Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications.

Table 2-8 Host I/O Timing (81 MHz)

Num	Characteristics	Min	Max	Unit
31	$\overline{HEN}/\overline{HACK}$ assertion width[1] • CVR, ICR, ISR, RXL read • IVR, RXH/M read • Write	 $T_C + 31$ 26 13	 — — —	 ns
32	$\overline{HEN}/\overline{HACK}$ deassertion width[1] • After TXL writes[2] • After RXL reads[3] • Between two CVR, ICR, or ISR reads	13 $2 \times T_C + 31$ $2 \times T_C + 31$ $2 \times T_C + 31$	— — — —	ns ns ns ns
33	Host data input setup time before $\overline{HEN}/\overline{HACK}$ deassertion	4	—	ns
34	Host data input hold time after $\overline{HEN}/\overline{HACK}$ deassertion	3	—	ns
35	$\overline{HEN}/\overline{HACK}$ assertion to output data active from high impedance	0	—	ns
36	$\overline{HEN}/\overline{HACK}$ assertion to output data valid	—	26	ns
37	$\overline{HEN}/\overline{HACK}$ deassertion to output data high impedance[5]	—	18	ns
38	Output data hold time after $\overline{HEN}/\overline{HACK}$ Deassertion[6]	2.5	—	ns
39	HR/$\overline{W}$ low setup time before $\overline{HEN}$ assertion	0	—	ns
40	HR/$\overline{W}$ low hold time after $\overline{HEN}$ deassertion	3	—	ns
41	HR/$\overline{W}$ high setup time to $\overline{HEN}$ assertion	0	—	ns
42	HR/$\overline{W}$ high hold time after $\overline{HEN}/\overline{HACK}$ deassertion	3	—	ns
43	HOA0–HOA2 setup time before $\overline{HEN}$ assertion	0	—	ns
44	HOA0–HOA2 Hold Time After $\overline{HEN}$ Deassertion	3	—	ns
45	DMA $\overline{HACK}$ assertion to $\overline{HOREQ}$ deassertion[4]	3	45	ns
46	DMA $\overline{HACK}$ deassertion to $\overline{HOREQ}$ assertion[4,5] • for DMA RXL read • for DMA TXL write • all other cases	 $T_L + T_C + T_H$ $T_L + T_C$ 0	 — — —	 ns ns ns

Table 2-8 Host I/O Timing (81 MHz) (Continued)

Num	Characteristics	Min	Max	Unit
47	Delay from $\overline{HEN}$ deassertion to $\overline{HOREQ}$ assertion for RXL read[4,5]	$T_L + T_C + T_H$	—	ns
48	Delay from $\overline{HEN}$ deassertion to $\overline{HOREQ}$ assertion for TXL write[4,5]	$T_L + T_C$	—	ns
49	Delay from $\overline{HEN}$ assertion to $\overline{HOREQ}$ deassertion for RXL read, TXL write[4,5]	3	58	ns

Note:
1. See **Host Port Considerations** in the section on **Design Considerations**.
2. This timing is applicable only if a write to the TXL is followed by writing the TXL, TXM, or TXH registers without first polling the TXDE or $\overline{HOREQ}$ flags, or waiting for $\overline{HOREQ}$ to be asserted.
3. This timing is applicable only if a read from the RXL is followed by reading the RXL, RXM or RXH registers without first polling the RXDF or $\overline{HOREQ}$ flags, or waiting for $\overline{HOREQ}$ to be asserted.
4. $\overline{HOREQ}$ is pulled up by a 1 kΩ resistor.
5. Specifications are periodically sampled and not 100% tested.
6. May decrease to 0 ns for future versions

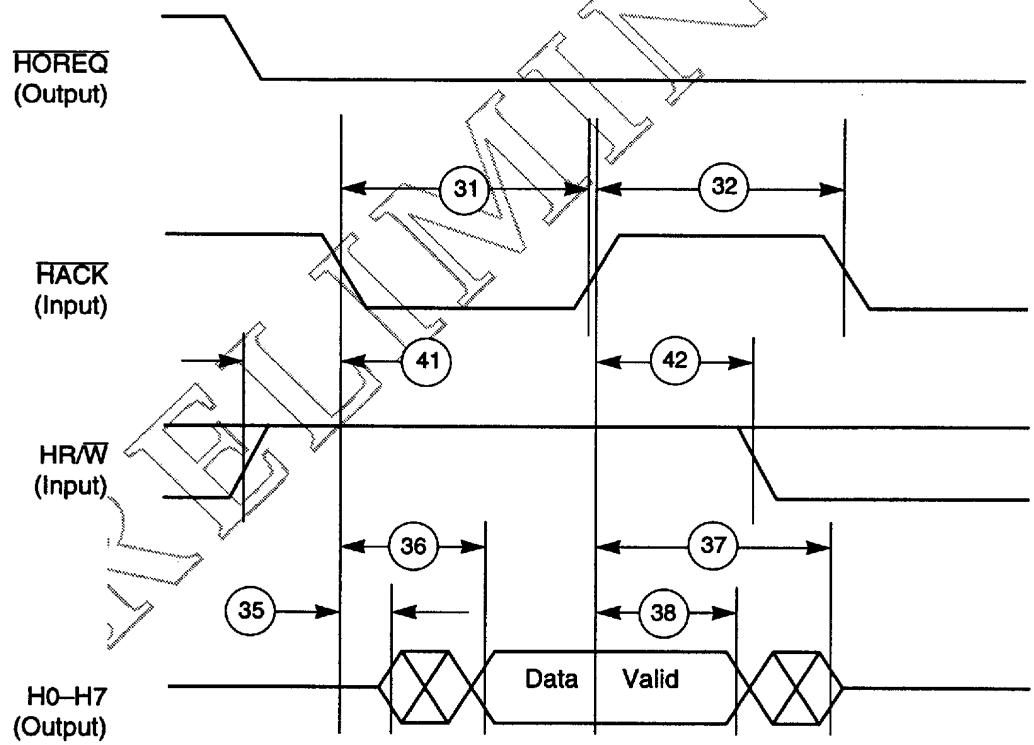


Figure 2-8 Host Interrupt Vector Register (IVR) Read

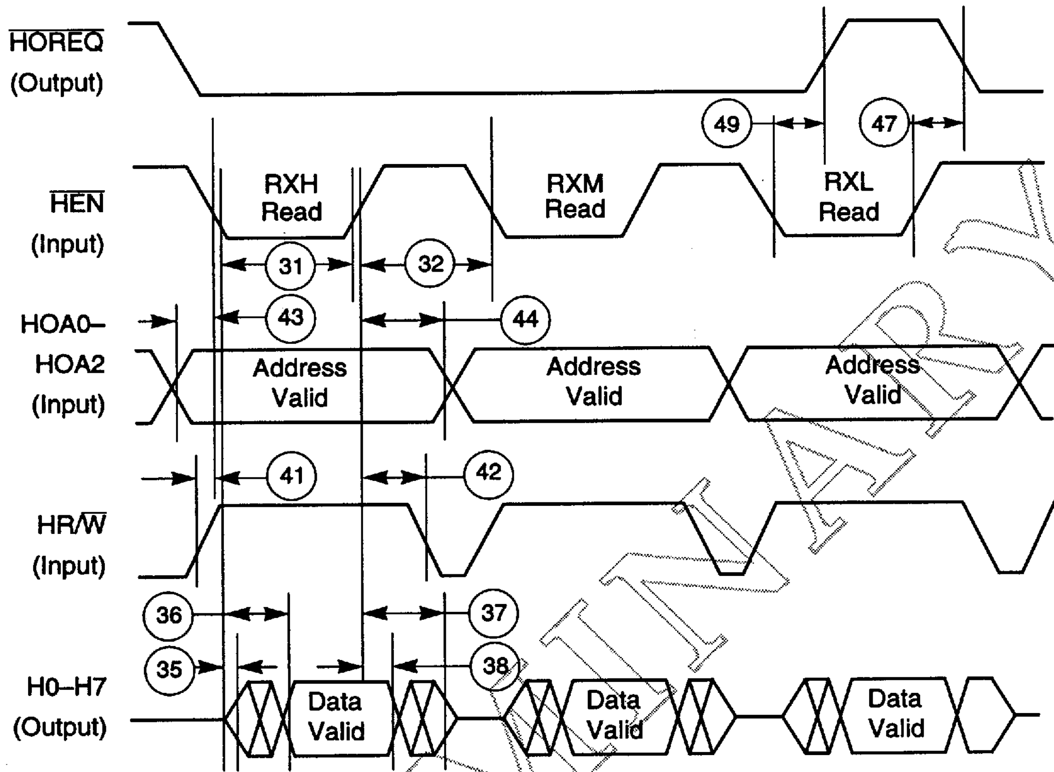


Figure 2-9 Host Read Cycle (Non-DMA Mode)

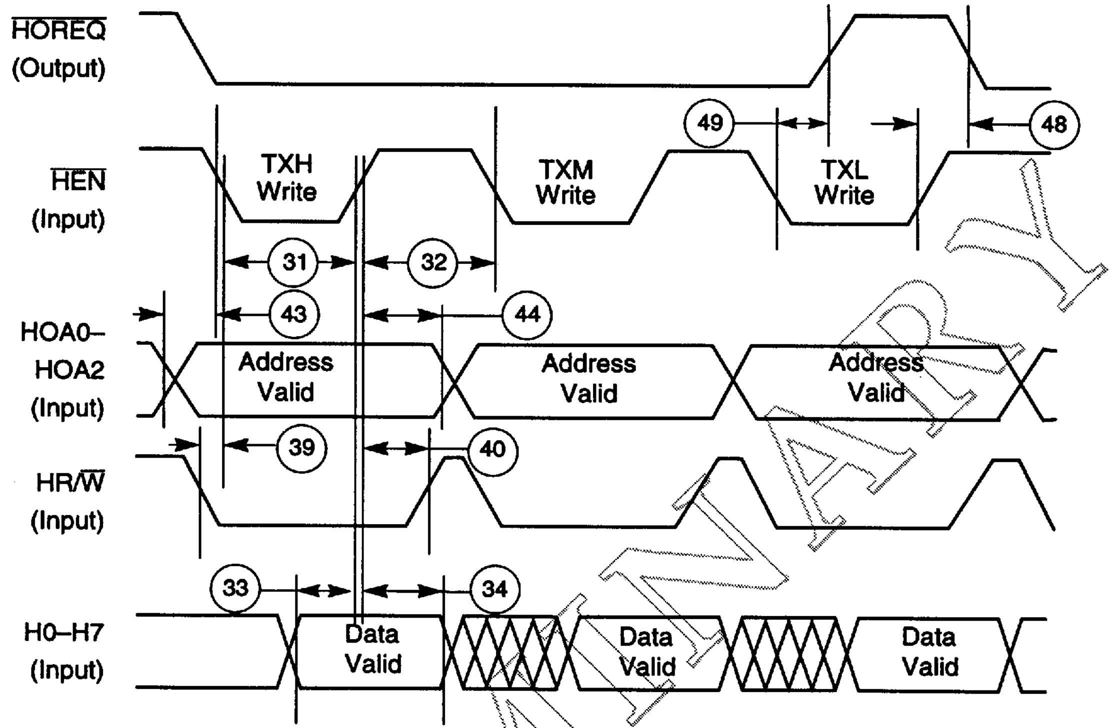


Figure 2-10 Host Write Cycle (Non-DMA Mode)

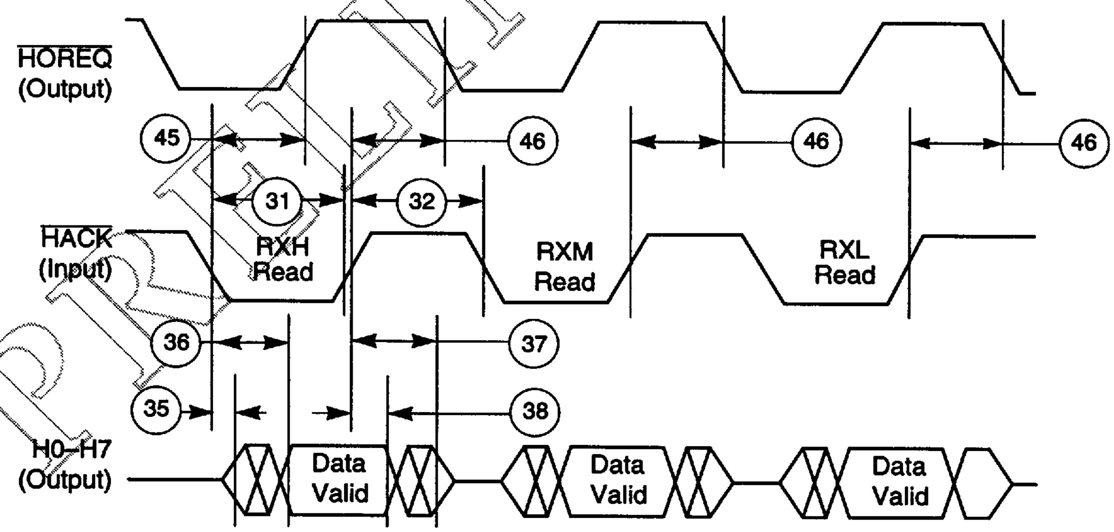


Figure 2-11 Host DMA Read Cycle

6367248 0148290 631

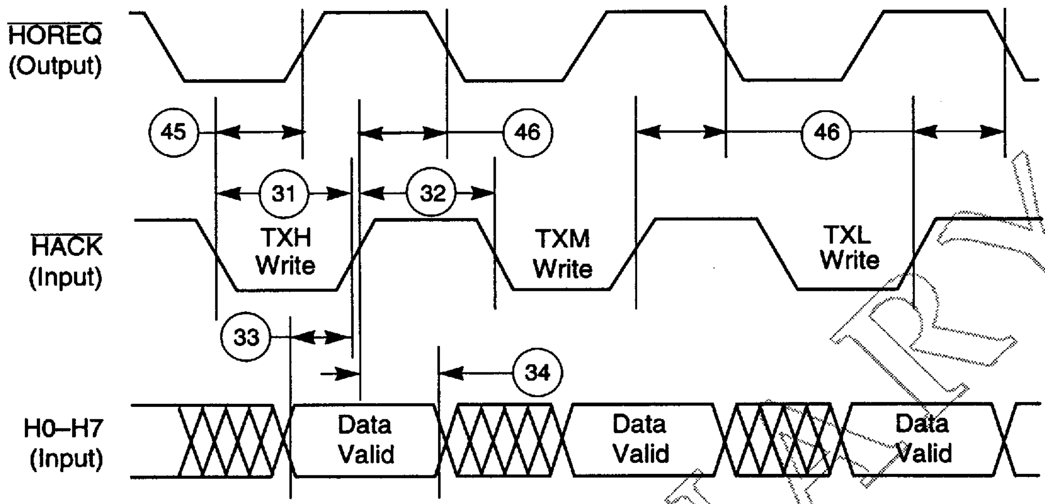


Figure 2-12 Host DMA Write Cycle

SERIAL AUDIO INTERFACE (SAI) TIMING

(V_{CC} = 5.0 V ± 5%, T_J = 125°C, C_L = 50pF + 2 TTL Loads)

Table 2-9 Serial Audio Interface (SAI) Timing

No.	Characteristics	Mode	Expression	81 MHz Min	81 MHz Max	Unit
111	Minimum Serial Clock cycle = t_{SAICC} (min)	Master	4 × Tc	49.4	—	ns
		Slave	3 × Tc + 5	42	—	ns
112	Serial Clock high period	Master	0.5 × t_{SAICC} − 8	16.7	—	ns
		Slave	0.35 × t_{SAICC}	14.7	—	ns
113	Serial Clock low period	Master	0.5 × t_{SAICC} − 8	16.7	—	ns
		Slave	0.35 × t_{SAICC}	14.7	—	ns
114	Serial Clock rise/fall time	Master	8	—	8	ns
		Slave	0.15 × t_{SAICC}	—	6.3	ns
115	Data input valid to SCKR edge (data input setup time)	Master	26	26	—	ns
		Slave	4	4	—	ns
116	SCKR edge to data input not valid (data input hold time)	Master	0	0	—	ns
		Slave	14	14	—	ns
117	SCKR edge to word select output valid (WSR out delay time)	Master	20	—	20	ns
118	Word select input valid to SCKR edge (WSR in setup time)	Slave	12	12	—	ns
119	SCKR edge to word select input not valid (WSR in hold time)	Slave	12	12	—	ns
121	SCKT edge to data output valid (data out delay time)	Master	13	—	13	ns
		Slave[1]	40	—	40	ns
		Slave[2]	Th + 34	—	40.2	ns
122	SCKT edge to word select output valid (WST output delay time)	Master	19	—	19	ns
123	Word select input valid to SCKT edge (WST in setup time)	Slave	12	12	—	ns

6367248 0148292 404

Table 2-9 Serial Audio Interface (SAI) Timing (Continued)

No.	Characteristics	Mode	Expression	81 MHz		Unit
				Min	Max	
124	SCKT edge to word select input not valid (WST in hold time)	Slave	12	12	—	ns

Notes: 1. When the Frequency Ratio between Parallel and Serial clocks is 1:4 or greater
2. When the Frequency Ratio between Parallel and Serial clocks is 1:3 – 1:4

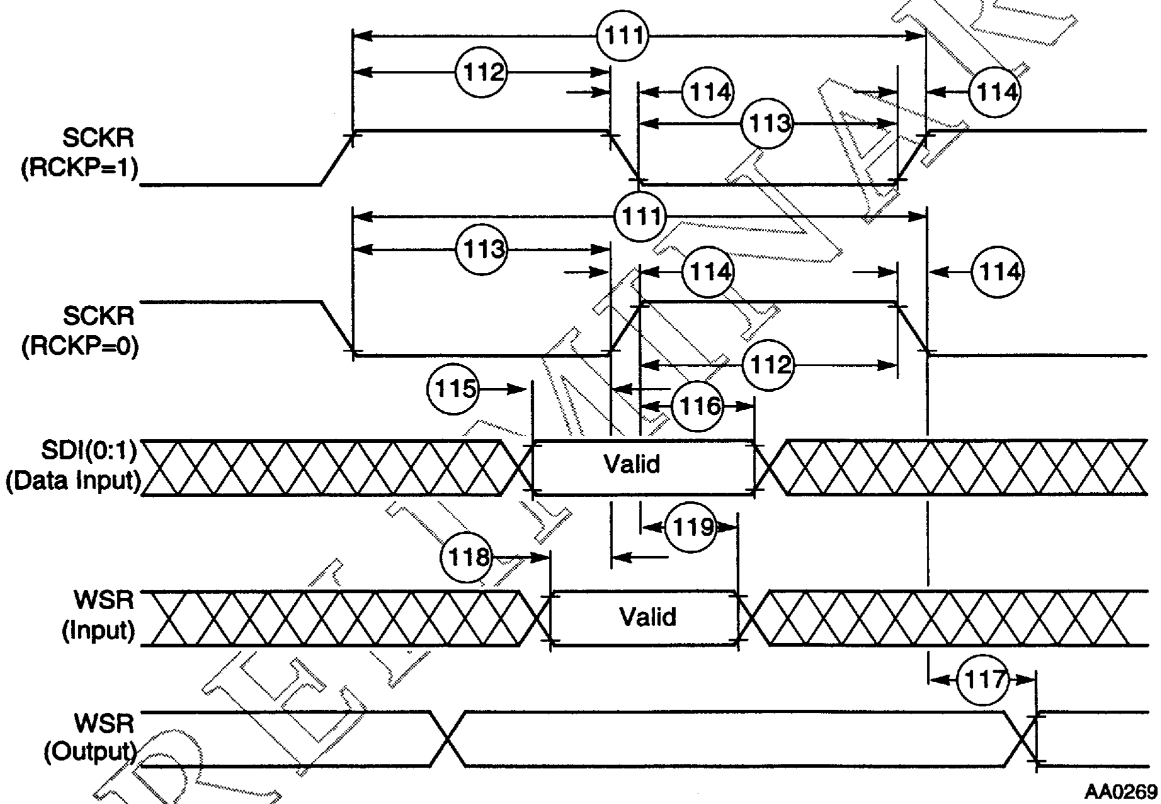


Figure 2-13 SAI Receiver Timing

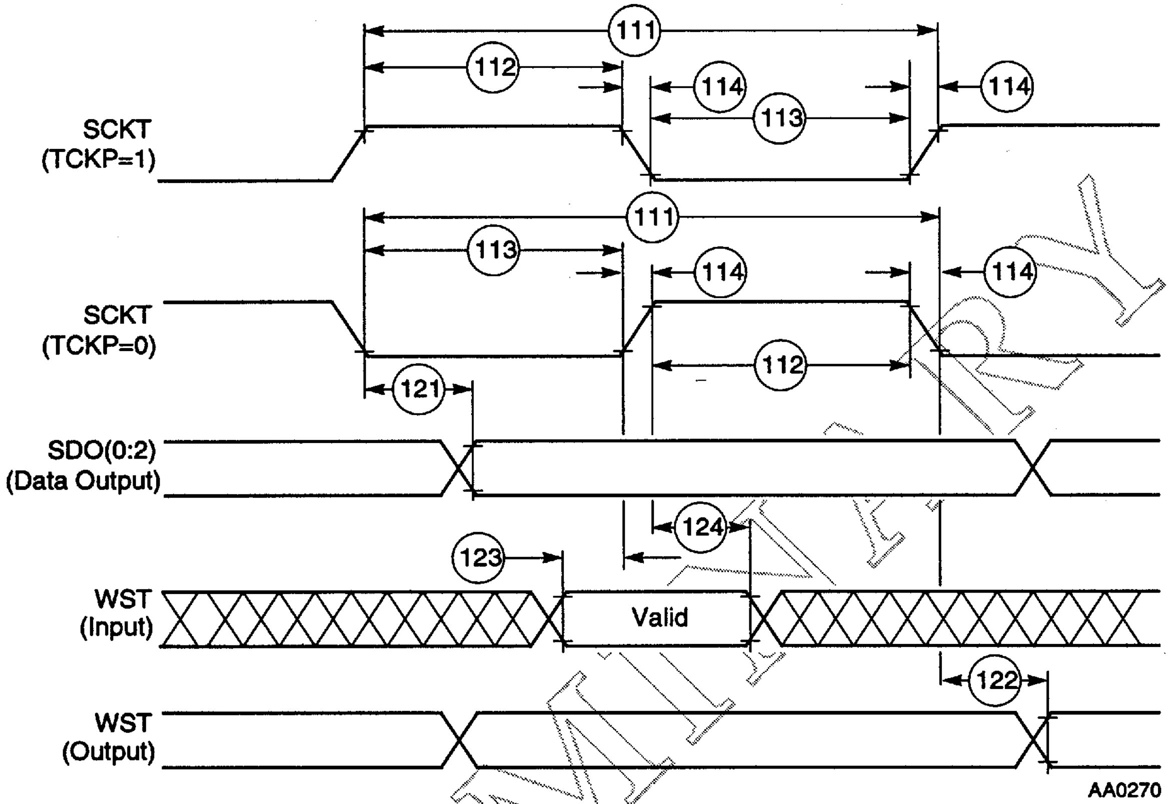


Figure 2-14 SAI Transmitter Timing

SERIAL HOST INTERFACE (SHI) SPI PROTOCOL TIMING

(V_{CC} = 5.0 V ± 5%, T_J = 125°C, C_L = 50 pF)

(V_{IHS} = 0.7 × V_{CC}, V_{ILS} = 0.3 × V_{CC})

Table 2-10 Serial Host Interface (SHI) SPI Protocol Timing

No.	Characteristics	Mode	Filter Mode	Expression	81 MHz Min	81 MHz Max	Unit
	Tolerable spike width on Clock or Data input		Bypassed		—	0	ns
			Narrow		—	20	ns
			Wide		—	100	ns
141	Minimum Serial Clock cycle = t_{SPICC}(min)						
	Frequency below 33 MHz[1]	Master	Bypassed	4 × Tc	—	—	ns
	Frequency above 33 MHz[1]		Bypassed	6 × Tc	74.1	—	ns
			Narrow	1000	1000	—	ns
			Wide	2000	2000	—	ns
	CPHA = 0, CPHA = 1[2]	Slave	Bypassed	3 × Tc	37	—	ns
			Narrow	3 × Tc + 25	62	—	ns
			Wide	3 × Tc + 85	122	—	ns
	CPHA = 1	Slave	Bypassed	3 × Tc + 79	116	—	ns
			Narrow	3 × Tc + 431	468	—	ns
			Wide	3 × Tc + 1022	1059	—	ns
142	Serial Clock high period	Master		0.5 × t_{SPICC} −10	27.0	—	ns
	CPHA = 0, CPHA = 1[2]	Slave	Bypassed	Tc + 8	20.3	—	ns
			Narrow	Tc + 31	43.3	—	ns
			Wide	Tc + 43	55.3	—	ns
	CPHA = 1	Slave	Bypassed	Tc + Th + 40	58.5	—	ns
			Narrow	Tc + Th + 216	235	—	ns
			Wide	Tc + Th + 511	536	—	ns

Table 2-10 Serial Host Interface (SHI) SPI Protocol Timing (Continued)

No.	Characteristics	Mode	Filter Mode	Expression	81 MHz Min	81 MHz Max	Unit
143	Serial Clock low period	Master		$0.5 \times t_{SPICC} - 10$	27.0	—	ns
	CPHA = 0, CPHA = 1[2]	Slave	Bypassed	Tc + 8	20.3	—	ns
			Narrow	Tc + 31	43.3	—	ns
			Wide	Tc + 43	55.3	—	ns
	CPHA = 1	Slave	Bypassed	Tc + Th + 40	58.5	—	ns
			Narrow	Tc + Th + 216	235	—	ns
			Wide	Tc + Th + 511	536	—	ns
144	Serial Clock rise/fall time	Master		10	—	10	ns
		Slave		2000	—	2000	ns
146	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	Bypassed	Tc + Th + 35	53.5	—	ns
			Narrow	Tc + Th + 35	53.5	—	ns
			Wide	Tc + Th + 35	53.5	—	ns
	CPHA = 1	Slave	Bypassed	6	6	—	ns
			Narrow	0	0	—	ns
			Wide	0	0	—	ns
147	Last SCK edge to $\overline{SS}$ not asserted CPHA = 0	Slave	Bypassed	Tc + 6	18.3	—	ns
			Narrow	Tc + 70	82.4	—	ns
			Wide	Tc + 197	209	—	ns
	CPHA = 1[3]	Slave	Bypassed	2	2	—	ns
			Narrow	66	66	—	ns
			Wide	193	193	—	ns
148	Data input valid to SCK edge (data input setup time)	Master	Bypassed	0	0	—	ns
			Narrow	MAX {(37 −Tc), 0}	25	—	ns
			Wide	MAX {(52 −Tc), 0}	40	—	ns
		Slave	Bypassed	0	0	—	ns
			Narrow	MAX {(38 −Tc), 0}	26	—	ns
			Wide	MAX {(53 −Tc), 0}	41	—	ns

Table 2-10 Serial Host Interface (SHI) SPI Protocol Timing (Continued)

No.	Characteristics	Mode	Filter Mode	Expression	81 MHz		Unit
					Min	Max	
149	SCK edge to data input not valid (data in hold time)	Master	Bypassed	2 × Tc + 17	41.7	—	ns
			Narrow	2 × Tc + 18	42.7	—	ns
			Wide	2 × Tc + 28	52.7	—	ns
		Slave	Bypassed	2 × Tc + 17	41.7	—	ns
			Narrow	2 × Tc + 18	42.7	—	ns
			Wide	2 × Tc + 28	52.7	—	ns
150	$\overline{SS}$ assertion to data out active	Slave		4	4	—	ns
151	$\overline{SS}$ deassertion to data tri-stated[4]	Slave		24	—	24	ns
152	SCK edge to data out valid (data out delay time)	Master	Bypassed	41	—	41	ns
			Narrow	214	—	214	ns
			Wide	504	—	504	ns
	CPHA = 0, CPHA = 1[2]	Slave	Bypassed	41	—	41	ns
			Narrow	214	—	214	ns
			Wide	504	—	504	ns
	CPHA = 1	Slave	Bypassed	Tc + Th + 40	—	58.5	ns
			Narrow	Tc + Th + 216	—	235	ns
			Wide	Tc + Th + 511	—	536	ns
153	SCK edge to data out not valid (data out hold time)	Master	Bypassed	0	0	—	ns
			Narrow	57	57	—	ns
			Wide	163	163	—	ns
		Slave	Bypassed	0	0	—	ns
			Narrow	57	57	—	ns
			Wide	163	163	—	ns
154	$\overline{SS}$ assertion to data output valid CPHA = 0	Slave		Tc + Th + 35	—	53.5	ns
157	First SCK sampling edge to $\overline{HREQ}$ output deassertation	Slave	Bypassed	3 × Tc + Th + 32	—	75	ns
			Narrow	3 × Tc + Th + 209	—	252	ns
			Wide	3 × Tc + Th + 507	—	550	ns

6367248 0148297 T96

Table 2-10 Serial Host Interface (SHI) SPI Protocol Timing (Continued)

No.	Characteristics	Mode	Filter Mode	Expression	81 MHz		Unit
					Min	Max	
158	Last SCK sampling edge to $\overline{\text{HREQ}}$ output not deasserted CPHA = 1	Slave	Bypassed Narrow Wide	2 × Tc + Th + 6 2 × Tc + Th + 63 2 × Tc + Th + 169	36.9 93.9 200	— — —	ns ns ns
159	$\overline{\text{SS}}$ deassertion to $\overline{\text{HREQ}}$ output not deasserted CPHA = 0	Slave		2 × Tc + Th + 7	37.9	—	ns
160	$\overline{\text{SS}}$ deassertion pulse width CPHA = 0	Slave		Tc + 4	16.3	—	ns
161	$\overline{\text{HREQ}}$ input assertion to first SCK edge	Master		0.5 × t_{SPICC} + 2 × Tc + 6	67.7	—	ns
162	$\overline{\text{HREQ}}$ input deassertion to last SCK sampling edge ($\overline{\text{HREQ}}$ input setup time) CPHA = 1	Master		0	0	—	ns
163	First SCK edge to $\overline{\text{HREQ}}$ input not asserted ($\overline{\text{HREQ}}$ input hold time)	Master		0	0	—	ns

Note:
1. For an internal clock frequency below 33 MHz, the minimum permissible internal clock to SCK frequency ratio is 4:1.
   For an internal clock frequency above 33 MHz, the minimum permissible internal clock to SCK frequency ratio is 6:1.
2. In CPHA = 1 mode, the SPI slave supports data transfers at t_{SPICC} = 3 × Tc, if the user assures that the HTX is written at least Tc ns before the first edge of SCK of each word.In CPHA = 1 mode, the SPI slave supports data transfers at t_{SPICC} = 3 × Tc, if the user assures that the HTX is written at least Tc ns before the first edge of SCK of each word.
3. When CPHA = 1, the $\overline{\text{SS}}$ line may remain active low between successive transfers.
4. Periodically sampled, not 100% tested

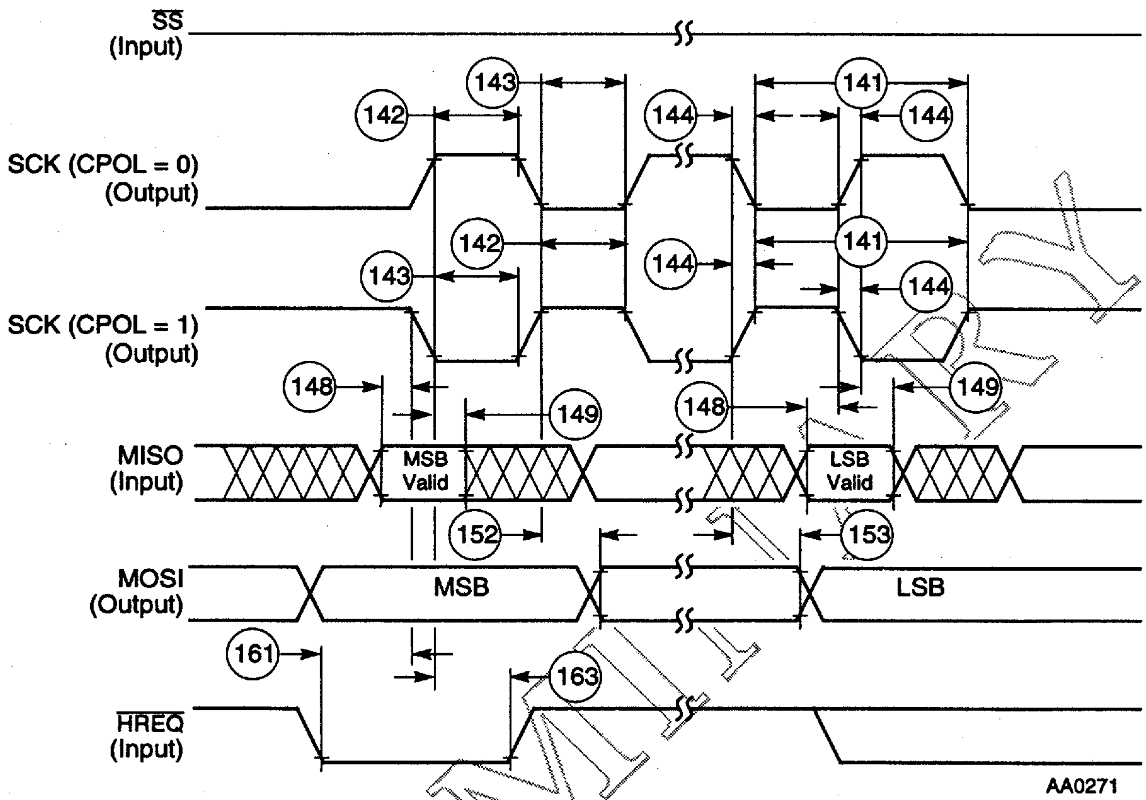


Figure 2-15 SPI Master Timing (CPHA = 0)

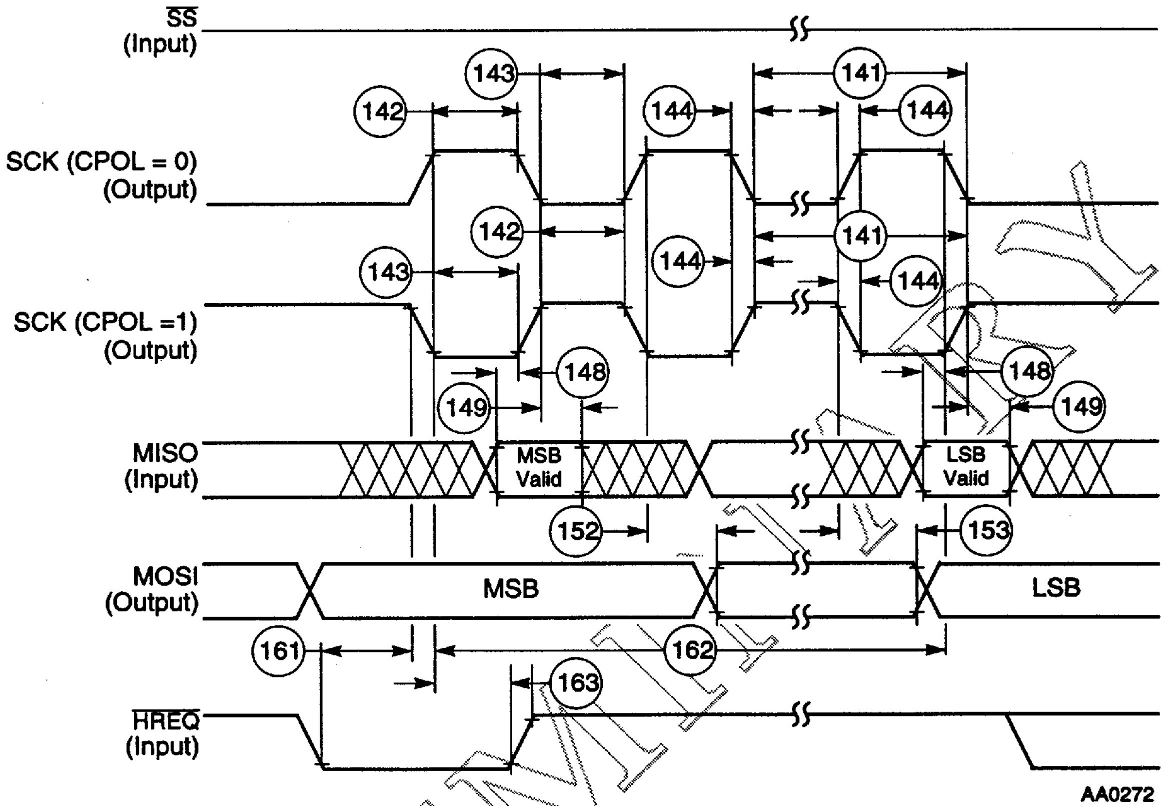


Figure 2-16 SPI Master Timing (CPHA = 1)

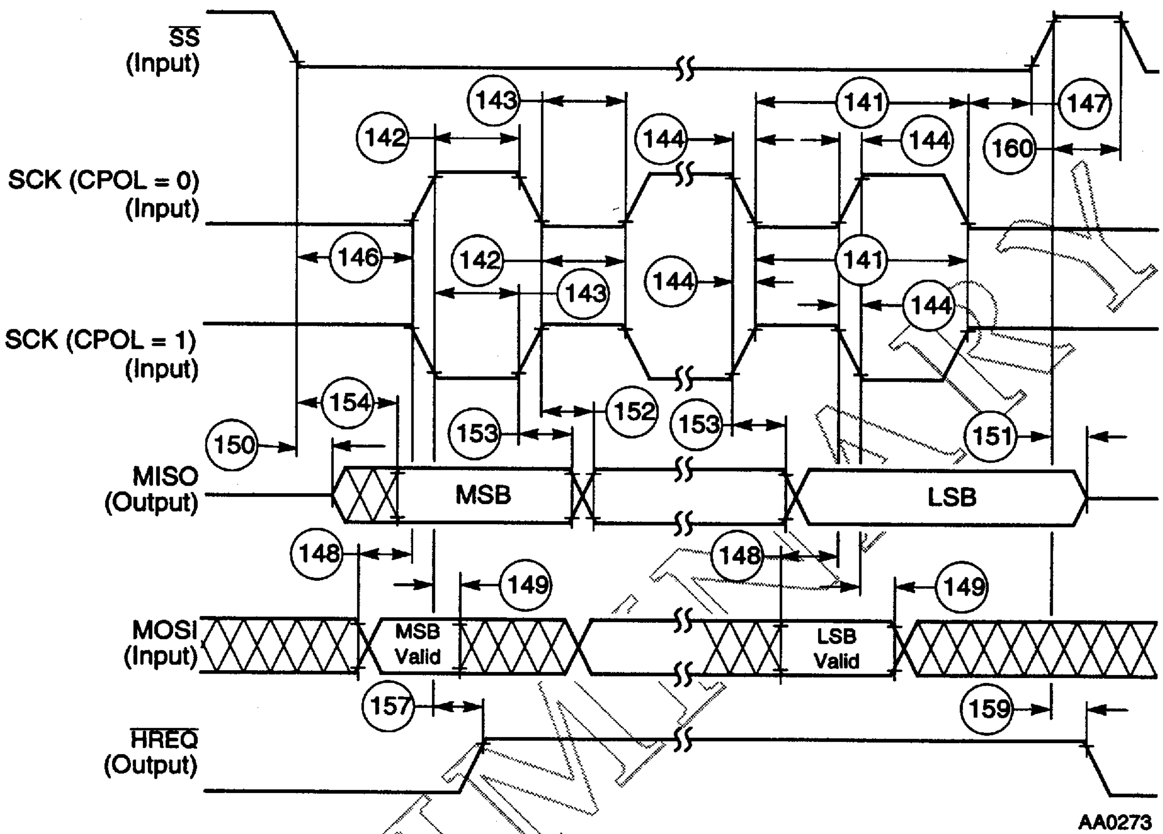


Figure 2-17 SPI Slave Timing (CPHA = 0)

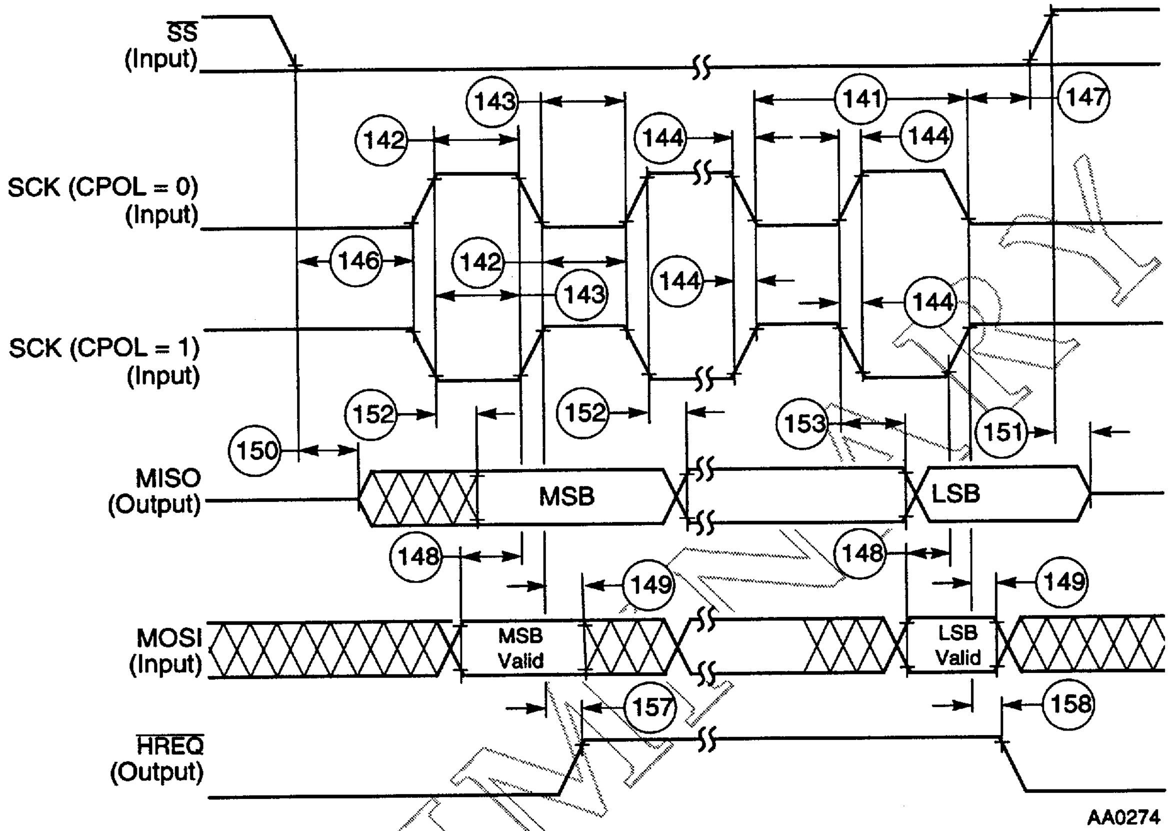


Figure 2-18 SPI Slave Timing (CPHA = 1)

SERIAL HOST INTERFACE (SHI) I^2C PROTOCOL TIMING

(V_{CC} = 5.0 V ± 5%, T_J = 125°C)
(V_{IHS} = 0.7 × V_{CC}, V_{ILS} = 0.3 × V_{CC})
(V_{OHS} = 0.8 × V_{CC}, V_{OLS} = 0.2 × V_{CC})
(R_P (min) = 1.5 kΩ)

Table 2-11 SHI I^2C Protocol Timing

Standard I^2C (C_L = 400 pF, R_P = 2 kΩ, 100 kHz)					
No.	**Characteristics**	**Symbol**	**81 MHz**		**Unit**
			Min	**Max**	
	Tolerable spike width on SCL or SDA filters bypassed		—	0	ns
	Narrow filters enabled		—	20	ns
	Wide filters enabled		—	100	ns
171	Minimum SCL Serial Clock cycle	t_{SCL}	10.0	—	µs
172	Bus free time	t_{BUF}	4.7	—	µs
173	Start condition setup time	$t_{SU;STA}$	4.7	—	µs
174	Start condition hold time	$t_{HD;STA}$	4.0	—	µs
175	SCL low period	t_{LOW}	4.7	—	µs
176	SCL high period	t_{HIGH}	4.0	—	µs
177	SCL and SDA rise time	t_r	—	1.0	µs
178	SCL and SDA fall time	t_f	—	0.3	µs
179	Data setup time	$t_{SU;DAT}$	250	—	ns
180	Data hold time	$t_{HD;DAT}$	0.0	—	ns
182	SCL low to data output valid	$t_{VD;DAT}$	—	3.4	µs
183	Stop condition setup time	$t_{SU;STO}$	4.0	—	µs

Programming the Serial Clock

The Programmed Serial Clock Cycle, t_{I^2CCP}, is specified by the value of the HDM5–HDM0 and HRS bits of the HCKR (SHI Clock control Register).

The expression for t_{I^2CCP} is:

$$t_{I^2CCP} = [Tc \times 2 \times (HDM[5:0] + 1) \times (7 \times (1 - HRS) + 1)]$$

where

- HRS is the Prescaler Rate Select bit. When HRS is cleared, the fixed divide-by-eight prescaler is operational. When HRS is set, the prescaler is bypassed.
- MDM5–HDM0 are the Divider Modulus Select bits.
- A divide ratio from 1 to 64 (HDM5–HDM0 = 0 to $3F) may be selected.

In I²C mode, you may select a value for the Programmed Serial Clock Cycle from:

```
6 × Tc (if HDM[5:0] = $02 and HRS = 1)
                        to
1024 × Tc  (if HDM[5:0] = $3F and HRS = 0)
```

The DSP56011 provides an improved I²C bus protocol. In addition to supporting the 100 kHz I²C bus protocol, the SHI in I²C mode supports data transfers at up to 1000 kHz. The actual maximum frequency is limited by the bus capacitances (C_L),the pull-up resistors (R_P), (which affect the rise and fall time of SDA and SCL, (see table below)), and by the input filters.

Considerations for programming the SHI Clock Control Register (HCKR)—Clock Divide Ratio

The master must generate a bus free time greater than T172 slave when operating with a DSP56011 SHI I^{2}C slave. **Table 2-12** on page 2-27 describes a few examples.

Table 2-12 Considerations for Programming the SHI Clock control Register (HCKR)

Conditions to be Considered						Resulting Limitations		
Bus Load	Master Operating Freq.	Slave Operating Freq.	Master Filter Mode	Slave Filter Mode	T172 Slave	Min. Permissible t_{I^2CCP}	T172 Master	Maximum I^{2}C Serial Frequency
$C_L = 50$ pF, $R_P = 2$ kΩ	81 MHz	81 MHz	Bypassed	Bypassed	36 ns	52 × Tc	41 ns	1010 kHz
			Narrow	Narrow	60 ns	56 × Tc	66 ns	825 kHz
			Wide	Wide	95 ns	62 × Tc	103 ns	634 kHz

Example: for $C_L = 50$ pF, $R_P = 2$ kΩ, f = 81 MHz, Bypassed filter mode: The master, when operating with a DSP56011 SHI I^{2}C slave with an 81 MHz operating frequency, must generate a bus free time greater than 36 ns (T172 slave). Thus, the minimum permissible t_{I^2CCP} is 52 × Tc, which gives a bus free time of at least 41 ns (T172 master). This implies a maximum I^{2}C serial frequency of 1010 kHz.

In general, bus performance may be calculated from the C_L and R_P of the bus, the input filter modes and operating frequencies of the master and the slave. **Table 2-15** contains the expressions required to calculate all relevant performance timing for a given C_L and R_P.

Table 2-13 SHI Improved I^{2}C Protocol Timing

Improved I^{2}C ($C_L = 50$ pF, $R_P = 2$ kΩ)								
No.	Characteristic	Sym.	Mode	Filter Mode	Expression	81 MHz[2] Min	81 MHz[2] Max	Unit
	Tolerable spike width on SCL or SDA			Bypassed	0	—	0	ns
				Narrow	20	—	20	ns
				Wide	100	—	100	ns

Table 2-13 SHI Improved I^2C Protocol Timing (Continued)

Improved I^2C (C_L = 50 pF, R_P = 2 kΩ)								
No.	Characteristic	Sym.	Mode	Filter Mode	Expression	81 MHz[2] Min	81 MHz[2] Max	Unit
171	SCL Serial Clock cycle	t_{SCL}	Master	Bypassed	$t_{I^2CCP} + 3 \times Tc + 72 + t_r$	989	—	ns
				Narrow	$t_{I^2CCP} + 3 \times Tc + 245 + t_r$	1212	—	ns
				Wide	$t_{I^2CCP} + 3 \times Tc + 535 + t_r$	1576	—	ns
			Slave	Bypassed	$4 \times Tc + Th + 172 + t_r$	466	—	ns
				Narrow	$4 \times Tc + Th + 366 + t_r$	660	—	ns
				Wide	$4 \times Tc + Th + 648 + t_r$	942	—	ns
172	Bus free time	t_{BUF}	Master	Bypassed	$0.5 \times t_{I^2CCP} - 42 - t_r$	41.1	—	ns
				Narrow	$0.5 \times t_{I^2CCP} - 42 - t_r$	65.8	—	ns
				Wide	$0.5 \times t_{I^2CCP} - 42 - t_r$	103	—	ns
			Slave	Bypassed	$2 \times Tc + 11$	35.7	—	ns
				Narrow	$2 \times Tc + 35$	59.7	—	ns
				Wide	$2 \times Tc + 70$	94.7	—	ns
173	Start condition setup time	$t_{SU;STA}$	Slave	Bypassed	12	12	—	ns
				Narrow	50	50	—	ns
				Wide	150	150	—	ns

Table 2-13 SHI Improved I^2C Protocol Timing (Continued)

Improved I^2C (C_L = 50 pF, R_P = 2 kΩ)								
No.	Characteristic	Sym.	Mode	Filter Mode	Expression	81 MHz[2] Min	81 MHz[2] Max	Unit
174	Start condition hold time	$t_{HD;STA}$	Master	Bypassed	$0.5 \times t_{I^2CCP} + 12 - t_f$	313	—	ns
				Narrow	$0.5 \times t_{I^2CCP} + 12 - t_f$	338	—	ns
				Wide	$0.5 \times t_{I^2CCP} + 12 - t_f$	375	—	ns
			Slave	Bypassed	$2 \times Tc + Th + 21$	51.9	—	ns
				Narrow	$2 \times Tc + Th + 100$	131	—	ns
				Wide	$2 \times Tc + Th + 200$	231	—	ns
175	SCL low period	t_{LOW}	Master	Bypassed	$0.5 \times t_{I^2CCP} + 18 - t_f$	319	—	ns
				Narrow	$0.5 \times t_{I^2CCP} + 18 - t_f$	344	—	ns
				Wide	$0.5 \times t_{I^2CCP} + 18 - t_f$	381	—	ns
			Slave	Bypassed	$2 \times Tc + 74 + t_r$	337	—	ns
				Narrow	$2 \times Tc + 286 + t_r$	536	—	ns
				Wide	$2 \times Tc + 586 + t_r$	849	—	ns
176	SCL high period	t_{HIGH}	Master	Bypassed	$0.5 \times t_{I^2CCP} + 2 \times Tc + 19$	365	—	ns
				Narrow	$0.5 \times t_{I^2CCP} + 2 \times Tc + 144$	514	—	ns
				Wide	$0.5 \times t_{I^2CCP} + 2 \times Tc + 356$	763	—	ns
			Slave	Bypassed	$2 \times Tc + Th - 1$	30	—	ns
				Narrow	$2 \times Tc + Th + 18$	49	—	ns
				Wide	$2 \times Tc + Th + 30$	61	—	ns
177	SCL rise time Output	t_r			$1.7 \times R_P \times (C_L + 20)$[1]	—	238	ns
	Input				2000	—	2000	ns

Table 2-13 SHI Improved I^2C Protocol Timing (Continued)

Improved I^2C (C_L = 50 pF, R_P = 2 kΩ)

No.	Characteristic	Sym.	Mode	Filter Mode	Expression	81 MHz[2] Min	81 MHz[2] Max	Unit
178	SCL fall time	t_f						
	Output				$20 + 0.1 \times (C_L - 50)$[1]	—	20	ns
	Input				2000	—	2000	ns
179	Data setup time	$t_{SU;DAT}$		Bypassed	Tc + 8	20	—	ns
				Narrow	Tc + 60	72	—	ns
				Wide	Tc + 74	86	—	ns
180	Data hold time	$t_{HD;DAT}$		Bypassed	0	0	—	ns
				Narrow	0	0	—	ns
				Wide	0	0	—	ns
182	SCL low to data output valid	$t_{VD;DAT}$		Bypassed	$2 \times Tc + 71 + t_r$	—	344	ns
				Narrow	$2 \times Tc + 244 + t_r$	—	507	ns
				Wide	$2 \times Tc + 535 + t_r$	—	798	ns
183	Stop condition setup time	$t_{SU;STO}$	Master	Bypassed	$0.5 \times t_{I^2CCP}$ + Tc + Th + 11	351	—	ns
				Narrow	$0.5 \times t_{I^2CCP}$ + Tc + Th + 69	433	—	ns
				Wide	$0.5 \times t_{I^2CCP}$ + Tc + Th + 183	584	—	ns
			Slave	Bypassed	11	11	—	ns
				Narrow	50	50	—	ns
				Wide	150	150	—	ns
184	$\overline{HREQ}$ input deassertion to last SCL edge ($\overline{HREQ}$ in setup time)		Master	Bypassed	0	0	—	ns
				Narrow	0	0	—	ns
				Wide	0	0	—	ns
186	First SCL sampling edge to $\overline{HREQ}$ output deassertion		Slave	Bypassed	3 × Tc + Th + 32	—	75	ns
				Narrow	3 × Tc + Th + 209	—	252	ns
				Wide	3 × Tc + Th + 507	—	550	ns

Table 2-13 SHI Improved I^{2}C Protocol Timing (Continued)

Improved I^{2}C (C_L = 50 pF, R_P = 2 kΩ)								
No.	Characteristic	Sym.	Mode	Filter Mode	Expression	81 MHz^2 Min	81 MHz^2 Max	Unit
187	Last SCL edge to $\overline{\text{HREQ}}$ output not deasserted		Slave	Bypassed	2 × Tc + Th + 6	37	—	ns
				Narrow	2 × Tc + Th + 63	93.9	—	ns
				Wide	2 × Tc + Th + 169	200	—	ns
188	$\overline{\text{HREQ}}$ input assertion to first SCL edge		Master	Bypassed	t_{I^2CCP} + 2 × Tc + 6	673	—	ns
				Narrow	t_{I^2CCP} + 2 × Tc + 6	722	—	ns
				Wide	t_{I^2CCP} + 2 × Tc + 6	796	—	ns
189	First SCL edge to $\overline{\text{HREQ}}$ input not asserted ($\overline{\text{HREQ}}$ input hold time)		Master		0	0	—	ns

Notes:
1. C_L is in pF, R_P is in kΩ, and result is in ns.
2. A t_{I^2CCP} of 52 × Tc (the maximum permitted for the given bus load) was used for the calculations in the Bypassed filter mode. A t_{I^2CCP} of 56 × Tc (the maximum permitted for the given bus load) was used for the calculations in the Narrow filter mode. A t_{I^2CCP} of 62 × Tc (the maximum permitted for the given bus load) was used for the calculations in the Wide filter mode.

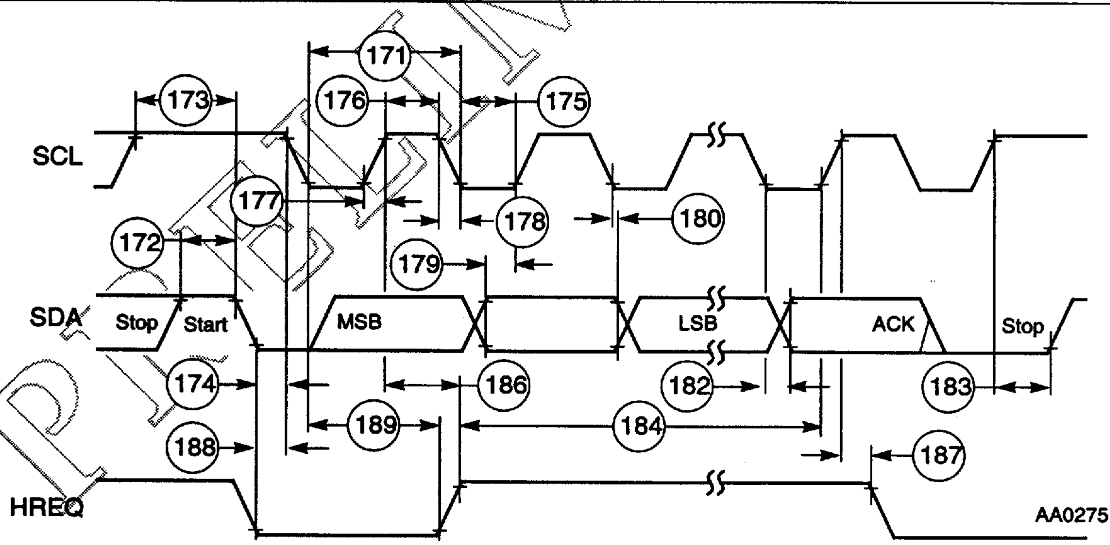


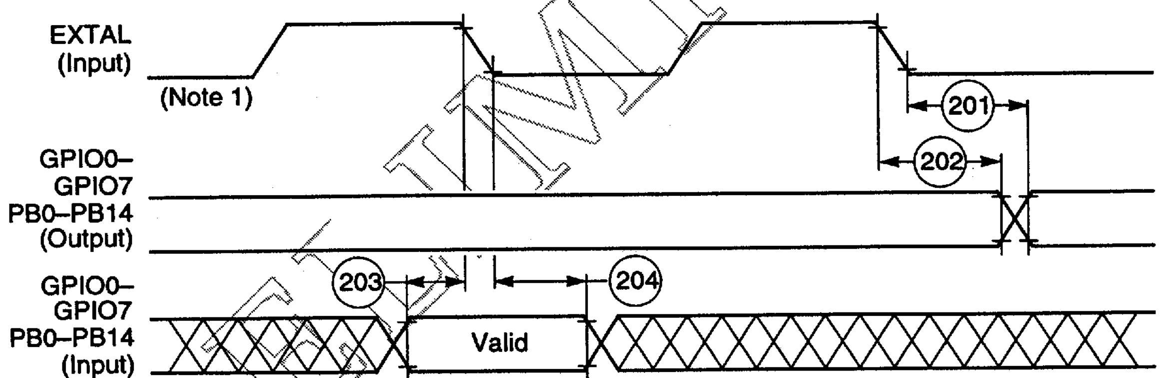
Figure 2-19 I^{2}C Timing

GENERAL PURPOSE I/O (GPIO) TIMING

(V_{CC} = 5.0 V ± 5%, T_J = 125°C, C_L = 50 pF + 2 TTL Loads)

Table 2-14 GPIO Timing

No.	Characteristics	Expression	81 MHz		Unit
			Min	Max	
201	EXTAL edge to GPIO output valid (GPIO output delay time)	26	—	26	ns
202	EXTAL edge to GPIO output not valid (GPIO output hold time)	2	2	—	ns
203	GPIO input valid to EXTAL Edge (GPIO input setup time)	10	10	—	ns
204	EXTAL edge to GPIO input not valid (GPIO input hold time)	6	6	—	ns



Note: 1. Valid when the ratio between EXTAL frequency and internal clock frequency equals 1

AA0276

Figure 2-20 GPIO Timing

DIGITAL AUDIO TRANSMITTER (DAX) TIMING

(V_{CC} = 5.0V ± 5%; T_J = -40° to +125°, C_L = 50 pF + 2 TTL Loads)

Table 2-15 56011 Digital Audio Transmitter Timing

No.	Characteristic	81 MHz		Unit
		Min	Max	
	ACI Frequency[1]	—	25	MHz
220	ACI Period	40	—	ns
221	ACI High Duration	0.5 × Tc	—	ns
222	ACI Low Duration	0.5 × Tc	—	ns
223	ACI Rising Edge to ADO Valid	—	35	ns

Notes: 1. In order to assure proper operation of the DAX, the ACI frequency should be less than 1/2 of the DSP56011 internal clock frequency. For example, if the DSP56011 is running at 40 MHz internally, the ACI frequency should be less than 20 MHz.

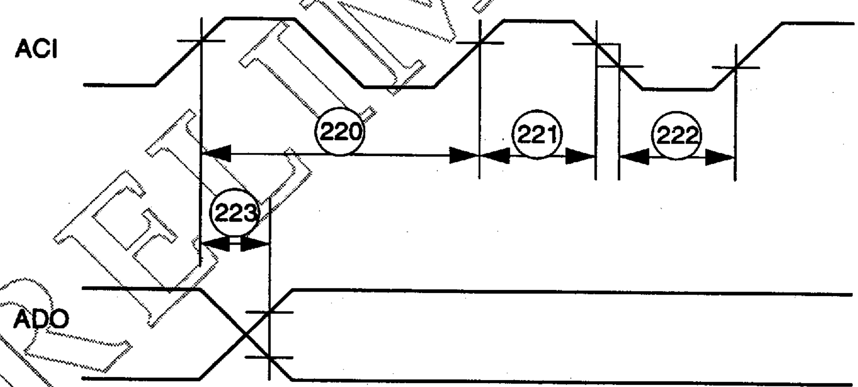


Figure 2-21 Digital Audio Transmitter Timing

ON-CHIP EMULATION (OnCE™) TIMING

(V_{CC} = 5.0 V ± 5%, T_J = 125°C, C_L = 50 pF + 2 TTL Loads)

Table 2-16 OnCE Timing

No.	Characteristics	81 MHz		Unit
		Min	Max	
230	DSCK low	40	—	ns
231	DSCK high	40	—	ns
232	DSCK cycle time	200	—	ns
233	$\overline{DR}$ asserted to DSO ($\overline{ACK}$) asserted	5 Tc	—	ns
234	DSCK high to DSO valid	—	42	ns
235	DSCK high to DSO invalid	3	—	ns
236	DSI valid to DSCK low (setup)	15	—	ns
237	DSCK Low to DSI Invalid (Hold)	3	—	ns
238	Last DSCK low to OS0–OS1, $\overline{ACK}$ active	3 Tc + Tl	—	ns
239	DSO ($\overline{ACK}$) asserted to first DSCK high	2 Tc	—	ns
240	DSO ($\overline{ACK}$) assertion width	4 Tc + Th – 3	5 Tc + 7	ns
241	DSO ($\overline{ACK}$) asserted to OS0–OS1 high impedance[1]	—	0	ns
242	OS0–OS1 valid to second EXTAL transition	Tc – 21	—	ns
243	Second EXTAL transition to OS0–OS1 invalid	0	—	ns
244	Last DSCK low of read register to first DSCK high of next command	7 Tc + 10	—	ns
245	Last DSCK low to DSO invalid (hold)	3	—	ns
246	$\overline{DR}$ assertion to second EXTAL transition for wake up from Wait state	10	Tc – 10	ns
247	Second EXTAL transition to DSO after wake up from Wait state	17 Tc	—	ns
248	$\overline{DR}$ assertion width • to recover from Wait • to recover from Wait and enter Debug mode	 15 13 Tc + 15	 12 Tc – 15 —	ns
249	$\overline{DR}$ assertion to DSO ($\overline{ACK}$) valid (enter Debug mode) after asynchronous recovery from Wait state	17 Tc	—	ns

6367248 0148312 022

Table 2-16 OnCE Timing (Continued)

No.	Characteristics	81 MHz		Unit
		Min	Max	
250A	$\overline{\text{DR}}$ assertion width to recover from Stop[2] • Stable External Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17 = 1	 15 15 15	 65548 Tc + Tl 20 Tc + Tl 13 Tc + Tl	 ns
250B	$\overline{\text{DR}}$ assertion width to recover from Stop and enter Debug mode[2] • Stable External Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17= 1	 65549 Tc + Tl 21 Tc + Tl 14 Tc + Tl	 — — —	ns
251	$\overline{\text{DR}}$ assertion to DSO ($\overline{\text{ACK}}$) valid (enter Debug mode) after recovery from Stop state[2] • Stable External Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17= 1	 65553 Tc + Tl 25 Tc + Tl 18 Tc + Tl	 — — —	 ns

Note: 1. Maximum Tl
2. Periodically sampled, not 100% tested

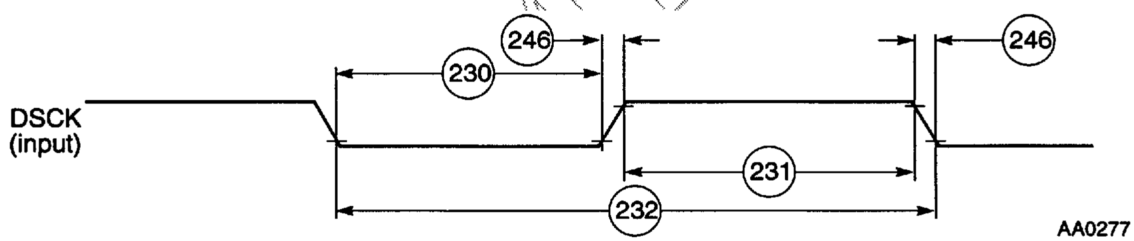


Figure 2-22 DSP56011 OnCE Serial Clock Timing

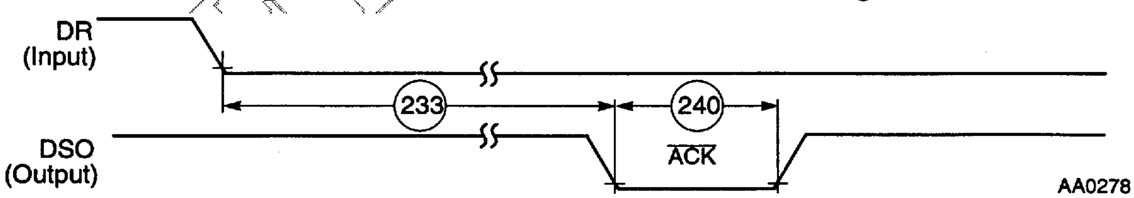
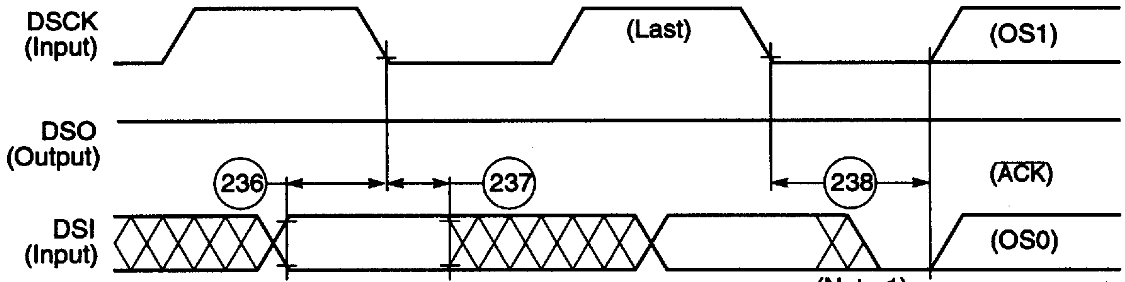


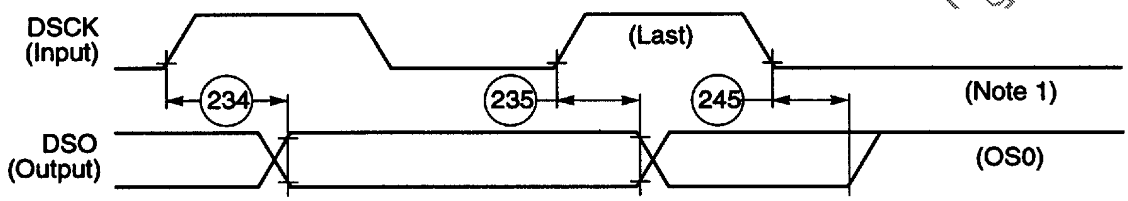
Figure 2-23 DSP56011 OnCE Acknowledge Timing



Note: 1. High Impedance, external pull-down resistor

AA0279

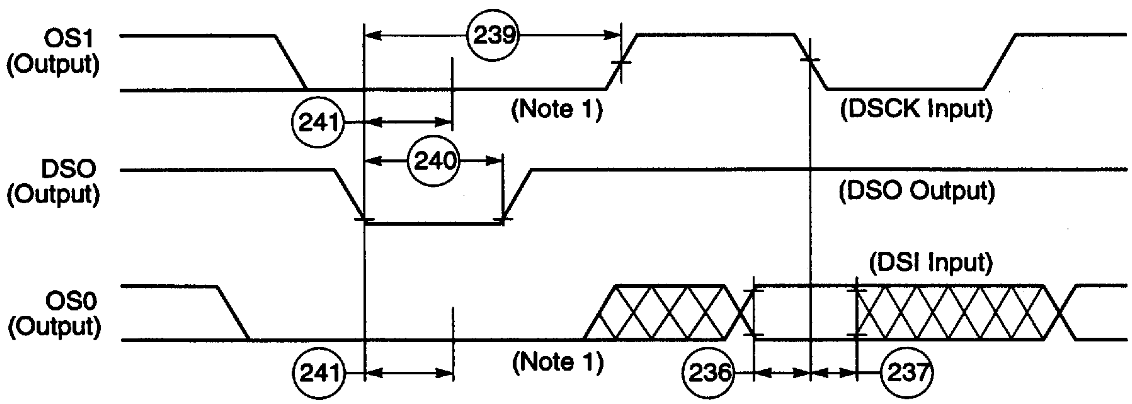
Figure 2-24 DSP56011 OnCE Data I/O to Status Timing



Note: 1. High Impedance, external pull-down resistor

AA0280

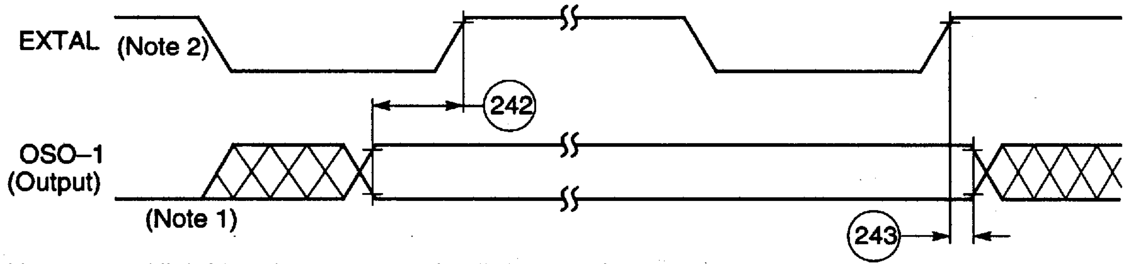
Figure 2-25 DSP56011 OnCE Read Timing



Note: 1. High Impedance, external pull-down resistor

AA0281

Figure 2-26 DSP56011 OnCE Data I/O Status Timing



Note: 1. High Impedance, external pull-down resistor
2. Valid when the ratio between EXTAL frequency and clock frequency equals 1

AA0282

Figure 2-27 DSP56011 OnCE EXTAL to Status Timing

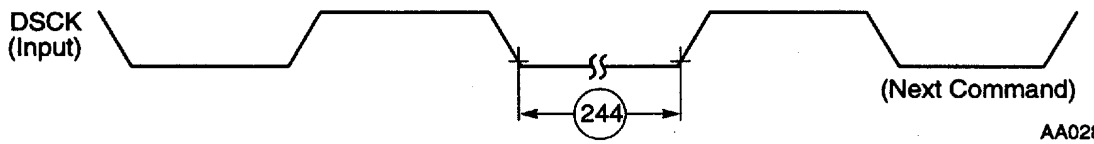


Figure 2-28 DSP56011 OnCE DSCK Next Command After Read Register Timing

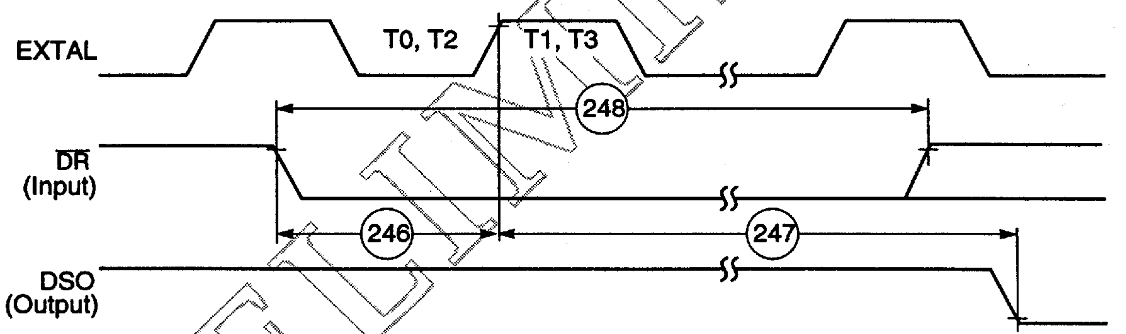


Figure 2-29 Synchronous Recovery from Wait State

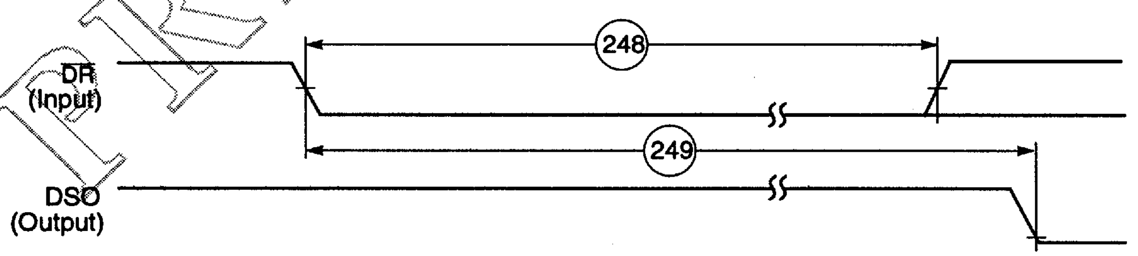


Figure 2-30 Asynchronous Recovery from Wait State

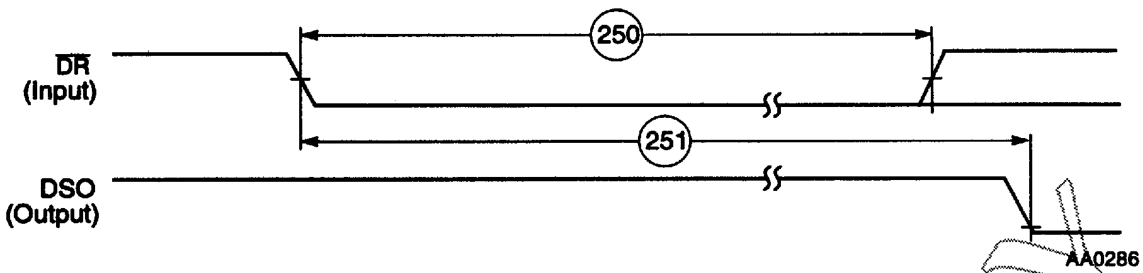


Figure 2-31 Asynchronous Recovery from Stop State